

# AC/DC Driver for General Lighting LED Driver IC with PWM and LINEAR Dimming

BD552JLFV / F

## General Description

The quasi-resonant controller type LED driver IC BD552JLFV/F supports an optimum system of LED lighting equipments. It is an LED driver which integrates an AC/DC step-down type switching controller with a constant current driver.

Owing to the quasi-resonant operation, the soft switching is achieved, and this contributes to the low EMI noise. And due to the switching MOSFET and the resistor for current sensing, which are externally found, it is possible to achieve a high degree of freedom for the power supply design.

This IC supports both isolated and non-isolated topology. Especially, in case of isolated topology, wherein LED current control is possible with an photocoupler-less application. This provides an optimum circuit for reducing the components.

Moreover, this IC supports both PWM dimming mode and LINEAR dimming mode allowing it to be used on various applications. Finally, with BURST operation in case of the dimming rate of lower than 20%, a deeper dimming level can be achieved.

## Key Specifications

- Step-down AC/DC converter with high efficiency
- Primary side control (no feedback circuit)
- PWM·LINEAR dimming control
- Supports non-isolated(buck) topology
- Supports photocoupler-less isolated(fly-back) topology
- Built-in regulator for internal power supply
- Low EMI noise by soft-switching function
- LED open detection function[shut down]
- Soft start function
- ZT trigger mask function
- ZT OVP function [shut down]
- UVLO detection function [self-reset]
- Output overload protection [self-reset]
- ISNS open protection circuit [shut down]

## Packages

**SSOP-B14** : 5.00mm x 6.40mm x 1.15mm (0.65mm pitch)

**SOP14** : 6.20mm x 8.70mm x 1.50mm (1.27mm pitch)

## Features

- Input voltage range: VCC : 8.5V to 25.5V
- Current consumption: UVLO detected : 20uA (Typ)  
operating : 2.2 mA (Typ)
- Operating temperature range: -40°C to +105°C

## Applications

LED lightings with PWM/LINEAR dimmer  
(downlight, spotlight, tube-typed LED etc.)

## Typical Application Circuit

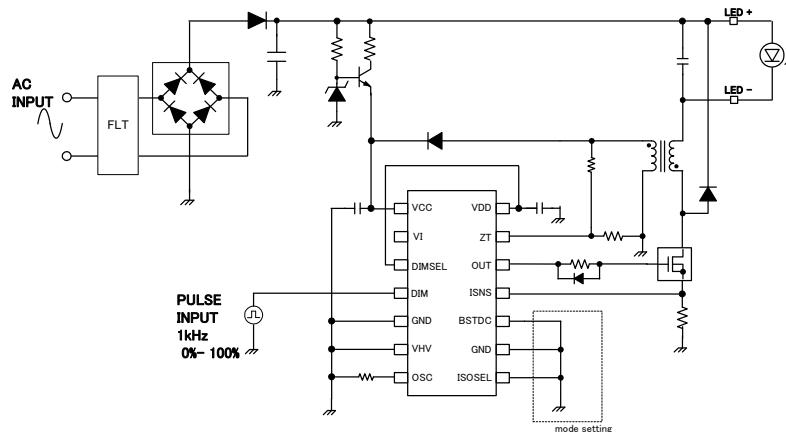


Figure1. Typical Application Circuit (Non-isolated / PWM dimming type)

## Absolute Maximum Ratings (Ta=25°C)

Parameters	Symbol	Ratings	Unit	Comments
Voltage Range 1	V <sub>MAX1</sub>	-0.3 to 30	V	V <sub>CC</sub>
Voltage Range 2	V <sub>MAX2</sub>	-0.3 to 4.5	V	V <sub>DD</sub> , ISOSEL, BSTDC, DIMSEL, DIM
Voltage Range 3	V <sub>MAX3</sub>	-0.3 to 6.5	V	ISNS, OSC
Voltage Range 4	V <sub>MAX4</sub>	-0.3 to 8.5	V	ZT
Voltage Range 5	V <sub>MAX5</sub>	-0.3 to 15	V	OUT, VI, VHV
ZT Pin Current	I <sub>ZT</sub>	±3.00	mA	
Maximum Power Dissipation	Pd	SSOP-B14: 500 (Note1) SOP14: 562 (Note2)	mW	
Operating Temperature Range	Topr	-40 to +105	°C	
Maximum Junction Temperature	Tjmax	150	°C	
Storage Temperature Range	Tstr	-55 to +150	°C	

(Note1) 70×70×1.6mm (mounted on glass epoxy substrate), derate by 4.0mW/°C when operating above Ta=25°C.

(Note2) 70×70×1.6mm (mounted on glass epoxy substrate), derate by 4.5mW/°C when operating above Ta=25°C.

## Recommended Operating Range (Ta=25°C)

Parameters	Symbol	Limits	Unit	Comments
Supply Voltage Range 1	V <sub>CC</sub>	8.5 to 25.5	V	VCC pin
Supply Voltage Range 2	V <sub>ZT</sub>	~6.5	V	ZT pin

## Electrical Characteristics (Unless otherwise specified, Ta=25°C, VCC=15V)

Parameters	Symbol	Limits			Unit	Comments
		Min	Typ	Max		
<b>[Circuit Current]</b>						
Circuit Current (OFF)	I <sub>OFF</sub>	-	20	40	uA	VCC=12V (UVLO state )
Circuit Current (ON)1	I <sub>ON1</sub>	-	2.80	4.80	mA	DIMSEL=H, DIM=H (While OUT keep switching )
Circuit Current (ON)2	I <sub>ON2</sub>	-	2.60	4.60	mA	DIMSEL=H, DIM=L (While OUT switching OFF)
<b>[VCC Pin]</b>						
VCC UVLO Release Voltage	V <sub>UVLO1</sub>	12.50	13.50	14.50	V	While VCC rising up
VCC UVLO Trigger Voltage	V <sub>UVLO2</sub>	6.10	6.50	7.00	V	While VCC falling down
VCC UVLO Hysteresis Voltage	V <sub>UVLO3</sub>	6.0	7.0	8.0	V	V <sub>UVLO3</sub> = V <sub>UVLO1</sub> - V <sub>UVLO2</sub>
VCC OVP Trigger Voltage	V <sub>OVP</sub>	25.0	27.5	30.0	V	While VCC rising up
VCC OVP Hysteresis Voltage	V <sub>OVP,hys</sub>	2.2	4.0	5.7	V	
<b>[ REG Block ]</b>						
VDD Output Voltage	V <sub>DD</sub>	3.20	3.30	3.40	V	
VDD Output Current	I <sub>VDD</sub>	20	-	-	mA	
VDD UVLO Release Voltage	V <sub>DDUVLO</sub>	2.50	2.80	3.10	V	While VDD rising up
<b>[ DCDC Turn OFF Block : ISNS ]</b>						
Average Current Sense Voltage	V <sub>isns</sub>	475	500	525	mV	
Maximum Switching Frequency	F <sub>sw,max</sub>	170	200	230	kHz	
Minimum Switching Frequency	F <sub>sw,min</sub>	18	20	22	kHz	OSC=GND
<b>[ DCDC Turn ON Block : ZT ]</b>						
ZT Converter 1	V <sub>zt1</sub>	40	100	160	mV	While ZT voltage is increasing
ZT Converter 2	V <sub>zt2</sub>	120	200	280	mV	While ZT voltage is decreasing
Timeout switching frequency	F <sub>to</sub>	80	100	120	kHz	OSC=OPEN
<b>[ OUT Pin ]</b>						
OUT Pin H Voltage	V <sub>OUTH</sub>	10.5	12.0	13.5	V	I <sub>o,OUT</sub> = -2mA, VCC=15V
OUT Pin L Voltage	V <sub>OUTL</sub>	-	-	0.30	V	I <sub>o,OUT</sub> = +2mA, VCC=15V
OUT Pin Pull-down Resistance	R <sub>PDOUT</sub>	75	100	125	kΩ	
OUT Pin High ON Resistance	R <sub>vouth</sub>	6.0	12.0	24.0	Ω	OUT =2mA Source
OUT Pin Low ON Resistance	R <sub>voutl</sub>	1.5	3.0	6.0	Ω	OUT =2mA Sink

## Electrical Characteristics (Unless otherwise specified, Ta=25°C, VCC=15V)

Parameters	Symbol	Limits			Unit	Comments
		Min	Typ	Max		
<b>[ DC/DC Protection Function ]</b>						
Switching Max Duty	Dmax	85.0	87.5	90.0	%	OSC=GND
Current Sensing Time	T <sub>isns<sub>t</sub></sub>	160	200	240	nsec	
ISNS OVP Trigger Voltage	V <sub>ovp</sub>	2.25	2.50	2.75	V	
ZT OVP Voltage	V <sub>ZTL</sub>	2.80	3.00	3.20	V	
Latch Release Voltage (VDD_UVLO)	V <sub>LATCH</sub>	2.40	2.65	2.90	V	While VDD is decreasing
Latch Mask Time	T <sub>LATCH</sub>	60	100	140	usec	
<b>[ Dimming Control ]</b>						
DIMSEL Pin H Input Voltage	VDIMSELH	0.7×VDD	-	VDD+0.3	V	
DIMSEL Pin M Input Voltage	VDIMSELM	1.20	1.45	1.70	V	
DIMSEL Pin L Input Voltage	VDIMSELL	-0.3	-	0.3	V	
DIM Pin PWM H Input Voltage	VDIMH	0.7×VDD	-	VDD+0.3	V	DIMSEL=VDD (PWM dimming)
DIM Pin PWM L Input Voltage	VDIML	-0.3	-	0.3×VDD	V	DIMSEL=VDD (PWM dimming)
DIM pin Start Input Voltage (LINEAR Dimming Mode)	VDIMLIN	-	-	0.4	V	DIMSEL=1.45V (LINEAR dimming)
<b>[ VHV Input Control Block ]</b>						
VHV Input DUTY H Voltage	DetPh	150	250	350	mV	While VHV is increasing
VHV Input DUTY L Voltage	DetPl	75	125	175	mV	While VHV is decreasing
VI_ON Setting VHV Input Voltage	DetSTRG	560	625	690	mV	
VHV Pin Input Voltage Range	VVHV	-0.3	-	9.0	V	
VHVOVP Trigger Voltage	V <sub>VHVOVP1</sub>	4.50	5.00	5.50	V	
VI Pin ON Resistance	R <sub>onVI</sub>	-	10	100	Ω	I <sub>VI</sub> =2mA Sink
VI Pin OFF Leakage Current	I <sub>LeakVI</sub>	-	-	1.0	uA	VI=10V
<b>[ State Setting Input Block ]</b>						
ISOSEL Pin H Input Voltage	VISOH	0.7×VDD	-	VDD+0.3	V	
ISOSEL Pin L Input Voltage	VISOL	-0.3	-	0.3×VDD	V	
BSTDC Pin H Input Voltage	VBSTH	0.7×VDD	-	VDD+0.3	V	
BSTDC Pin L Input Voltage	VBSTL	-0.3	-	0.3×VDD	V	

## Pin Configuration

Table 1. I/O PIN Functions

No.	Pin Name	I/O	Function	ESD Protection System		
				VCC	VDD	GND
1	VCC	I	Supply Voltage			○
2	VI	O	Phase Angle Detection			○
3	DIMSEL	I	Dimming Mode Selection			○
4	DIM	I	Dimming Signal			○
5	GND	I	GND pin	○		
6	VHV	I	Phase Angle Detection			○
7	OSC	O	Switching Frequency			○
8	ISOSEL	I	Non-isolated/Isolated Control Selection L : buck / H : fly-back		○	○
9	GND	I	GND pin	○		
10	BSTDC	O	Output Mode Selection while Dimming L : DC Output / H : DC + BURST Output		○	○
11	ISNS	I	Feedback Signal			○
12	OUT	O	Gate Driver Pin of Switching MOS			○
13	ZT	I	Zero Current Detection			○
14	VDD	O	Regulator Output / Internal power supply 3.3V			○

I/O Equivalent Circuit Diagram

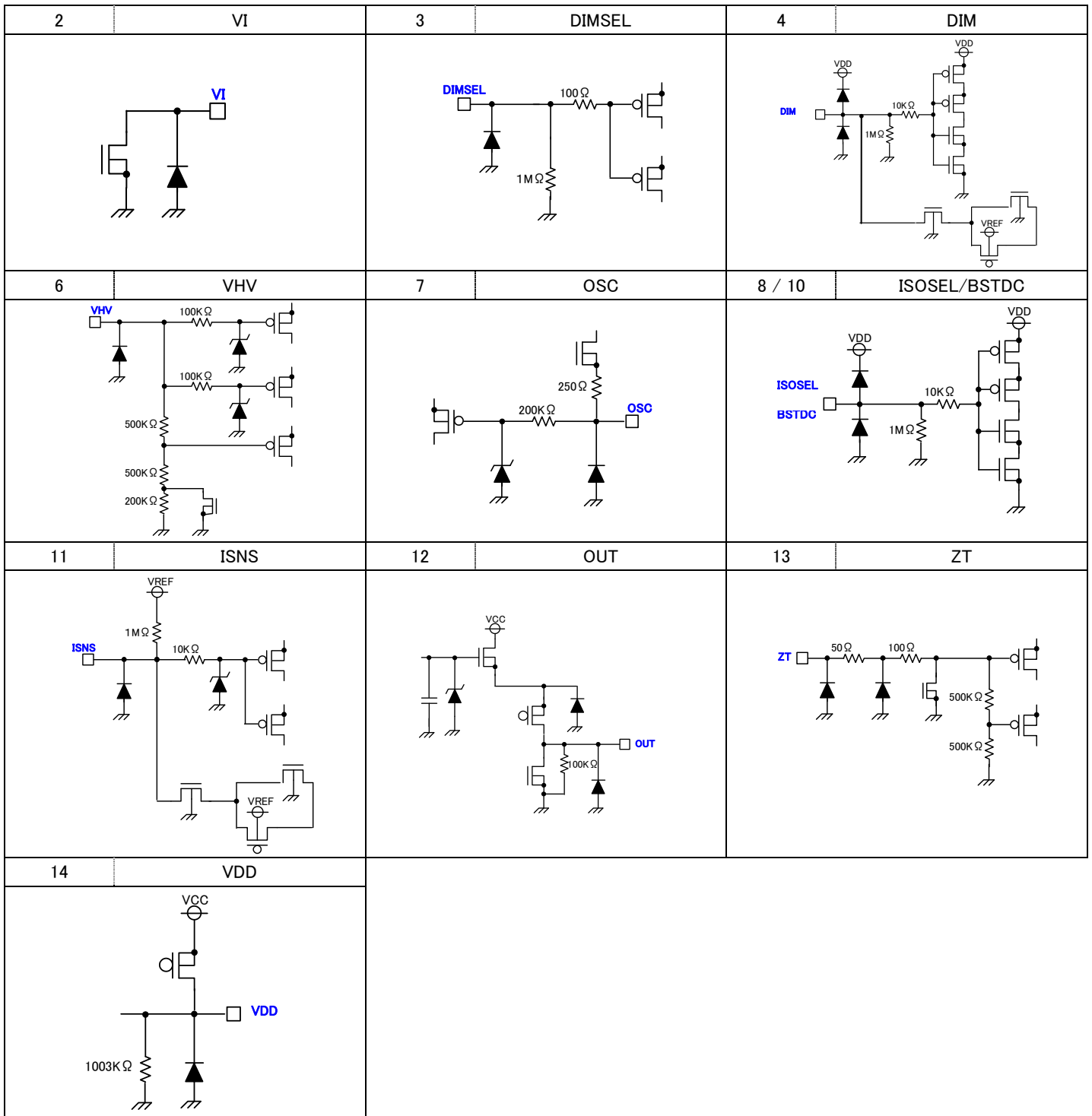


Figure 2. I/O Equivalent Circuit Diagram

Block Diagram

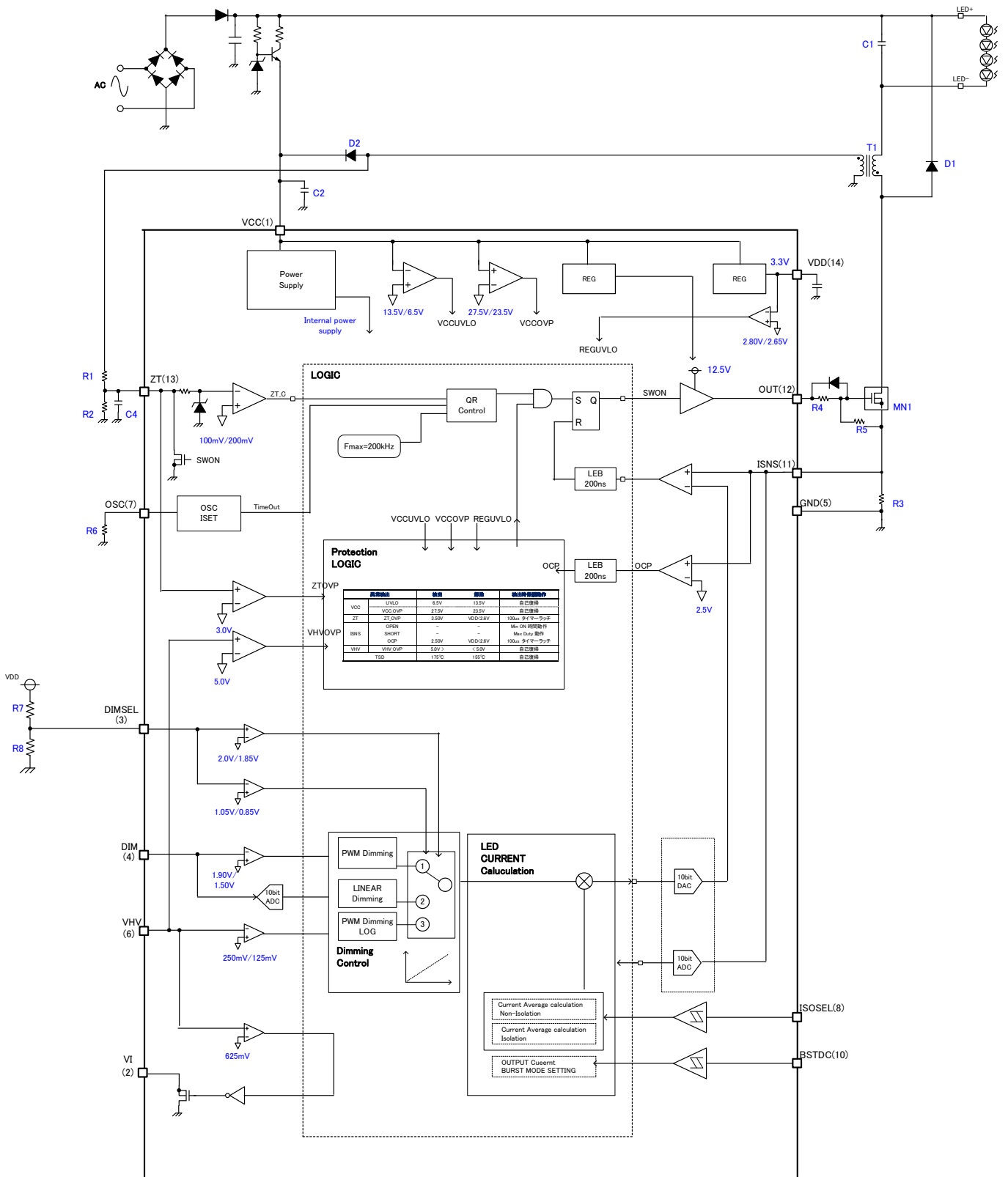


Figure 3. BD552JL Block Diagram

## Block Descriptions

## ( 1 ) Bootstrap Circuit

## ( 1 -1) Start Sequence

The details for each block are described in following sections.

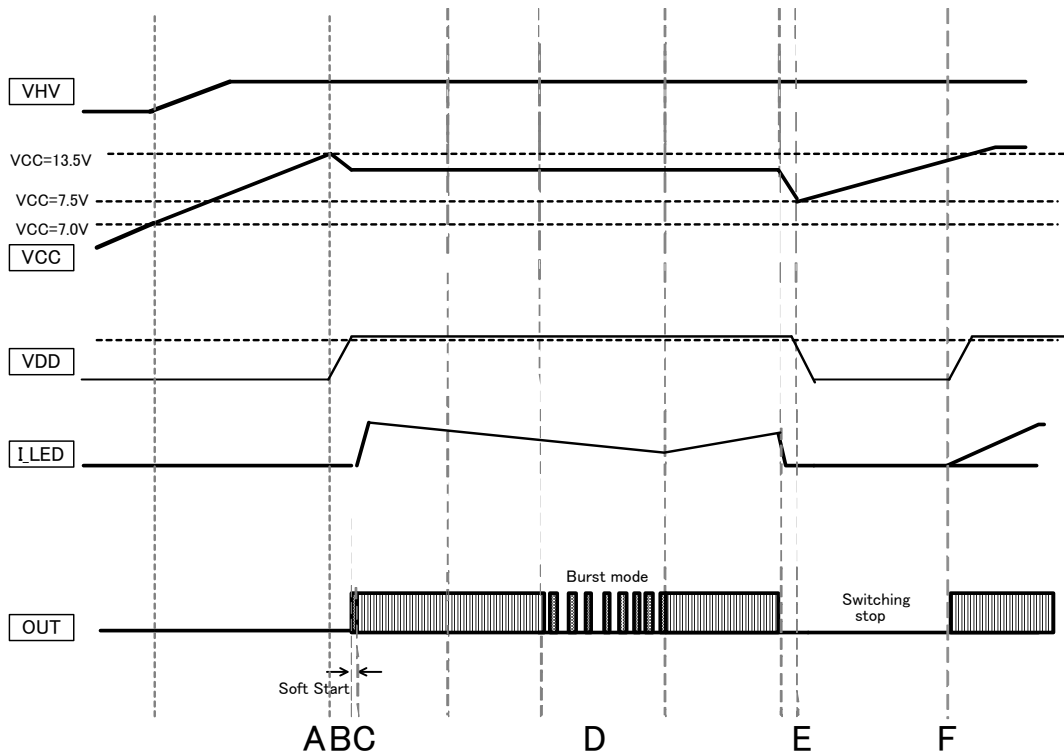


Figure 4. Start Sequence

**A** : VCC pin voltage (1pin) increases, when  $VCC > VUVLO1$  (typ =13.5V) . The IC starts to work.

When the protection function is normal, the switching begins. In this case, due to the power consumption of VCC pin, the voltage of VCC has to be decreased. While the power supply circuit, which is composed by the transistor auxiliary winding of the DCDC section, is set, the power supply to VCC is possible by the switching operation.

**B** : Due to the built-in soft start function, the voltage of ISNS pin (11pin) can be adjusted without an excessive voltage or increase in current. (soft start time : typ =100ms)

**C** : While the switching begins, the LED turns ON.

**D** : When reducing the LED current to a low dimming rate, the LED is turned on by BURST operation. (BSTDC=H)

**E** : VCC pin voltage (1pin) decreases, when the VCC pin voltage (1pin)  $< VUVLO2$  (typ =6.5V) ,  $VCCUVLO$  is triggered and the switching stops. At this time, the bootstrap circuit works, and starts to charge the VCC pin (1pin) .

**F** : When the VCC pin voltage (1pin)  $> VUVLO1$  (typ =13.5V) , the switching operation restarts, and the charging is proceeded by the auxiliary winding of the transistor. Then, charging from the bootstrap circuit stops.

(2) DC/DC Driver

The control mode used in this IC is PFM (Pulse Frequency Modulation) mode. By monitoring the ISNS pin (11pin) and ZT pin (13pin), it supports an optimum system as DC/DC. The ON duty (turn OFF) of the switching MOSFET is controlled by ISNS pin(11pin), and the OFF duty (turn ON) is controlled by ZT pin (13pin). The details are explained as follows. (refer to Figure 5)

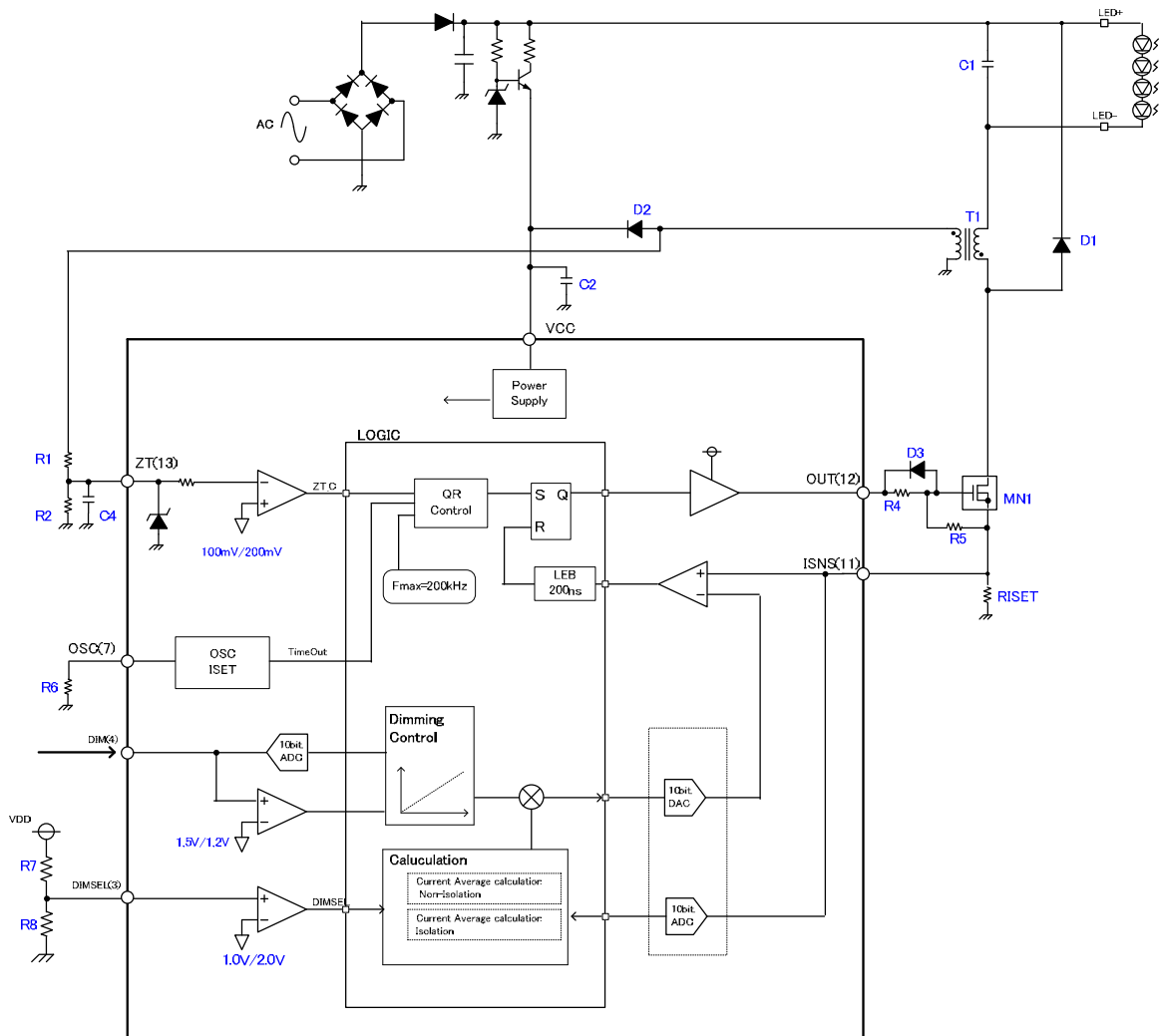


Figure 5. DCDC Block Diagram



**(2-1) ON Duty Operation (Turn OFF) of the LED Current Control**

By monitoring the coil current through the ISNS pin during the ON phase of the switching, the switching controller controls the average current in the coil to keep the value to what is set by the R3 resistor. In the example of the application circuit shown in Figure 6, while the MN1 is OFF, the current flows through the regenerative diode.

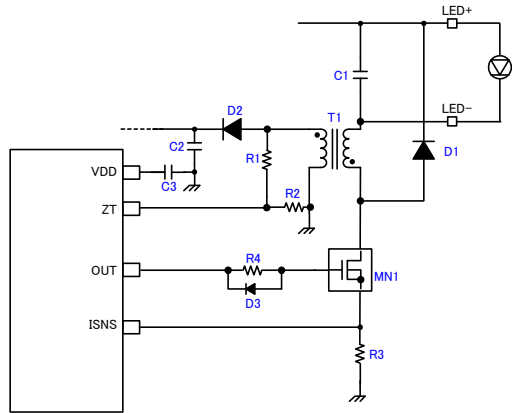


Figure 6. Current Control Section Application Circuit

The setting of the LED current is determined by controlling the average current in the coil. The average LED current ILED\_AVE can be set by the resistor R3 which is connected to the ISNS pin. The set current can be calculated by the formula below, and VISNS which is the voltage for the average current setting is 500mV(typ).

- ① Buck Converter Non-isolated Topology (ISOSEL=L)

$$I_{LED\_AVE} = \frac{VISNS}{R3}$$

- ② Fly-back Converter Isolated Topology (ISOSEL=H)

$$I_{LED\_AVE} = \frac{VISNS}{R3} \sqrt{\frac{Lp}{Ls}}$$

While using the Fly-back topology, Lp, Ls means the L value of the primary side and the secondary side of T1 respectively.

LED Current Setting by R3 (Buck or Fly-back Lp:Ls=1:1)

R3	Average LED Current
5.10Ω	98mA
2.00Ω	250mA
1.50Ω	333mA
1.00Ω	500mA
0.75Ω	667mA
0.68Ω	735mA

In case of Fly-back topology, due to the dispersion of the transistor turn ratio of the primary and secondary side, and the power supply to the auxiliary winding, there may be a difference between the theoretical value and the true value of the LED current. In this case, the value of the R3 has to be adjusted.

**(2-2) LEB (Leading Edge Blanking) Function**

While the switching MOSFET turns ON, surge current is produced due to parasitic capacitance and drive current causing the voltage of ISNS pin(11pin) to increase for a moment which may result to a false detection in circuit current limit. For preventing the ISNS pin from false detection, after OUT pin (5pin) L->H, a blanking function, which masks the ISNS pin for  $T_{LEB}$  (typ=200ns) time is built in. Owing to this blanking function, the noise filter can be reduced.

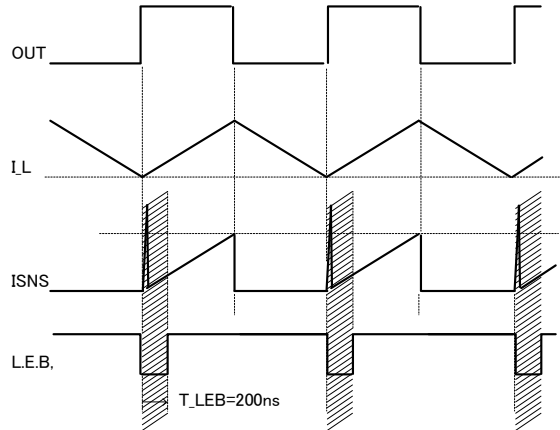


Figure 7. LEB Operation while ISNS detected

**(2-3) OFF Duty Operations (Turn ON)**

The OFF duty control is proceeded by the ZT pin (13pin). During the OFF phase of the switching, secondary output capacitor is charged by the electric power which is stored in the coil. When the charging is over, the current in the secondary side becomes zero, triggering the resonance operation to start. The resonance operation is caused by the capacitance between the transistor and the  $V_{ds}$  of the MOSFET. This resonance waveform is divided by R1 and R2, and the resulting voltage is serves as an input to ZT pin (13pin). When this voltage level is lower than  $V_{ZT}$  (typ=100mV), the bottom is triggered by the ZT comparator. The real bottom and the trigger time of the comparator can be adjusted by the time constant decided by C4, R1 and R2 which are set around the ZT pin (13pin).

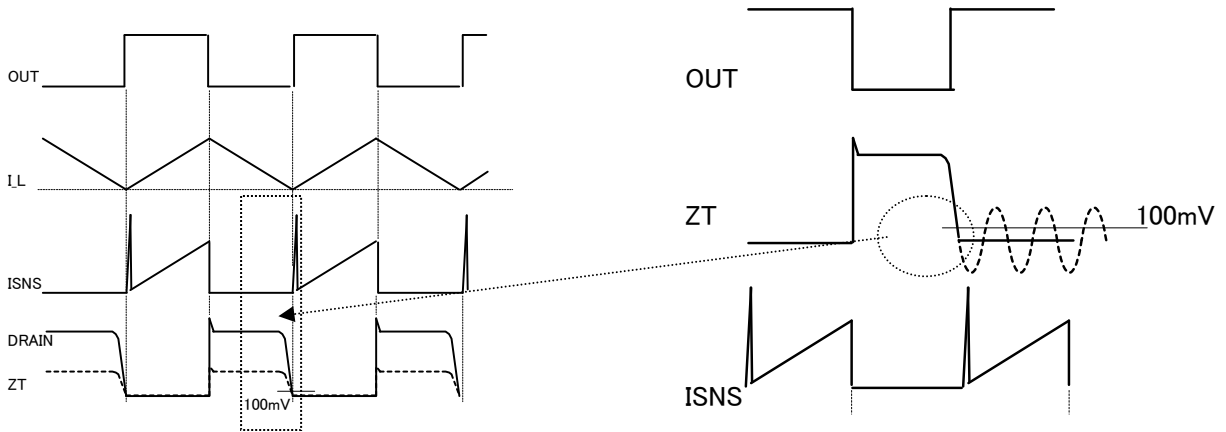


Figure 8. Zero-cross Trigger by ZT Pin

Otherwise, a ZT trigger mask function (instructed in 2-4) and a ZT timeout function (instructed in 2-5) are built in.

**(2-4) ZT Trigger Mask Function**

During the switching from ON to OFF, the noise may occur at ZT pin (13pin).

In this case, to prevent the ZT pin from malfunctioning, the function of ZT pin is masked for a  $T_{ZTMASK}$  time (typ=600ns).

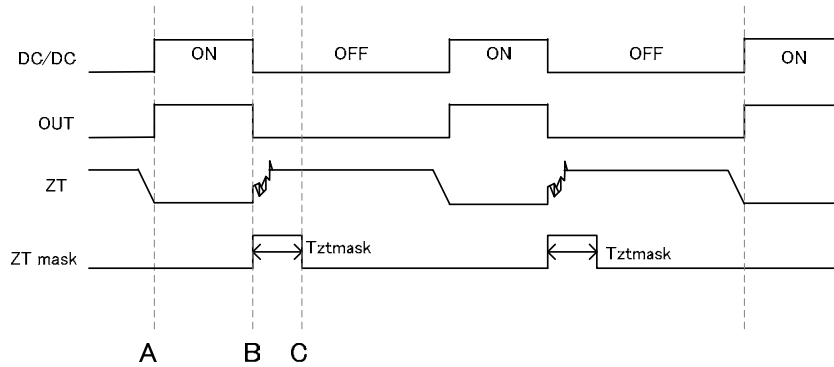


Figure 9. ZT Trigger Mask Function

- A: DC/DC OFF=>ON
- B: DC/DC ON=>OFF
- C: Due to the noise that may occur at ZT pin, the function of ZT pin is masked for a  $T_{ZTMASK}$  time.

**(2-5) ZT Timeout Function**

After the signal is triggered by ZT converter and the next trigger does not occur at a given time (Timeout Time), the switching turns ON forcibly. While the secondary output voltage is low such as when the IC starts, the auxiliary winding voltage  $V_A$  becomes low too, and the voltage of ZT pin (1pin) is lower than  $V_{ZT2}$  (typ =100mV). In this case, the ZT timeout function makes the switching turning ON forcibly.

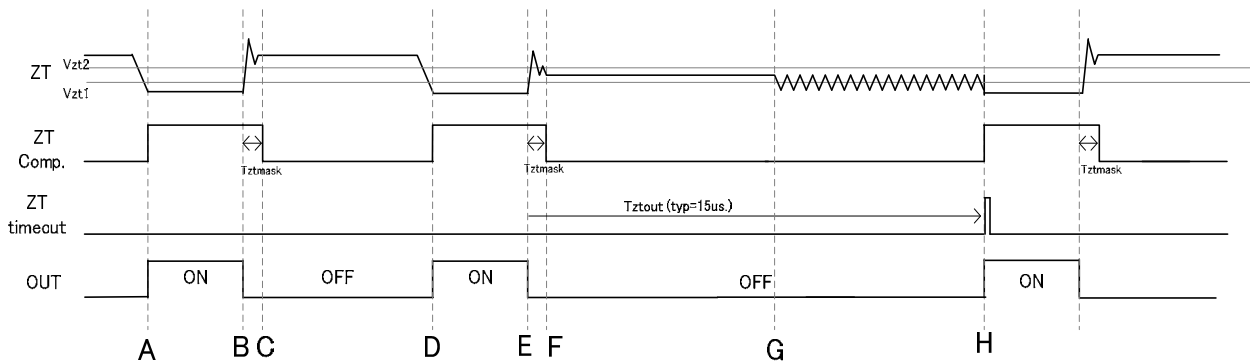


Figure 10. ZT Timeout Function

- A:  $ZT < V_{ZT1}$ , OUT turns ON by the bottom trigger.
- B: DC/DC ON=>OFF and  $ZT > V_{zt2}$ , the timeout function does not work.
- C: The noise occurs at ZT pin, due to the  $T_{ZTMASK}$ , ZT comparator does not work.
- D:  $ZT < V_{zt1}$ , OUT turns ON by the bottom trigger.
- E: DC/DC ON=>OFF and  $ZT < V_{zt2}$ . From this point of time, the timeout function works.
- F: Same as C.
- G: The timeout operation continues during  $ZT < V_{zt2}$ .
- H: During  $T_{ZTOUT}$ , due to the state of  $ZT < V_{zt2}$  holds all the time, DC/DC OFF=>ON forcibly. (timeout operation)

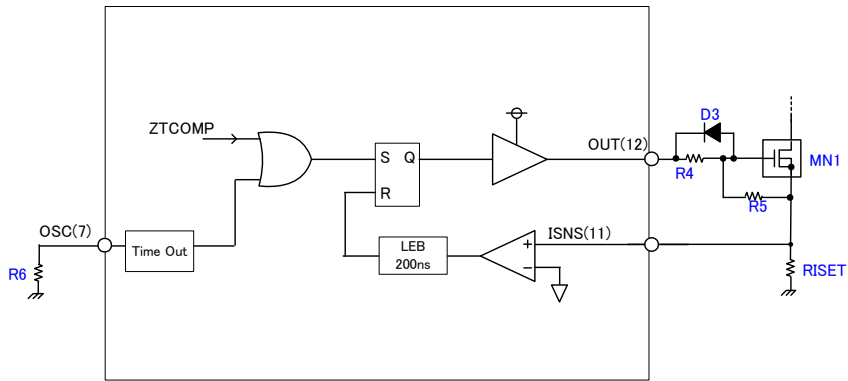


Figure 11. OSC Pin Setting

Timeout time can be set by the resistance which is connected to the OSC pin (7pin), and when there is no bottom trigger by ZT, the switching operation follows the timeout operating frequency showed in Table 2 below.

When the timeout frequency is set to be too high, due to the output of the OUT pin becomes H before the boundary conduction mode works, if there is no limit on the minimum operating frequency, please set the timeout operating frequency to 20kHz by shorting the OSC pin to the GND.

Table 2. OSC Pin Resistance and Timeout Operating Frequency

OSC Pin Resistance R6	Timeout Operating Frequency
OPEN	100kHz
300k Ω	28kHz
150k Ω	50kHz
68k Ω	120kHz
27k Ω	300kHz
GND	20kHz

**(3) Conversion of Non-isolated Topology / Isolated Topology**

This IC can support applications of both non-isolated (Buck converter) and isolated (Fly-back) topology by setting the ISOSEL pin.

Item	Symbol	Min	Typ	Max	Unit	Settings
ISOSEL pin H input voltage	$V_{ISO\_ENH}$	$0.7 \times VDD$	-	$VDD+0.3$	V	Isolated driver selection
ISOSEL pin L input voltage	$V_{ISO\_ENL}$	-0.3	-	$0.3 \times VDD$	V	Non-isolated driver selection

**(3-1) Non-isolated Topology (Buck converter)**

An application with non-isolated Buck converter can be selected by shorting the ISOSEL pin to the GND pin to gain a low level. By this setting, the circuit inside the IC for calculating the LED current is based on Buck topology. The basic application circuit is shown in Figure 12.

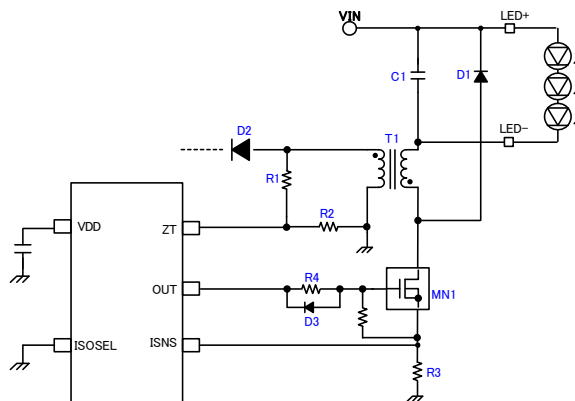


Figure 12. Non-isolated Buck Converter Circuit

**(3-2) Isolated Topology (Fly-back Converter)**

An application with isolated Fly-back topology can be selected by shorting the ISOSEL pin to the VDD pin to gain a high level. Monitoring the current in the coil by the ISNS pin, an isolated application with a high current control precision can be achieved even without the photocoupler.

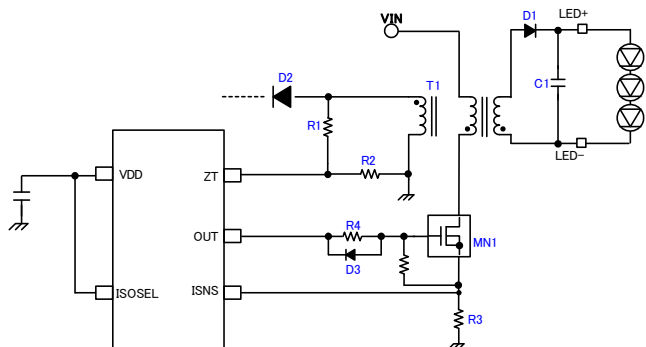


Figure 13. Isolated Fly-back Converter Circuit

(4) Dimming Operations

(4-1) Dimming Modes

This IC supports dimming modes of both the ON duty of the pulse signal and the DC signal level. The shift between PWM dimming mode and the LINEAR dimming mode can be achieved by setting DIMSEL pin (3pin). The block diagram of the dimming settings is shown in Figure 14. In addition, the selection of the dimming modes which is decided by the DIMSEL (3pin) voltage is shown in the table below.

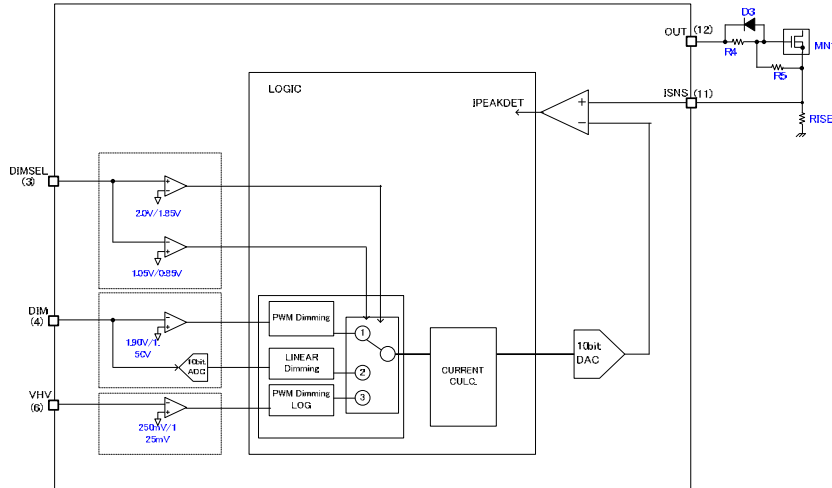
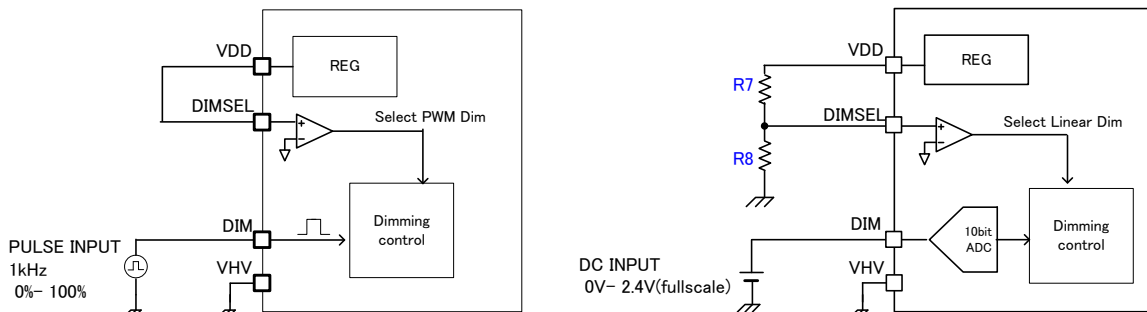


Figure 14. Dimming Mode Setting using DIMSEL Pin

Item	Symbol	Min	Typ	Max	Unit	Settings
DIMSEL pin H input voltage	$V_{ISO\_ENH}$	$0.7 \times VDD$	VDD	$VDD+0.3$	V	DIM pin input : PWM dimming
DIMSEL pin M input voltage	$V_{ISO\_ENL}$	1.20	1.45	1.70	V	DIM pin input : LINEAR dimming
DIMSEL pin L input voltage	$V_{ISO\_ENL}$	-0.3	-	0.3	V	VHV pin input : PWM dimming

The DIMSEL pin settings are shown in Figure 15. ①PWM dimming mode setting by shorting DIMSEL pin to VDD pin, ② LINEAR dimming mode setting by shorting DIMSEL pin to the VDD voltage divider R7 and R8 (Recommended : R7=56kΩ, R8=43kΩ). For the dimming signal to input to DIM pin, please refer to the table below.



①Circuit Example for Pin Settings of PWM Dimming Mode ②Circuit Example for Pin Settings of LINEAR Dimming Mode

Figure 15. DIMSEL Pin Settings and Dimming Inputs

**DIMSEL=H: PWM Dimming Settings**

Item	Symbol	Min	Typ	Max	Unit	Settings
DIM pin H input voltage	VDIMH	$0.7 \times VDD$	-	$VDD+0.3$	V	DIMSEL=VDD (PWM dimming)
DIM pin L input voltage	VDIML	-0.3	-	$0.3 \times VDD$	V	DIMSEL=VDD (PWM dimming)
DIM pin PWM dimming frequency range	FDIM	0.08	-	4.1	kHz	DIMSEL=VDD (PWM dimming)

**DIMSEL=M: LINEAR Dimming Settings**

DIM pin LINEAR dimming input voltage range	VDIMH	0.3	-	2.4	V	DIMSEL=1.45V (LINEAR Dimming)
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**(4-2) LED Current Output Mode**

In each dimming mode, when a low dimming rate of less than 20% of LED current is needed, the BURST mode for LED output current can be selected. BY setting BSTDC=H, the LED output driver enters BURST operation. Hence, a deep dimming operation can be achieved. The settings for BSTDC pin are shown in the table below.

Item	Symbol	Min	Typ	Max	Unit	Settings
BSTDC pin H input voltage	$V_{BSTDCH}$	$0.7 \times VDD$	-	$VDD+0.3$	V	DC+BURST output setting
BSTDC pin L input voltage	$V_{BSTDCL}$	-0.3	-	$0.3 \times VDD$	V	DC output setting

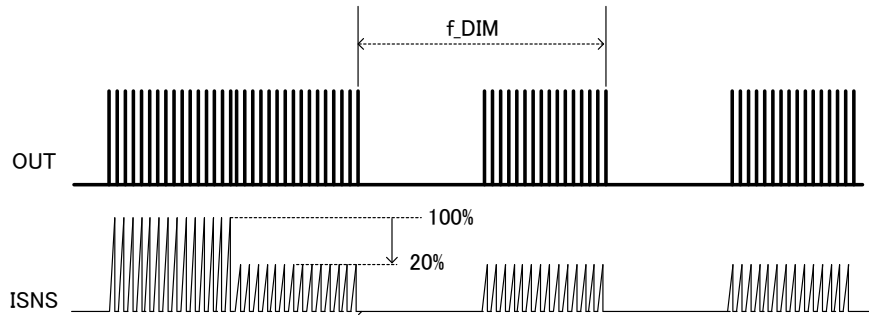
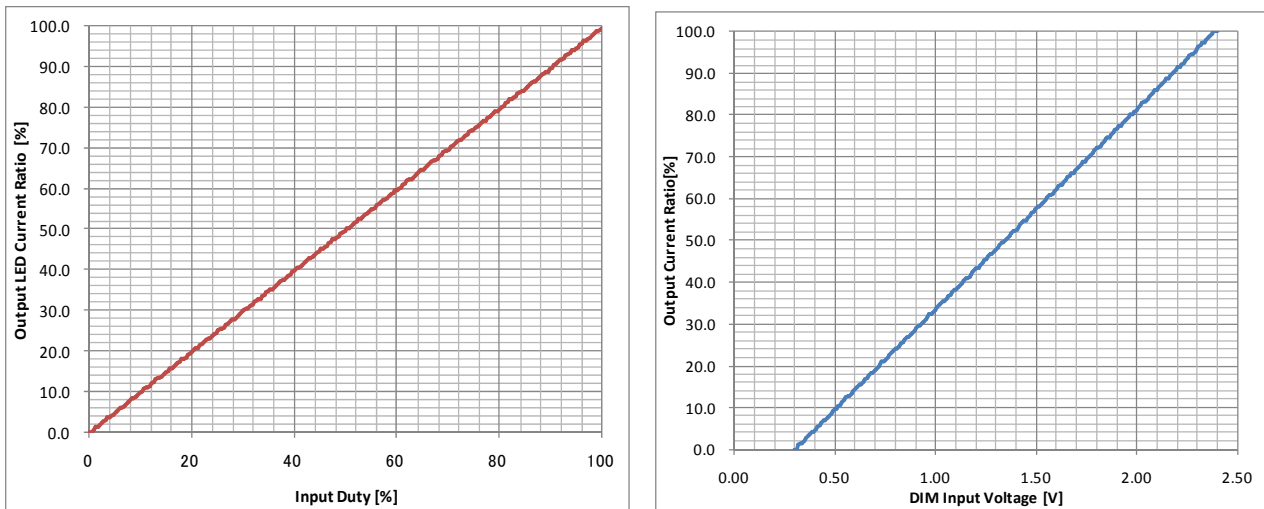


Figure 16. Dimming by BURST Output

When the dimming rate is lower than 20%, the BURST mode operates, as shown in Figure 16, with BURST frequency pf 900Hz (typ), the LED current reduces with a decrease of the output time of the OUT pin which follows the decrease in the dimming proportion.

**(4-3) LED Dimming Curve**

The characteristic curves which show the proportion of the output current in each dimming mode are shown in Figure 17.



① PWM Dimming Characteristic

② LINEAR Dimming Characteristic

Figure 17. Dimming Characteristic Curves

**(5) Protection Functions**

**(5-1) VCC UVLO**

VCC UVLO function is achieved by a self-reset comparator which has a voltage hysteresis. The operation of this function is shown in Figure 18.

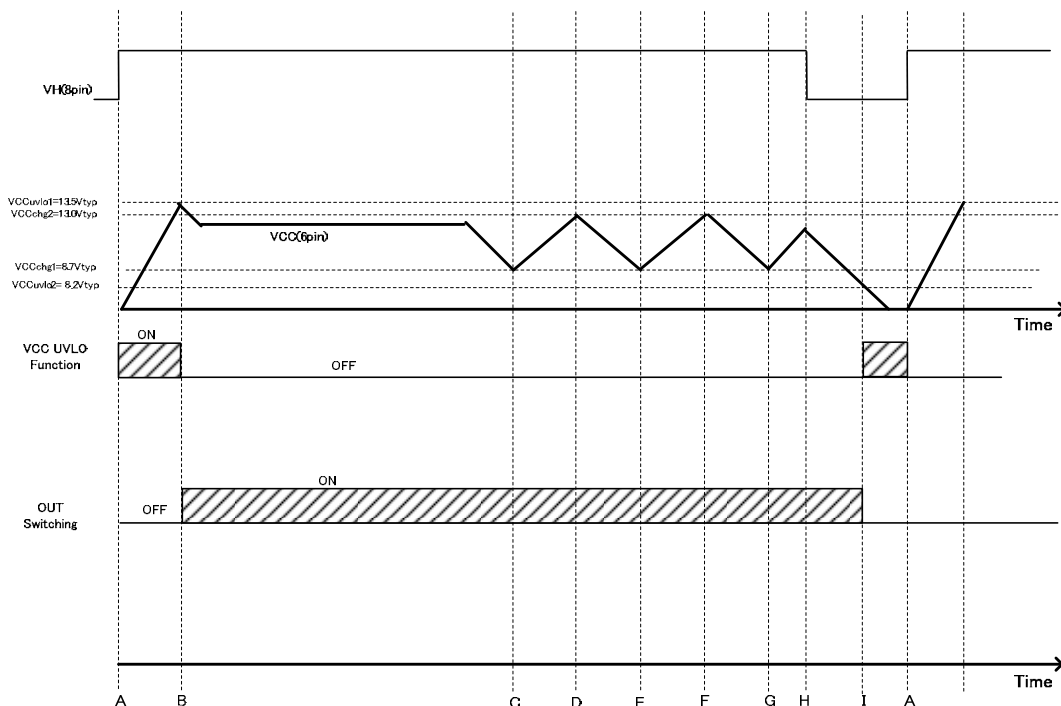


Figure 18. VCC UVLO Time Chart

**(5-2) ZT Pin (13pin) OVP(Over Voltage Protection)**

OVP (Over Voltage Protection) function is built in ZT pin (13pin). The protection mode for OVP protection is latch. ZT OVP function supports a DC trigger to ZT pin. To prevent ZT OVP from malfunctioning,  $T_{LATCH}$  (typ=100us) timer is built in.



**(5-3) ISNS Pin (11pin) OPEN Protection**

When the ISNS pin (11pin) is OPEN, to prevent the OUT pin (12pin) from malfunctioning caused by noise, an OPEN protection circuit for ISNS pin is built in. The switching of the OUT pin (12pin) stops. (100us timer latch protection) when the ISNS pin (11pin) is OPEN.

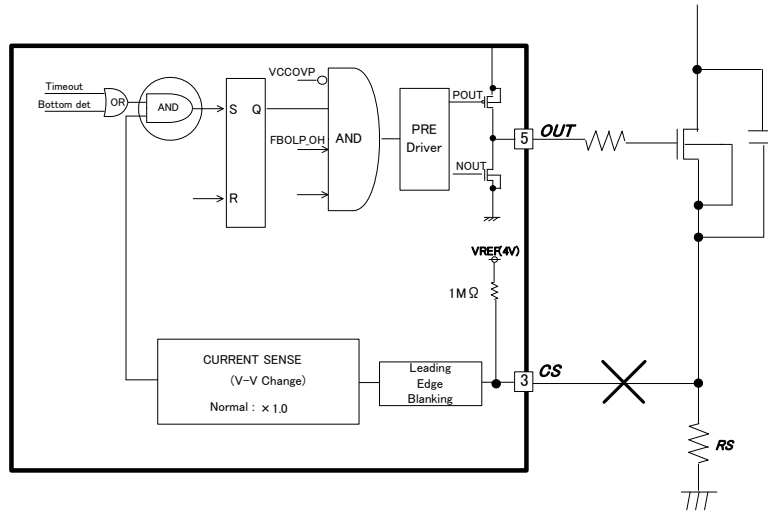


Figure 19. ISNS Pin OPEN Protection Circuit

**(5-4) OUT Pin (12pin) Clamp Function**

To protect the external MOSFET, the H level of the OUT pin is clamped at  $V_{OUTH}$  (typ=12.5V). This function prevents the damaging the MOSFET which is caused by the rising of the voltage of VCC pin (1pin). The OUT pin (12Pin) is pulled down by  $R_{PDOUT}$  (typ=100kΩ) internally.

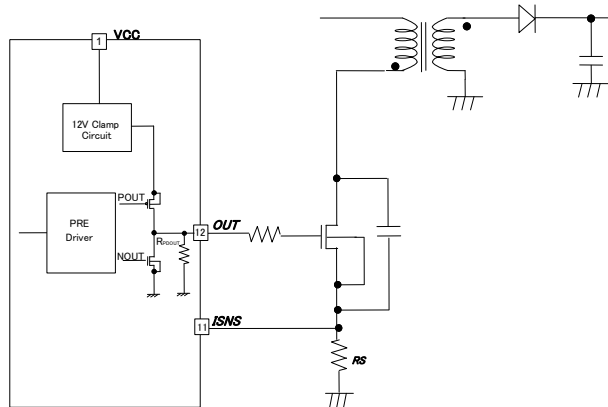


Figure 20. OUT Pin (12pin) Schematic

**Operation Modes of Protection Circuit**

All operation modes of the different protection circuits are shown in Table 4.

Table 4. Operation Modes of Protection Circuit

Anomaly Detection		Trigger	Release	Protecting Operation While Triggered
VCC	UVLO	6.5V	13.5V	Self-reset
	VCC_OVP	27.5V	23.5V	Self-reset
ZT	ZT_OVP	3.00V	VDD<2.6V	100us timer latch
ISNS	OPEN	-	-	Min ON time operation
	SHORT	-	-	Max Duty operation
	OC	2.50V	VDD<2.6V	100us timer latch
VHV	VHV_OVP	5.0V >	< 5.0V	Self-reset
TSD		175°C	155°C	Self-reset

**Power Dissipation**

According to the thermal design, please observe the conditions below when using this IC.  
 (The temperatures shown below are guaranteed temperatures, please consider the margin during application.)

1. The ambient temperature  $T_a$  must be 105°C or less.
2. The consumption of the IC must be within the allowable dissipation  $P_d$ .

The thermal dissipation characteristics are as follows.  
 (PCB: 70 mm x 70mm x 1.6 mm, mounted on glass epoxy substrate)

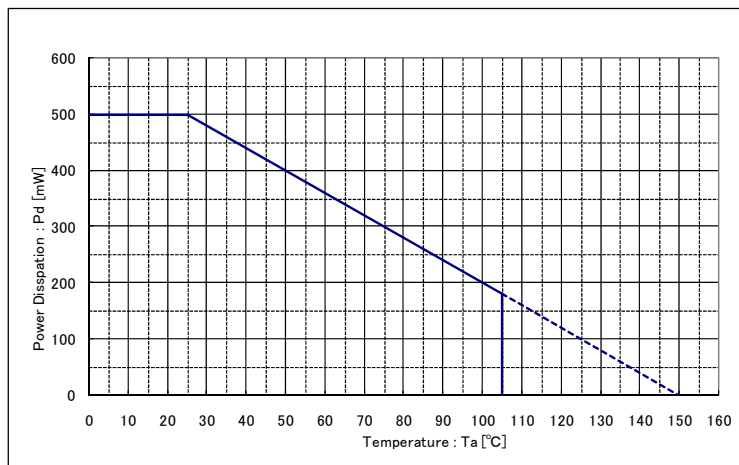


Figure 21-1. SSOP-B14 Thermal Dissipation Characteristics

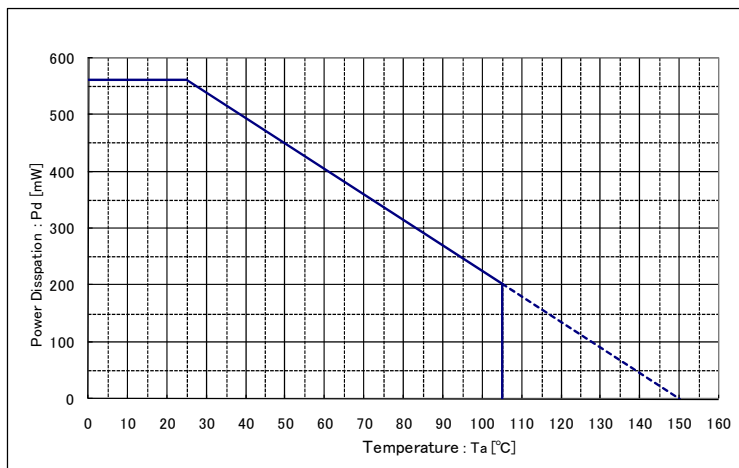


Figure 21-2. SOP14 Thermal Dissipation Characteristics

## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

### 6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

### 7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

### 9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

## Operational Notes – continued

**11. Unused Input Terminals**

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

**12. Regarding the Input Pin of the IC**

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When  $GND > Pin A$  and  $GND > Pin B$ , the P-N junction operates as a parasitic diode.  
When  $GND > Pin B$ , the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

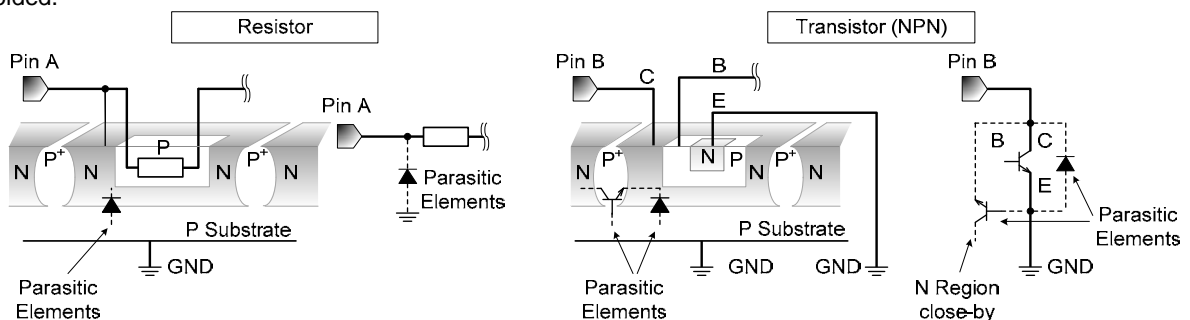


Figure xx. Example of monolithic IC structure

**13. Ceramic Capacitor**

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

**14. Area of Safe Operation (ASO)**

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

**15. Thermal Shutdown Circuit(TSD)**

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature ( $T_j$ ) will rise which will activate the TSD circuit that will turn OFF all output pins. When the  $T_j$  falls below the TSD threshold, the circuits are automatically restored to normal operation.

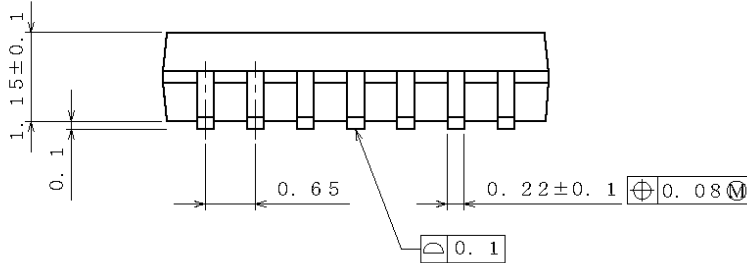
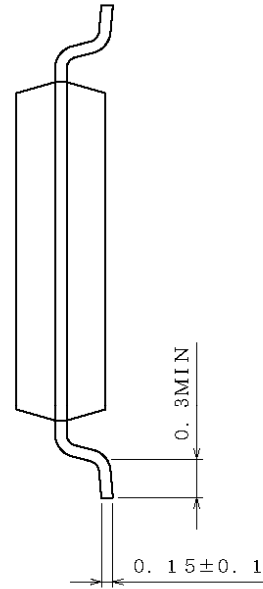
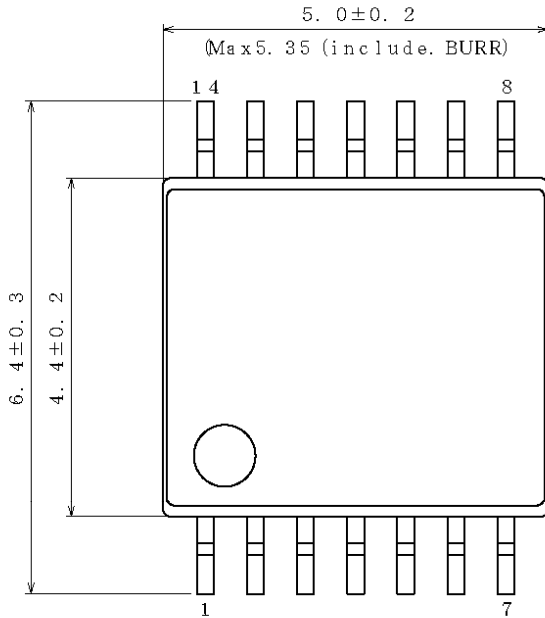
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

**16. Over Current Protection Circuit (OCP)**

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Physical Dimension, Tape and Reel Information

Package Name	SSOP-B14
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(UNIT : mm)  
 PKG : SSOP-B14  
 Drawing No. EX152-5002

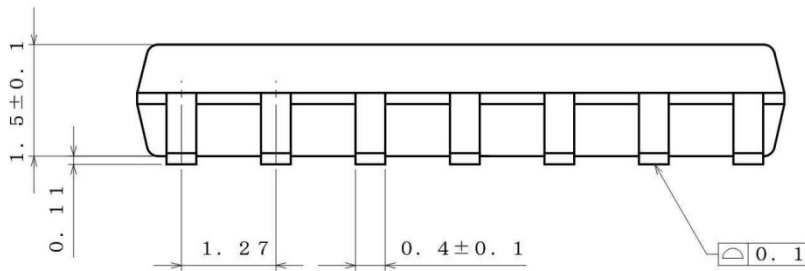
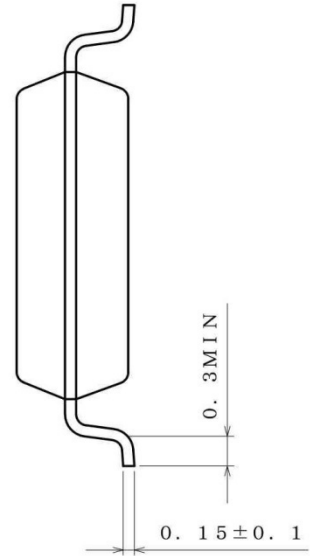
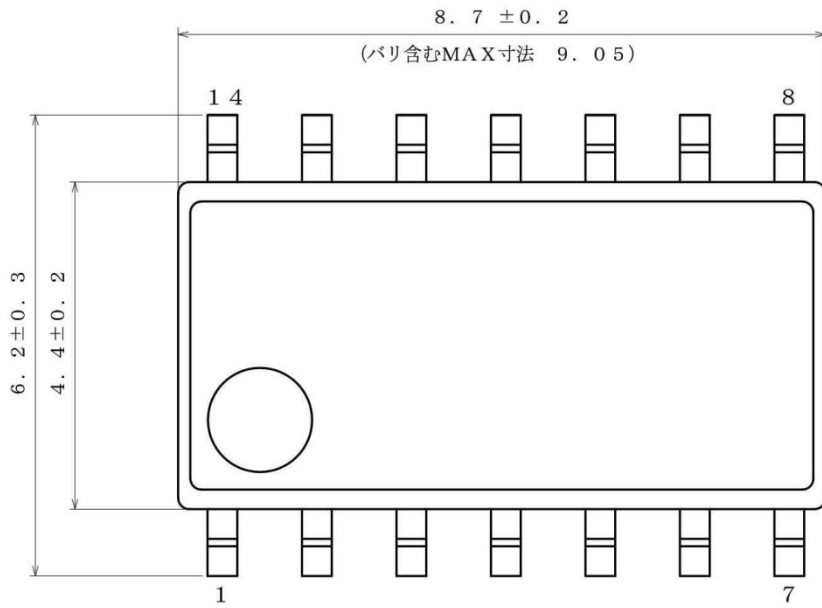
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 ( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand )

Reel      1pin      Direction of feed

\*Order quantity needs to be multiple of the minimum quantity.

Package Name	SOP14
--------------	-------



(UNIT : mm)  
 PKG : SOP14  
 図番 : EX113-5001

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 ( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand )

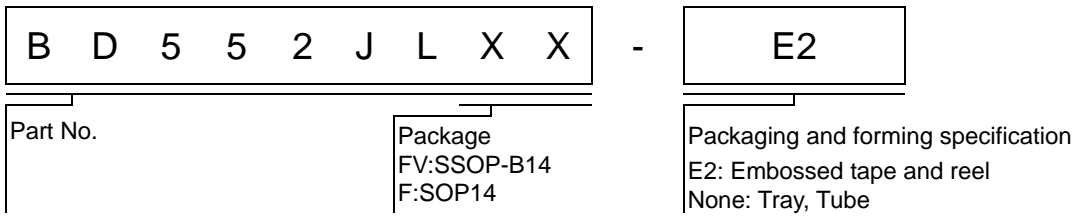
Reel

1pin

Direction of feed

\*Order quantity needs to be multiple of the minimum quantity.

Ordering Information



Marking Diagram

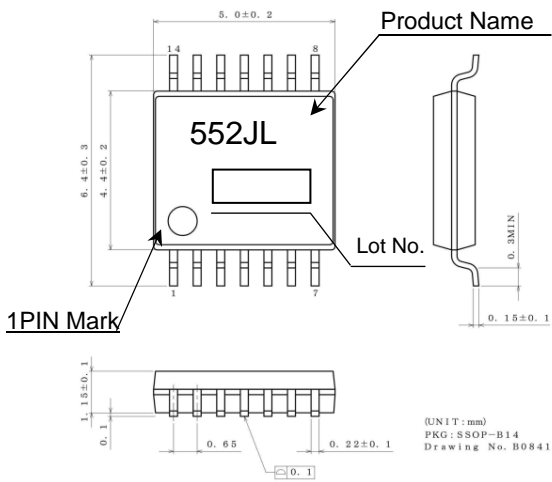


图-22-1 SSOP-B14 Package View

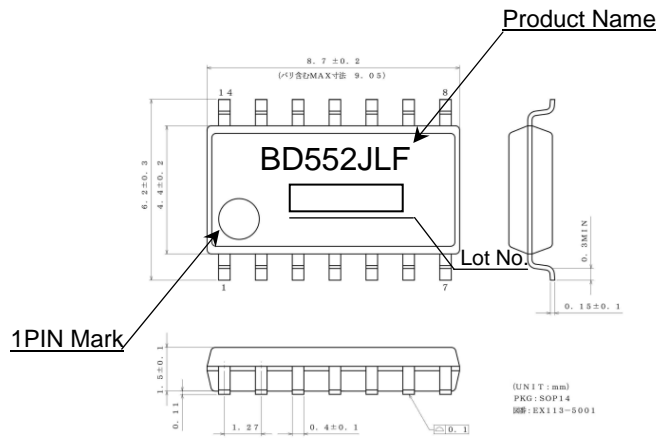


图-22-2 SOP14 Package View

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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  - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
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  - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
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- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
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- Confirm that operation temperature is within the specified range described in the product specification.
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  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
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