AS8202NF

DataSheet

TTP-C2NF Communication Controller

1 General Description

The AS8202NF communication controller is an integrated device supporting serial communication according to the TTP specification version 1.1. It performs all communication tasks such as reception and transmission of messages in a TTP cluster without interaction of the host CPU. TTP provides mechanisms that allow the deployment in high-dependability distributed real-time systems. It provides the following services:

- Predictable transmission of messages with minimal jitter
- Fault-tolerant distributed clock synchronization
- Consistent membership service with small delay
- Masking of single faults

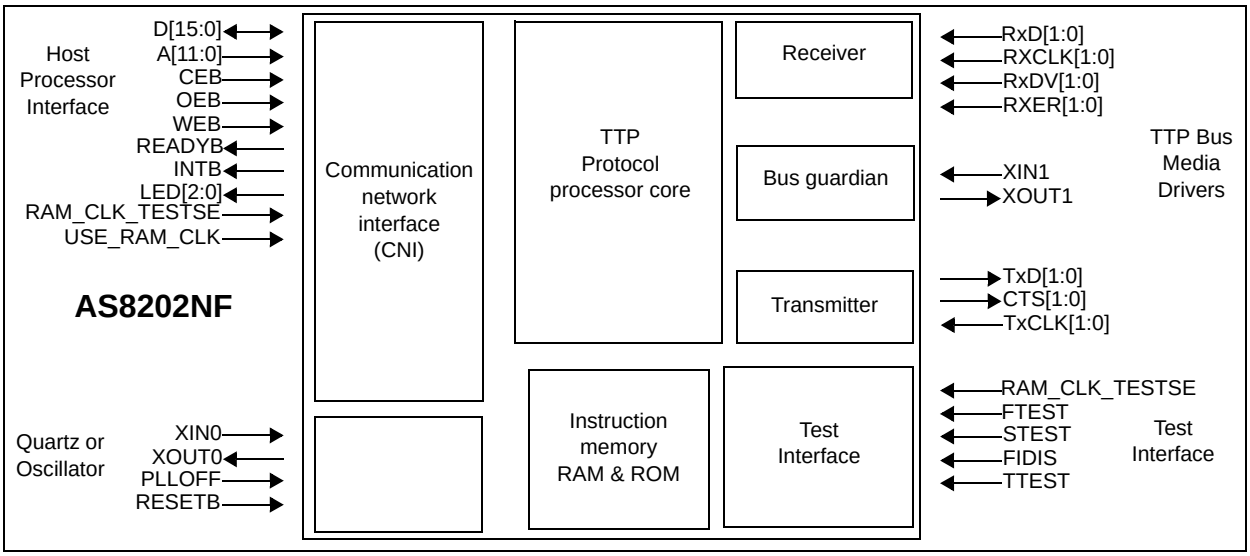
2 Key Features

- Dual-channel controller for redundant data transfers
- Dedicated controller supporting TTP (time-triggered protocol class C)
- Suited for dependable distributed real-time systems with guaranteed response time
- Asynchronous data rate up to 5 Mbit/s (MFM/ Manchester)
- Synchronous data rate 5 to 25 Mbit/s
- Bus interface (speed, encoding) for each channel selectable independently
- 40 MHz main clock with support for 10 MHz crystal, 10 MHz oscillator or 40 MHz oscillator
- 16 MHz bus guardian clock with support for 16 MHz crystal or 16 MHz oscillator
- Single power supply 3.3V, 0.35µm CMOS process
- Full automotive temperature range (-40ºC to 125ºC)
- 16k x 16 SRAM for message, status, control area (communication network interface) and for scheduling information (MEDL)
- 4k x 16 (plus parity) instruction code RAM for protocol execution code
- Data sheet conforms to protocol revision 2.04
- 16k x 16 instruction code ROM containing startup execution code and deprecated protocol code revision 1.00
- 16 Bit non-multiplexed asynchronous host CPU interface
- 16 Bit RISC architecture
- Software tools, design support, development boards available (www.tttech.com)
- Certification support package according to RTCA/ DO-254 DAL A available (www.tttech.com)
- 80 pin LQFP80 Package

3 Applications

Application fields: automotive (by-wire braking, steering, vehicle dynamics control, drive train control), aerospace (aircraft electronic systems), industrial systems, railway systems.

Figure 1. Block Diagram



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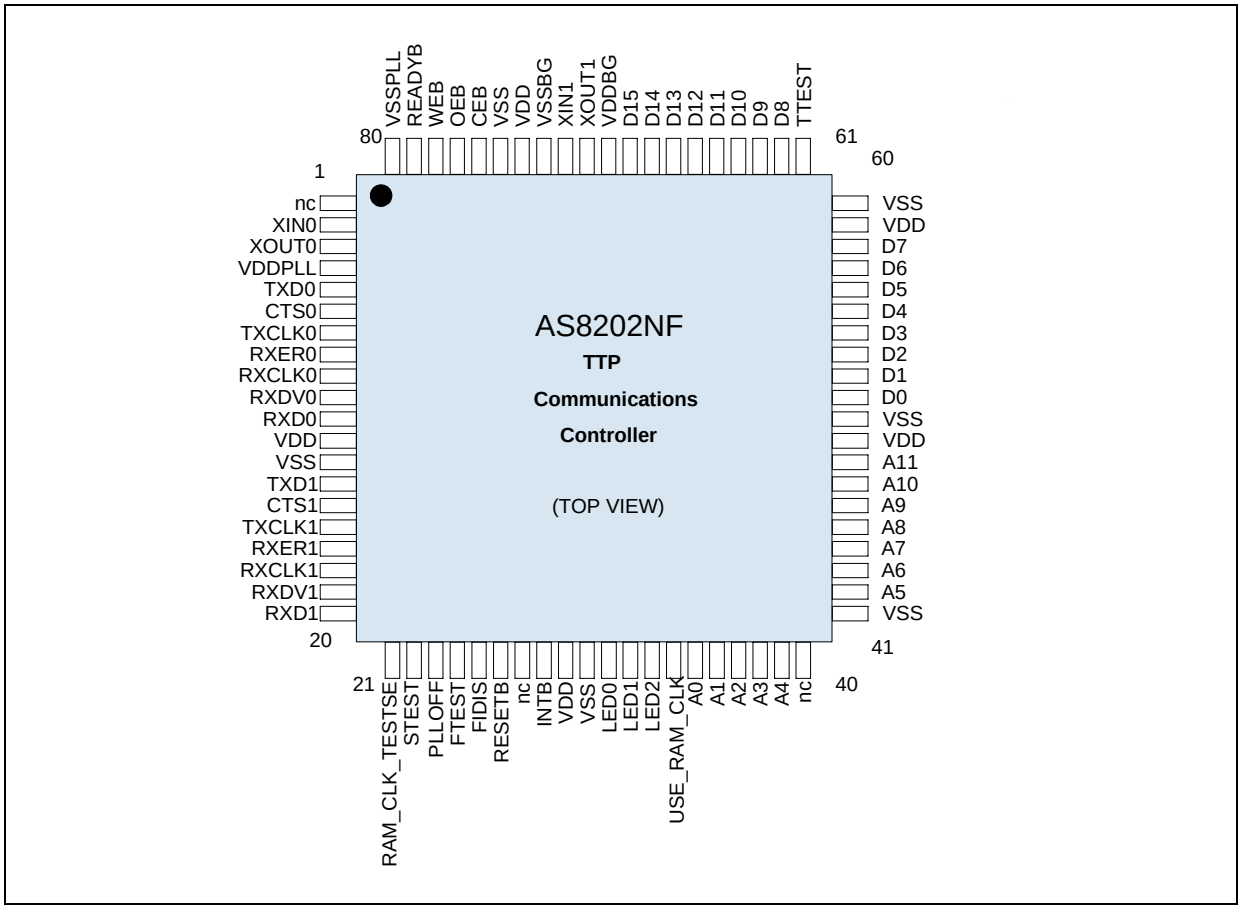
4 Pin Assignments

Figure 2. Pin Assignments LQFP80 Package



Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Dir	Description
V_{DD}	12,29,49,59, 74	P	Positive Power Supply
V_{SS}	13,30,41,50, 60,75	P	Negative Power Supply
V_{DDBG}	70	P	Positive Power Supply for Bus Guardian (connect to V_{DD})
V_{SSBG}	73	P	Negative Power Supply for Bus Guardian (connect to V_{SS})
V_{DDPLL}	4	P	Positive Power Supply for Main Clock PLL (connect to V_{DD})
V_{SSPLL}	80	P	Negative Power Supply for Main Clock PLL (connect to V_{SS})
RAM_CLK_TESTSE	21	I_{PD}	RAM_CLK when STEST=0 and USE_RAM_CLK=1, else Test Input, connect to V_{SS} if not used
STEST	22	I_{PD}	Test Input, connect to V_{SS}
FTEST	24	I_{PD}	Test Input, connect to V_{SS}
FIDIS	25	I_{PD}	Test Input, connect to V_{SS}
TTEST	61	I_{PU}	Test Input, connect to V_{DD}
USE_RAM_CLK	34	I_{PD}	RAM_CLK Pin Enable, connect to V_{SS} if not used

Table 1. Pin Descriptions

Pin Name	Pin Number	Dir	Description
XIN0	2	A	Main Clock: Analog CMOS Oscillator Input, use as input when providing external clock
XOUT0	3	A	Main Clock: Analog CMOS Oscillator Output, leave open when providing external clock
PLLOFF	23	I_{PD}	Main Clock PLL Disable Pin, connect to Vss when providing 10 MHz crystal for enabling the internal PLL
XIN1	72	A	Bus Guardian Clock: Analog CMOS Oscillator Input, use as input when providing external clock
XOUT1	71	A	Bus Guardian Clock: Analog CMOS Oscillator Output, leave open when providing external clock
RESETB	26	I_{PU}	Main Reset Input, active low
TxD0	5	O_{PU}	TTP Bus Channel 0: Transmit Data
CTS0	6	O_{PD}	TTP Bus Channel 0: Transmit Enable
RxD0	11	I_{PU}	TTP Bus Channel 0: Receive Data
TxCLK0	7	I_{PD}	TTP Bus Channel 0: Transmit Clock (MII mode)
RxER0	8	I_{PU}	TTP Bus Channel 0: Receive Error (MII mode)
RxCLK0	9	I_{PD}	TTP Bus Channel 0: Receive Clock (MII mode)
RxDV0	10	I_{PU}	TTP Bus Channel 0: Receive Data Valid (MII mode)
TxD1	14	O_{PU}	TTP Bus Channel 1: Transmit Data
CTS1	15	O_{PD}	TTP Bus Channel 1: Transmit Enable
RxD1	20	I_{PU}	TTP Bus Channel 1: Receive Data
TxCLK1	16	I_{PD}	TTP Bus Channel 1: Transmit Clock (MII mode)
RXER1	17	I_{PU}	TTP Bus Channel 1: Receive Error (MII mode)
RXCLK1	18	I_{PD}	TTP Bus Channel 1: Receive Clock (MII mode)
RxDV1	19	I_{PU}	TTP Bus Channel 1: Receive Data Valid (MII mode)
A[11:0]	48-42, 39-35	I	Host Interface (CNI) Address Bus[1]
D[15:0]	69-62, 58-51	I/O	Host Interface (CNI) Data Bus, tristate
CEB	76	I_{PU}	Host Interface (CNI) Chip Enable, active low
OEB	77	I_{PU}	Host interface (CNI) output enable, active low
WEB	78	I_{PU}	Host interface (CNI) write enable, active low
READYB	79	O_{PU}	Host interface (CNI) transfer finish signal, active low, open drain[2]
INTB	28	O_{PU}	Host interface (CNI) time signal (interrupt), active low, open drain
LED[2:0]	33-31	O_{PD}	Configurable generic output port
nc	1, 27, 40		Not connected, leave open

1. The device is addressed at 16-bit data word boundaries. If the device is connected to a CPU with a byte-granular address bus, remember that A[11:0] of the AS8202NF device has to be connected to A[12:1] of the CPU (considering a little endian CPU address bus)
2. At de-assertion READYB is driven to the inactive value (high) for a configurable time.

Table 2. Pin Directions

Dir	Description
I	TTL Input
I_{PU}	TTL Input with Internal Weak Pull-Up
I_{PD}	TTL Input with Internal Weak Pull-Down
I/O	TTL Input/Output with Tristate
O_{PU}	TTL Output with Internal Weak Pull-Up at Tristate

Table 2. Pin Directions

Dir	Description
O_{PD}	TTL Output with Internal Weak Pull-Down at Tristate
A	Analog CMOS Pin
P	Power Pin

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 7 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
DC Supply Voltage (V_{DD})	-0.3	5.0	V	
Input Voltage (V_{IN})	-0.3	V_{DD}+0.3	V	any pin
Input Current (I_{IN})	-100	100	mA	any pin, T_{AMB}=25ºC
Storage Temperature (T_{STRG})	-55	150	ºC	
Soldering Temperature (T_{SOLD})		235	ºC	t=10 sec, Reflow and Wave
Package body temperature (T_{body})		240	ºC	1
Humidity (H)	5	85	%	
Electrostatic Discharge (ESD)	1000		V	HBM: 1KV Mil.std.883, Method 3015.7

1. The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020C “Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices”. The lead finish for packages is (85%/15% Sn/Pb).

6 Electrical Characteristics

T_{AMB} = -40 to +125 ºC, V_{DD} = 3V to +3.6V, V_{SS} = 0V unless otherwise specified.

Table 4. Electrical Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Operating Conditions							
I_{DDs}	Static Supply Current	all inputs tied to V_{DD}/V_{SS}, clocks stopped, exclusive of I/O drive requirements, V_{DD}=3.6V		5		900	µA
I_{DD}	Operating Supply Current[1]	V_{DD}=3.3V, PLL active, exclusive of I/O drive requirements				100	mA
CLK0_EXT_PLL	Clock Period of Main Clock (external)[1]	PLL active[2]			100		ns
CLK0_EXT		PLL inactive			25		ns
CLK1	Clock Period of Bus Guardian Clock[1]				62.5		ns
TTL Input Pins and TTL Bidirectional Pins in Input/Tristate Model							
V_{IL}	Input Low Voltage					0.8	V
V_{IH}	Input High Voltage			2.0			V
I_{INleak}	Input Leakage Current	Pins without pad resistors, V_{DD}=3.6V		-1		1	µA
I_{IL}	Input Low Current	Pins with pull-down resistors V_{DD}=3.0V	V_{IN}=0.4V	4.9[3]			µA
			V_{IN}=0.8V	8.8[3]			
		Pins with pull-up resistors	V_{DD}=3.6V V_{IN}=0V	-15		-75	
I_{IH}	Input High Current	Pins with pull-down resistors	V_{DD}=3.6V V_{IN}=3.6V	15		75	µA
		Pins with pull-up resistors V_{DD}=3.0V	V_{IN}=2.0V	-10.7[3]			
			V_{IN}=2.5V	-6[3]			
C_{IN}	Input Capacitance				4.5[4]		pF
RxD Pin							
t_{ASYM_Rx} $t(V_{IN}=0.5*V_{DD})$	Asymmetric Receiver Delay RxD	T = 125 ºC, V_{DD}=3.0V, C_{LOAD}=35pF	RxD[1,0]	-2[4]		2[4]	ns
CMOS Inputs (XIN), drive from external clock generator							
Drive at XIN (XOUT = open)							
C_{XIN}	Input Capacitance				1.9	2.5	pF
I_{XIN}	Input Current					±1[4]	µA
V_{IL_XIN}	Input Low Voltage			0		0.3* V_{DD}	V
V_{IH_XIN}	Input High Voltage			0.7* V_{DD}		V_{DD}	V

Table 4. Electrical Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Outputs and TTL Bidirectional Pins in Output Mode							
I_{OL}	Output Low Current	V_{DD}=3.0V, Vo = 0.4V				-4	mA
I_{OH}	Output High Current	V_{DD}=3.0V, Vo = 2.5V				4	mA
I_{OZ}	Output Tristate Current	V_{DD}=3.6V				±10[4]	µA
t_{RISE} t(V_{OUT}=0.1*V_{DD}) to t(V_{OUT}=0.9*V_{DD})	Transition Time – Rise	T = 125 ºC, V_{DD}=3.0V, C_{LOAD}=35pF	CTS[1,0], LED[2:0], INTB			8.1[3]	ns
			D[15:0], READYB			8.9[3]	
t_{FALL} t(V_{OUT}=0.9*V_{DD}) to t(V_{OUT}=0.1*V_{DD})	Transition Time – Fall	T = 125 ºC, V_{DD}=3.0V, C_{LOAD}=35pF	CTS[1,0], LED[2:0], INTB			6[3]	ns
			D[15:0], READYB			7[3]	
TxD Pins							
t_{RISE} t(V_{OUT}=0.3*V_{DD}) to t(V_{OUT}=0.7*V_{DD})	Transition Time – Rise TxD	T = 125 ºC, V_{DD}=3.0V, C_{LOAD}=35pF	TxD[1,0]			4.5[4]	ns
t_{FALL} t(V_{OUT}=0.7*V_{DD}) to t(V_{OUT}=0.3*V_{DD})	Transition Time – Fall TxD	T = 125 ºC, V_{DD}=3.0V, C_{LOAD}=35pF	TxD[1,0]			3[4]	ns
t_{ASYM_Rx} t(V_{OUT}=0.5*V_{DD})	Asymmetric Driver Delay TxD	T = 125 ºC, V_{DD}=3.0V, C_{LOAD}=35pF	TxD[1,0]	-3[4]		3[4]	ns

1. Typical values: CLK0=40 MHz, CLK1=16 MHz
2. Using the internal PLL multiplies the main clock frequency by 4
3. Implicitly tested.
4. Guaranteed by design; not tested during production

Note: If Min/Max values are both negative, they are ordered according to their absolute value.

7 Detailed Description

The AS8202NF is the first TTP controller to support both MFM and Manchester coding. Manchester coding is important for DC-free data transmission, which allows the use of transformers in the data stream. The AS8202NF is pin-compatible with its predecessor, the AS8202. The AS8202NF provides support for fault-tolerant, high-speed bus systems in a single device. The communication controller is qualified for the full temperature range required for automotive applications and is certifiable according to RTCA standards. It offers superior reliability and supports data transfer rates of 25 Mbit/s with MII and up to 5 Mbit/s with MFM/Manchester.

The CNI (communication network interface) forms a temporal firewall. It decouples the controller network from the host subsystem by use of a dual ported RAM (CNI). This prevents the propagation of control errors. The interface to the host CPU is implemented as a 16-bit wide non-multiplexed asynchronous bus interface.

The TTP follows a conflict-free media access strategy called time division multiple access (TDMA). This means, TTP deploys a time slot technique based on a global time that is permanently synchronized. Each node is assigned a time slot in which it is allowed to perform transmit operation. The sequence of time slots is called TDMA round, a set of TDMA rounds forms a cluster cycle. The operation of the network is repeated after one cluster cycle. The sequence of interactions forming the cluster cycle is defined in a static time schedule, called message descriptor list (MEDL). The definition of the MEDL in conjunction with the global time determines the response time for a service request.

The membership of all nodes in the network is evaluated by the communications controller. This information is presented to all correct cluster members in a consistent fashion. During operation, the status of all other nodes is propagated within one TDMA round. Please read more about TTP and request the TTP specification at www.tttech.com.

Host CPU Interface

The host CPU interface, also referred to as CNI (Communication Network Interface), connects the application circuitry to the AS8202NF TTP controller. All related signal pins provide an asynchronous read/write access to a dual ported RAM located in the AS8202NF. There are no setup/hold constraints referring to the microtick (main clock “CLK0”).

All accesses have to be executed on a granularity of 16 bit (2 byte), the device does not support byte-wide accesses. The pin A0 (LSB) of the device differentiates even and odd 16 bit word addresses and is typically connected to A1 of a little-endian host CPU. The A0 of host CPU is not connected to the device, and the application/driver on the host CPU should force all accesses to be 16 bit. For efficiency reasons, the host CPU application/driver may access some memory locations of the AS8202NF using wider accesses (e.g. 32 bit), and the bus interface of the host CPU will automatically split the access into two consecutive 16-bit wide accesses to the TTP controller. Note that particularly in such a setup all timing parameters of the host CPU interface must be met, especially the inactivity timeouts described as symbols 16–19.

The host interface features an interrupt or time signal INTB to notify the application circuitry of programmed and protocol-specific, synchronous and asynchronous events.

The host CPU interface allows access to the internal instruction code memory. This is required for proper loading of the protocol execution code into the internal instruction code RAM, for extensive testing of the instruction code RAM and for verifying the instruction code ROM contents.

INTB is an open-drain output, i.e. the output is only driven to '0' and is weak-pull-up at any other time, so external pull-up resistors or transistors may be necessary depending on the application.

READYB is also an open-drain output, but with a possibility to be driven to ‘1’ for a defined time (selectable by register) before weak-pull-up at any other time.

The **LED** port is software-configurable to automatically show some protocol-related states and events, see below for the LED port configuration.

Table 5. Host Interface Ports

Pin Name	Mode	Width	Comment
A[11:0]	in	12	CNI address bus, 12 bit (A0 is LSB)
D[15:0]	inout (tri)	16	CNI data bus, 16 bit (D0 is LSB)
CEB	in	1	CNI chip enable, active low
WEB	in	1	CNI write enable, active low

Table 5. Host Interface Ports

Pin Name	Mode	Width	Comment
OEB	In	1	CNI output enable, active low
READYB	out (open drain)	1	CNI ready, active low
INTB	out (open drain)	1	CNI interrupt, time signal, active low
RAM_CLK_TESTSE	in	1	HOST clock
USE_RAM_CLK	in	1	HOST clock pin enable

Asynchronous READYB permits the shortest possible bus cycle but eventually requires signal synchronization in the application. Connect USE_RAM_CLK to VSS to enable this mode of operation.

Synchronous READYB uses an external clock (usually the host processor's bus clock) for synchronization of the signal, eliminating external synchronization logic. Connect USE_RAM_CLK to VDD and RAM_CLK_TESTSE to the host processor's bus clock to enable this mode of operation.

Note: Due to possible metastability occurrence, it is not recommended to be used in safety critical systems.

Table 6. Asynchronous DPRAM interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Tc	Controller Cycle Time			25		ns
1a	Input Valid to CEB, WEB (Setup Time)	A[11:0]	5			ns
2a		D[15:0]				
1b	CEB, WEB to Input Invalid (Hold Time)	A[11:0]	3			ns
2b		D[15:0]	4			
3	Input Rising to CEB, WEB Falling	CEB, WEB, OEB	5[1]			ns
4	CEB, WEB Rising to Input Falling	CEB, WEB, OEB	5[1,2]			ns
5	Write Access Time (CEB, WEB to READYB)	min = 1 Tc, max = 4 Tc	25		100	ns
6	CEB, WEB de-asserted to READYB de-asserted				9.4	ns
7a	Input Valid to CEB, OEB (Setup Time)	A[11:0]	5			ns
7b	CEB, OEB to Input Invalid (Hold Time)	A[11:0]	2			ns
8	Input Rising to CEB, OEB Falling	CEB, WEB, OEB	5[1]			ns
9	CEB, OEB Rising to Input Falling	CEB, WEB, OEB	5[1]			ns
10	Read Access Time (CEB, OEB to READYB)	min = 1.5 Tc, max = 8 Tc	37.5		200	ns
11a	CEB, OEB asserted to signal asserted	D[15:0]	4.0		8.4	ns
11b	CEB, OEB de-asserted to signal de-asserted	D[15:0]	3.8		8	ns
11c		READYB			8.8	
12	READYB, D skew				±2	ns
13	RAM_CLK_TESTSE Rising to READYB Falling	USE_RAM_CLK=1	3.7		13.5	ns

Table 6. Asynchronous DPRAM interface

Symbol	Parameter	Conditions		Min	Typ	Max	Units
14	RAM_CLK_TESTSE Rising to READYB Rising	USE_RAM_CLK=1		3		9.7	ns
15	RAM_CLK_TESTSE Rising to READYB Deactivated 1->Z	USE_RAM_CLK =1	Ready delay='00'	3.6		12.9	ns
			Ready delay=01	4.5		15.4	
			Ready delay=10	5.4		18.8	
			Ready delay=11	6.4		22.2	
16	Read to Read Access Inactivity Time (CEB, OEB low to CEB, OEB low)	min = 1.5 Tc		37.5[1]			ns
17	Read to Write Access Inactivity Time (CEB, OEB low to CEB, WEB low)			5[1]			ns
18	Write to Write Access Inactivity Time (CEB, WEB low to CEB, WEB low)			5[1,2]			ns
19	Write to Read Access Inactivity Time (CEB, WEB low to CEB, OEB low)			5[1,2]			ns

1. Prior to starting a read or write access, CEB, WEB and OEB have to be stable for at least 5 ns (see symbol 3, 4, 8, 9). In addition the designer has to consider the minimum inactivity time according to symbols 16, 17, 18, 19. For more information on the inactivity times (see Figure 3).
2. To allow proper internal initialization, after finishing any write access (CEB or WEB is high) to the internal CONTROLLER_ON register, CEB OEB and WEB have to be stable high within 200 ns (min = 8 Tc).

Note: All values not tested during production, guaranteed by design.

Figure 3. Read/Write Access Inactivity Time

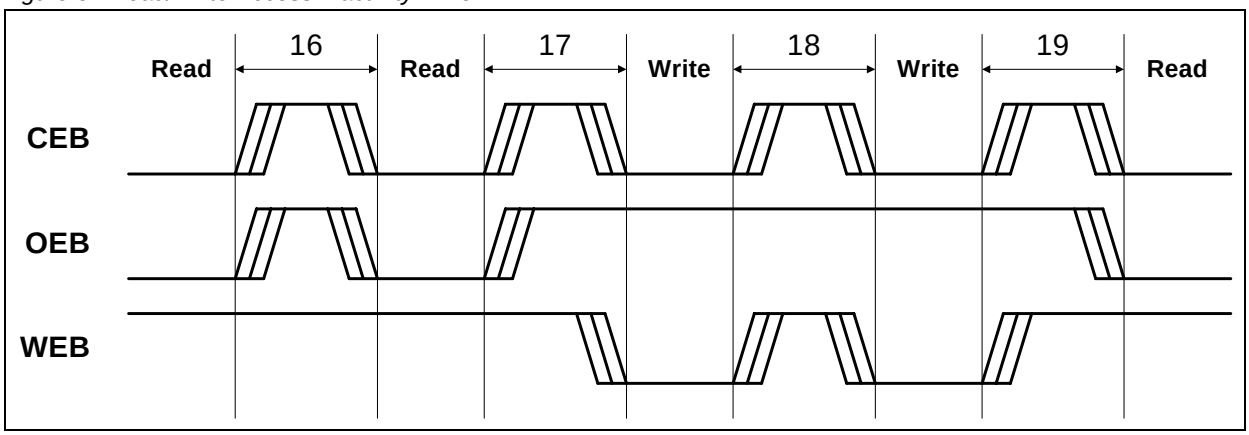


Figure 4. Write Access Timing (CEB Controlled)

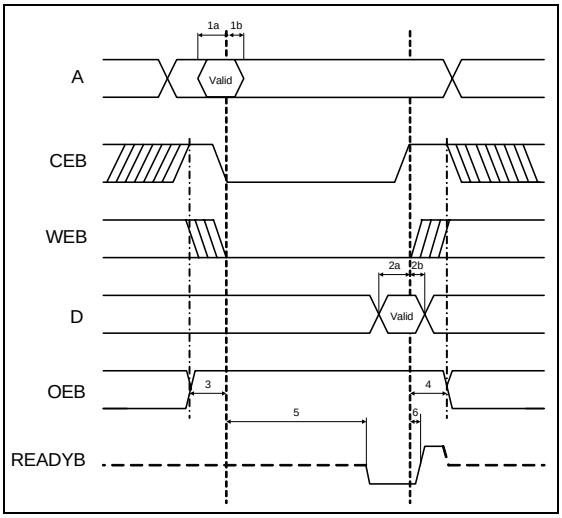


Figure 5. Write Access Timing (WEB Controlled)

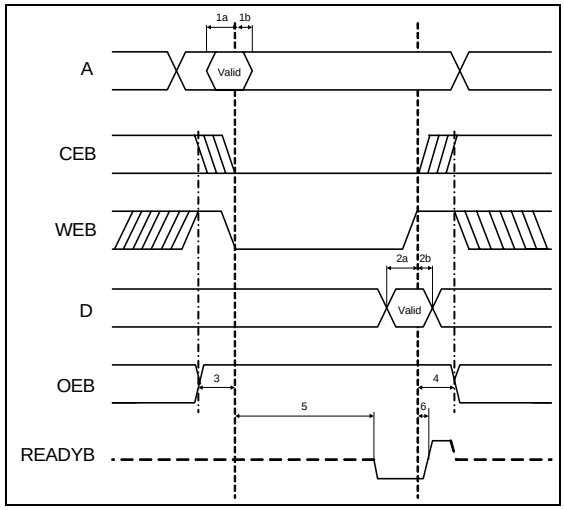


Figure 6. Read Access Timing (CEB Controlled)

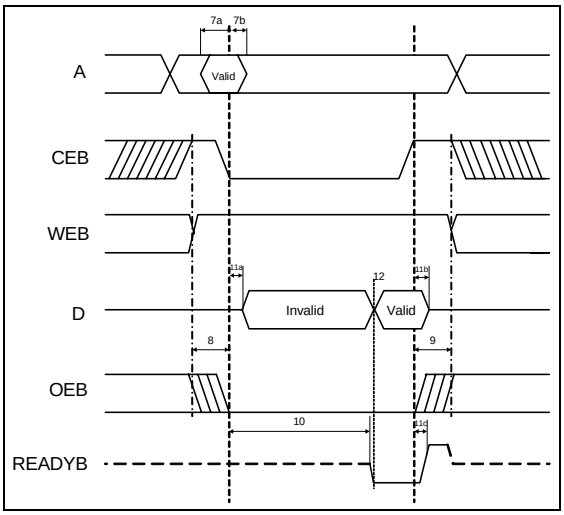
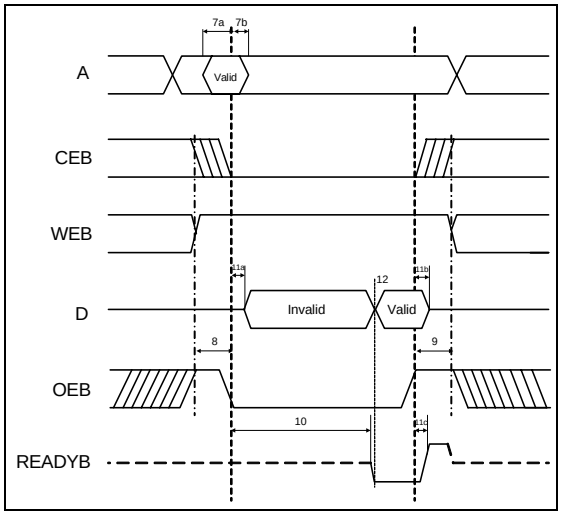
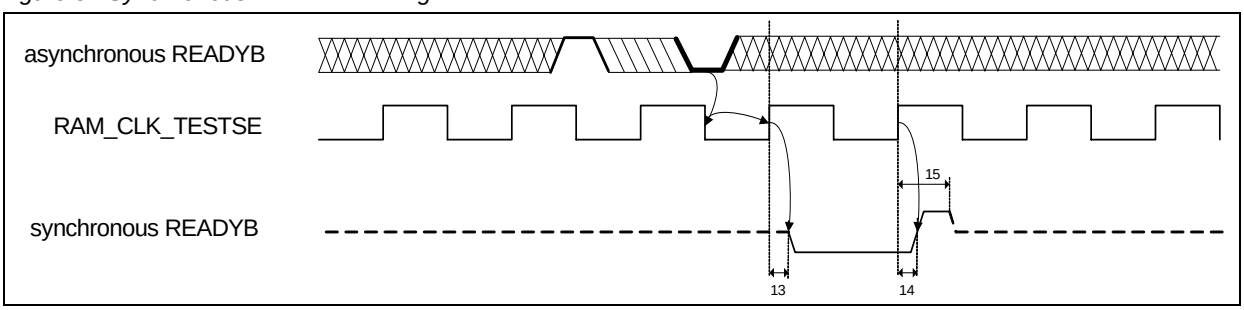


Figure 7. Read Access Timing (OEB Controlled)



Synchronous READYB Generation

Figure 8. Synchronous READYB Timing



Synchronous READYB is aligned to host clock (with pulse duration of one host clock cycle) to fulfill the required host timing constraints for input setup and input hold time to/after host clock rising edge.

Note: Connect USE_RAM_CLK to V_{DD} and RAM_CLK_TESTSE to the host processor's bus clock to enable this mode of operation. Due to possible metastability occurrence, it is not recommended to be used in safety critical systems.

Reset and Oscillator

Table 7. Pin mode

Pin Name	Mode	Comment
XIN0	analog	main oscillator input (external clock input)
XOUT0	analog	main oscillator output
XIN1	analog	bus guardian oscillator input (external clock input)
XOUT1	analog	bus guardian oscillator output
PLLOFF	in	PLL disable
RESETB	in	external reset

External Reset Signal

To issue a reset of the chip the RESETB port has to be driven low for at least 1 us. Pulses under 50 ns duration are discarded. At power-up the reset must overlap the build-up time of the power supply.

Integrated Power-On Reset

The Device has an internal Power-On Reset generator. When supply voltage ramps up, the internal reset signal is kept active (low) for 33 µs typical.

Table 8. Parameters

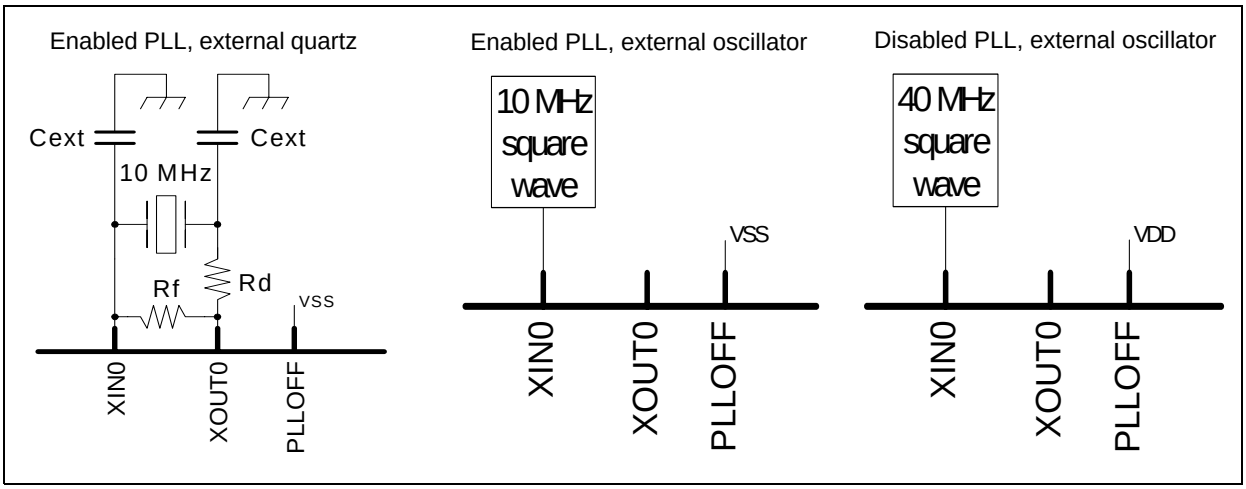
Symbol	Parameter	Min	Typ	Max	Unit
dV/dt	supply voltage slope	551	-	-	V/ms
tpores	power on reset active time after V_{DD} > 1,0V	25	33	49	µs

Note: In case of non-compliance keep the external reset (RESETB) active for min. 5 ms after supply voltage is valid and oscillator inputs active.

Oscillator Circuitry

The internal oscillators for main and bus guardian clock require external quartzes or external oscillators. The main clock features a PLL multiplying a 10 MHz XIN0/XOUT0 oscillation to an internal frequency of 40 MHz when enabled.

Figure 9. Main clock setup



Rf will normally not be soldered, it is only provided to get maximum flexibility.
Cext, typ = 15/18 pF. Rd has to be calculated, if the measured drive level will be too high; if drive level is ok, Rd = 0.

If using an external oscillator at 10 MHz with enabled internal PLL, the oscillator must have a period of 100 ns with low jitter. Note that a crystal-based clock is recommended over a derived clock (i.e., PLL-based) to allow best internal PLL performance.

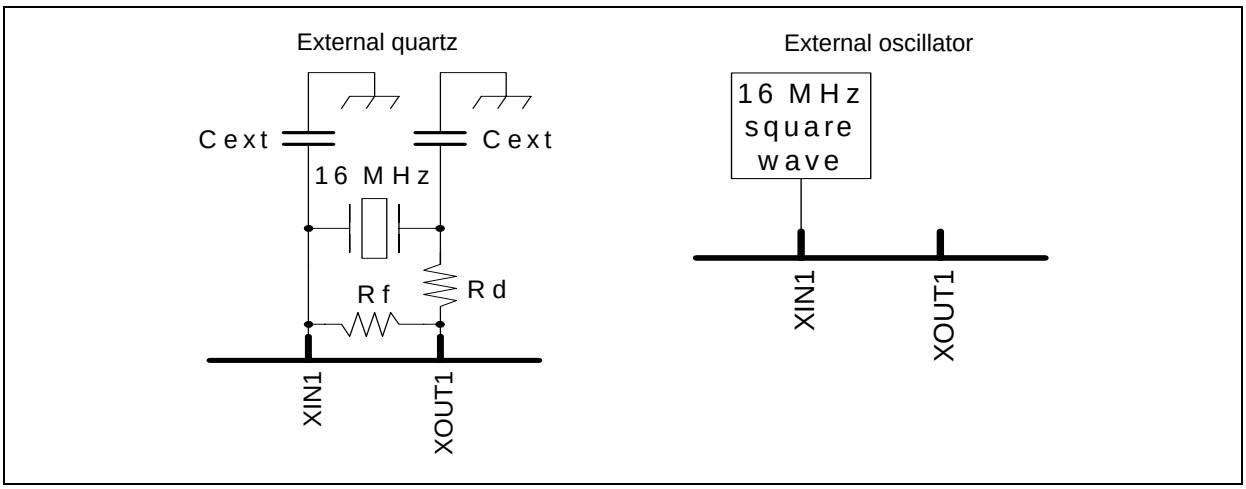
Table 9. Parameters

Parameter	Condition	Min	Typ	Max	Unit
R_osc10	Oscillation margin @ 10 MHz, C_{LOAD} = 18 pF	0.95[1]	1.62[1]		kΩ
R_osc16	Oscillation margin @ 16 MHz, C_{LOAD} = 18 pF	0.37[1]	0.64[1]		kΩ
R_osc20	Oscillation margin @ 20 MHz, C_{LOAD} = 18 pF	0.24[1]	0.41[1]		kΩ

1. Not tested during production.

Note: C_{LOAD} is the value of the external load capacitors towards ground. The total load capacitance seen by the quartz will be C_{LOAD}_tot = (C_{LOAD} + Cpar)/2. Cpar is the equivalent parasitic capacitance of the oscillator cell inputs and the PCB and is derived from measurements to be about 3.5 … 4.0 pF.

Figure 10. Bus Guardian clock setup



Both the XIN0/XOUT0 (main clock) and the XIN1/XOUT1 (bus guardian clock) cells support driving a quartz crystal oscillation as well as clock input by an external oscillator.

Build-up Characteristics

Table 10. Characteristics

Symbol	Pin	Parameter	Min	Typ	Max	Unit	Note
Tosc_startup0	XIN0/ XOUT0	Oscillator startup time (Main clock)			20	ms	Quartz frequency: 10 MHz
Tosc_startup1	XIN1/ XOUT1	Oscillator startup time (Bus Guardian clock)			20 ms	ms	Quartz frequency: 16 MHz
Tpll_startup0	XIN0/ XOUT0	PLL startup time (Main clock)			20 ms	ms	Quartz frequency: 10 MHz

TTP Bus Interface

The AS8202NF contains two TTP bus units, one for each TTP channel, building the TTP bus interface. Each TTP bus channel contains a transmitter and a receiver and can be configured to be either in the asynchronous or synchronous mode of operation. Note that the two channels (channel 0 and channel 1) can be configured independently for either of these modes.

The drivers of the TxD and CTS pins are actively driven only during a transmission window, all the other time the drivers are switched off and the weak pull resistors are active. External pull resistors must be used to define the signal levels during idle phases.

Note: The transmission window may be different for each channel.

Table 11. Bus Interface Connections

Pin Name	Tx inactive
TxD[0]	weak pull-up
CTS[0]	weak pull-down
TxD[1]	weak pull-up
CTS[1]	weak pull-down

TTP Asynchronous Bus Interface

When in asynchronous mode of operation the channel's bus unit uses a self-clocking transmission encoding which can be either MFM or Manchester at a maximum data rate of 5 Mbit/s on a shared media (physical bus). The pins can either be connected to drivers using recessive/dominant states on the wire as well as drivers using active push/pull functionality.

The RxD signal uses '1' as the inactivity level. In the so-called RS485 compatible mode longer periods of '0' are treated as inactivity. If the RS485 compatible mode is not used, the application must care to drive RxD to '1' during inactivity on the bus.

Table 12. Asynchronous Bus Interface Connections

Pin Name	Mode	Connect to PHY	Note
TxD[0]	out	TxD	Transmit data channel 0
CTS[0]	out	CTS	Transmit enable channel 0
TxCLK[0]	in		No function (do not connect)
RXER[0]	in		No function (do not connect)
RXCLK[0]	in		No function (do not connect)
RxDV[0]	in		No function (do not connect)
RxD[0]	in	RxD	Receive data channel 0
TxD[1]	out	TxD	Transmit data channel 1
CTS[1]	out	CTS	Transmit enable channel 1
TxCLK[1]	in		No function (do not connect)
RXER[1]	in		No function (do not connect)
RXCLK[1]	in		No function (do not connect)
RxDV[1]	in		No function (do not connect)
RxD[1]	in	RxD	Receive data channel 1

TTP Synchronous Bus Interface

When in synchronous mode of operation, the bus unit uses a synchronous transfer method to transfer data at a rate between 5 and 25 Mbit/s. The interface is designed to run at 25 Mbit/s and to be gluelessly compatible with the commercial 100 Mbit/s Ethernet MII (Media Independent Interface) according to IEEE standard 802.3 (Ethernet CSMA/CD).

Connecting the synchronous TTP bus unit to a 100 Mbit/s Ethernet PHY is done by connecting TxD, CTS, TxCLK, RXER, RXCLK, RxDV and RxD of any channel to TxD0TxD0, TxEN, TxCLK, RXER, RXCLK, RxDV and RxD0 of the PHY's MII. The pins TxD1, TxD2 and TxD3 of the PHY's MII should be linked to VSS. The signals RxD1, RxD2, RxD3, COL and CRS as well as the MMII (Management Interface) should be left open or can be used for diagnostic purposes by the application.

Note that the frames sent by the AS8202NF are not Ethernet compatible and that an Ethernet Hub (not a Switch) can be used as a 'star coupler' for proper operation. Also note that the Ethernet PHY must be configured for Full Duplex operation (even though the Hub does not support full duplex), because TTP has its own collision management that should not interfere with the PHY's Half-Duplex collision management. In general, the PHY must not be configured for automatic configuration ('Auto negotiation') but be hard-configured for 100 Mbit/s, Full Duplex operation.

Note: To run the interface at a rate other than 25 Mbit/s other transceiver PHY components have to be used.

Table 13. Synchronous Bus Interface Connections

Pin Name	Mode	Connect to PHY	Note
TxD[0]	out	TxD0TxD0	Transmit data channel 0
CTS[0]	out	TxEN	Transmit enable channel 0
TxCLK[0]	in	TxCLK	Transmit clock channel 0
RXER[0]	in	RXER	Receive error channel 0
RXCLK[0]	in	RXCLK	Receive clock channel 0
RxDV[0]	in	RxDV	Receive data valid channel 0
RxD[0]	in	RxD0	Receive data channel 0
TxD[1]	out	TxD0	Transmit data channel 1
CTS[1]	out	TxEN	Transmit enable channel 1
TxCLK[1]	in	TxCLK	Transmit clock channel 1
RXER[1]	in	RXER	Receive error channel 1
RXCLK[1]	in	RXCLK	Receive clock channel 1
RxDV[1]	in	RxDV	Receive data valid channel 1
RxD[1]	in	RxD0	Receive data channel 1

Test Interface

The Test Interface supports the manufacturing test and characterization of the chip. In the application environment test pins have to be connected as following:

- STEST, FTEST, FIDIS: connect to VSS
- TTEST: connect to VDD

Warning: Any other connection of these pins may cause permanent damage to the device and to additional devices of the application.

LED Signals

The LED port consists of three pins. Via the MEDL each of these pins can be independently configured for any of the three modes of operation. At Power-Up and after Reset the LED port is inactive and only weak pull-down resistors are connected. After the controller is switched on by the host and when it is processing its initialization, the LED port is initialized to the selected mode of operation.

Table 14. LED Signals

Pin Name	Protocol Mode	Timing Mode	Bus Guardian Mode
LED2	RPV[1] or Protocol activity7	Time Overflow[2]	Action Time[3]
LED1	Sync Valid[4]	Time Tick[2]	BDE1[5]
LED0	Protocol activity[6] or RPV[7]	Microtick[8]	BDE0[5]

1. RPV is Remote Pin Voting. RPV is a network-wide agreed signal used typically for agreed power-up or power-down of the application's external drivers.
2. Time Overflow is active for one clock cycle at the event of an overflow of the internal 16-bit time counter. Time Tick is active for one clock cycle when the internal time is counted up. Time Overflow and Time Tick can be used to externally clone the internal time control unit (TCU). With this information the application can precisely sample and trigger events, for example.
3. Action Time signals the start of a bus access cycle.
4. The controller sets this output when cluster synchronization is achieved (after integration from the LISTEN state, after acknowledge in the COLDSTART state).
5. BDE0 and BDE1 show the Bus Guardian's activity, '1' signals an activated transmitter gate on the respective channel.
6. Protocol activity is typically connected to an optical LED. The flashing frequency and rhythm give a simple view to the internal TTP protocol state.
7. LED2's RPV mode and LED0's Protocol activity mode can be swapped with a MEDL parameter.
8. Microtick is the internal main clock signal.

Each LED pin can be configured to be either a push/pull driver (drives both LOW and HIGH) or to be only an open-drain output (drives only LOW).

8 Package Drawings and Markings

The product is available in LQFP80 package.

Figure 11. package Diagram

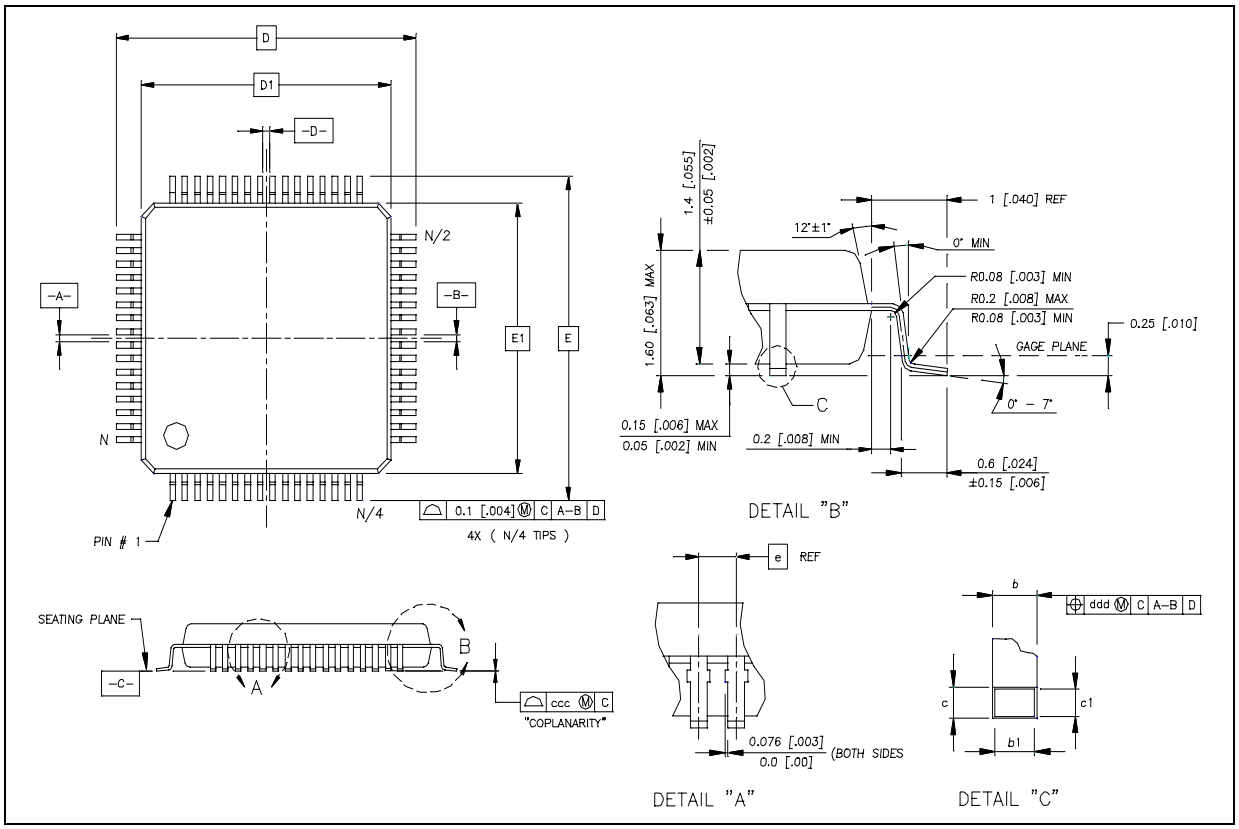


Table 15. package Dimensions

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
D	15.8	16	16.2	c1	0.09		0.16
D1	13.9	14	14.1	e		0.65	
E	15.8	16	16.2	ccc		0.10	
E1	13.9	14	14.1	ddd		0.13	
b	0.22	0.32	0.38	N		80	
b1	0.22	0.3	0.33	N/2		40	
c	0.09		0.2	N/4		20	

Note:

1. All dimensions are in millimeters, angle is in degrees.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Dimensioning and tolerancing conform to *JEDEC MS-026 Rev A.*
4. The top package body size may be smaller than the bottom body size by as much as 0.15 mm.

9 Ordering Information

Table 16. Ordering Information

Type	Marking	Description	Delivery Form	Package
AS8202NF-ALQR	AS8202NF	TTP communication controller	Tray	LQFP80
AS8202NF-ALQT	AS8202NF	TTP communication controller	Tape&Reel	LQFP80
AS8202NF-ALQU	AS8202NF	TTP communication controller	Tube	LQFP80

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