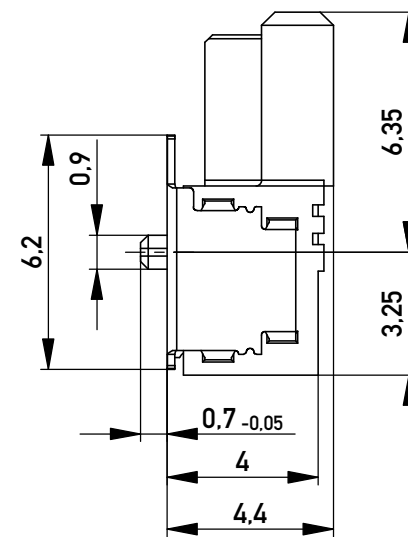
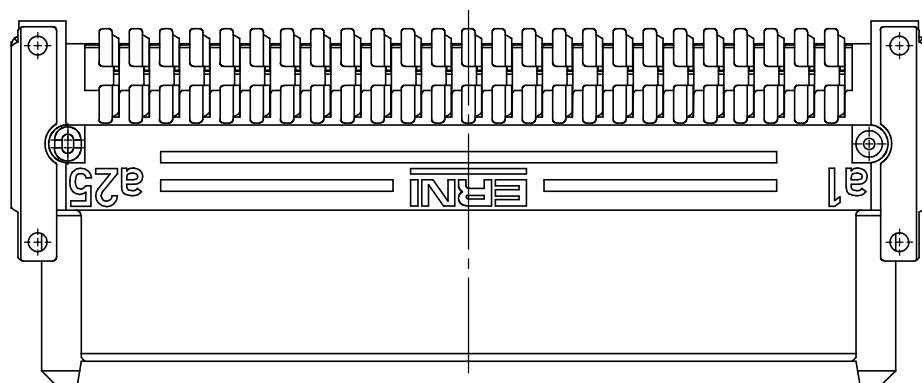
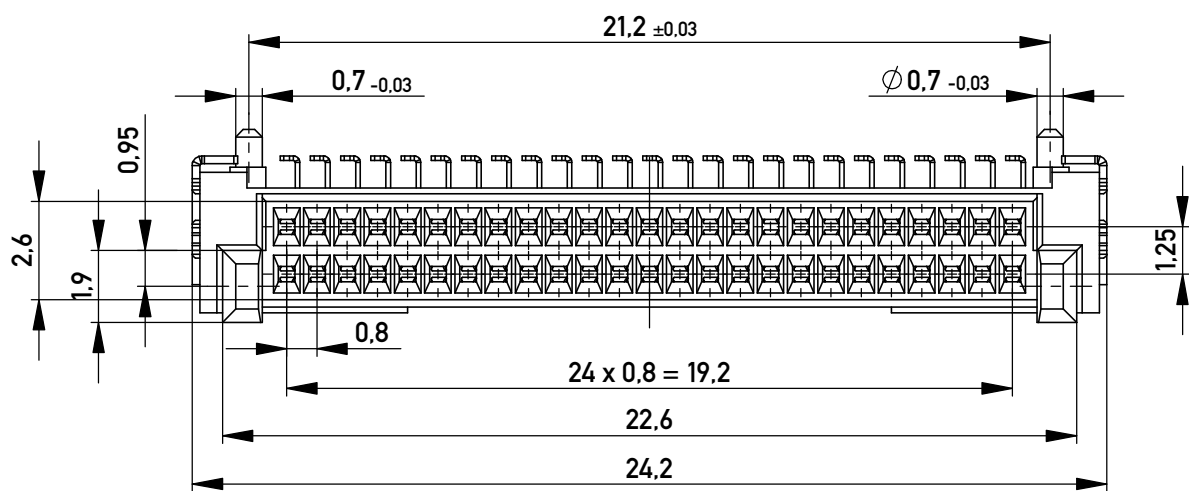
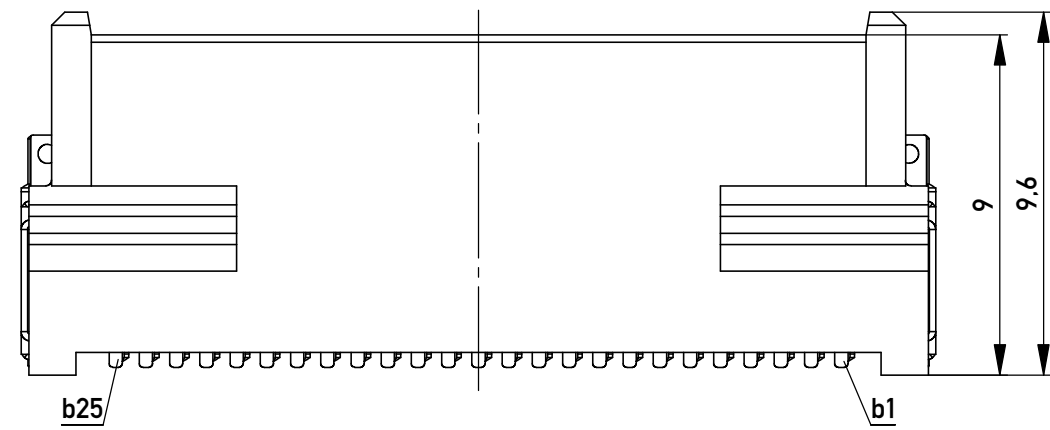
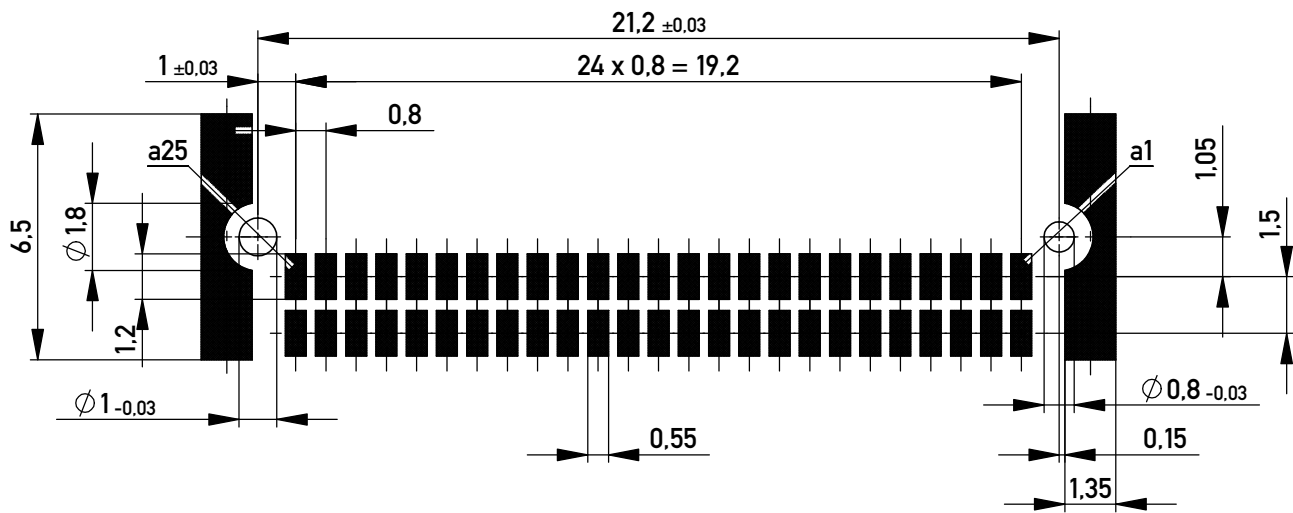


Leiterplatten-Layout Vorschlag für SMT
PCB-Layout Proposal for SMT



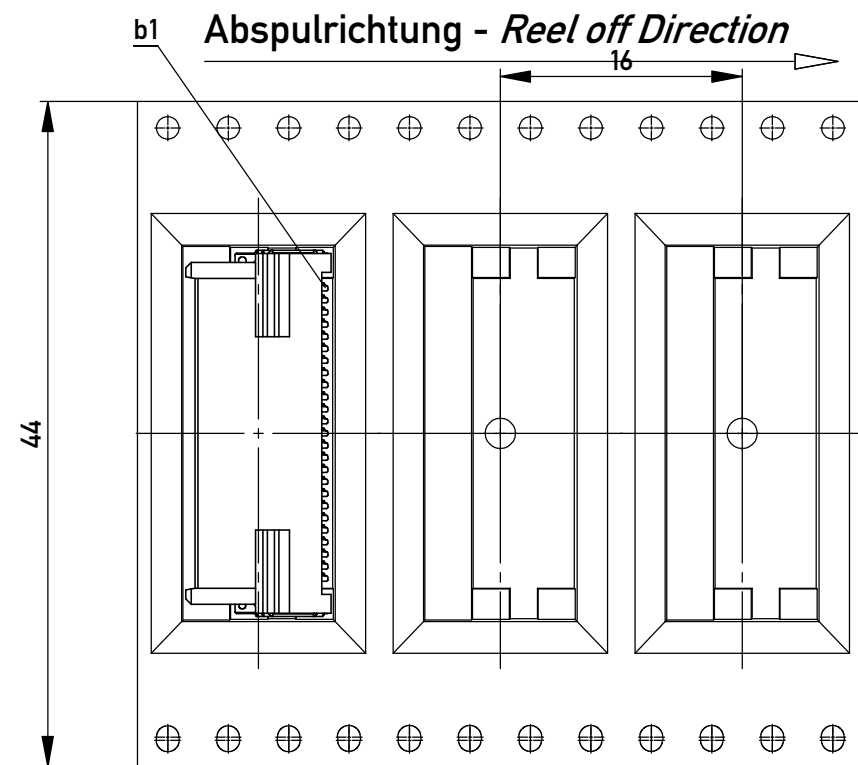
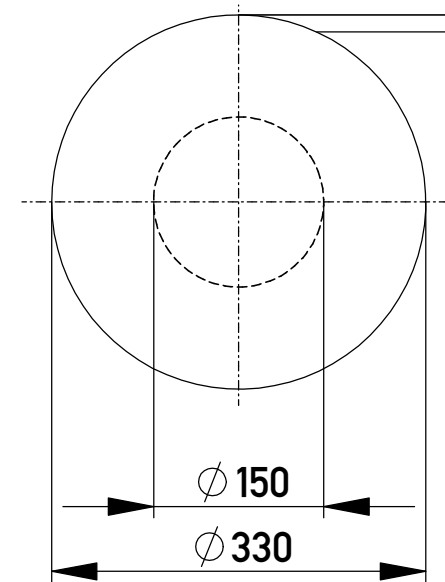
Anforderungsstufe 1
Performance Level 1

Kontaktbereich vergoldet
Mating Area gold plating

Anschlussbereich verzinkt 4-6 µm
Terminal Area 4-6 µm tin plating

Koplanarität der Anschlüsse ≤ 0,1 mm
Coplanarity Area of Termination ≤ 0.1 mm

Verpackt im Gurt nach DIN IEC 60286-3
Tape on Reel Packaging according to DIN IEC 60286-3
Verpackungseinheit: 650 Stück
Packaging unit: 650 pcs



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Information:		Tolerances	 All Dimensions in mm	Scale	5:1
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 www.ERNI.com		 www.ERNI.com		0,8 DRC-Q, F 50 polig 0,8 DRC-Q, F 50 pin	
a	26.02.2014			100100100005	
Index	Date			Class DRCQ	
				K A3	