



SPC5604

N & P Pair Enhancement Mode MOSFET

DESCRIPTION

The SPC5604 is the N- and P-Channel enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where high-side switching, low in-line power loss, and resistance to transients are needed.

FEATURES

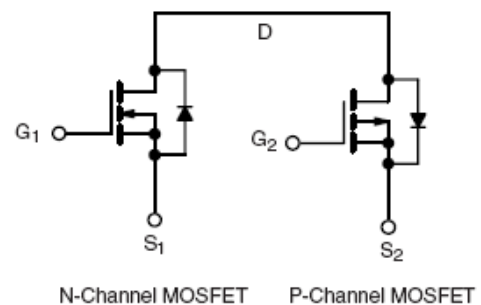
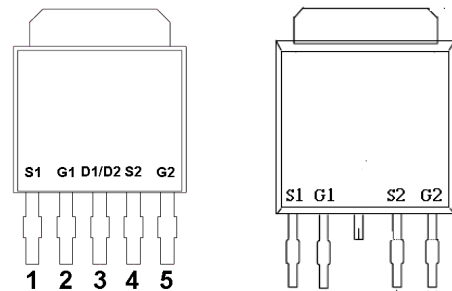
- ◆ N-Channel
 - 40V/10A, $R_{DS(ON)} = 24m\Omega @ V_{GS} = 10V$
 - 40V/ 8A, $R_{DS(ON)} = 28m\Omega @ V_{GS} = 4.5V$
 - 40V/ 6A, $R_{DS(ON)} = 32m\Omega @ V_{GS} = 2.5V$
- ◆ P-Channel
 - 40V/-10A, $R_{DS(ON)} = 32m\Omega @ V_{GS} = -10V$
 - 40V/- 8A, $R_{DS(ON)} = 42m\Omega @ V_{GS} = -4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-252-5L package design

APPLICATIONS

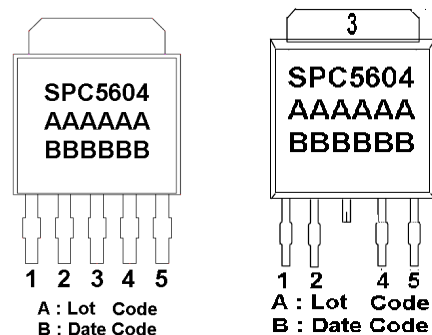
- Power Management in Note book
- Battery Powered System
- DC/DC Converter
- LCD Display inverter

PIN CONFIGURATION

(TO-252-5L) (TO-252-4L)



PART MARKING





SPC5604

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PIN DESCRIPTION

Pin	Description(TO-252-5L)	Description(TO-252-4L)
1	Source 1	Source 1
2	Gate 1	Gate 1
3	Drain1/Drain2	Drain
4	Source 2	Source 2
5	Gate 2	Gate 2

ORDERING INFORMATION

Part Number	Package	Part Marking
SPC5604T255RGB	T0-252-5L	SPC5604
SPC5604T254RGB	T0-252-4L	SPC5604

※ SPC5604T255RGB: 13" Tape Reel ; Pb – Free ; Halogen – Free

※ SPC5604T254RGB :13" Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical		Unit	
		N-Channel	P-Channel		
Drain-Source Voltage	V _{DSS}	40	-40	V	
Gate –Source Voltage	V _{GSS}	±20	±20	V	
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	10.0	-10.0	A
		TA=70°C	7.0	-7.0	
Pulsed Drain Current	I _{DM}	25	-25	A	
Continuous Source Current(Diode Conduction)	I _S	2.3	-2.3	A	
Power Dissipation	P _D	TA=25°C	2.5	2.8	W
		TA=70°C	1.6	1.8	
Operating Junction Temperature	T _J	-55/150		°C	
Storage Temperature Range	T _{STG}	-55/150		°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	T ≤ 10sec	50	52	°C/W
		Steady State	80	80	



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ELECTRICAL CHARACTERISTICS (NMOS)

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5		1.0	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=32V, V_{GS}=0V$			1	uA
		$V_{DS}=32V, V_{GS}=0V$ $T_J=85^\circ C$			10	
On-State Drain Current	$I_{D(on)}$	$V_{DS}= 5V, V_{GS} =4.5V$	10			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}= 10V, I_D=10A$		0.018	0.024	Ω
		$V_{GS}=4.5V, I_D= 8A$		0.022	0.028	
		$V_{GS}=2.5V, I_D= 6A$		0.026	0.032	
Forward Transconductance	g_{fs}	$V_{DS}=15V, I_D=6.2A$		13		S
Diode Forward Voltage	V_{SD}	$I_S=2.3A, V_{GS} =0V$		0.8	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=20V, V_{GS}=4.5V$ $I_D= 5A$		10	14	nC
Gate-Source Charge	Q_{gs}			2.8		
Gate-Drain Charge	Q_{gd}			3.2		
Input Capacitance	C_{iss}	$V_{DS}=20V, V_{GS}=0V$ $f=1MHz$		850		pF
Output Capacitance	C_{oss}			110		
Reverse Transfer Capacitance	C_{rss}			75		
Turn-On Time	$t_{d(on)}$	$V_{DD}=20V, R_L=4\Omega$ $I_D=5.0A, V_{GEN}=10V$ $R_G=1\Omega$		6	12	nS
	t_r			10	20	
Turn-Off Time	$t_{d(off)}$			20	36	
	t_f			6	12	



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ELECTRICAL CHARACTERISTICS (PMOS)

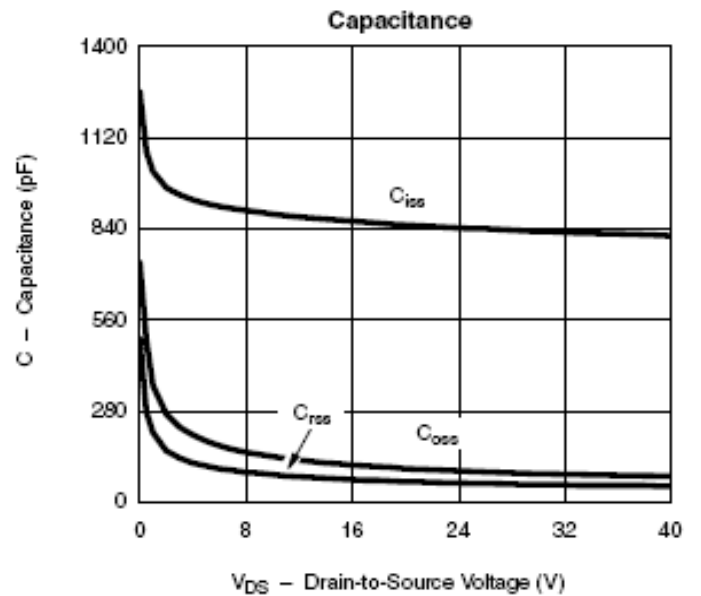
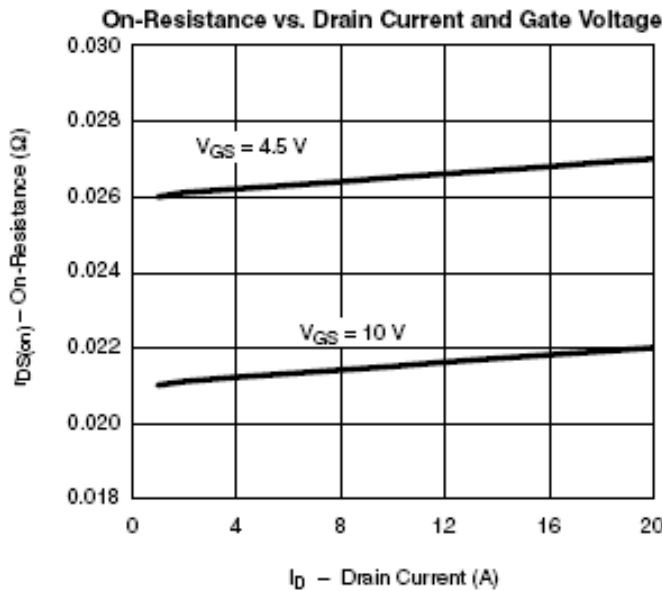
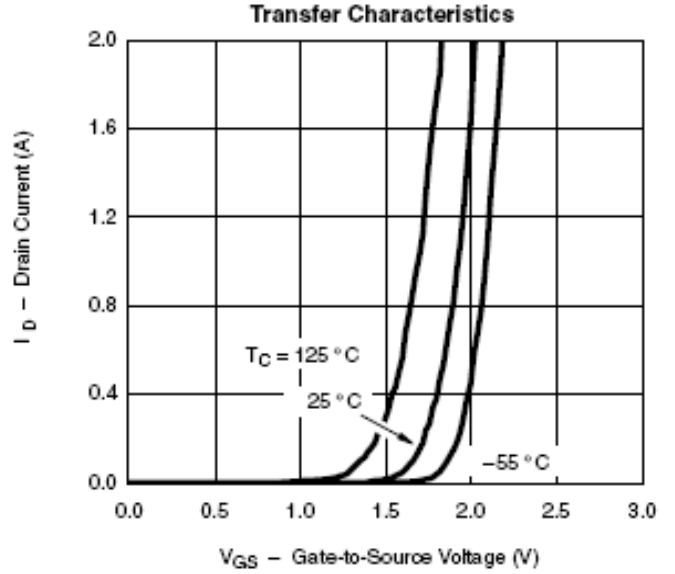
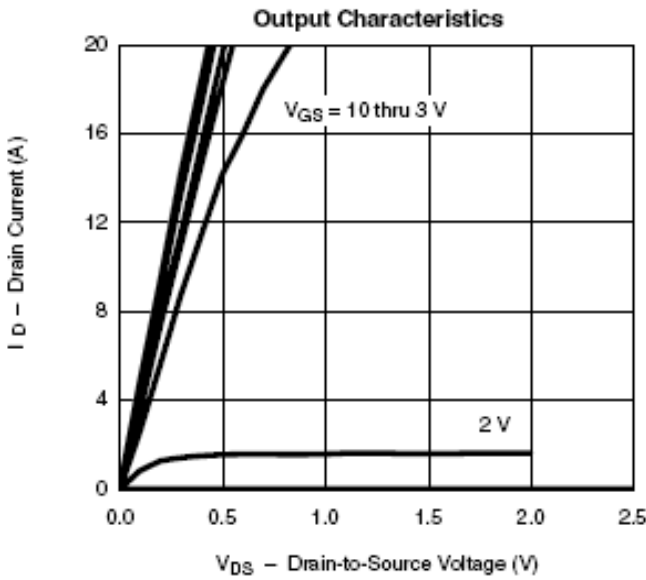
(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.8		-2.5	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-32V, V_{GS}=0V$			-1	uA
		$V_{DS}=-32V, V_{GS}=0V$ $T_J=85^\circ C$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS}=-5V, V_{GS}=-4.5V$	-10			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-10A$		0.028	0.032	Ω
		$V_{GS}=-4.5V, I_D=-8A$		0.038	0.042	
Forward Transconductance	g_{fs}	$V_{DS}=-15V, I_D=-5.7A$		13		S
Diode Forward Voltage	V_{SD}	$I_S=-2.3A, V_{GS}=0V$		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-20V, V_{GS}=-4.5V$ $I_D=-5.0A$		13	20	nC
Gate-Source Charge	Q_{gs}			4.5		
Gate-Drain Charge	Q_{gd}			6.5		
Input Capacitance	C_{iss}	$V_{DS}=-20V, V_{GS}=0V$ $f=1MHz$		1100		pF
Output Capacitance	C_{oss}			145		
Reverse Transfer Capacitance	C_{rss}			115		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-20V, R_L=4\Omega$ $I_D=-5.0A, V_{GEN}=-4.5V$ $R_G=1\Omega$		40	80	nS
	t_r			55	100	
Turn-Off Time	$t_{d(off)}$			30	60	
	t_f			12	20	



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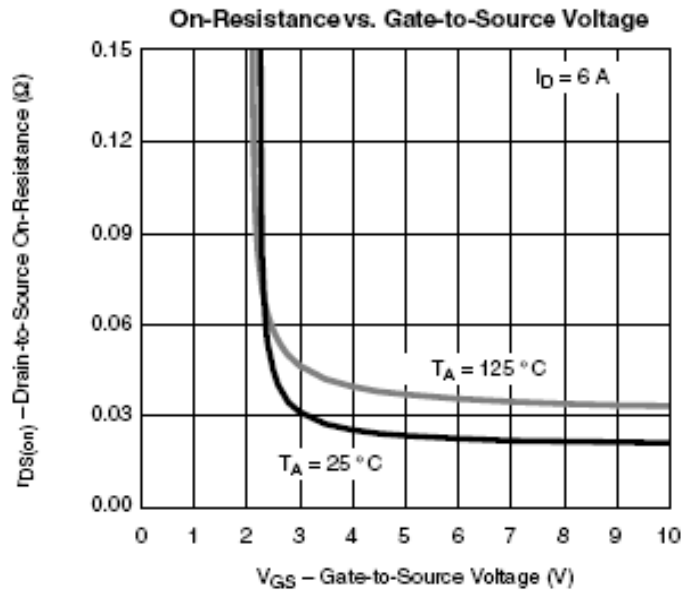
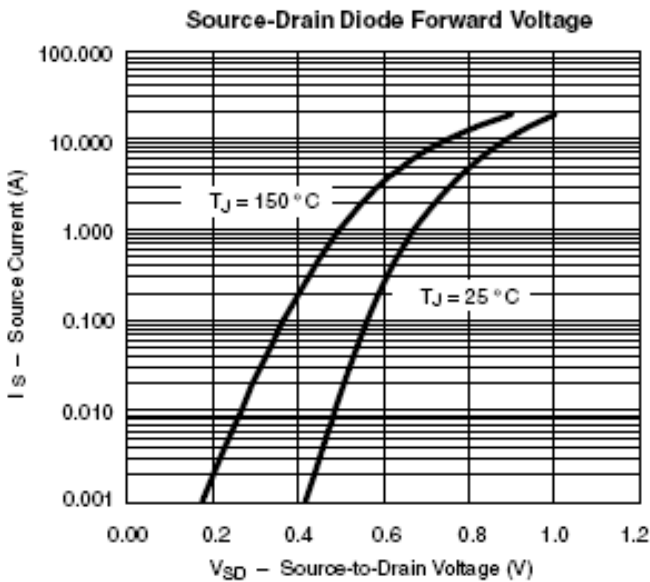
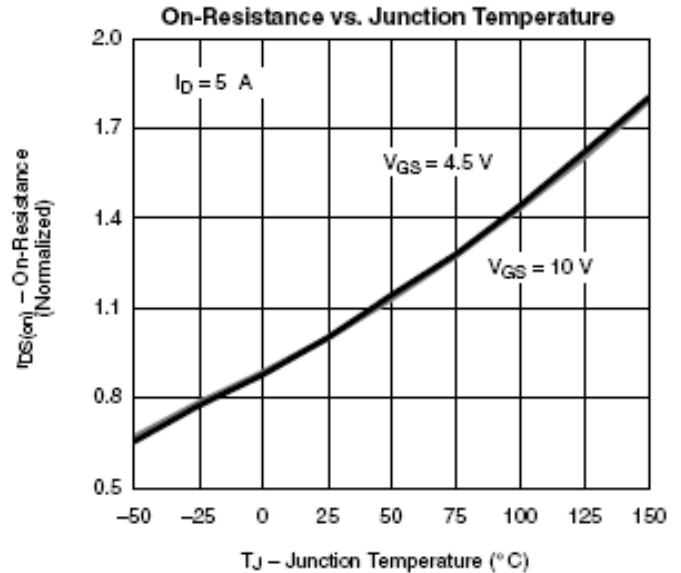
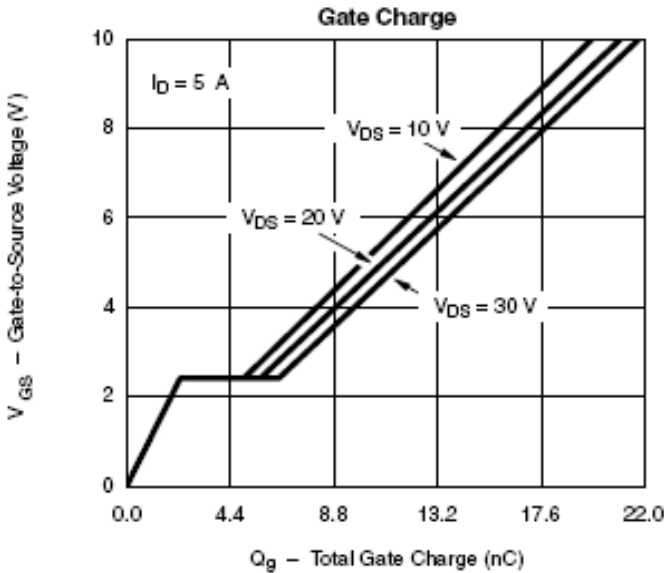
TYPICAL CHARACTERISTICS (NMOS)





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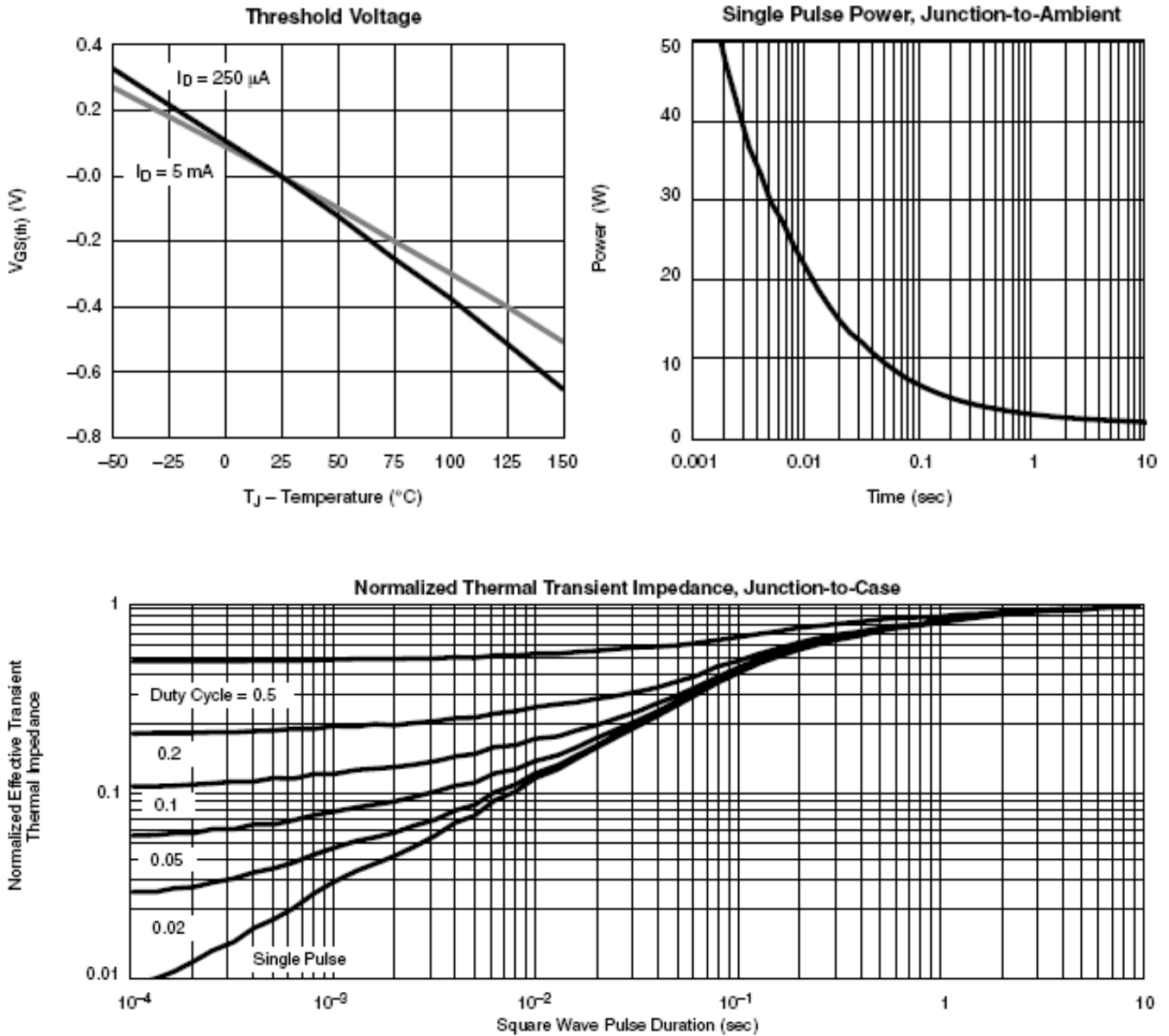
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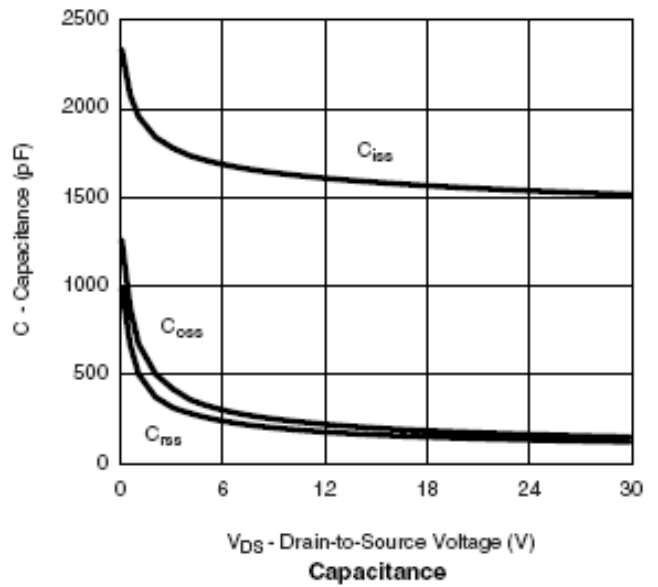
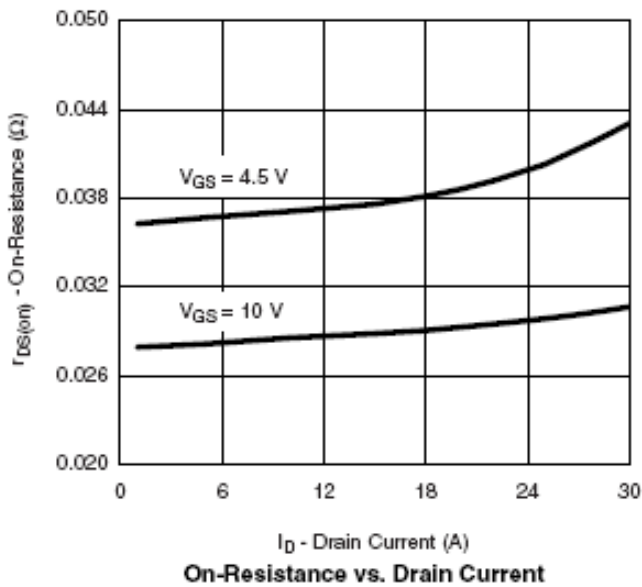
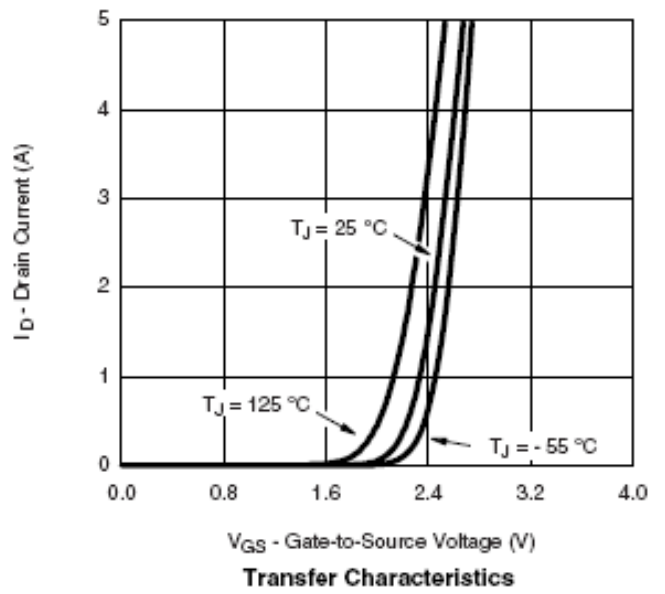
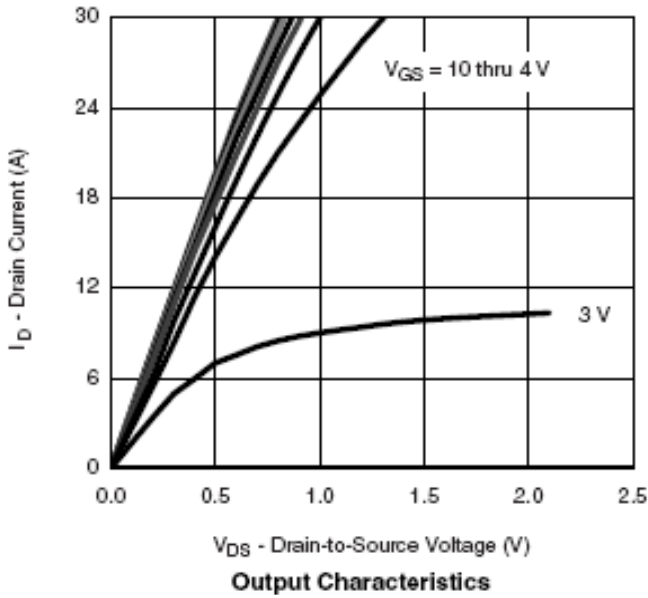




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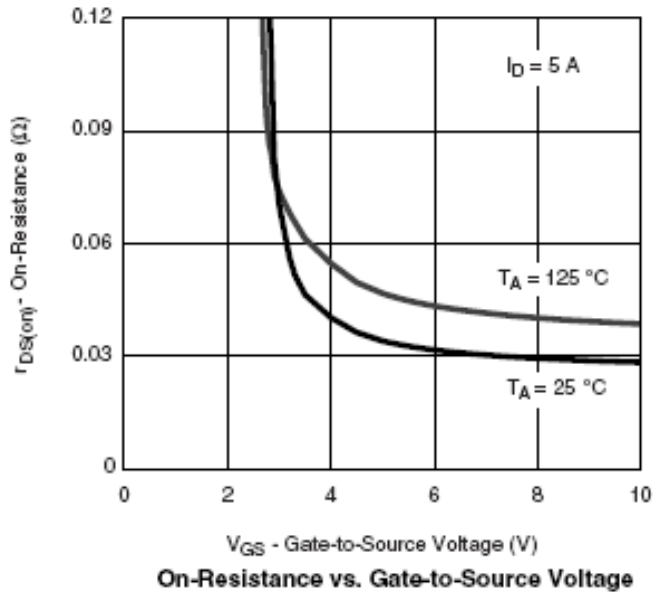
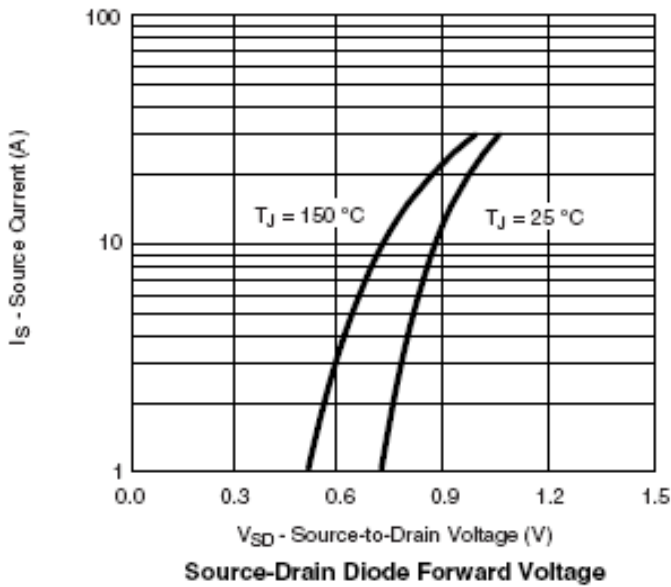
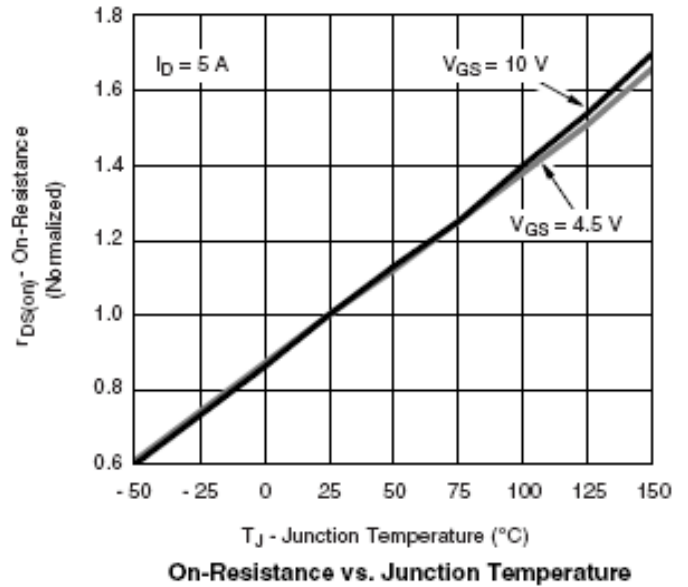
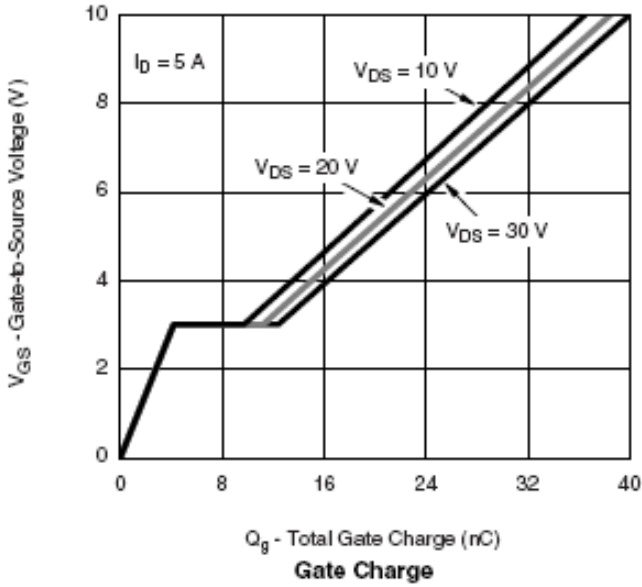
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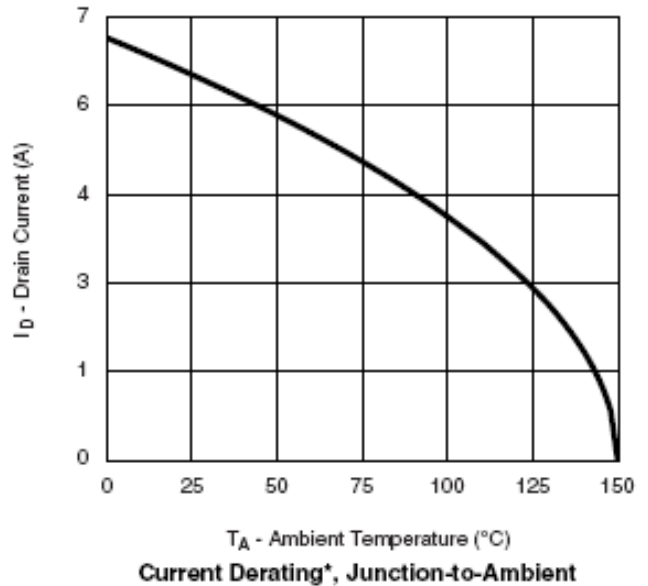
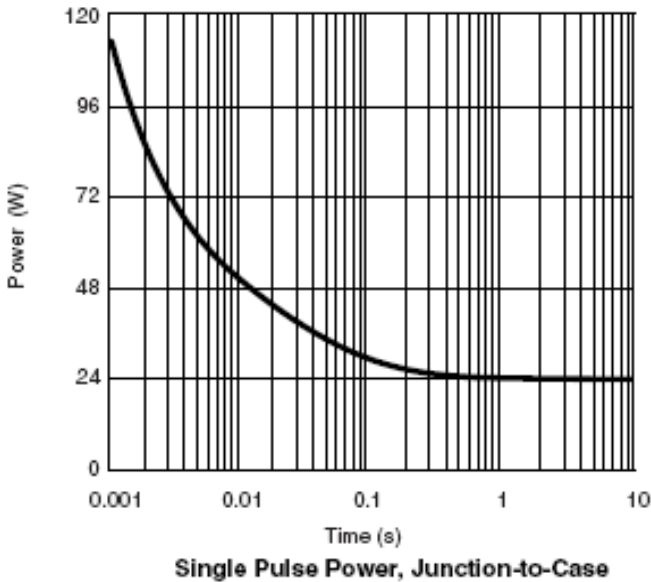
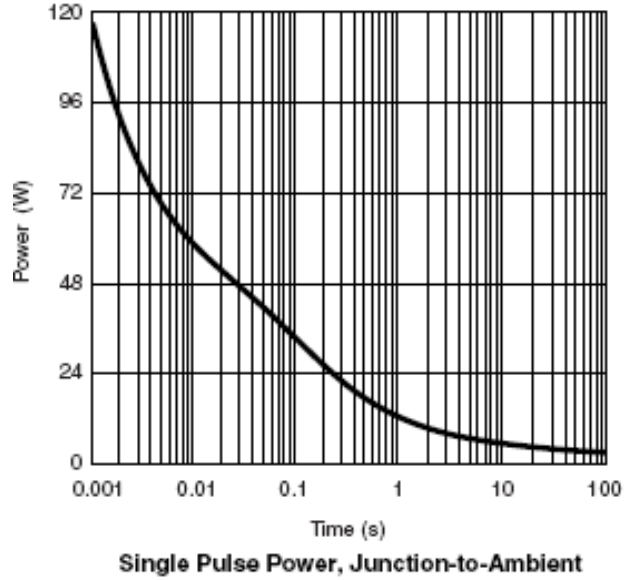
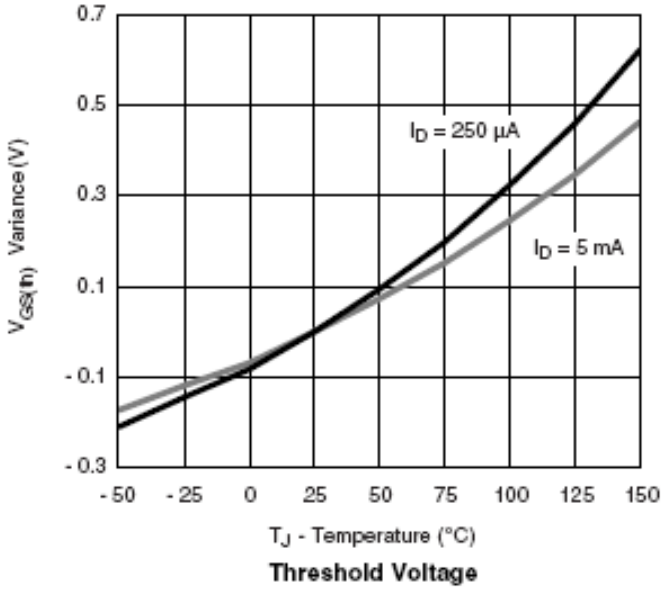
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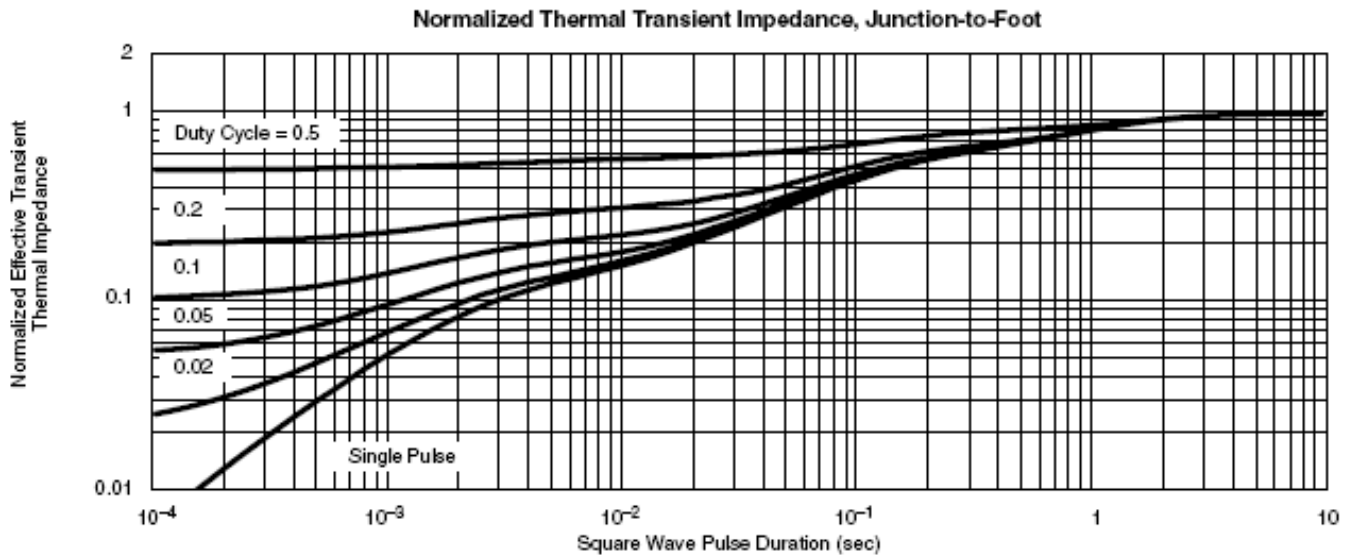
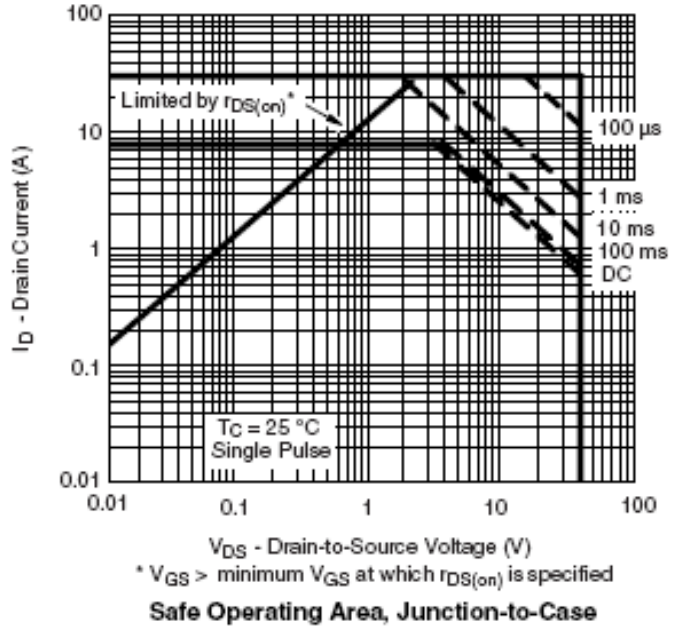
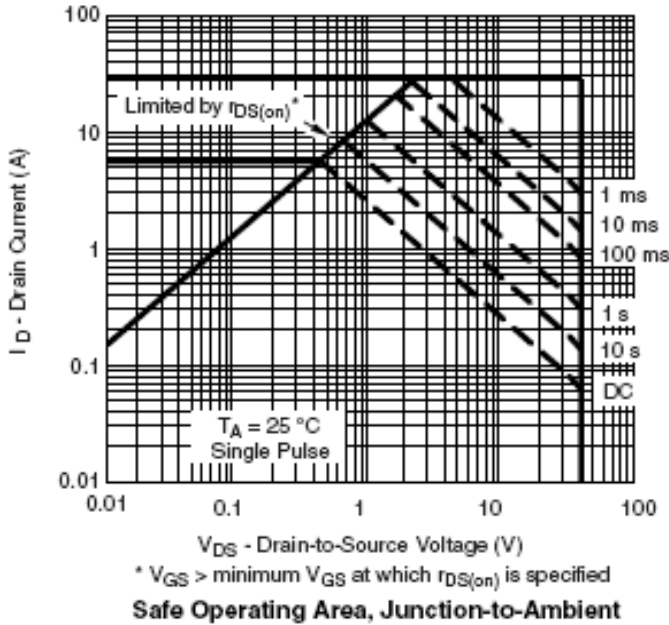
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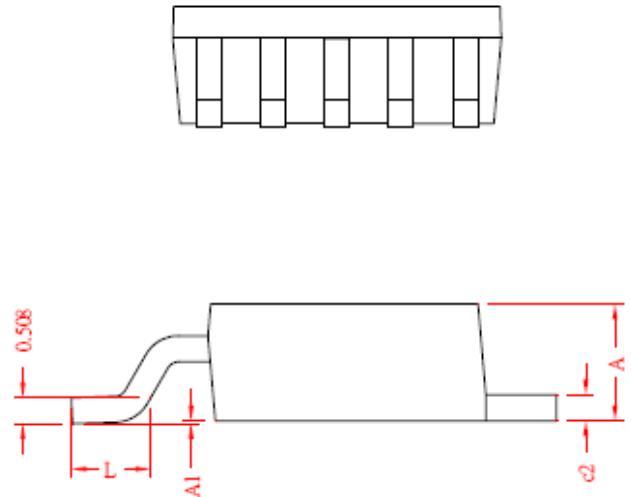
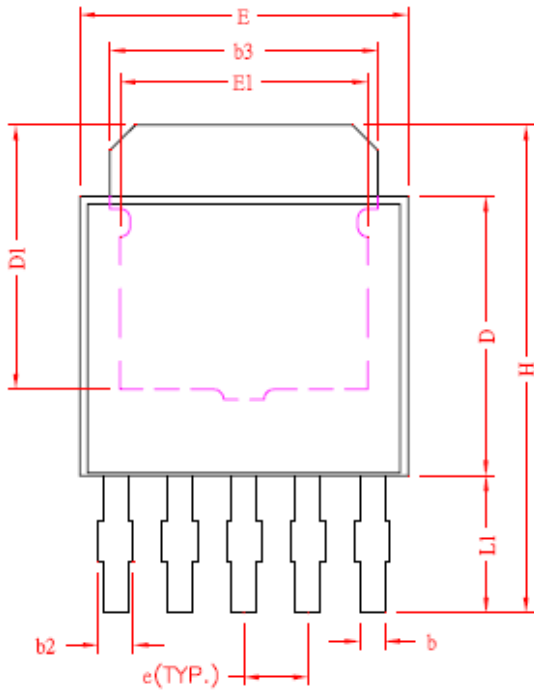




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TO-252-5L PACKAGE OUTLINE



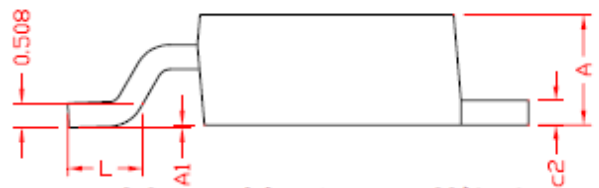
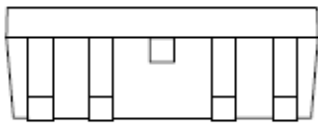
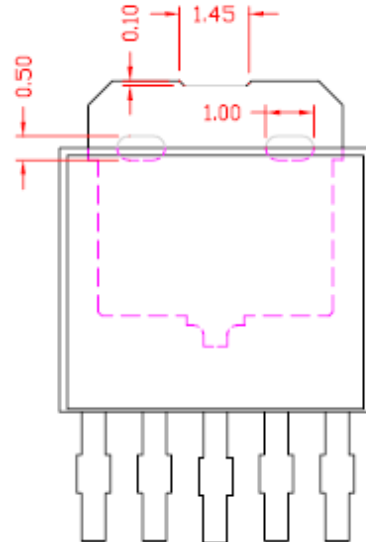
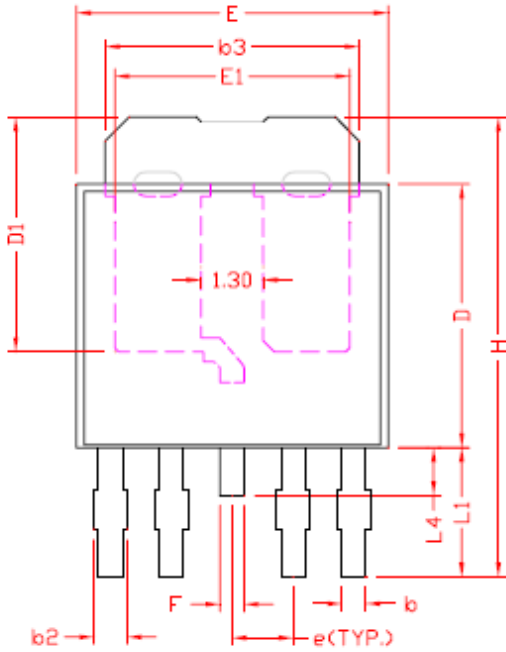
DIMENSIONS					
REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.20	2.40	D1	4.57	---
A1	0	0.15	E	6.35	6.73
b	0.45	0.60	E1	3.81	---
b2	0.50	0.80	e	1.27 REF.	
b3	5.21	5.46	H	9.40	10.20
c2	0.46	0.58	L	1.40	1.77
D	5.40	5.59	L1	2.40	3.00



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TO-252-4L PACKAGE OUTLINE



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.20	2.40	E	6.40	6.80
A1	0	0.15	E1	3.81	---
b	0.40	0.60	e	1.27 REF.	
b2	0.50	0.80	F	0.40	0.60
b3	5.20	5.50	H	9.40	10.20
c2	0.45	0.55	L	1.40	1.77
D	5.40	5.80	L1	2.40	3.00
D1	4.27	---	L4	0.80	1.20



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