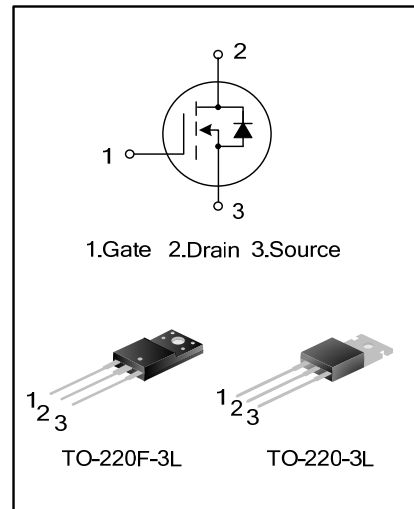


12A, 600V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVD12N60T/F is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary S-Rin™ structure DMOS technology. The improved planar stripe cell and the improved guarding ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

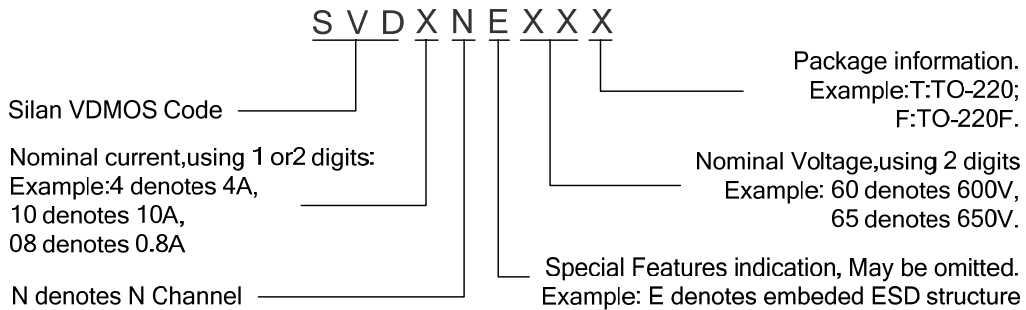
These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

- * 12A,600V, $R_{DS(on)(typ)}=0.58\Omega@V_{GS}=10V$
- * Low gate charge
- * Low Crss
- * Fast switching
- * Improved dv/dt capability

NOMENCLATURE



ORDERING SPECIFICATIONS

Part No.	Package	Marking	Material	Packing
SVD12N60T	TO-220-3L	SVD12N60T	Pb free	Tube
SVD12N60F	TO-220F-3L	SVD12N60F	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Rating		Unit
		SVD12N60T	SVD12N60F	
Drain-Source Voltage	V_{DS}	600		V
Gate-Source Voltage	V_{GS}	± 30		V
Drain Current	I_D	12		A
Drain Current Pulsed	I_{DM}	48		A
Power Dissipation($T_C=25^{\circ}\text{C}$) -Derate above 25°C	P_D	225	51	W
		1.8	0.41	W/ $^{\circ}\text{C}$
Single Pulsed Avalanche Energy (Note 1)	E_{AS}	1206		mJ
Operation Junction Temperature	T_J	150		$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-55~+150		$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

Parameter	Symbol	Rating		Unit
		SVD12N60T	SVD12N60F	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.56	2.44	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	120	$^{\circ}\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	$B_{V_{DS}}$	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	600	--	--	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=600\text{V}, V_{GS}=0\text{V}$	--	--	10	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 30\text{V}, V_{DS}=0\text{V}$	--	--	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu\text{A}$	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=6.0\text{A}$	--	0.58	0.8	Ω
Input Capacitance	C_{iss}	$V_{DS}=25\text{V}, V_{GS}=0\text{V},$ $f=1.0\text{MHZ}$	--	1876	--	pF
Output Capacitance	C_{oss}		--	167	--	
Reverse Transfer Capacitance	C_{rss}		--	20	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=300\text{V}, I_D=12\text{A},$ $R_G=25\Omega$ (Note 2,3)	--	30	--	ns
Turn-on Rise Time	t_r		--	79	--	
Turn-off Delay Time	$t_{d(off)}$		--	150	--	
Turn-off Fall Time	t_f		--	89	--	
Total Gate Charge	Q_g	$V_{DS}=480\text{V}, I_D=12\text{A},$ $V_{GS}=10\text{V}$ (Note 2,3)	--	51.7	--	nC
Gate-Source Charge	Q_{gs}		--	9.6	--	
Gate-Drain Charge	Q_{gd}		--	18.6	--	

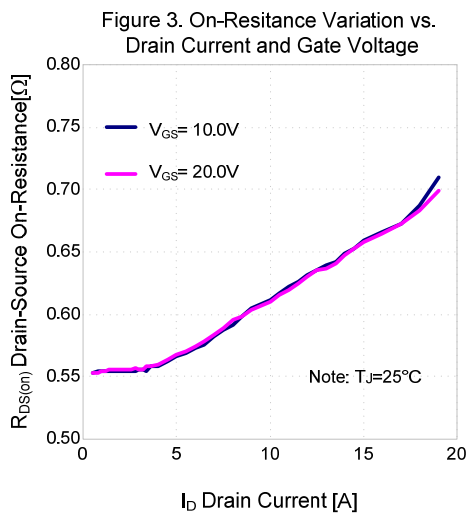
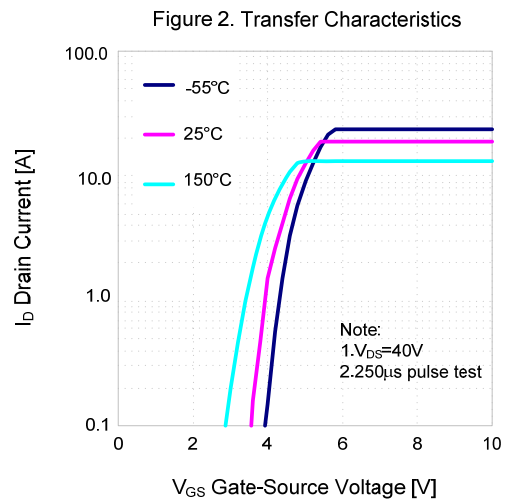
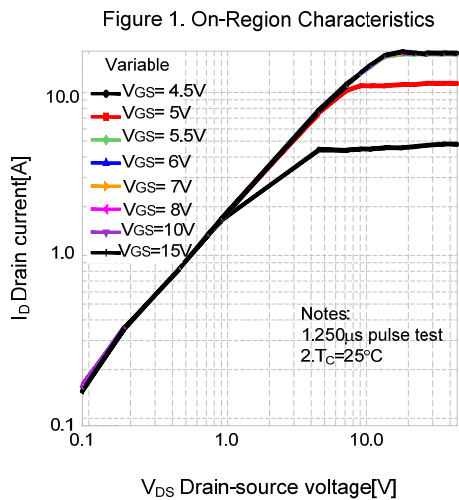
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse p-n	--	--	12	A
Pulsed Source Current	I_{SM}	Junction Diode in the MOSFET	--	--	48	
Diode Forward Voltage	V_{SD}	$I_S=12A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_S=12A, V_{GS}=0V,$	--	420	--	ns
Reverse Recovery Charge	Q_{rr}	$di/dt=100A/\mu S$ (Note 2)	--	4.9	--	μC

Notes:

1. $L=30mH, I_{AS}=7.5A, V_{DD}=245V, R_G=25\Omega,$ starting $T_J=25^\circ C;$
2. Pulse Test: Pulse width $\leq 300\mu s,$ Duty cycles $\leq 2\%;$
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (continued)

Figure 5. Breakdown Voltage Variation vs. Temperature

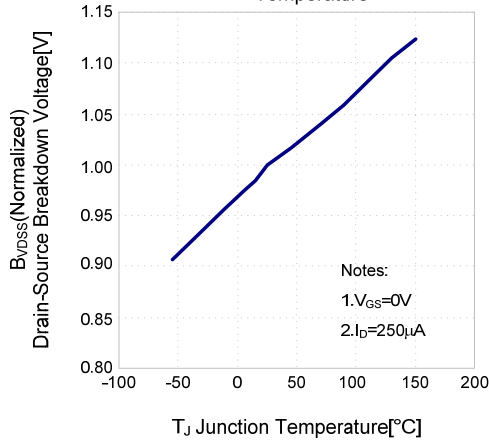


Figure 6. On-resistance Variation vs Temperature

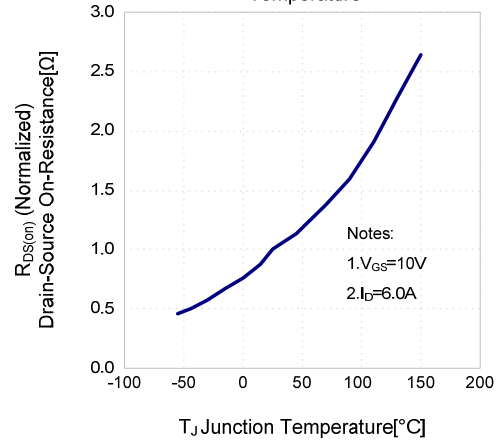


Figure 7 Capacitance Characteristics

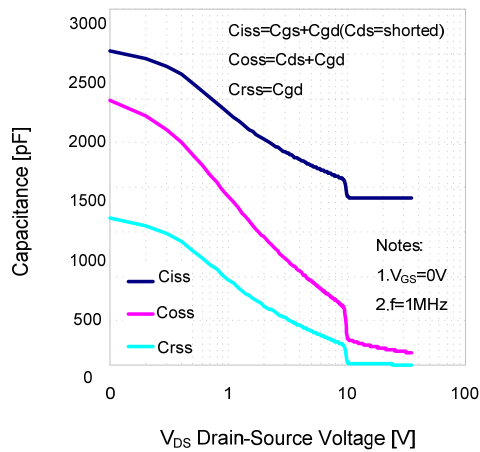


Figure 8-1. Max. Safe Operating Area(SVD12N60T)

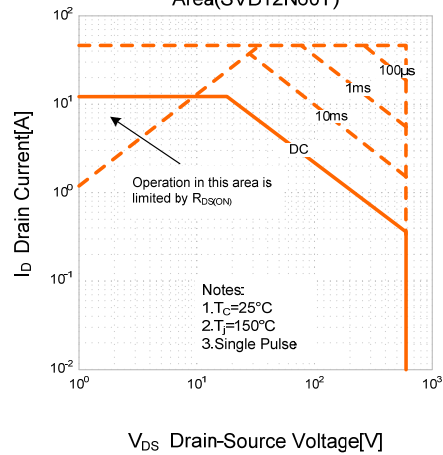


Figure 8-2. Max. Safe Operating Area(SVD12N60F)

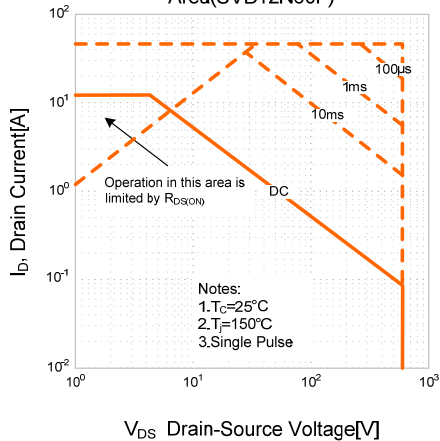
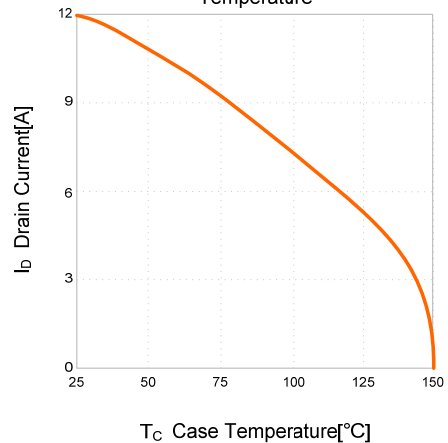
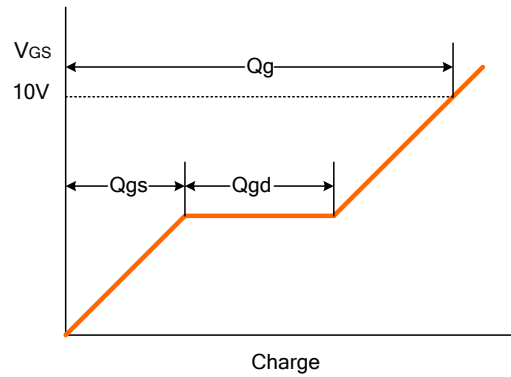
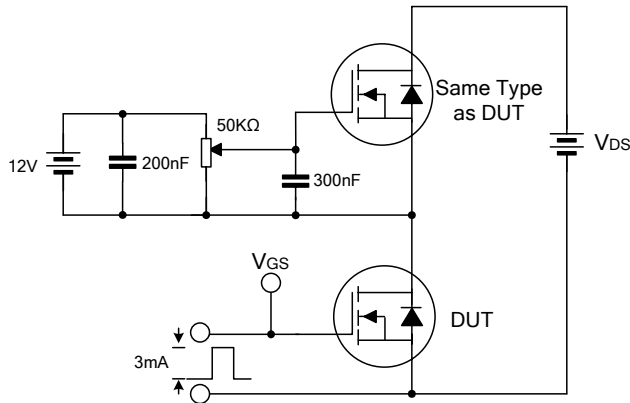


Figure 9. Max. Drain Current vs. Case Temperature

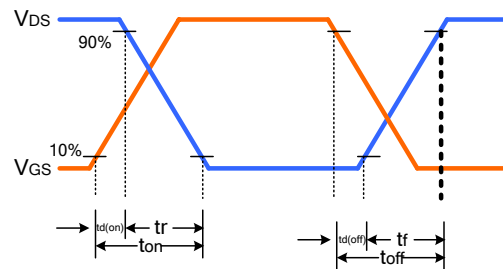
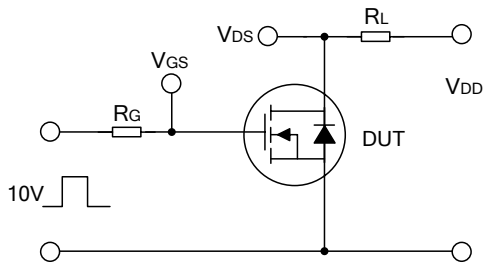


TYPICAL TEST CIRCUIT

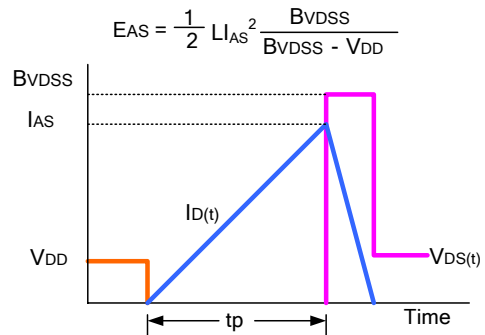
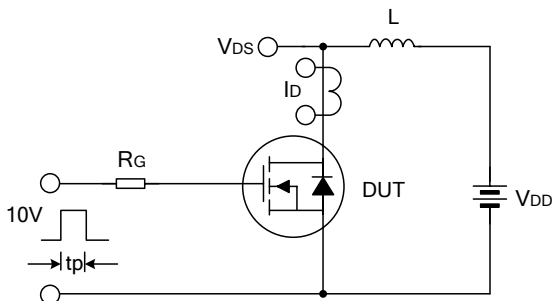
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



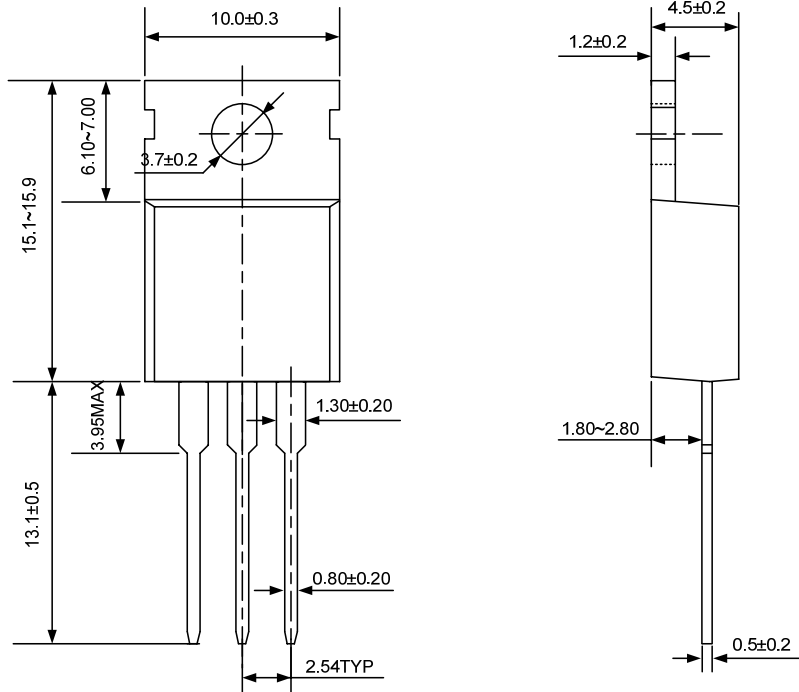
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

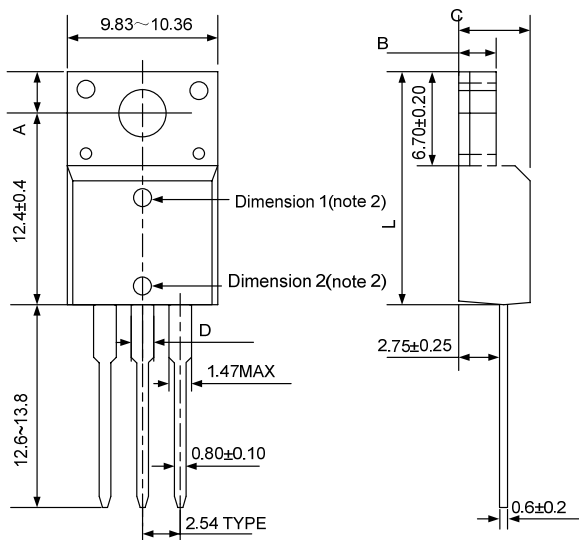
TO-220-3L

UNIT: mm



TO-220F-3L

UNIT: mm



Symbol(note1)	Dimension1	Dimension2
A	3.30±0.15	2.70±0.15
B	2.55±0.20	3.0±0.20
C	4.72±0.2	4.50±0.20
D	1.47MAX	1.75MAX
L	15.75±0.30	15.00±0.30

Note1: There may be two values for some products due to different plastic mould machine, so two dimensions of the same position are listed;
 Note2: When the product size is Dimension1, the thimble hole is on top of the surface; when the size is Dimension2, the center hole is on bottom of the surface.



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- Silan will supply the best possible product for customers!



ATTACHMENT

Revision History

Date	REV	Description	Page
2010.05.25	1.0	Original	
2010.09.20	1.1	Modify" ABSOLUTE MAXIMUM RATINGS"; "THERMAL CHARACTERISTICS", Add SOA and ID-TC	
2010.10.21	1.2	Modify" TYPICAL CHARACTERISTICS", the template of Datasheet	