SC4626

2.5MHz, 1A Synchronous Step Down Regulator in SOT23-5

Features

- V_{IN} Range: 2.9 – 5.5V
- V_{OUT} Options: 1.0 - 3.3V
- Up to 1A Output Current
- 2.5MHz Switching Frequency
- Efficiency Up to 93%
- Low Output Noise Across Load Range
- Excellent Transient Response
- Start Up into Pre-Bias Output
- 100% Duty-Cycle Low Dropout Operation
- <1µA Shutdown Current
- Internal Soft Start
- Input Under-Voltage Lockout
- Output Over-Voltage, Current Limit Protection
- Over-Temperature Protection
- Adjustable Output Voltage
- SOT23-5 Package
- Fully WEEE and RoHS Compliant

Applications

- Bluetooth Radios
- DSC and PMPs
- GPS Devices
- xDSL Systems
- POL Regulators
- Portable HDD
- Wireless LAN

Description

The SC4626 is a high efficiency, synchronous step-down regulator providing up to 1A output current in a SOT23-5 package. The device requires only three external filter components for a complete step-down regulator solution. The input voltage range is 2.9 to 5.5V with either factory programmed outputs from 1.0 to 3.3V or adjustable output via an external resistor divider.

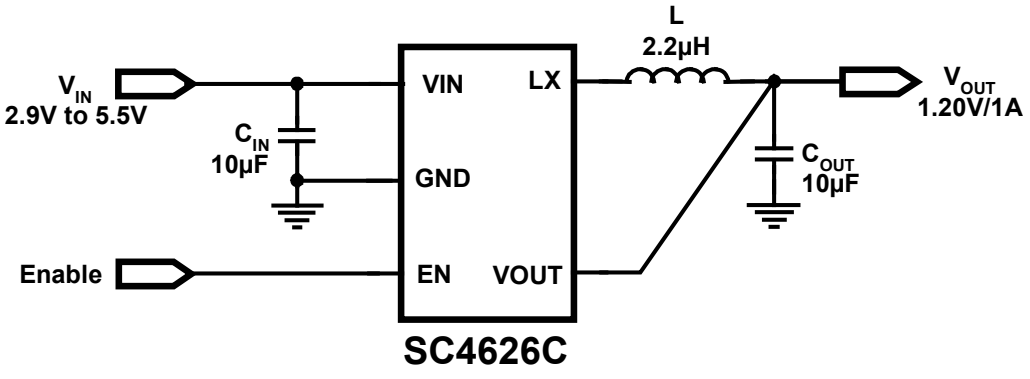
The converter operates at fixed 2.5MHz switching frequency allowing small L/C filtering components. The voltage mode architecture is compatible with chip inductors and capacitors for minimum PCB footprint and lowest overall system cost.

Up to 93% efficiency is achieved with low $R_{DS(ON)}$ internal switches. PWM constant frequency operation ensures low output ripple across the load range. 100% duty-cycle provides 300mV dropout voltage at 1A which extends the minimum input voltage for 2.5V and 3.3V outputs. Excellent transient response is achieved with no external compensation components.

The SC4626 provides input under-voltage, output over-voltage, output short circuit and over-temperature protection to safeguard the device and system under fault conditions. The regulator provides integrated soft-start to minimize inrush currents. Standby quiescent current is less than 1µA.

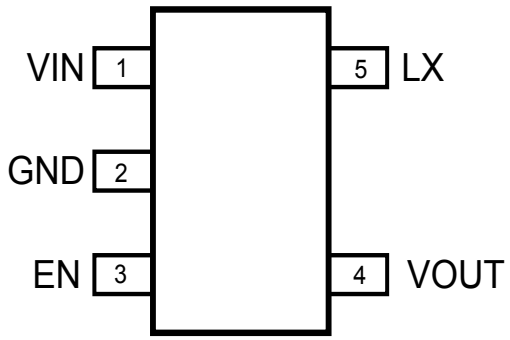
The SC4626 is available in a SOT23-5 package.

Typical Application Circuit



Pin Configuration

(TOP VIEW)



SOT23-5

θ_{JA} = 90°C/W(1)

Ordering Information

Device	Package & Description
SC4626xSKTRT(2)(3)(4)	SOT23-5
SC4626xEVB(5)	Evaluation Board - Standard Size (i.e., Wire Wound Inductor)
SC4626xEVB-1(5)	Evaluation Board - Small Size (i.e., Chip Inductor)

Notes:

(1) Measured in free convection, mounted on 10mm x 10mm, 2 layer FR4 PCB shown in figure 4 with copper of 1oz for each layer.

(2) Available in tape and reel only. A reel contains 3,000 devices.

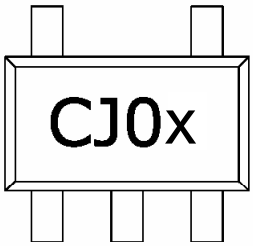
(3) Device is Pb-free, Halogen free, and RoHS/WEEE compliant.

(4) "x" is the code of the output voltage. See Table 1 for the code. For example, the device number for VOUT= 1.20V is SC4626CSKTRT.

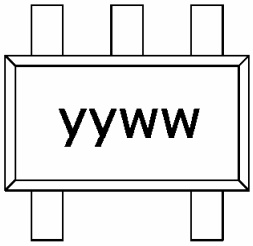
(5) "x" is the code of the output voltage. See Table 1 for the code. For example, the EVB for VOUT= 1.20V is SC4626CEVB (Standard Size) or SC4626CEVB-1 (Small Size).

Marking Information

Top Mark



Bottom Mark



Marking for SOT23, 5 Lead Package:
x = Code of the output voltage (Example: C for VOUT=1.20V)
yyww = Datecode (Example: 0852)

Table 1: Available Output Voltages

Code	VOUT(1)
A	1.00
C	1.20
E	1.28
F	1.30
H	1.50
L	1.80
Y	2.50
Z	3.30

Notes:

(1) Contact factory for unavaliable output voltage options.

Absolute Maximum Ratings

VIN Supply Voltage ..... -0.3 to 6.0V
LX Voltage ..... -1 to V_{IN}+1V, -3V (20ns Max), 6V Max
VOUT Voltage ..... -0.3 to V_{IN}+0.3V
EN Voltage ..... -0.3 to V_{IN}+0.3V
Peak IR Reflow temperature ..... 260°C
ESD Protection Level(2) 3kV

Recommended Operating Conditions

VIN Supply Voltage ..... 2.9 to 5.5V
Maximum Output Current 1.0A

Thermal Information

Thermal Resistance, Junction to Ambient(1) ..... 90°C/W
Maximum Junction Temperature ..... +150°C
Operating Junction Temperature ..... -40 to +125°C
Storage Temperature Range ..... -65 to +150 °C

Exceeding the absolute maximum ratings may result in permanent damage to the device and/or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

Notes:
(1) Measured in free convection, mounted on 10mm x 10mm, 2 layer FR4 PCB shown in figure 4 with copper of 1oz for each layer.
(2) Tested according to JEDEC standard JESD22-A114-B.

Electrical Characteristics

Unless specified: V_{IN} = 5.0V; -40°C<T_A<+85 °C; $T_{J(MAX)}$=125°C; Unless otherwise noted typical values are T_A=+25 °C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Under-Voltage Lockout	UVLO	Rising V_{IN}	2.60	2.70	2.80	V
		Hysteresis		250		mV
Output Voltage Tolerance(1)	ΔV_{OUT}	V_{IN}=3.6V to 5.0V; No Load	-2.5		+2.5	%
Current Limit	I_{LIMIT}	Peak inductor current	1.5			A
VIN Supply Current	I_Q	EN= VIN, No Load		7.5		mA
VIN Shutdown Current	I_{SHDN}	EN= GND		1	10	µA
High Side Switch Resistance	R_{DSON_P}	I_{LX}= 100mA		0.15		Ω
Low Side Switch Resistance	R_{DSON_N}	I_{LX}= -100mA		0.125		
LX Leakage Current	$I_{LK(LX)}$	V_{IN}=5.5V; L_X=0V; EN=GND		1	10	µA
		V_{IN}=5.5V; L_X=5.0V; EN=GND	-10	-1		
Line Regulation	$\Delta V_{LINE-REG}$	V_{IN}= 3.6 – 5.0V; I_{OUT}=0A		±1.0		%
Load Regulation(2)	$\Delta V_{LOAD-REG}$	V_{IN}= 5.0V; I_{OUT}=10mA – 1.0A		±1.0		%
Oscillator Frequency	F_{OSC}		2.0	2.5	3.0	MHz
Soft-Start Time(2)	T_{SS}			100		µs
EN Input High Current	I_{EN_HI}	EN=VIN	-2.0		2.0	µA
EN Input Low Current	I_{EN_LO}	EN=GND	-2.0		2.0	µA
EN Input High Threshold	V_{EN_HI}		1.2			V
EN Input Low Threshold	V_{EN_LO}				0.4	V

Electrical Characteristics (continued)

Unless specified: V_{IN} = 5.0V; -40°C<T_A<+85 °C; $T_{J(MAX)}$=125°C; Unless otherwise noted typical values are T_A=+25 °C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VOUT Over Voltage Protection(2)	V_{OVP}			115		%
Thermal Shutdown Temperature (2)	T_{SD}	Junction Temperature		+160		°C
Thermal Shutdown Hysteresis (2)	T_{SD_HYS}	Junction Temperature		10		°C

Notes:

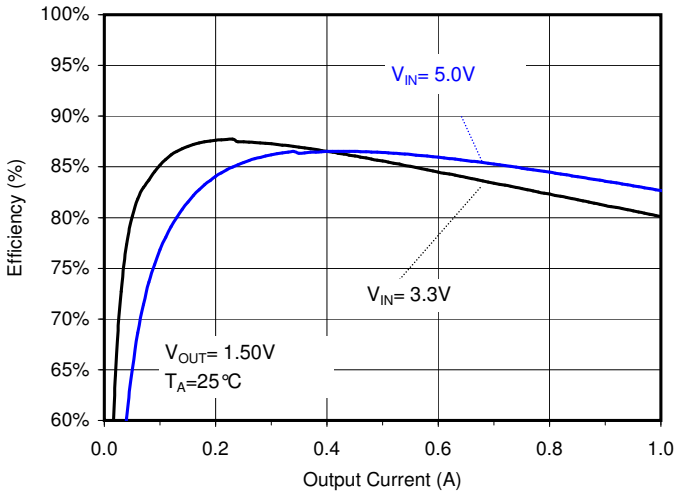
(1) The "Output Voltage Tolerance" includes output voltage accuracy, voltage drift over temperature and the line regulation.

(2) Guaranteed by design.

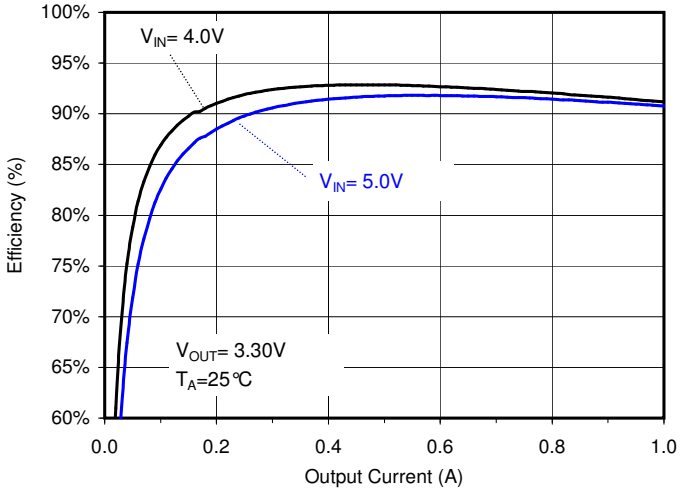
Typical Characteristics

Circuit Conditions: V_{OUT}=1.0V (SC4626A), 1.5V (SC4626H) & 3.3V (SC4626Z);C_{IN}= 10uF/6.3V;C_{OUT}= 10uF/6.3V for L=2.2uH;C_{OUT}= 22uF/6.3V for L=1uH. Unless otherwise noted, L= 2.2uH (TOKO: 1071AS-2R2M).

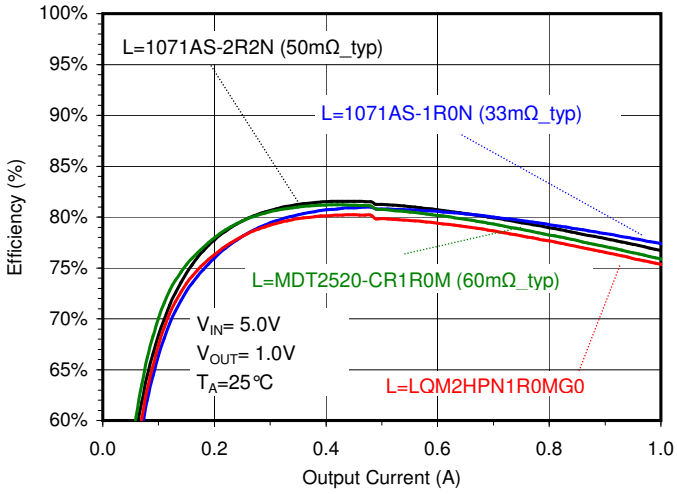
Efficiency vs. Load Current (V_{OUT}=1.5V)



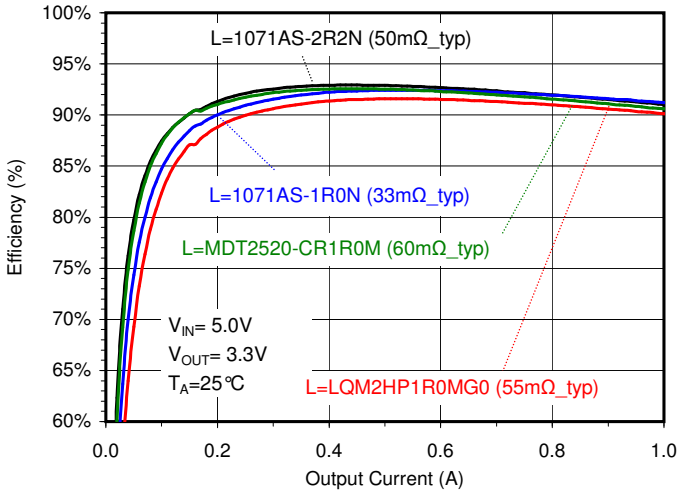
Efficiency vs. Load Current (V_{OUT}=3.3V)



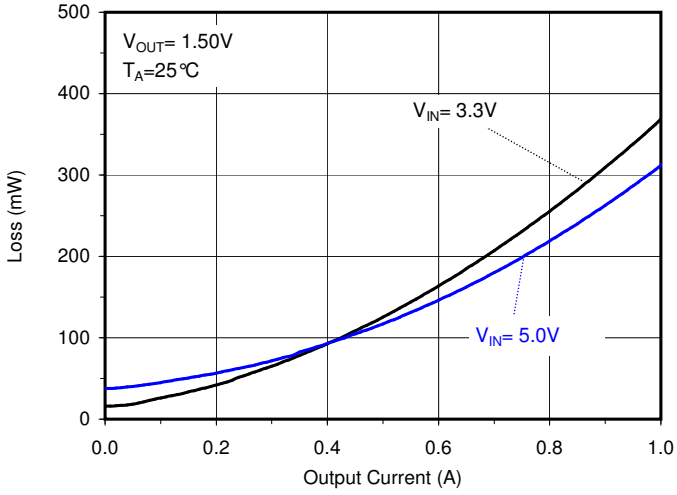
Efficiency vs. Load Current (V_{IN}=5.0V, V_{OUT}=1.0V)



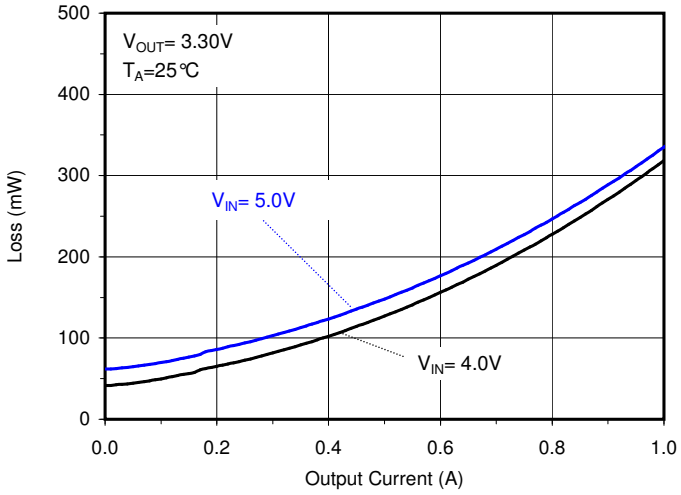
Efficiency vs. Load Current (V_{IN}=5.0V, V_{OUT}=3.3V)



Total Loss vs. Load Current (V_{OUT}=1.5V)



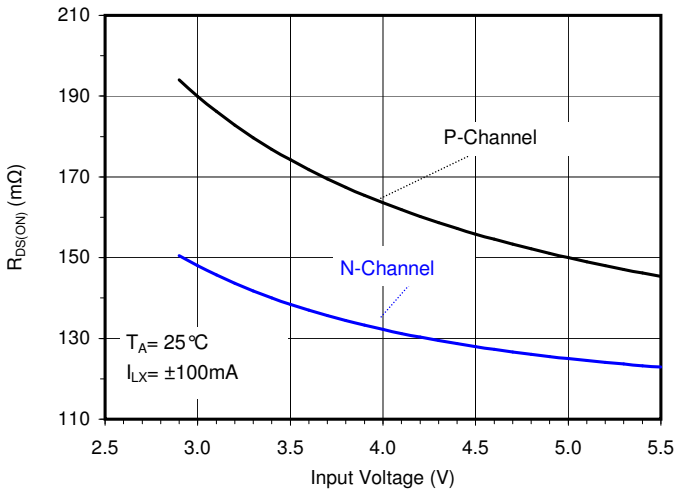
Total Loss vs. Load Current (V_{OUT}=3.3V)



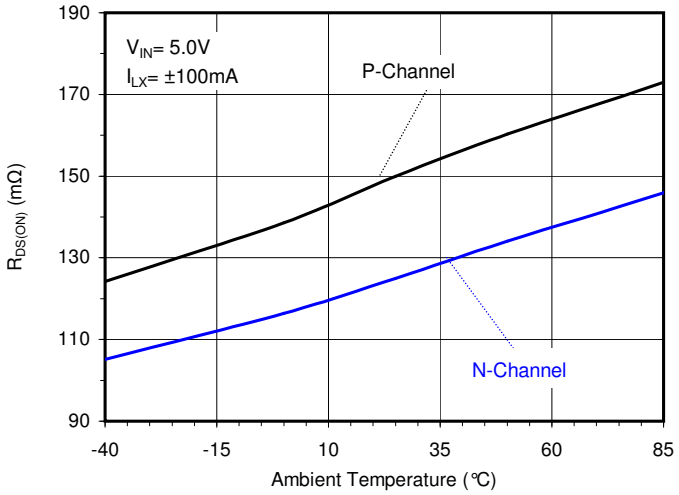
Typical Characteristics (continued)

Circuit Conditions: V_{OUT}=1.0V (SC4626A), 1.5V (SC4626H) & 3.3V (SC4626Z);C_{IN}= 10uF/6.3V;C_{OUT}= 10uF/6.3V for L=2.2uH;C_{OUT}= 22uF/6.3V for L=1uH. Unless otherwise noted, L= 2.2uH (TOKO: 1071AS-2R2M).

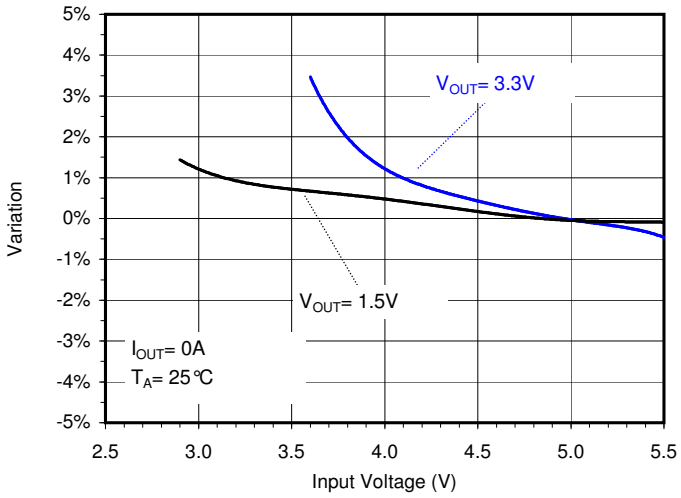
$R_{DS(ON)}$ vs. Input Voltage



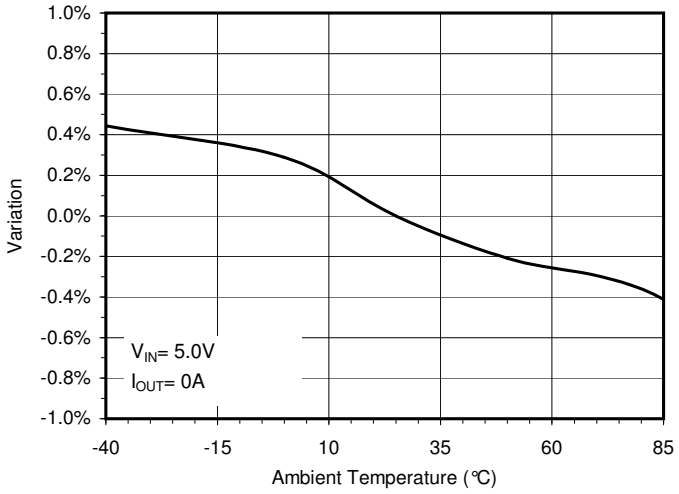
$R_{DS(ON)}$ vs. Temperature



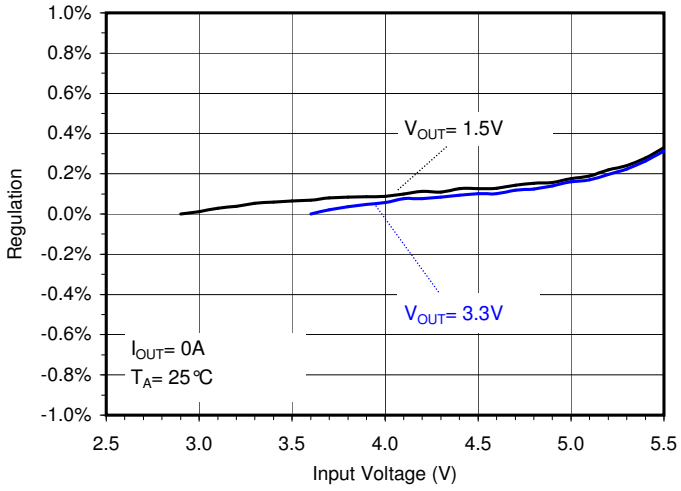
Switching Frequency vs. Input Voltage



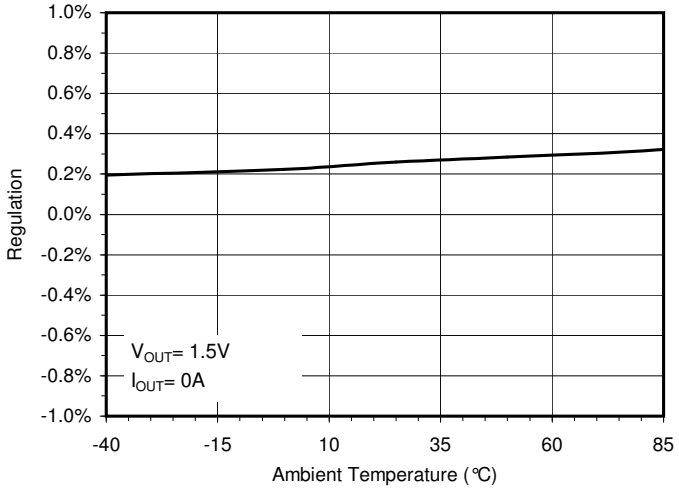
Switching Frequency vs. Temperature



Line Regulation



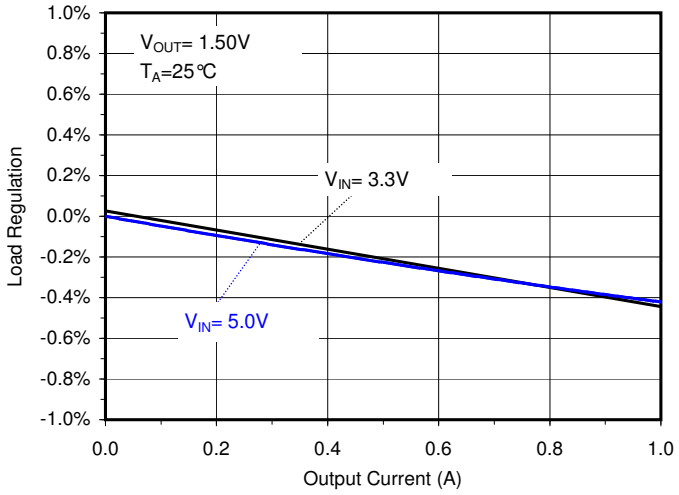
Line Regulation vs. Temperature



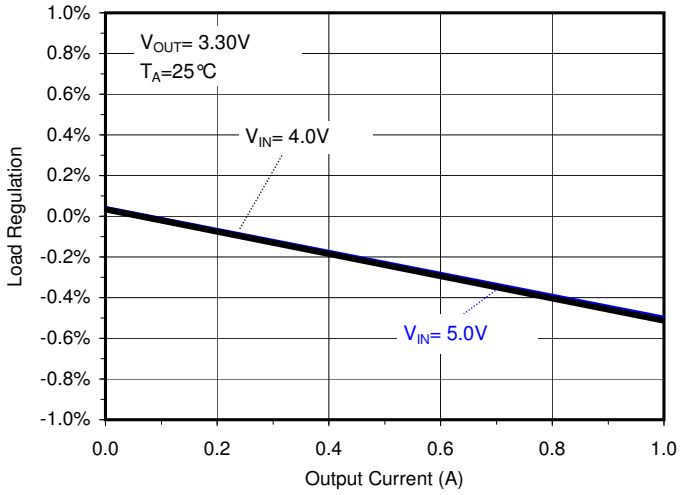
Typical Characteristics (continued)

Circuit Conditions: V_{OUT}=1.0V (SC4626A), 1.5V (SC4626H) & 3.3V (SC4626Z);C_{IN}= 10uF/6.3V;C_{OUT}= 10uF/6.3V for L=2.2uH;C_{OUT}= 22uF/6.3V for L=1uH. Unless otherwise noted, L= 2.2uH (TOKO: 1071AS-2R2M).

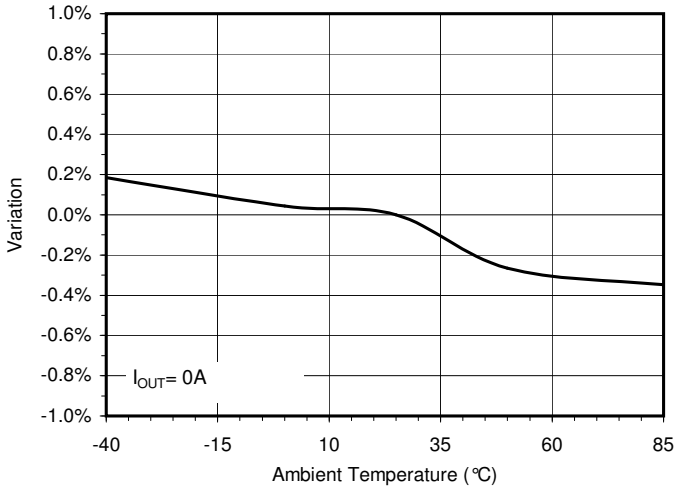
Load Regulation (V_{OUT}=1.5V)



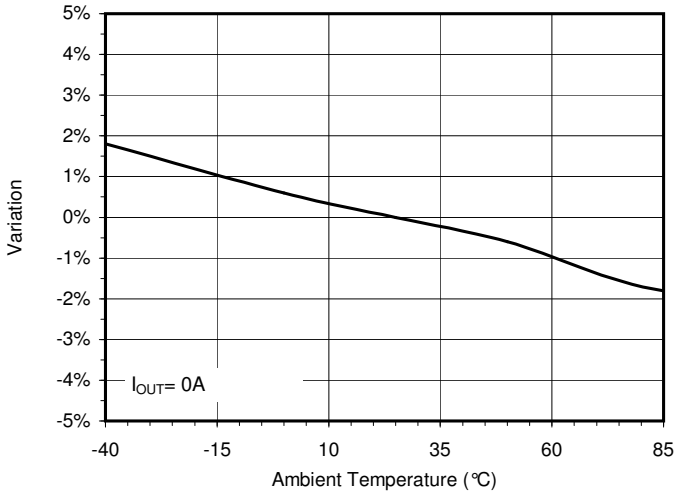
Load Regulation (V_{OUT}=3.3V)



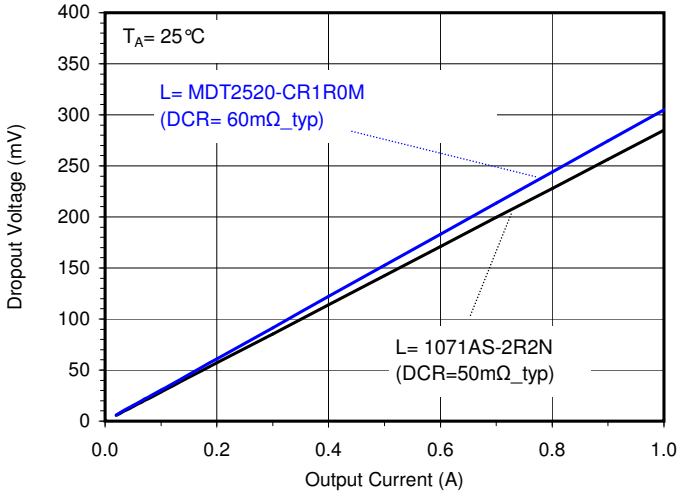
UVLO Rising Threshold Variation



UVLO Hysteresis Variation



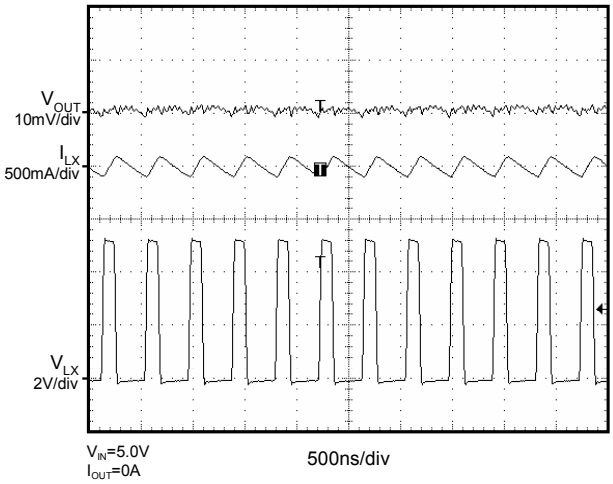
Dropout Voltage in 100% Duty Cycle Operation



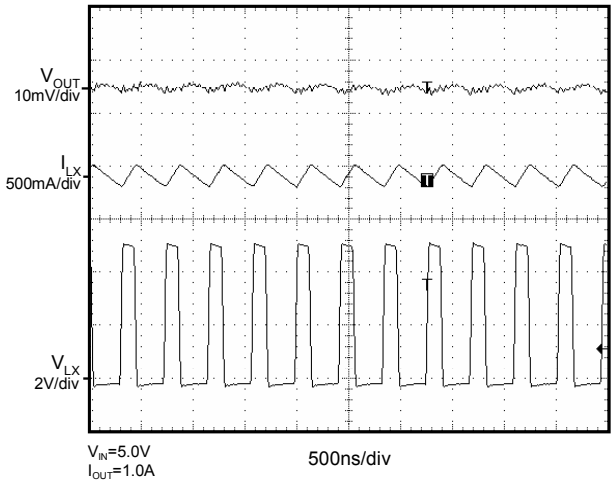
Typical Waveforms

Circuit Conditions: V_{OUT}=1.5V (SC4626H); L= 2.2uH (TOKO: 1071AS-2R2M); C_{IN}= C_{OUT}= 10uF/6.3V (Murata: GRM21BR60J106K).

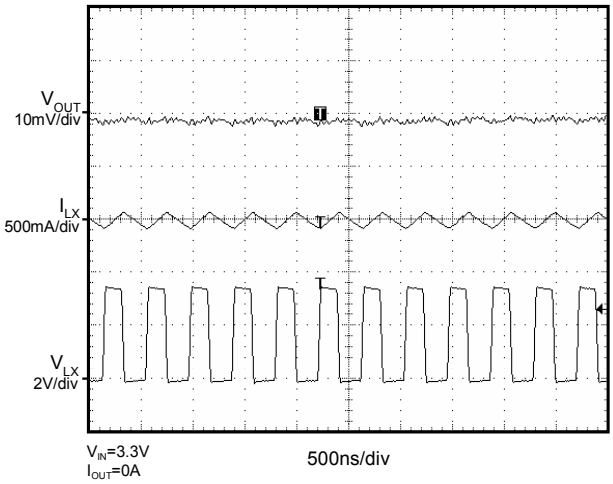
Output Voltage Ripple (V_{OUT}=1.5V)



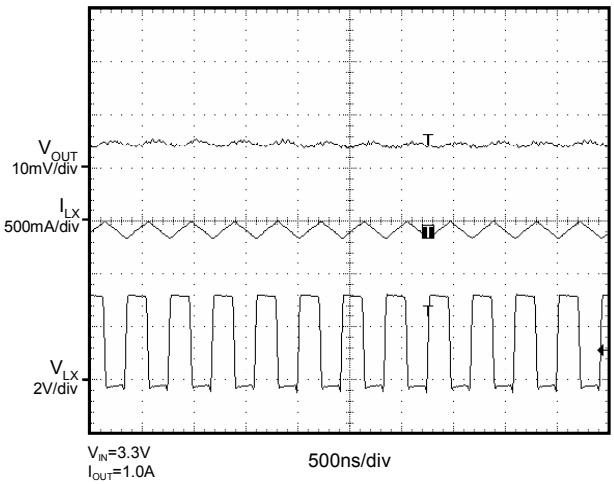
Output Voltage Ripple (V_{OUT}=1.5V)



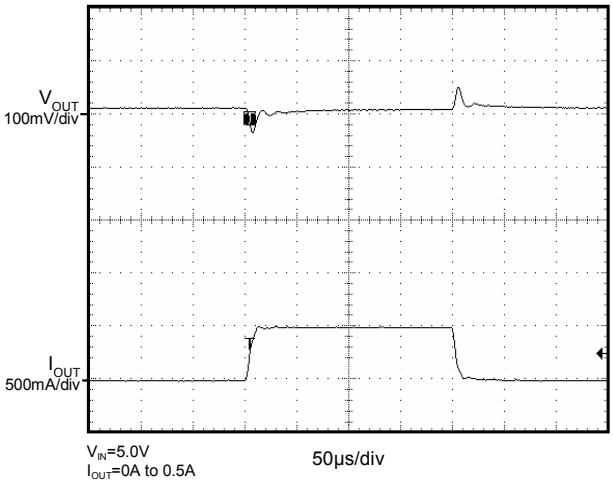
Output Voltage Ripple (V_{OUT}=1.5V)



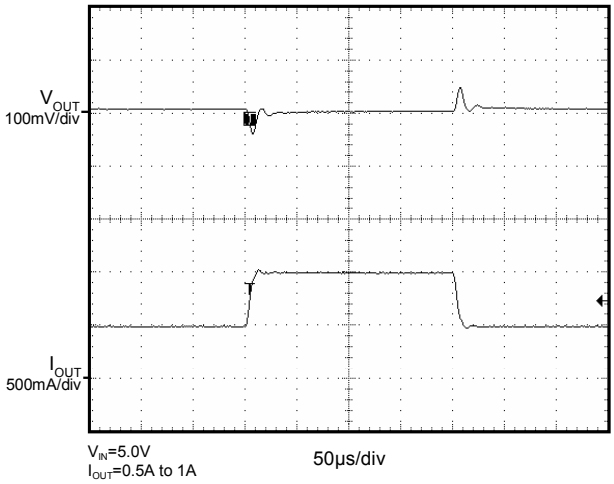
Output Voltage Ripple (V_{OUT}=1.5V)



Transient Response (V_{OUT}=1.5V; 0A to 0.5A)



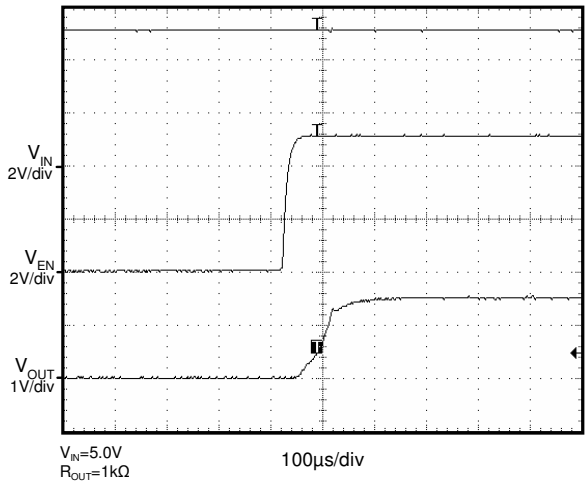
Transient Response (V_{OUT}=1.5V; 0.5A to 1.0A)



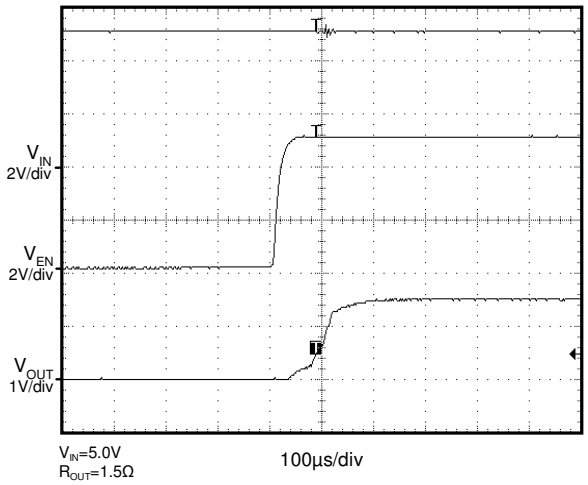
Typical Waveforms (continued)

Circuit Conditions: V_{OUT}=1.5V (SC4626H); L= 2.2uH (TOKO: 1071AS-2R2M); C_{IN}= C_{OUT}= 10uF/6.3V (Murata: GRM21BR60J106K).

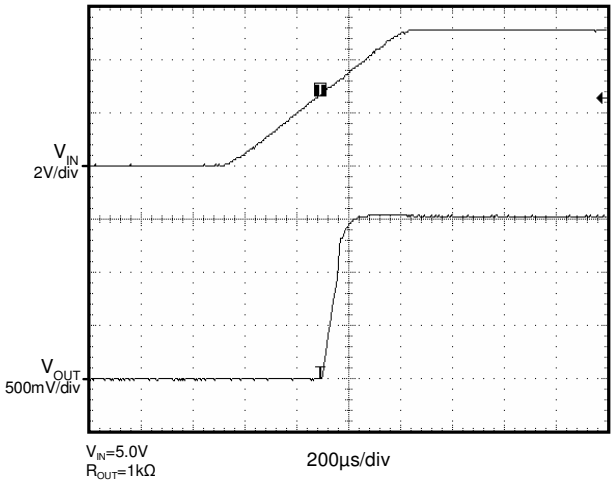
Start Up (Enable)(V_{OUT}=1.5V)



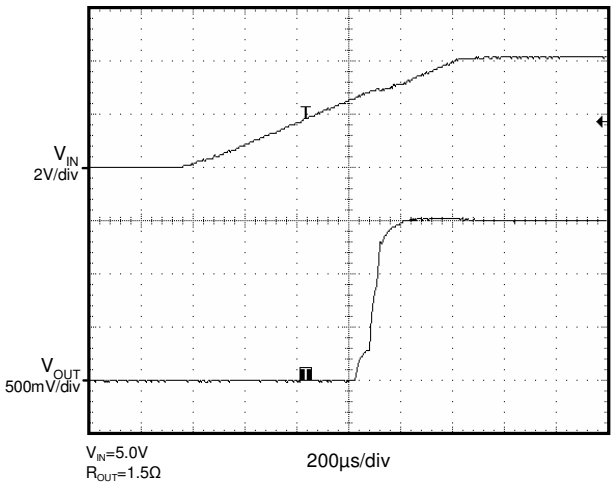
Start Up (Enable)(V_{OUT}=1.5V)



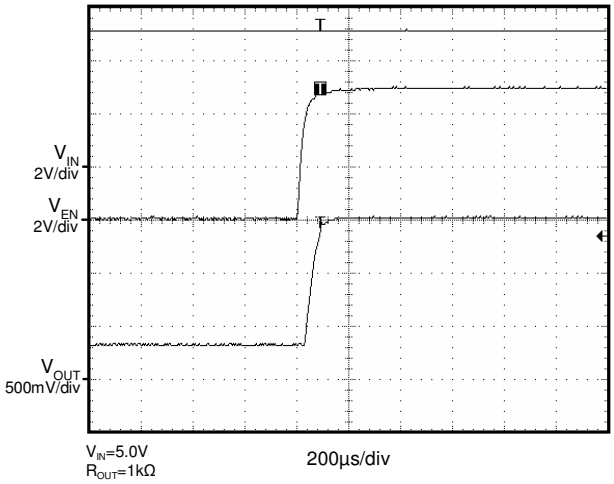
Start Up (Power up V_{IN}) (V_{OUT}=1.5V)



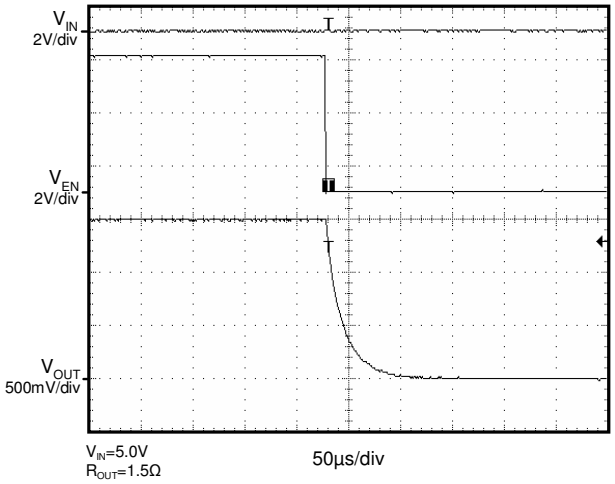
Start Up (Power up V_{IN}) (V_{OUT}=1.5V)



Start Up into Pre-Bias Output (Enable)



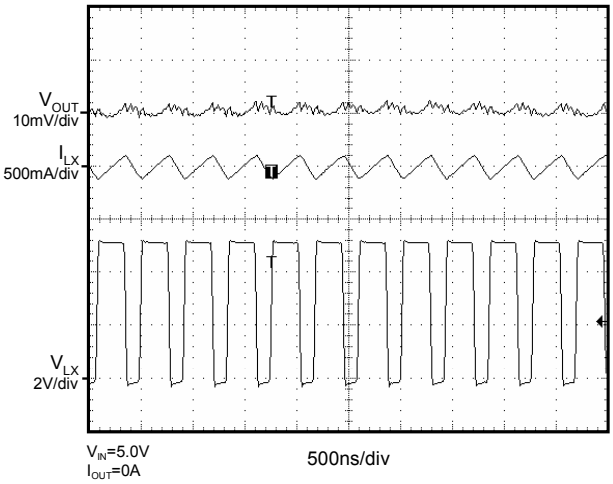
Shutdown (Disable) (V_{OUT}=1.5V)



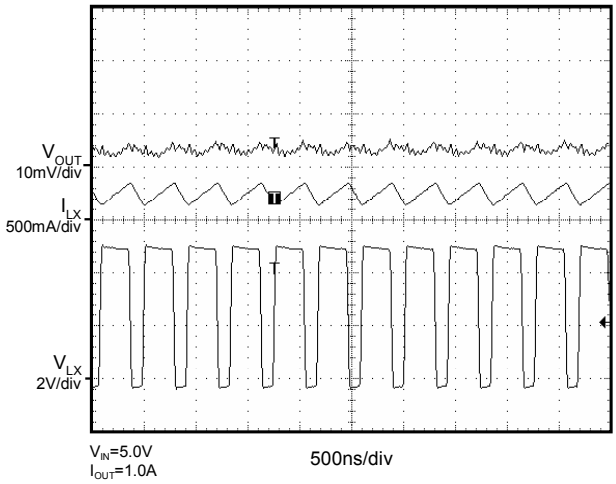
Typical Waveforms (continued)

Circuit Conditions: V_{OUT}=3.3V (SC4626Z); L= 2.2uH (TOKO: 1071AS-2R2M); C_{IN}= C_{OUT}= 10uF/6.3V (Murata: GRM21BR60J106K).

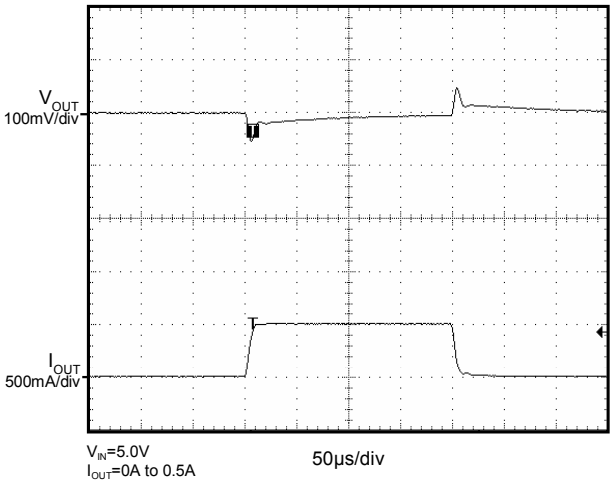
Output Voltage Ripple (V_{OUT}=3.3V)



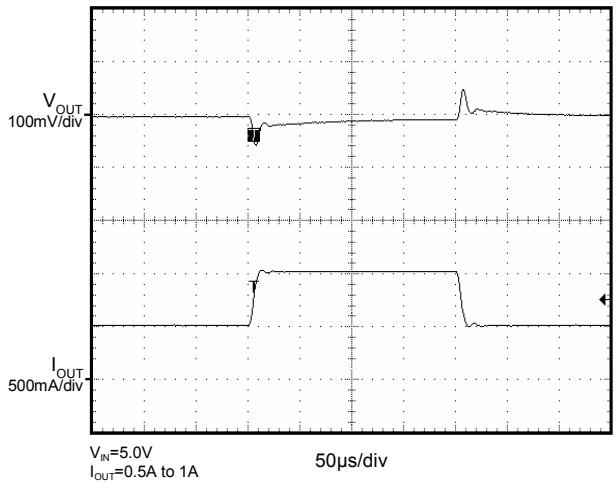
Output Voltage Ripple (V_{OUT}=3.3V)



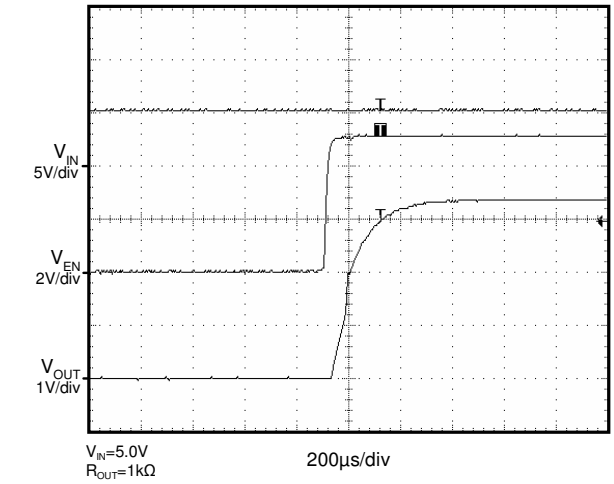
Transient Response (V_{OUT}=3.3V; 0A to 0.5A)



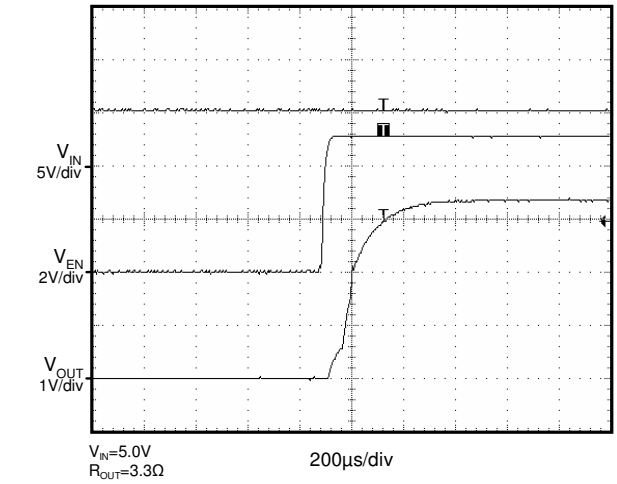
Transient Response (V_{OUT}=3.3V; 0.5A to 1.0A)



Start Up (Enable)(V_{OUT}=3.3V)



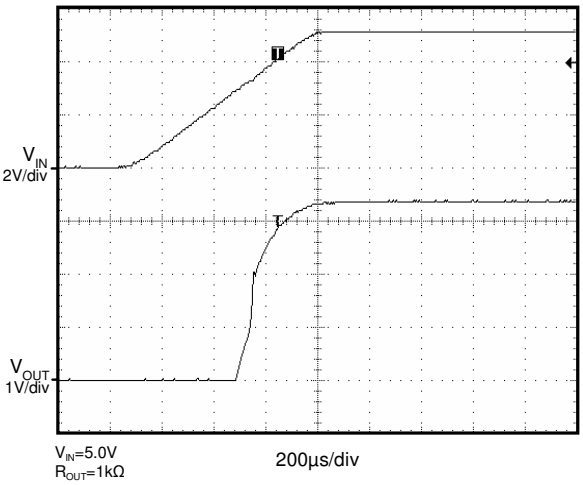
Start Up (Enable)(V_{OUT}=3.3V)



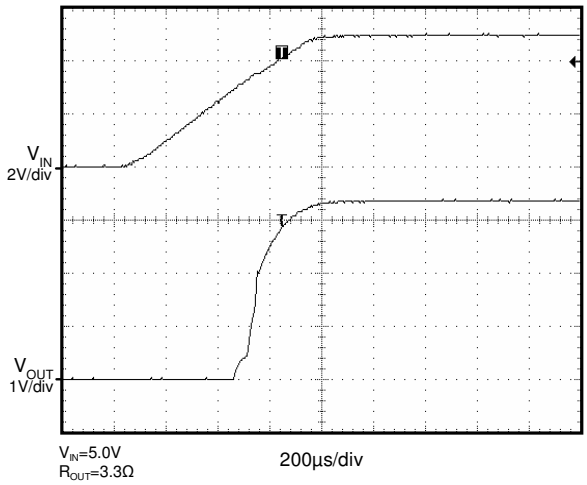
Typical Waveforms (continued)

Circuit Conditions: V_{OUT}=3.3V (SC4626Z); L= 2.2uH (TOKO: 1071AS-2R2M); C_{IN}= C_{OUT}= 10uF/6.3V (Murata: GRM21BR60J106K).

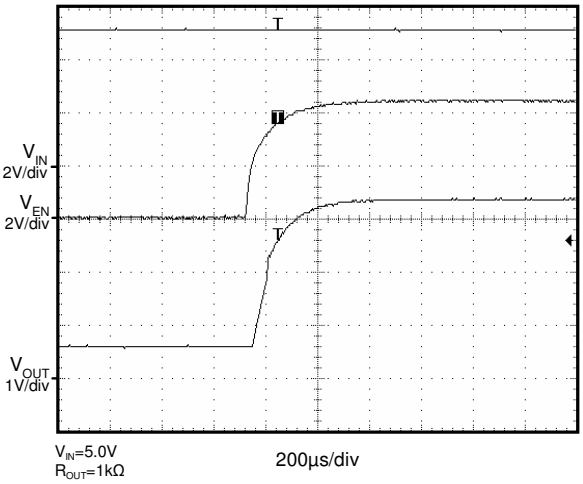
Start Up (Power up V_{IN}) (V_{OUT}=3.3V)



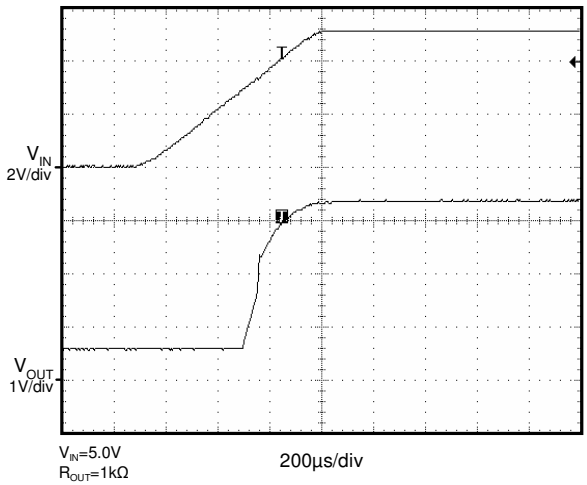
Start Up (Power up V_{IN}) (V_{OUT}=3.3V)



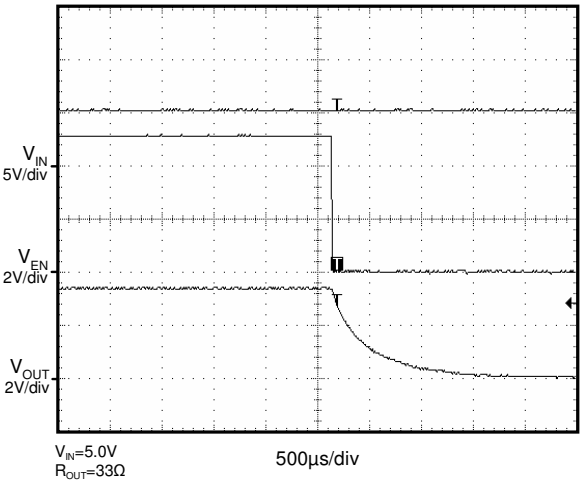
Start Up into Pre-Bias Output (Enable)



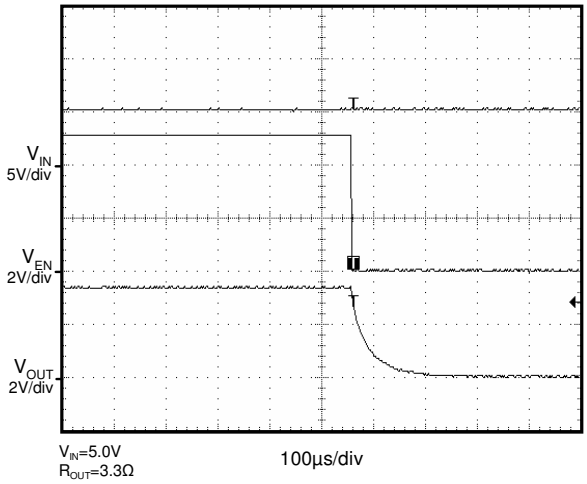
Start Up into Pre-Bias Output (Power Up V_{IN})



Shutdown (Disable) (V_{OUT}=3.3V)



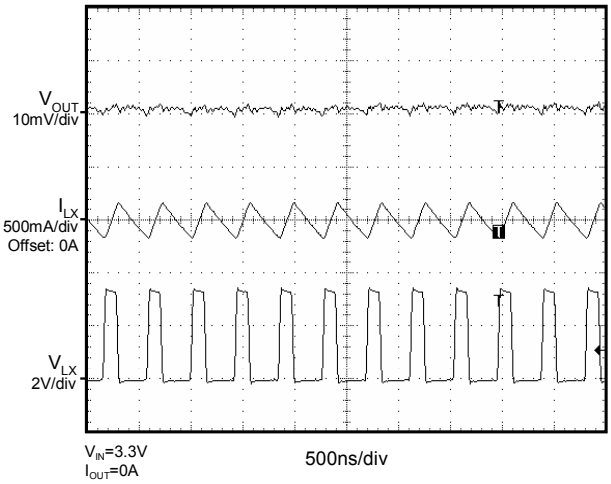
Shutdown (Disable) (V_{OUT}=3.3V)



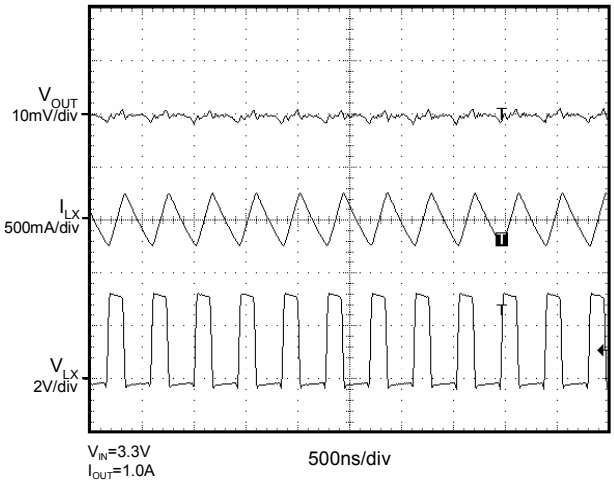
Typical Waveforms (continued)

Circuit Conditions: V_{OUT}=1.0V (SC4626A); L= 1.0uH (Murata: LQM2HPN1R0NG0L); C_{IN}= 10uF/6.3V; C_{OUT}= 22uF/6.3V (Murata: GRM21BR60J226M).

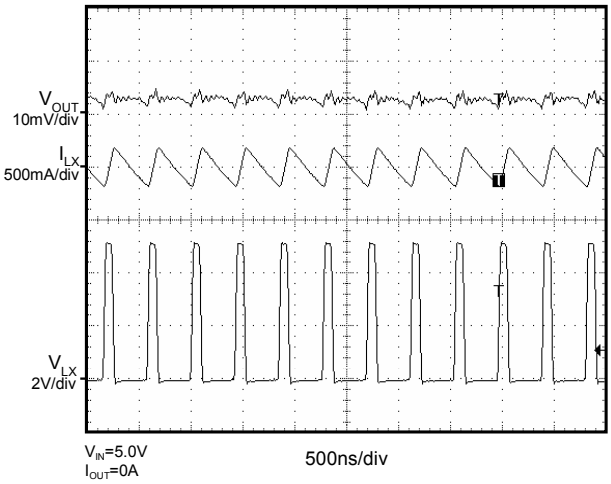
Output Voltage Ripple (V_{OUT}=1.0V)



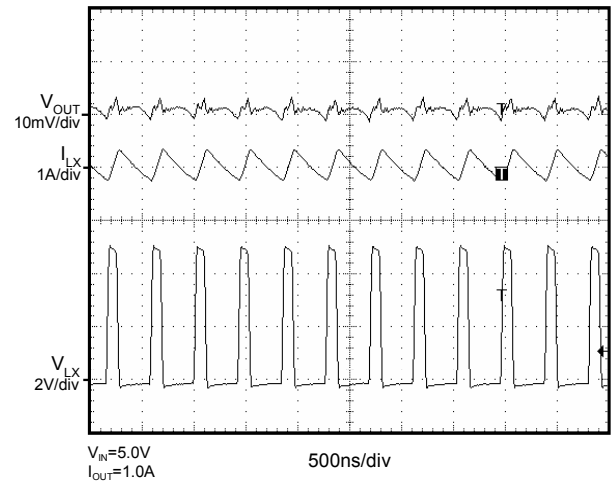
Output Voltage Ripple (V_{OUT}=1.0V)



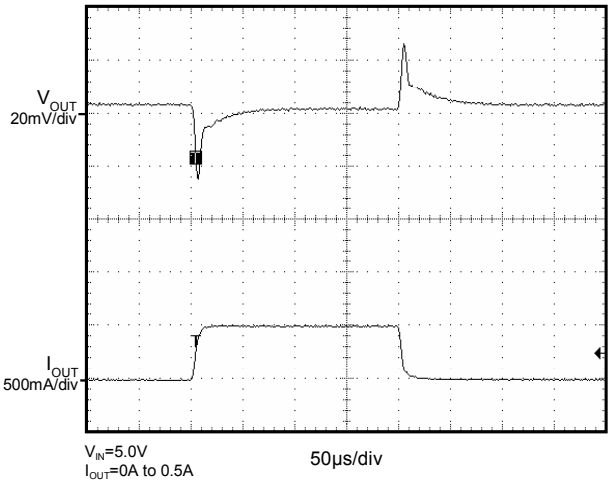
Output Voltage Ripple (V_{OUT}=1.0V)



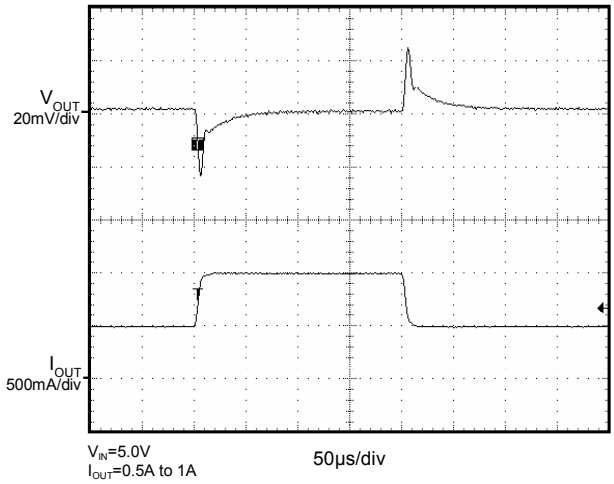
Output Voltage Ripple (V_{OUT}=1.0V)



Transient Response (V_{OUT}=1.0V)



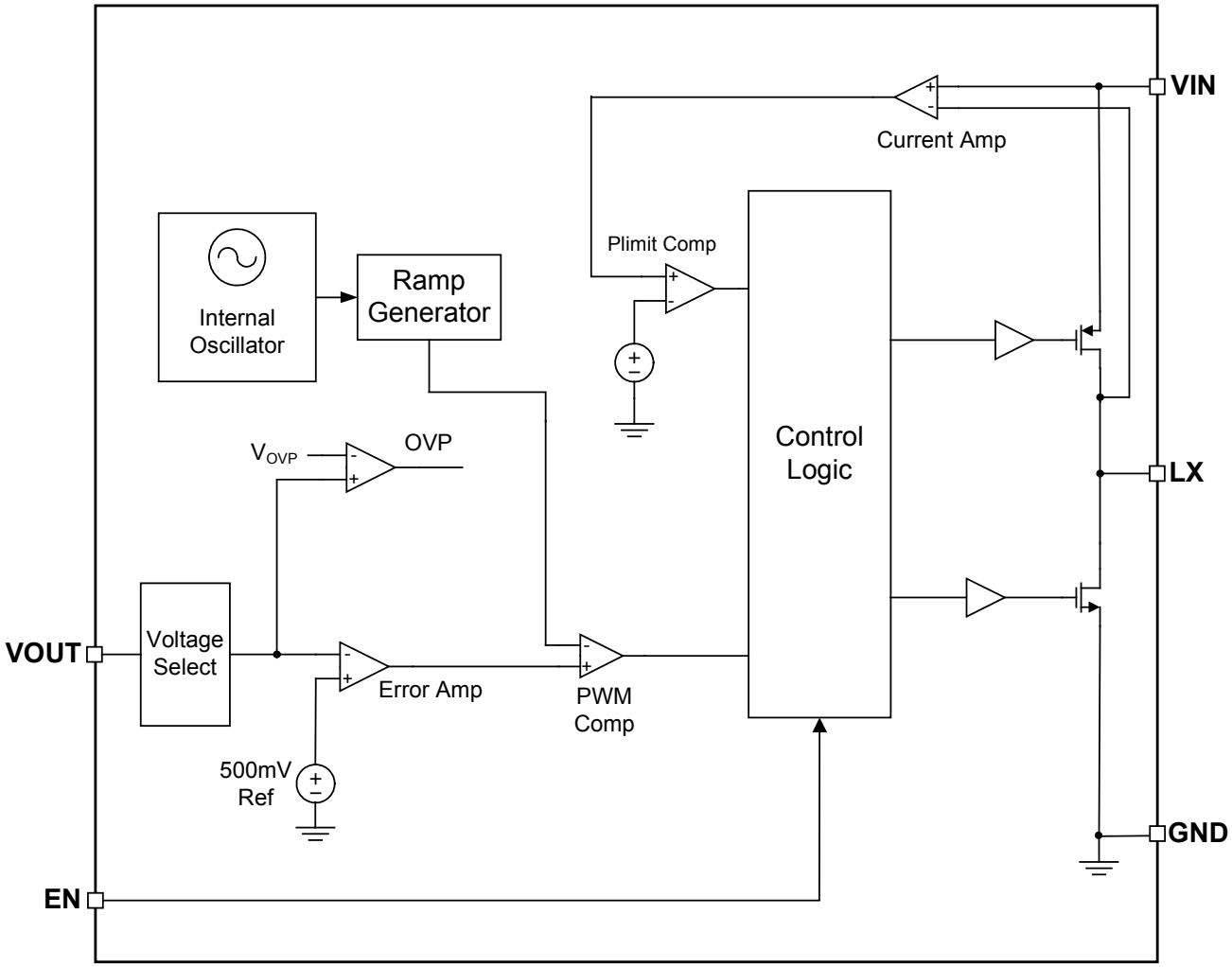
Transient Response (V_{OUT}=1.0V)



Pin Descriptions

Pin #	Pin Name	Pin Function
1	VIN	Input power supplies. Powers the internal circuitry and is connected to the source of high-side P channel MOSFET.
2	GND	Ground connection.
3	EN	Enable pin. When connected to logic high or tied to VIN pin, the SC4626 is on. When connected to logic low, the device enters shutdown and consumes less than 1µA of current. The enable pin has a 1 MΩ internal pulldown resistor. This resistor is switched in circuit whenever the EN pin is below the enable input high threshold, or when the part is in undervoltage lockout.
4	VOUT	Output voltage sense pin.
5	LX	Switching node - connect an inductor between this pin and the output capacitor.

Block Diagram



Applications Information

Detailed Description

The SC4626 is a synchronous step-down pulse width modulated (PWM) voltage mode DC-DC regulator operating at 2.5MHz fixed-frequency. The switching frequency is chosen to minimize the size of the external inductor and capacitors while maintaining high efficiency.

Operation

During normal operation, the internal high-side PMOS device is activated on each rising edge of the internal oscillator. The voltage feedback loop uses an internal feedback resistor divider. The period is set by the on board oscillator when in PWM mode at average to high loads. The device has an internal low-side synchronous NMOS device and does not require a Schottky diode on the LX pin. The device operates as a buck converter in PWM mode with a fixed frequency of 2.5MHz.

Output Voltage Selection

The SC4626 is designed for fixed output voltage. There are some options for preset output voltage shown in Table 1. If the voltage desired is not shown in the Table 1, it can be programmed via an external resistor divider. There will be typical 1uA current flowing into the VOUT pin. The typical schematic of adjustable output voltage option from the part with standard 1.0V, the SC4626A, is shown in Figure 1. The C_{FF} is needed for maintain the performance of the transient response. The proper value of C_{FF} can be calculated by the equation

$$C_{FF}[nF] = 10 \times \frac{(V_{OUT} - 0.5)^2}{R_{FB1}[k\Omega] \cdot (V_{OUT} - V_{OSTD})} \times \left(\frac{V_{OSTD}}{V_{OSTD} - 0.5}\right)$$

,where the V_{OSTD} is the standard voltage shown in Table 1. To simplify the design, it is recommended to program the desired output voltage from standard 1.0V as shown in Figure 1 with a proper C_{FF} calculated from the equation shown above. For programming the output voltage from other standard voltage, the R_{FB1}, R_{FB2} and C_{FF} need to be adjusted to meet the equation shown above.

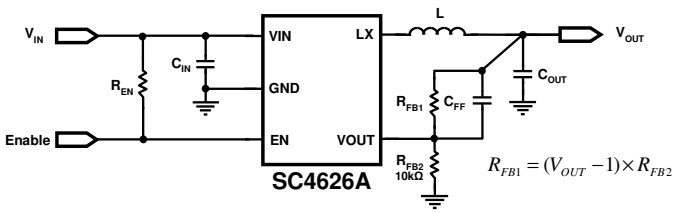


Figure 1 — Typical schematic for adjustable output voltage option from standard 1.0V of SC4626A

Protection Features

The SC4626 provides the following protection features:

- Thermal Shutdown
- Current Limit
- Over-Voltage Protection
- Soft-Start Operation

Thermal Shutdown

The device has a thermal shutdown feature to protect the SC4626 if the junction temperature exceeds 160°C. During thermal shutdown, the on-chip power devices are disabled with the LX output floating. When the die temperature drops by 10°C, the part will initiate a soft start recovery to normal operation.

Current Limit

The internal PMOS power device in the switching stage is protected by current limit feature. If the output is loaded above the PMOS current limit for 32 consecutive cycles, the SC4626 enters foldback current limit mode and the output current is limited to the current limit holding current (I_{CL_HOLD}) of a few hundred milliampere. Under these conditions the output voltage will be the product of I_{CL_HOLD} and the load resistance. The current limit holding current (I_{CL_HOLD}) will be decreased when output voltage is increased. The load presented must fall below the current limit holding current for the SC4626 to exit foldback current limit mode. Figure 2 shows the typical current limit holding current decreasing rate over different output voltage. The SC4626 is capable of sustaining a indefinite short circuit without damage and will resume normal operation when the fault is removed. The foldback current limit mode will be disabled during the soft-start.

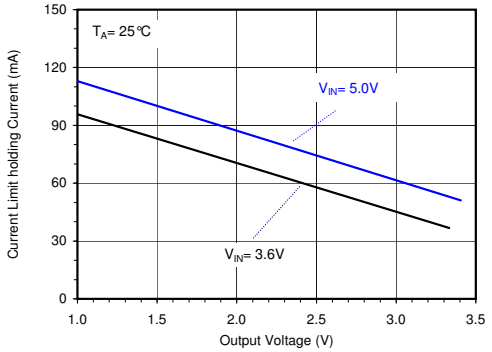


Figure 2 — Current limit holding current decreasing rate vs. output voltage

Applications Information (continued)

Over-Voltage Protection

In the event of a 15% over-voltage on the output, the PWM drive is disabled with LX pin floating.

Soft-Start

The soft-start mode is activated after VIN reaches its UVLO and EN signal is set high to enable the part. An over temperature shutdown event will also activate the soft start sequence. Soft-start mode controls the maximum current during startup thus limiting in-rush current. The PMOS current limit is stepped through four soft start levels of approximately 20%, 25%, 40%, & 100%. Each step is maintained for 20µs following internal reference start up of 20µs giving the total nominal startup period of 100µs. During startup, the chip operates in controlling the inductor current swings between 0A and current limit. If V_{OUT} reaches 90% of the target within the first 2 current levels, the chip continues in hysteretic mode till the end of the soft-start time period before switching to PWM mode. If V_{OUT} does not reach 90% by the end of the second current limit level, soft start will continue to level 3 or level 4 till the output voltage reaches 96% and will then transition into PWM mode. After the full soft start time period, the SC4626 will switch into PWM mode operation regardless of the V_{OUT} level.

The SC4626 is capable of starting up into a pre-biased output. When the output is precharged by another supply rail, the SC4626 will not discharge the output during the soft start interval.

Shut Down

When the EN pin voltage goes low, the SC4626 will run in shutdown mode, drawing less than 1µA from the input power supply. The internal switches and bandgap voltage will be immediately turned off.

Inductor Selection

The SC4626 converter has internal loop compensation. The compensation is designed to work with a output filter corner frequency is less than 100kHz over any operating condition, tolerance and bias effect. The corner frequency of output filter can be defined by the equation

$$f_C = \frac{1}{2\pi\sqrt{L \cdot C_{OUT}}}$$

Values outside this range may lead to instability, malfunction, or out-of-specification performance.

When choosing an inductor, it is important to consider the change in inductance with DC bias current. The inductor saturation current is specified as the current at which the inductance drops a specific percentage from the nominal value. This is approximately 30%. Except for short-circuit or other fault conditions, the peak current must always be less than the saturation current specified by the manufacturer. The peak current is the maximum load current plus one half of the inductor ripple current at the maximum input voltage. Load and/or line transients can cause the peak current to exceed his level for short durations. Maintaining the peak current below the inductor saturation specification keeps the inductor ripple current and the output voltage ripple at acceptable levels. Manufacturers often provide graphs of actual inductance and saturation characteristics versus applied inductor current. The saturation characteristics of the inductor can vary significantly with core temperature. Core and ambient temperatures should be considered when examining the core saturation characteristics.

When the inductance has been determined, the DC resistance (DCR) must be examined. The efficiency that can be achieved is dependent on the DCR of the inductor. The lower values give higher efficiency. The RMS DC current rating of the inductor is associated with losses in the copper windings and the resulting temperature rise of the inductor. This is usually specified as the current which produces a 40˚C temperature rise. Most copper windings are rated to accommodate this temperature rise above maximum ambient.

Magnetic fields associated with the output inductor can interfere with nearby circuitry. This can be minimized by the use of low noise shielded inductors which use the minimum gap possible to limit the distance that magnetic fields can radiate from the inductor. However shielded inductors typically have a higher DCR and are thus less efficient than a similar sized non-shielded inductor.

Applications Information (continued)

Vout Code (Vout)		A(1.0V),C(1.2V),E(1.28V),F(1.3V),H(1.5V)				
Inductor			Output Capacitor			
Description	Vender	Part Number	Description	Vender	Part Number	Qty.
2.2uH, 60mΩ(max) Wire Wound 2.8x3.0x1.5(mm)	TOKO	1071AS-2R2M	10uF,6.3V X5R,0805	Murata	GRM21BR60J106K	1
1.0uH, 40mΩ(max) Wire Wound 2.8x3.0x1.5(mm)	TOKO	1071AS-1R0N	22uF,6.3V X5R,0805	Murata	GRM21BR60J226M	1
2.2uH, 120mΩ(max) Wire Wound 2.5x2.0x1.2(mm)	TOKO	1222AS-H-2R2M	10uF,6.3V X5R,0805	Murata	GRM21BR60J106K	1
1.0uH, 80mΩ(max) Multilayer Chip 2.5x2.0x1.0(mm)	TOKO	MDT2520-CR1R0M	22uF,6.3V X5R,0805	Murata	GRM21BR60J226M	1
			10uF,6.3V X5R,0805	Murata	GRM219R60J106K	1
1.0uH, 69mΩ(max) Multilayer Chip 2.5x2.0x1.0(mm)	Murata	LQM2HPN1R0MG0	22uF,6.3V X5R,0805	Murata	GRM21BR60J226M	1
			10uF,4.0V X5R,0603	Murata	GRM188R60G106M	2

Table 2a – Recommended L and output capacitors for Vout=1.0V to 1.5V

Vout Code (Vout)		L(1.8V),Y(2.5V),Z(3.3V)				
Inductor			Output Capacitor			
Description	Vender	Part Number	Description	Vender	Part Number	Qty.
2.2uH, 60mΩ(max) Wire Wound 2.8x3.0x1.5(mm)	TOKO	1071AS-2R2M	10uF,6.3V X5R,0805	Murata	GRM21BR60J106K	1
1.0uH, 40mΩ(max) Wire Wound 2.8x3.0x1.5(mm)	TOKO	1071AS-1R0N	22uF,6.3V X5R,0805	Murata	GRM21BR60J226M	1
2.2uH, 120mΩ(max) Wire Wound 2.5x2.0x1.2(mm)	TOKO	1222AS-H-2R2M	10uF,6.3V X5R,0805	Murata	GRM21BR60J106K	1
1.0uH, 80mΩ(max) Multilayer Chip 2.5x2.0x1.0(mm)	TOKO	MDT2520-CR1R0M	22uF,6.3V X5R,0805	Murata	GRM21BR60J226M	1
			10uF,4.0V X5R,0603	Murata	GRM188R60G106M	2

Table 2b – Recommended L and output capacitors for Vout=1.8V to 3.3V

Applications Information (continued)

The SC4626 is compatible with small shielded chip inductors for low cost, low profile applications. The inductance roll off characteristic of chip inductor is worse resulting in high ripple current and increased output voltage ripple at heavy load operation. SC4626 has OCP peak inductor current threshold of 1.5A minimum, to support 1A DC load current, the inductor ripple current at 1A DC load current needs to be less than 1A.

Final inductor selection depends on various design considerations such as efficiency, EMI, size, and cost. Table 2a and 2b list the manufacturers of recommended inductor and output capacitors options. Chip inductors provide smaller footprint and height with lower efficiency and increased output voltage ripple. Transient load performance is equivalent to wire wound inductors. Figure 3 shows the typical efficiency curves for different inductors.

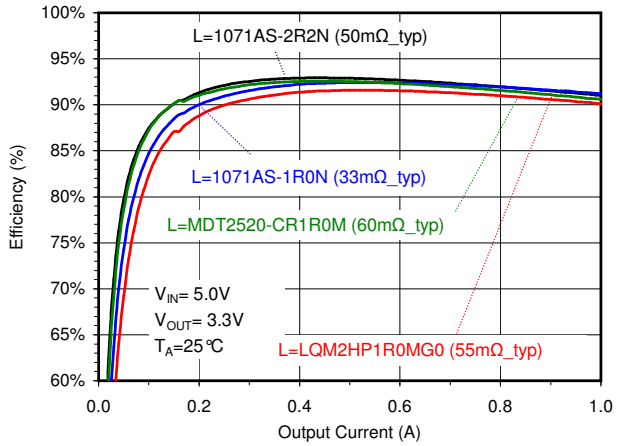


Figure 3 — Typical efficiency curves (V_{IN}=5.0V, V_{OUT}=3.3V)

C_{OUT} Selection

The internal voltage loop compensation in the SC4626 limits the minimum output capacitor value to 10µF if using the inductor of 2.2µH. This is due to its influence on the the loop crossover frequency, phase margin, and gain margin. Increasing the output capacitor above this minimum value will reduce the crossover frequency and provide greater phase margin. A total output capacintance should not exceed 30uF to avoid any start-up problems. For most typical applications, it is recommended to use output capacitance of 10uF to 22uF. When choosing output capacitor's capacitance, verify the voltage derating effect from the capacitor vendors data sheet.

Capacitors with X7R or X5R ceramic dielectric are recommended for their low ESR and superior temperature and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them unsuitable for this application.

The output voltage droop due to a load transient is determined by the capacitance of the ceramic output capacitor. The ceramic capacitor supplies the load current initially until the loop responds. Within a few switching cycles the loop will respond and the inductor current will increase to match the required load. The output voltage droop during the period prior to the loop responding can be related to the choice of output capacitor by the relationship

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot f_{OSC}}$$

The output capacitor RMS current ripple may be calculated from the equation

$$I_{COUT(RMS)} = \frac{1}{2\sqrt{3}} \left(\frac{V_{OUT} \cdot \left(V_{IN(MAX)} - V_{OUT}\right)}{L \cdot f_{OSC} \cdot V_{IN}} \right)$$

Table 3 lists the manufacturers of recommended output capacitor options.

C_{IN} Selection

The SC4626 source input current is a DC supply current with a triangular ripple imposed on it. To prevent large input voltage ripple, a low ESR ceramic capacitor is required. A minimum value of 4.7µF should be used. It is important to consider the DC voltage coefficient characteristics when determining the actual required value. To estimate the required input capacitor, determine the acceptable input ripple voltage and calculate the minimum value required for C_{IN} from the equation

$$C_{IN} = \frac{\frac{V_{OUT}}{V_{IN}} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{\left(\frac{\Delta V}{I_{OUT}} - ESR\right) \cdot f_{OSC}}$$

The input capacitor RMS ripple current varies with the

Applications Information (continued)

input and output voltage. The maximum input capacitor RMS current is found from the equation

$$I_{CIN(RMS)} = \sqrt{\frac{V_{OUT}}{V_{IN}}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}$$

The input voltage ripple and RMS current ripple are at maximum when the input voltage is twice the output voltage or 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the PMOS switch. Low ESR/ESL X5R ceramic capacitors are recommended for this function. To minimise stray inductance ,the capacitor should be placed as closely as possible to the VIN and GND pins of the SC4626.

Manufacturer Part Nunber	Value (µF)	Type	Rated Voltage (VDC)	Value at 3.3V (µF)	Dimensions LxWxH (mm)
Murata GRM21BR61A106K	10±10%	X5R	10	4.42	2.0x1.25x1.25 (EIA:0805)
Murata GRM21BR71A106K	10±10%	X7R	10	4.88	2.0x1.25x1.25 (EIA:0805)
Murata GRM21BR60J106K	10±10%	X5R	6.3	4.05	2.0x1.25x1.25 (EIA:0805)
Murata GRM21BR70J106K	10±10%	X7R	6.3	4.91	2.0x1.25x1.25 (EIA:0805)
Murata GRM21BR60J226M	22±20%	X5R	6.3	6.57	2.0x1.25x1.25 (EIA:0805)

Table 3 – Recommended Capacitors

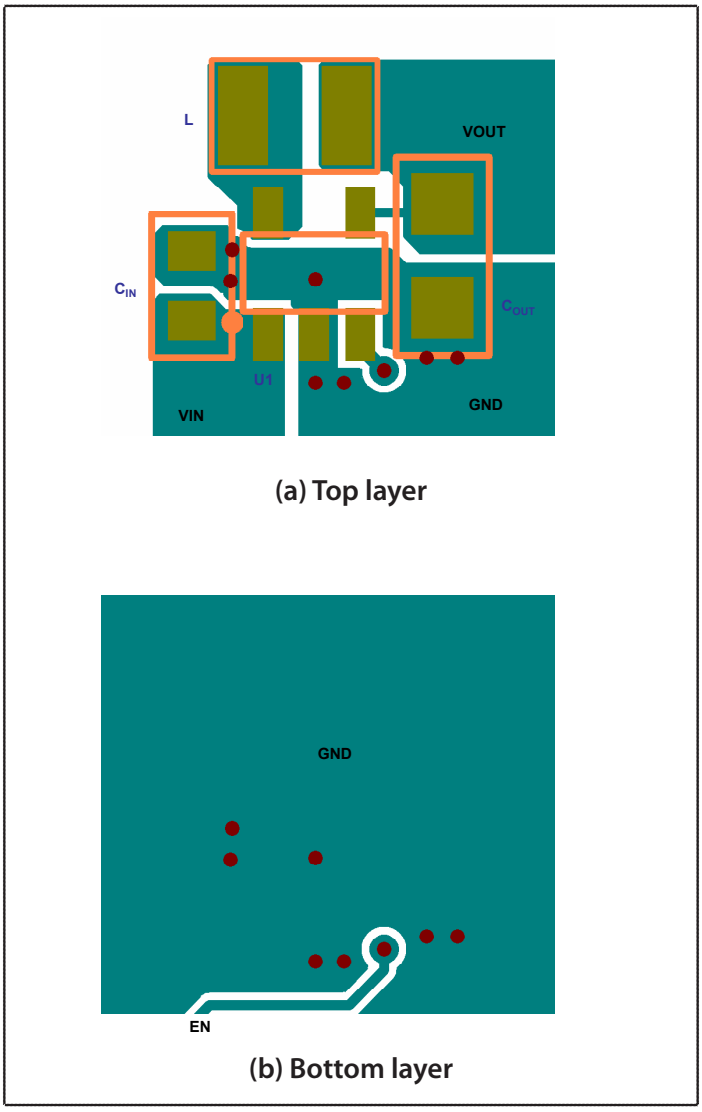
Applications Information (continued)

PCB Layout Considerations

The layout diagram in Figure 4 shows a recommended PCB top-layer and bottom layer for the SC4626 and supporting components. Fundamental layout rules must be followed since the layout is critical for achieving the performance specified in the Electrical Characteristics table. Poor layout can degrade the performance of the DC-DC converter and can contribute to EMI problems, ground bounce, and resistive voltage losses. Poor regulation and instability can result.

The following guidelines are recommended when developing a PCB layout:

1. The input capacitor, C_{IN} should be placed as close to the VIN and GND pins as possible. This capacitor provides a low impedance loop for the pulsed currents present at the buck converter's input. Use short wide traces to connect as closely to the IC as possible. This will minimize EMI and input voltage ripple by localizing the high frequency current pulses.
2. Keep the LX pin traces as short as possible to minimize pickup of high frequency switching edges to other parts of the circuit. C_{OUT} and L should be connected as close as possible between the LX and GND pins, with a direct return to the GND pin from C_{OUT}.
3. Route the output voltage feedback/sense path away from inductor and LX node to minimize noise and magnetic interference.
4. Use a ground plane referenced to the SC4626 GND pin. Use several vias to connect to the component side ground to further reduce noise and interference on sensitive circuit nodes.
5. If possible, minimize the resistance from the VOUT and GND pins to the load. This will reduce the voltage drop on the ground plane and improve the load regulation. And it will also improve the overall efficiency by reducing the copper losses on the output and ground planes.

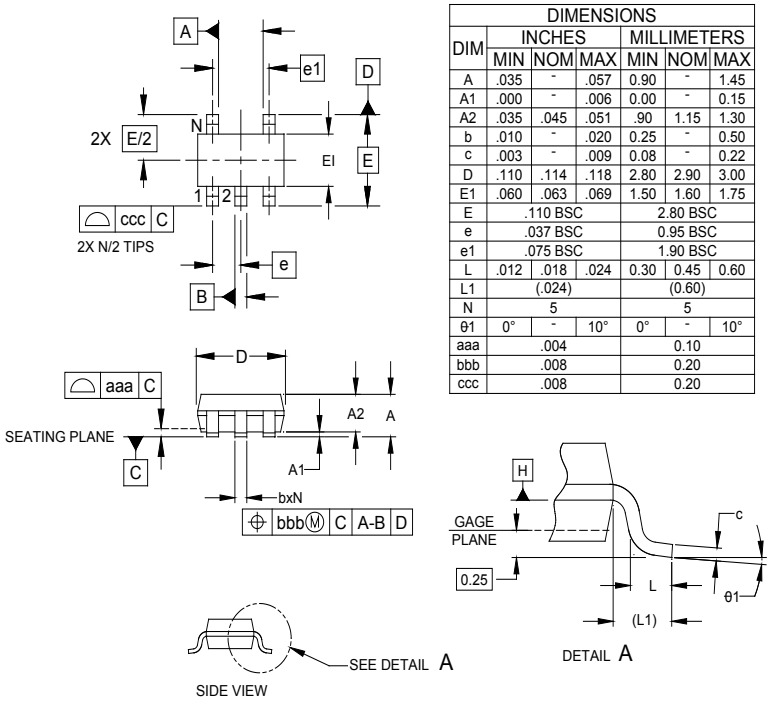


(a) Top layer

(b) Bottom layer

Figure 4 — Recommended PCB Top & Bottom Layer Layout

Outline Drawing – SOT23-5

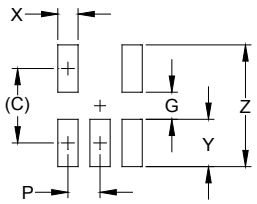


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.035	-	.057	0.90	-	1.45
A1	.000	-	.006	0.00	-	0.15
A2	.035	.045	.051	.90	1.15	1.30
b	.010	-	.020	0.25	-	0.50
c	.003	-	.009	0.08	-	0.22
D	.110	.114	.118	2.80	2.90	3.00
E1	.060	.063	.069	1.50	1.60	1.75
E	.110 BSC			2.80 BSC		
e	.037 BSC			0.95 BSC		
e1	.075 BSC			1.90 BSC		
L	.012	.018	.024	0.30	0.45	0.60
L1	(.024)			(0.60)		
N	5			5		
θ1	0°	-	10°	0°	-	10°
aaa	.004			0.10		
bbb	.008			0.20		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

Land Pattern – SOT23-5



DIM	INCHES	MILLIMETERS
C	(.098)	(2.50)
G	.055	1.40
P	.037	0.95
X	.024	0.60
Y	.043	1.10
Z	.141	3.60

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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