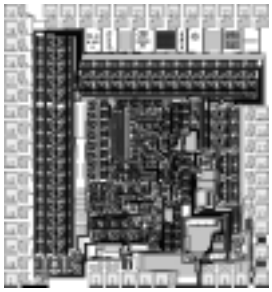
RAM MAPPING 32x4 LCD CONTROLLER FOR I/O μC

DESCRIPTION

The SC16232 is a 128 pattern(32x4), memory mapping, and multi-function LCD driver. The S/W configuration feature of the SC16232 makes it suitable for multiple LCD applications including LCD modules and display subsystems. Only three or four lines are required for the interface between the host controller and the SC16232. The SC16232 contains a power down command to reduce power consumption.



Chip Topography

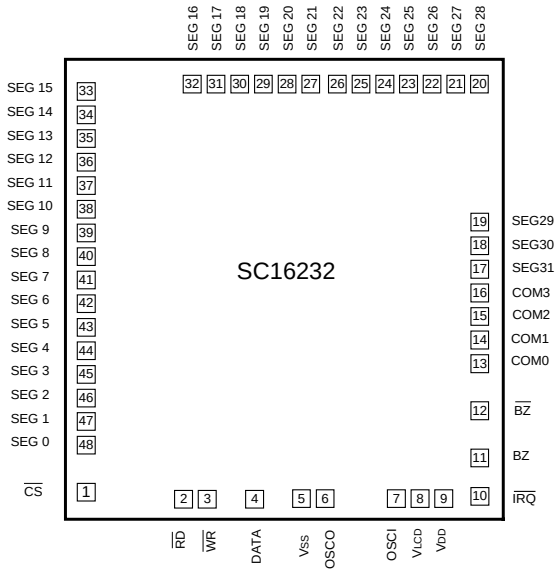
FEATURES

* Operating voltage: 2.4V ~ 5.2V
* Built-in 256kHz RC oscillator
* External 32.768kHz crystal or 256kHz frequency source input
* Selection of 1/2 or 1/3 bias, and selection of 1/2 or 1/3 or 1/4 duty LCD applications
* Internal time base frequency sources
* Two selectable buzzer frequencies(2kHz/4kHz)
* Power down command reduces power consumption
* Built-in time base generator and WDT
* Time base or WDT overflow output
* 8 kinds of time base/WDT clock sources
* 32x4 LCD driver
* Built-in 32x4 bit display RAM
* 3-wire serial interface
* Internal LCD driving frequency source
* Software configuration feature
* Data mode and command mode instructions
* R/W address auto increment
* Three data accessing modes
* VLCD pin for adjusting LCD operating voltage

ORDERING INFORMATION

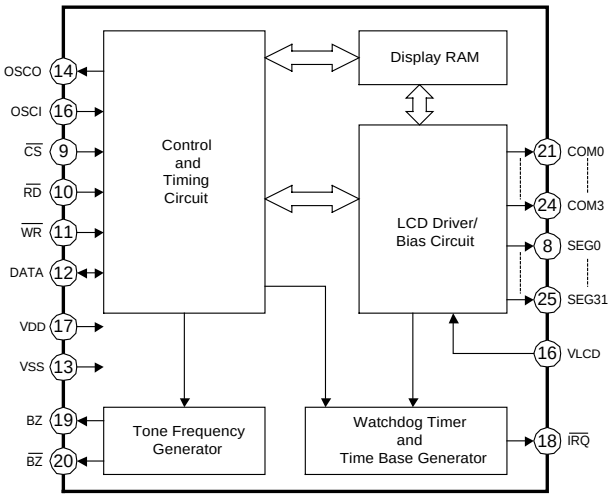
Device	Package
SC16232	COB

PAD ASSIGNMENT



Note: The IC substrate should be connected to V_{DD} in the PCB layout artwork.

BLOCK DIAGRAM



Notes: CS : Chip selection ; BZ, BZ : Tone outputs ; WR , RD , DATA: Serial interface
COM0 ~ COM3; SEG) ~ SEG31: LCD outputs ; IRQ : Time base or WDT overflow output

ABSOLUTE MAXIMUM RATING

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 ~ 5.5	V
Input Voltage	V_{IN}	Vss-0.3 ~ V_{DD}+0.3	V
Storage temperature	T_{STG}	-50 ~ +125	°C
Operating Temperature	T_{OPR}	-25 ~ + 75	°C

D.C. ELECTRICAL CHARACTERISTICS (Tamb=25°C, Unless otherwise specified)

Parameter	Symbol	Test conditions		Min	Typ	Max	Unit
		V_{DD}	Conditions				
Operating Voltage	V_{DD}	--	--	2.4	--	5.2	V
Operating Current	I_{DD1}	3V	No load/LCD ON	--	150	300	μA
		5V	On-chip RC oscillator	--	300	600	μA
	I_{DD2}	3V	No load/LCD ON	--	60	120	μA
		5V	Crystal oscillator	--	120	240	μA
	I_{DD3}	3V	No load/LCD ON	--	100	200	μA
		5V	External clock source	--	200	400	μA
Standby Current	I_{STB}	3V	No load	--	0.1	5	μA
		5V	Power down mode	--	0.3	10	μA
Input Low Voltage	V_{IL}	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	0	--	0.6	V
		5V		0	--	1.0	V
Input High Voltage	V_{IH}	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	2.4	--	3.0	V
		5V		4.0	--	5.0	V
DATA, BZ, $\overline{BZ}$, $\overline{IRQ}$	I_{OL1}	3V	V_{OL}=0.3V	0.5	1.2	--	mA
		5V	V_{OL}=0.5V	1.3	2.6	--	mA
DATA, BZ, $\overline{BZ}$	I_{OH1}	3V	V_{OH}=2.7V	-0.4	-0.8	--	mA
		5V	V_{OH}=4.5V	-0.9	-1.8	--	mA
LCD Common Sink Current	I_{OL2}	3V	V_{OL}=0.3V	80	150	--	μA
		5V	V_{OL}=0.5V	150	250	--	μA
LCD Common Source Current	I_{OH2}	3V	V_{OH}=2.7V	-80	-120	--	μA
		5V	V_{OH}=4.5V	-120	-200	--	μA
LCD Segment Sink Current	I_{OL3}	3V	V_{OL}=0.3V	60	120	--	μA
		5V	V_{OL}=0.5V	120	200	--	μA
LCD Segment Source Current	I_{OH3}	3V	V_{OH}=2.7V	-40	-70	--	μA
		5V	V_{OH}=4.5V	-70	-100	--	μA
Pull-high Resistor	R_{PH}	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	40	80	150	kΩ
		5V		30	60	100	kΩ

A.C. ELECTRICAL CHARACTERISTICS(Tamb=25°C, Unless otherwise specified)

Parameter	Symbol	Test conditions		Min	Typ	Max	Unit
		V_{DD}	Conditions				
System Clock	f_{SYS1}	3V	On-chip RC oscillator	--	256	--	kHz
		5V		--	256	--	kHz
System Clock	f_{SYS2}	3V	Crystal oscillator	--	32.768	--	kHz
		5V		--	32.768	--	kHz
System Clock	f_{SYS3}	3V	External clock source	--	256	--	kHz
		5V		--	256	--	kHz
LCD Clock	f_{LCD}	--	On-chip RC oscillator	--	f_{SYS1}/1024	--	Hz
		--	Crystal oscillator	--	f_{SYS2}/128	--	Hz
		--	External clock source	--	f_{SYS3}/1024	--	Hz
LCD Common Period	t_{COM}	--	n: Number of COM	--	n/f_{LCD}	--	S
Serial Data Clock ($\overline{WR}$ pin)	f_{CLK1}	3V	Duty cycle 50%	--	--	150	kHz
		5V		--	--	300	kHz
Serial Data Clock ($\overline{RD}$ pin)	f_{CLK2}	3V	Duty cycle 50%	--	--	75	kHz
		5V		--	--	150	kHz
Tone Frequency	f_{TONE}	--	On-chip RC oscillator	--	2.0 or 4.0	--	kHz
Serial Interface Reset Pulse Width (Figure 3)	t_{CS}	--	$\overline{CS}$	--	250	--	nS
$\overline{WR}$, $\overline{RD}$ Input Pulse Width (Figure 1)	t_{CLK}	3V	Write mode	3.34	--	--	μS
			Read mode	6.67	--	--	
		5V	Write mode	1.67	--	--	μS
			Read mode	3.34	--	--	
Rise/Fall Time Serial Data Clock Width (Figure 1)	t_R,t_F	3V	--	--	120	--	nS
		5V					
Setup Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	t_{su}	3V	--	--	120	--	nS
		5V					
Hold Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	t_h	3V	--	--	120	--	nS
		5V					
Setup Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	t_{su1}	3V	--	--	100	--	nS
		5V					
Hold Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	t_{h1}	3V	--	--	100	--	nS
		5V					

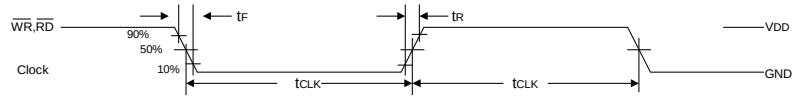


Figure 1

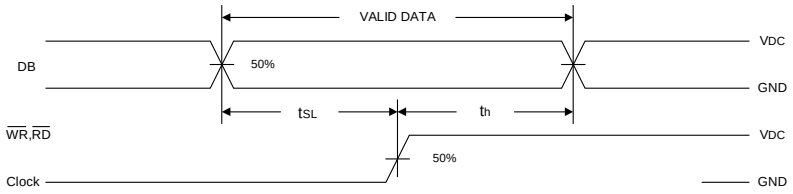


Figure 2

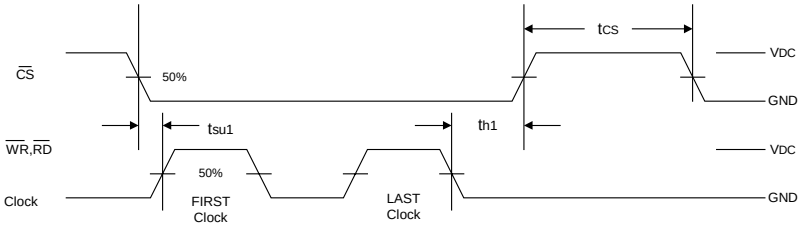


Figure 3

PAD DESCRIPTION

Pad No.	Symbol	I/O	Description
1	$\overline{CS}$	I	Chip selection input with pull-high resistor. When the $\overline{CS}$ is logic high, the data and command read from or written to the SC16232 are disabled. The serial interface circuit is also reset. But if $\overline{CS}$ is at logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the SC16232 are all enabled.
2	$\overline{RD}$	I	READ clock input with pull-high resistor. Data in the RAM of the SC16232 are clocked out on the falling edge of the $\overline{RD}$ signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data.

(to be continued)

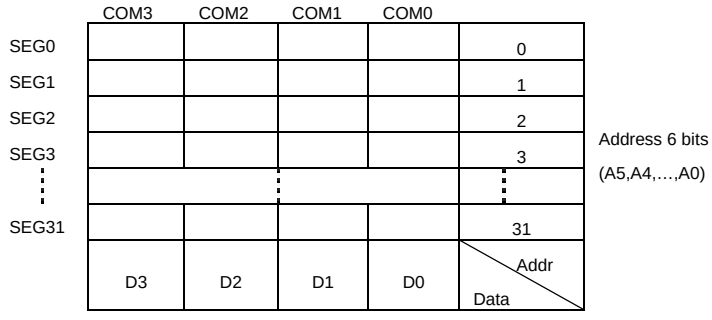
PAD DESCRIPTION (continued)

Pad No.	Symbol	I/O	Description
3	$\overline{WR}$	I	WRITE clock input with pull-high resistor. Data on the DATA line are latched into the SC16232 on the rising edge of the $\overline{WR}$ signal.
4	DATA	I/O	Serial data input/output with pull-high resistor.
5	V_{SS}	--	Negative power supply, GND.
7	OSCI	I	The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected instead, the OSCI and OSCO pads can be left open,
6	OSCO	O	
8	V_{LCD}	I	LCD power supply.
9	V_{DD}	--	Positive power supply.
10	$\overline{IRQ}$	O	Time base or WDT overflow flag, NMOS open drain output.
11,12	BZ, $\overline{BZ}$	O	2kHz or 4kHz tone frequency output pair.
13 ~16	COM0 ~ COM3	O	LCD common outputs.
48 ~17	SEG0 ~ SEG31	O	LCD segment outputs.

FUNCTIONAL DESCRIPTION

1. DISPLAY MEMORY – RAM

The static display memory(RAM) is organized into 32x4 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD pattern:



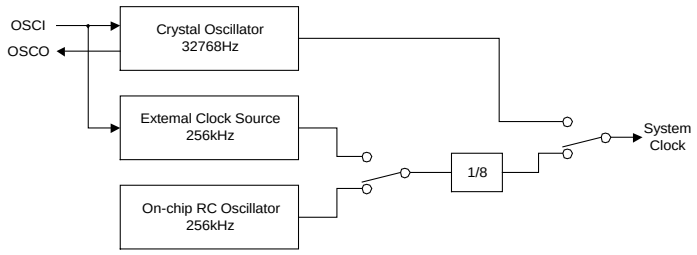
Data 4 bits (D3,D2,D1,D0)

RAM mapping

2. SYSTEM OSCILLATOR

The SC16232 system clock is used to generate the time base/watchdog timer(WDT) clock frequency, LCD driving clock, and tone frequency. The source of the clock may be from an on-chip RC oscillator(256 kHz), a crystal oscillator(32.768 kHz), or an external 256kHz clock by the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is, however, available only for the on-chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the time base/WDT lose its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The crystal oscillator option can be applied to connect an external frequency source of 32kHz to the OSCI pin. In this case, the system fails to enter the power down mode, similar to the case in the external 256kHz clock source operation. At the initial system power on, The SC16232 is at the SYS DIS state.



System oscillator configuration

3. TIME BASE AND WATCHDOG TIMER (WDT)

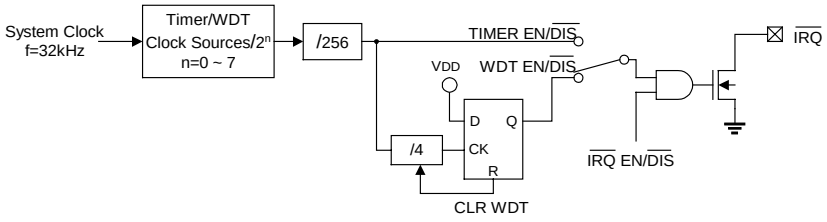
The time base generator is comprised by an 8-stage count-up ripple counter and is designed to generate an accurate time base. The watch dog timer (WDT), on the other hand, is composed of an 8-stage time base generator along with a 2-stage count-up counter, and is designed to break the host controller or other subsystems from abnormal states such as unknown or unwanted jump, execution errors, etc. The WDT time-out will result in the setting of an internal WDT time-out flag. The outputs of the time base generator and of the WDT time-out flag can be connected to the $\overline{IRQ}$ output by a command option. There are totally eight frequency sources available for the time base generator and the WDT clock. The frequency is calculated by the following equation.

$$f_{WDT}=\frac{32kHz}{2^n}$$

Where the value of n ranges from 0 to 7 by command options. The 32kHz in the above equation indicates that the source of the system frequency is derived from a crystal oscillator of 32.768kHz, an on-chip oscillator(256kHz), or an external frequency of 256kHz.

If an on-chip oscillator(256kHz) or an external 256kHz frequency is chosen as the source of the system frequency, the frequency source is by default prescaled to 32kHz by a 3-stage prescaler. Employing both the time base generator and the WDT related commands, one should be careful since the time base generator and WDT share the same 8-stage counter. For example, invoking the WDT DIS command disables the time base generator whereas executing the WDT EN command not only enables the time base generator but activates the WDT time-out flag output (connect the WDT time-out flag to the $\overline{IRQ}$ pin). After the TIMER EN command is transferred, the WDT is disconnected from the $\overline{IRQ}$ pin, and the output of the time base generator is connected to the $\overline{IRQ}$ pin. The WDT can be cleared by executing the CLR WDT command, and the contents of the time base generator is cleared by executing the CLR WDT or CLR TIMER command. The CLR WDT or the CLR TIMER command should be executed prior to the WDT EN or the TIMER EN command respectively. Before executing the $\overline{IRQ}$ EN command the CLR WDT or CLR TIMER command should be executed first. The CLR TIMER command has to be executed before switching from the WDT mode to the time base mode. Once the WDT time-out occurs, the $\overline{IRQ}$ pin will stay at a logic low level until the CLR WDT or the $\overline{IRQ}$ DIS command is issued. After the $\overline{IRQ}$ output is disable the $\overline{IRQ}$ pin will remain at the floating state. The $\overline{IRQ}$ output can be enabled or disabled by executing the $\overline{IRQ}$ EN or the $\overline{IRQ}$ DIS command, respectively. The $\overline{IRQ}$ EN makes the output of the time base generator or of the WDT time-out flag appear on the $\overline{IRQ}$ pin. The configuration of the time base generator along with the WDT are as shown. In the case of on-chip RC oscillator or crystal oscillator, the power down mode can reduce power consumption since the oscillator can be turned on or off by the corresponding system commands. At the power down mode the time base/WDT loses all its functions.

On the other hand, if an external clock is selected as the source of system frequency the SYS DIS command turns out invalid and the power down mode fails to be carried out. That is, after the external clock source is selected, the SC16232 will continue working until system power fails or the external clock source is removed. After the system power on, the $\overline{IRQ}$ will be disabled.



Timer and WDT configuration

4. TONE OUTPUT

A simple tone generator is implemented in the SC16232. The tone generator can output a pair of differential driving signals on the BZ and $\overline{BZ}$, which are used to generate a single tone. By executing the TONE4K and TONE2K commands there are two tone frequency outputs selectable. The TONE4K and TONE2K commands set the tone frequency to 4kHz and 2kHz, respectively. The tone output can be turned on or off by invoking the TONE ON or the TONE OFF command. The tone outputs, namely BZ and $\overline{BZ}$, are a pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the BZ and the $\overline{BZ}$ outputs will remain at low level.

5. LCD DRIVER

The SC16232 is a 128(32x4) pattern LCD driver. It can be configured as 1/2 or 1/3 bias and 2 or 3 or 4 commons of LCD driver by the S/W configuration. This feature makes the SC16232 suitable for multiply LCD applications. The LCD driving clock is derived from the system clock. The value of the driving clock is always 256Hz even when it is at a 32.768kHz crystal oscillator frequency, an on-chip RC oscillator frequency, or an external frequency. The LCD corresponding commands are summarized in the table below.

Name	Command Code	Function
LCD OFF	**1 0 0** 0 0 0 0 0 0 1 0 X	Turn off LCD outputs
LCD ON	**1 0 0** 0 0 0 0 0 0 1 1 X	Turn on LCD outputs
BIAS & COM	**1 0 0** 0 0 1 0 a b X c X	c=0: 1/2 bias option c=1: 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option

The bold form of 1 0 0, namely **1 0 0**, indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command, will be omitted. The LCD OFF command turns the LCD display off by disabling the LCD bias generator. The LCD ON command, on the other hand, turns the LCD display on by enabling the LCD bias generator. The BIAS and COM are the LCD panel related commands. Using the LCD related commands, the SC16232 can be compatible with most types of LCD panels.

6.COMMAND FORMAT

The SC16232 can be configured by the S/W setting. There are two mode commands to configure the SC16232 resources and to transfer the LCD display data. The configuration mode of the SC16232 is called command mode, and its command mode ID is **1 0 0**. The command mode consists of a system configuration command, a system frequency selection command, a LCD configuration command, a tone frequency selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations. The following are the data mode IDs and the command mode ID:

Operation	Mode	ID
READ	Data	1 1 0
WRITE	Data	1 0 1
READ-MODIFY-WRITE	Data	1 0 1
COMMAND	Command	1 0 0

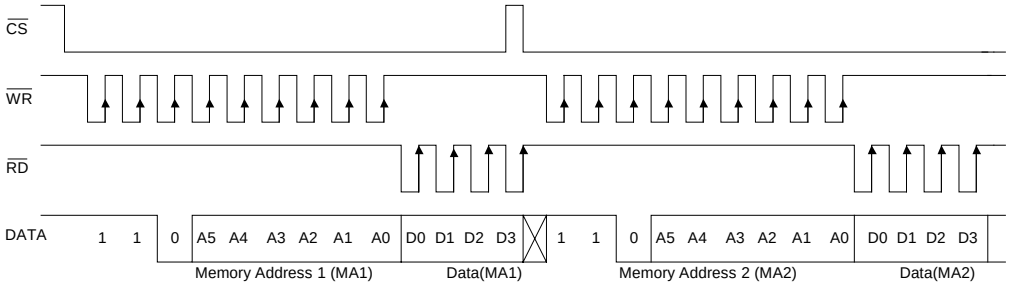
The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID, namely **1 0 0**, can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the $\overline{CS}$ pin should be set to "1" and the previous operation mode will be reset also. Once the $\overline{CS}$ pin returns to "0", a new operation mode ID should be issued first.

7. INTERFACING

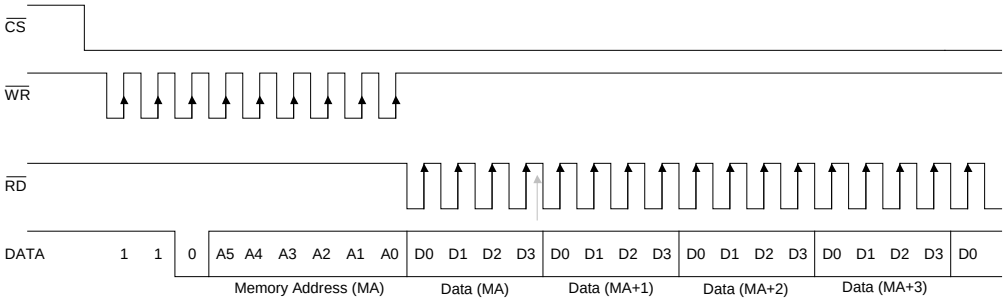
Only four lines are required to interface with the SC16232. The $\overline{CS}$ line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the SC16232. If the $\overline{CS}$ pin is set to 1, the data and command issued between the host controller and the SC16232 are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the SC16232. The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line. The $\overline{RD}$ line is the READ clock input. Data in the RAM are clocked out on the falling edge of the $\overline{RD}$ signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval between the rising edge and the next falling edge of the $\overline{RD}$ signal. The $\overline{WR}$ line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the SC16232 on the rising edge of the $\overline{WR}$ signal. There is an optional $\overline{IRQ}$ line to be used as an interface between the host controller and the SC16232. The $\overline{IRQ}$ pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by being connected with the $\overline{IRQ}$ pin of the SC16232.

TIMING DIAGRAMS

Read mode (command code : 1 1 0)

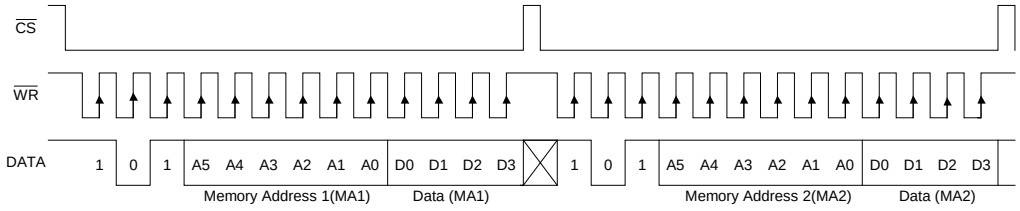


READ mode (successive address reading)

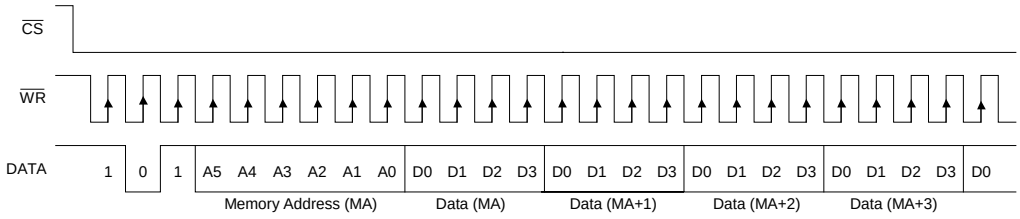


TIMING DIAGRAMS(continued)

WRITE mode (command code : 1 0 1)

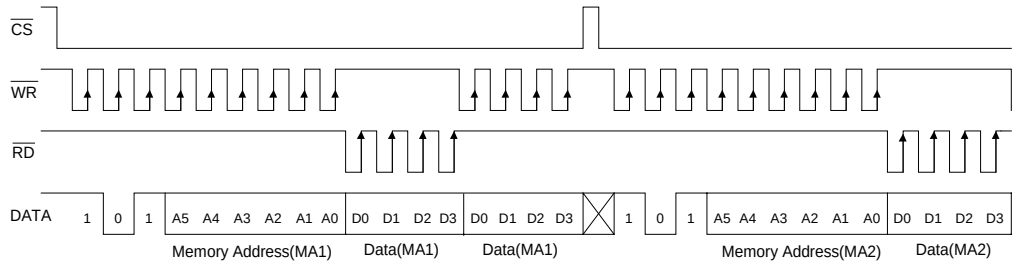


WRITE mode (successive address writing)

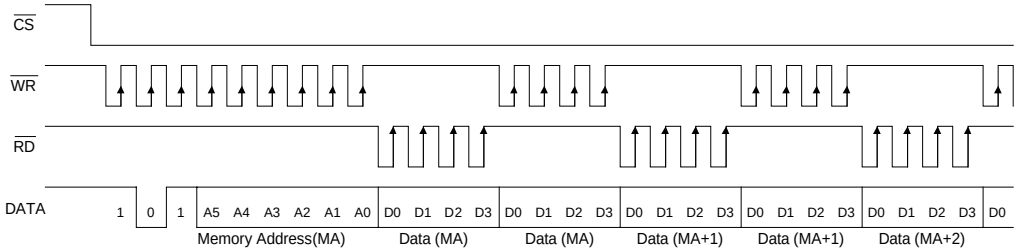


TIMING DIAGRAMS(continued)

READ-MODIFY-WRITE MODE (command code : 1 0 1)

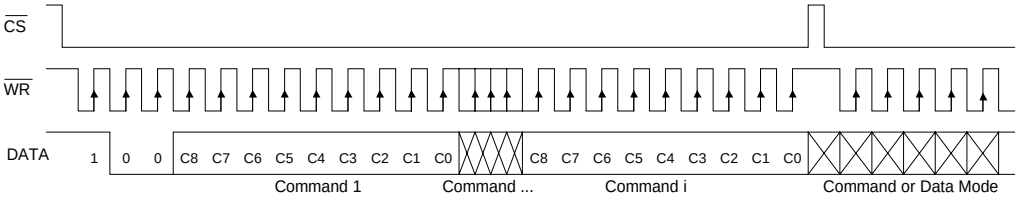


READ-MODIFY-WRITE mode (successive address accessing)

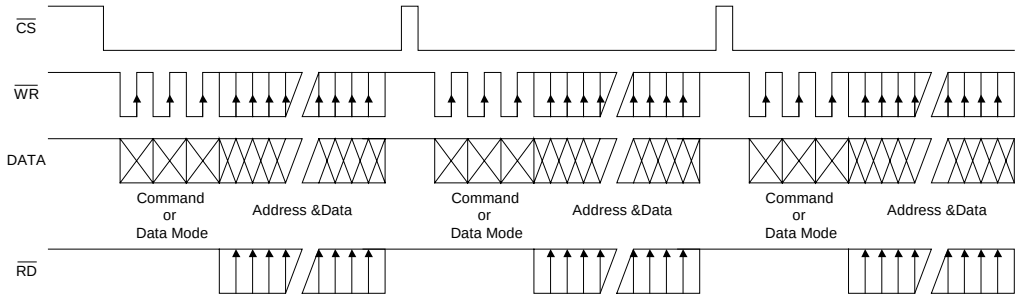


TIMING DIAGRAMS(continued)

Command mode (command code : 1 0 0)

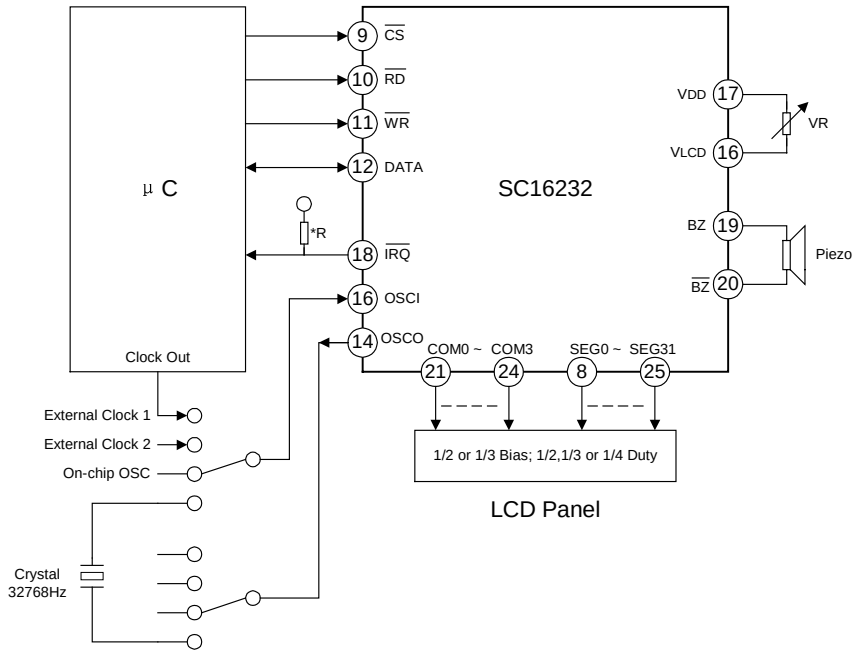


Mode (data and command mode)



Note: It is recommended that the host controller should read in the data from the DATA line between the rising edge of the $\overline{RD}$ line and the falling edge of the next $\overline{RD}$ line.

TYPICAL APPLICATION CIRCUITS



Notes: The connection of $\overline{IRQ}$ and $\overline{RD}$ pin can be selected depending on the requirement of the μC.

The voltage applied to V_{LCD} pin must be lower than V_{DD}.

Adjust V_R to fit LCD display, at V_{DD}=5V,

V_{LCD}=4V,VR=15kΩ±20%, Adjust R(external pull-high resistance) to fit user's time base clock.

COMMAND SUMMARY

Name	ID	Command Code	D/C	Function	Def.
READ	**1 1 0**	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	**1 0 1**	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	**1 0 1**	A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	**1 0 0**	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	**1 0 0**	0000-0001-X	C	Turn on system oscillator	
LCD OFF	**1 0 0**	0000-0010-X	C	Turn off LCD bias generator	Yes
LCD ON	**1 0 0**	0000-0011-X	C	Turn on LCD bias generator	
TIMER DIS	**1 0 0**	0000-0100-X	C	Disable time base output	
WDT DIS	**1 0 0**	0000-0101-X	C	Disable WDT time-out flag output	
TIMER EN	**1 0 0**	0000-0110-X	C	Enable time base output	
WDT EN	**1 0 0**	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	**1 0 0**	0000-1000-X	C	Turn off tone outputs	Yes
TONE ON	**1 0 0**	0000-1001-X	C	Turn on tone outputs	
CLR TIMER	**1 0 0**	0000-11XX-X	C	Clear the contents of time base generator	
CLR WDR	**1 0 0**	0000-111X-X	C	Clear the contents of WDT stage	
XTAL 32K	**1 0 0**	0001-01XX-X	C	System clock source, crystal oscillator	
RC 256K	**1 0 0**	0001-10XX-X	C	System clock source, on-chip RC oscillator	Yes
EXT 256K	**1 0 0**	0001-11XX-X	C	System clock source, external clock source	
BIAS 1/2	**1 0 0**	0010-abX0-X	C	LCD 1/2 bias option ab=00:2 commons option ab=01:3 commons option ab=10:4 commons option	
BIAS 1/3	**1 0 0**	0010-abX1-X	C	LCD 1/3 bias option ab=00:2 commons option ab=01:3 commons option ab=10:4 commons option	
TONE 4K	**1 0 0**	010X-XXXX-X	C	Tone frequency, 4kHz	
TONE 2K	**1 0 0**	011X-XXXX-X	C	Tone frequency, 2kHz	
$\overline{\text{IRQ}}$ DIS	**1 0 0**	100X-0XXX-X	C	Disable $\overline{\text{IRQ}}$ output	Yes

(to be continued)

COMMAND SUMMARY (continued)

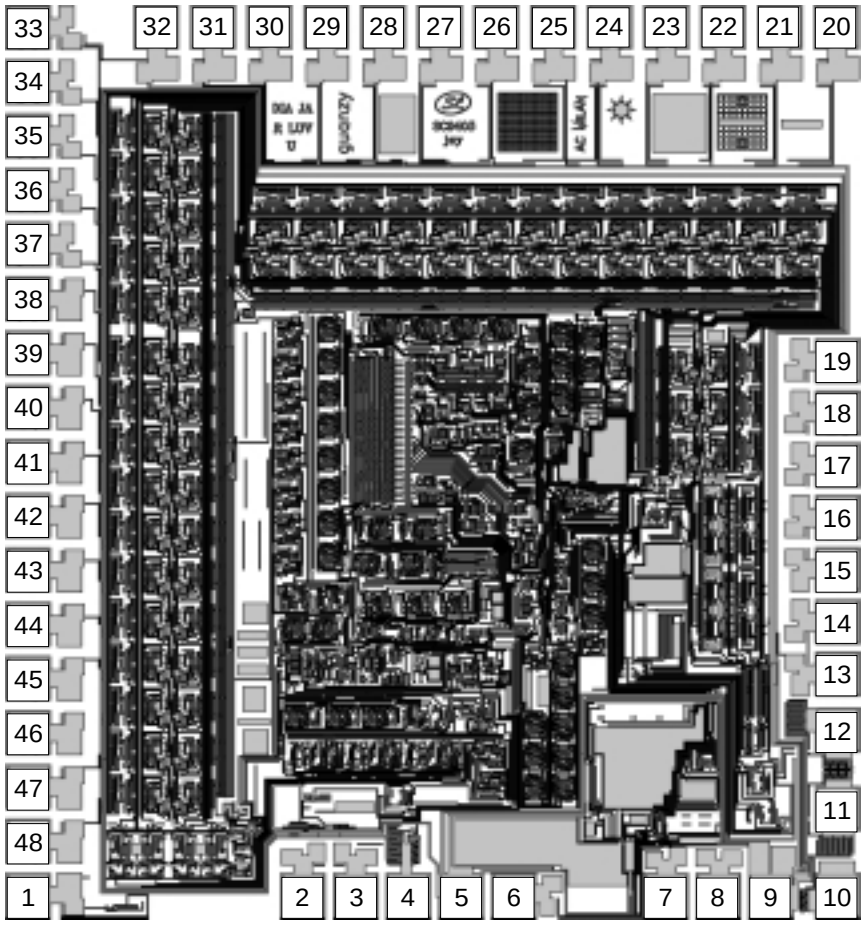
Name	ID	Command Code	D/C	Function	Def.
$\overline{\text{IRQ}}$ EN	**1 0 0**	100X-1XXX-X	C	Enable $\overline{\text{IRQ}}$ output	
F1	**1 0 0**	101X-X000-X	C	Time base/WDT clock Output: 1Hz The WDT time-out flag after: 4s	
F2	**1 0 0**	101X-X001-X	C	Time base/WDT clock Output: 2Hz The WDT time-out flag after: 2s	
F4	**1 0 0**	101X-X010-X	C	Time base/WDT clock Output: 4Hz The WDT time-out flag after:1s	
F8	**1 0 0**	101X-X011-X	C	Time base/WDT clock Output: 8Hz The WDT time-out flag after:1/2s	
F16	**1 0 0**	101X-X100-X	C	Time base/WDT clock Output: 16Hz The WDT time-out flag after:1/4s	
F32	**1 0 0**	101X-X101-X	C	Time base/WDT clock Output: 32Hz The WDT time-out flag after:1/8s	
F64	**1 0 0**	101X-X110-X	C	Time base/WDT clock Output: 64Hz The WDT time-out flag after:1/16s	
F128	**1 0 0**	101X-X111-X	C	Time base/WDT clock Output: 128Hz The WDT time-out flag after:1/32s	Yes
TOPT	**1 0 0**	1110-0000-X	C	Test mode	
TNORMAL	**1 0 0**	1110-0011-X	C	Normal mode	Yes

Notes: X: Don't care, A5 ~ A0: RAM addresses, D3 ~ D0: RAM data, D/C: Data/command mode,

Def.: Power on reset default.

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive command have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base/WDT clock frequency can be derived from an on-chip 256kHz RC oscillator, a 32,768kHz crystal oscillator, or an external 256kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the SC16232 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the SC16232.

CHIP TOPOGRAPHY



Chip size: 2.25 x 2.42(mm ^{2})

PAD COORDINATES(Unit: μm)

PAD NO.	X	Y	PAD NO.	X	Y
1	-1000	-1080	25	300	1080
2	-320	-1080	26	150	1080
3	-190	-1080	27	15	1080
4	-60	-1080	28	-125	1080
5	70	-1080	29	-265	1080
6	200	-1080	30	-405	1080
7	575	-1080	31	-545	1080
8	705	-1080	32	-685	1080
9	835	-1080	33	-1000	1080
10	1000	-1080	34	-1000	945
11	1000	-865	35	-1000	810
12	1000	-670	36	-1000	675
13	1000	-530	37	-1000	540
14	1000	-400	38	-1000	405
15	1000	-270	39	-1000	270
16	1000	-140	40	-1000	135
17	1000	-10	41	-1000	0
18	1000	120	42	-1000	-135
19	1000	250	43	-1000	-270
20	995	1080	44	-1000	-405
21	855	1080	45	-1000	-540
22	715	1080	46	-1000	-675
23	575	1080	47	-1000	-810
24	435	1080	48	-1000	-945

Note: The original point of the coordinate is the die center.

Attach

Revision History

Data	REV	Description	Page
2000.12.31	1.0	Original	
2002.04.26	2.0	Add the " ORDERING INFORMATION" The "SC1621" change to "SC16232"	1