



Dear customers,

**About the change in the name such as "Oki Electric Industry Co. Ltd." and "OKI" in documents to OKI Semiconductor Co., Ltd.**

The semiconductor business of Oki Electric Industry Co., Ltd. was succeeded to OKI Semiconductor Co., Ltd. on October 1, 2008. Therefore, please accept that although the terms and marks of "Oki Electric Industry Co., Ltd.", "Oki Electric", and "OKI" remain in the documents, they all have been changed to "OKI Semiconductor Co., Ltd.". It is a change of the company name, the company trademark, and the logo, etc. , and NOT a content change in documents.

October 1, 2008  
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**MSM5839B**

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**40-DOT SEGMENT DRIVER**

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**GENERAL DESCRIPTION**

The MSM5839B is a dot matrix LCD segment driver LSI which is fabricated using low power CMOS metal gate technology. This LSI consists of two 20-bit shift registers, two 20-bit latches, a 40-bit level shifter and a 40-bit 4-level driver.

It converts serial data, which is received from an LCD controller LSI, to parallel data and outputs LCD driving waveform to the LCD panel.

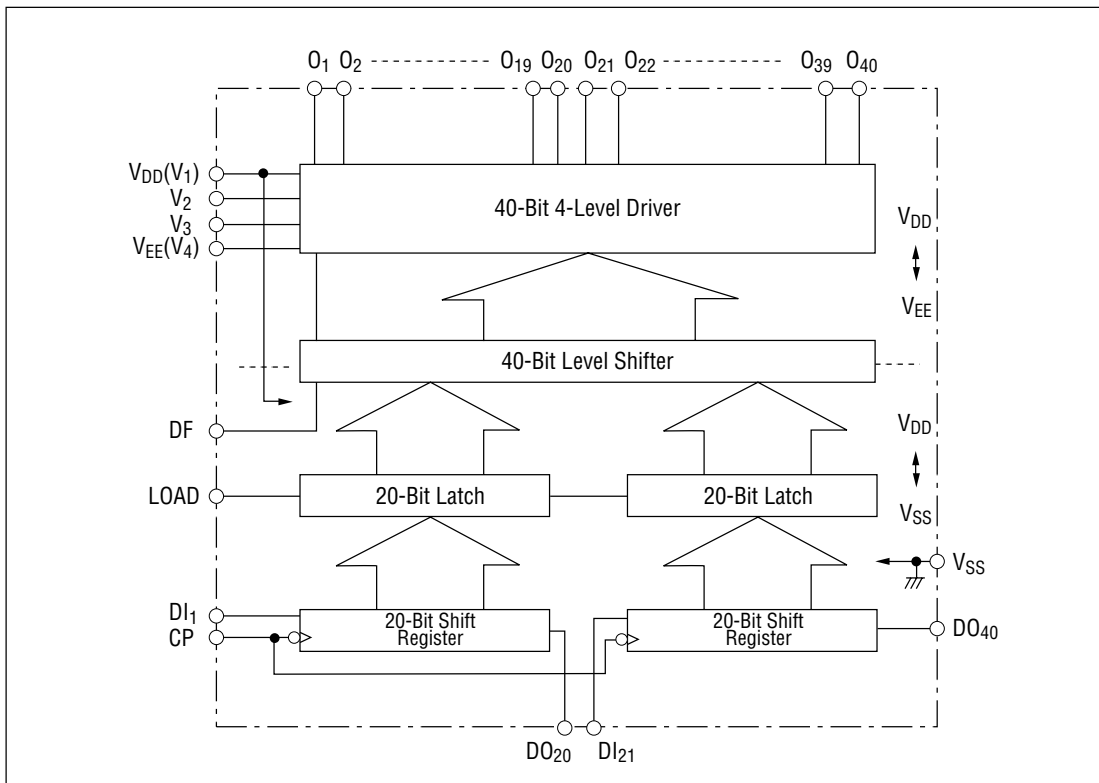
Expansion of display can easily be made by increasing the number of characters and character patterns.

This LSI can drive a variety of LCD panels because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from the external source.

**FEATURES**

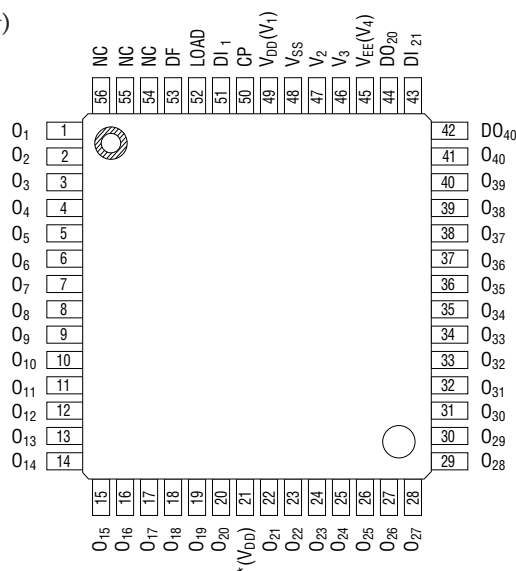
- Supply voltage : 4.5 to 5.5V
- LCD driving voltage : 8 to 18V
- Applicable LCD duty : 1/32 to 1/128
- Bias voltage can be supplied externally
- Applicable common driver : MSM5238 (32 outputs)
- Package options:
  - 56-pin plastic QFP (QFP56-P-910-0.65-K) (Product name: MSM5839B GS-K)
  - 56-pin plastic QFP (QFP56-P-910-0.65-L2) (Product name: MSM5839B GS-L2)
  - 56-pin plastic QFP (QFP56-P-910-0.65-2K) (Product name: MSM5839B GS-2K)

## BLOCK DIAGRAM

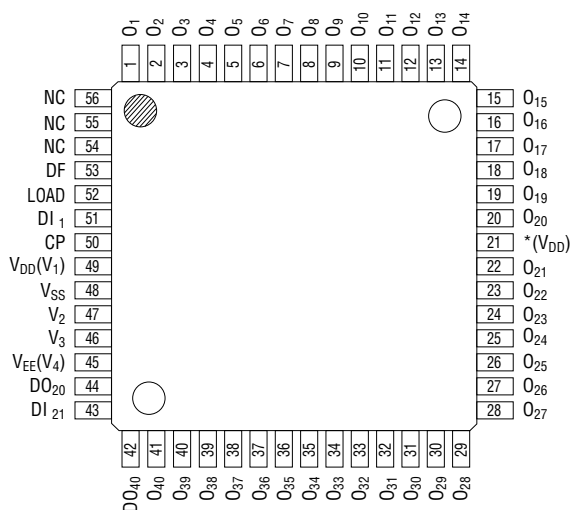


## PIN CONFIGURATION

(Top view)



### 56-Pin Plastic QFP (Type K)



### 56-Pin Plastic QFP (Type L)

\* This pin is internally connected to  $V_{DD}$ , so connect it to the power supply or leave it open.

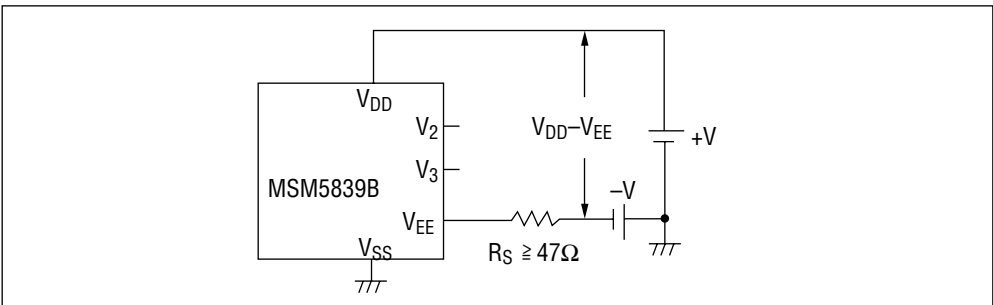
Note : The figure for Type L shows the configuration viewed from the reverse side of the package.  
Pay attention to the difference in pin arrangement.

# ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage (1)	$V_{DD}$ <sup>*1</sup>	$T_a = 25^{\circ}\text{C}$	-0.3 to +6	V
Supply Voltage (2)	$V_{DD}-V_{EE}$ <sup>*1</sup>	$T_a = 25^{\circ}\text{C}$	0 to 18	V
	$V_{DD}-V_{EE}$ <sup>*2</sup>	$T_a = 25^{\circ}\text{C}$	0 to 18	V
Input Voltage	$V_1$	$T_a = 25^{\circ}\text{C}$	-0.3 to $V_{DD} + 0.3$	V
Storage Temperature	$T_{STG}$	—	-55 to +150	$^{\circ}\text{C}$

\*1  $V_{DD} > V_2 > V_3 > V_{EE}$

\*2 Applies when a series resistor of  $47\Omega$  or more is connected as shown below.

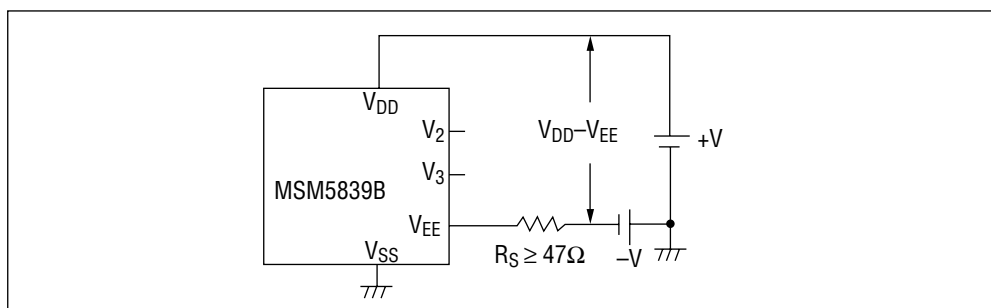


## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage (1)	$V_{DD}$	—	4.5 to 5.5	V
Supply Voltage (2)	$V_{DD}-V_{EE}$ *1	—	8 to 16	V
	$V_{DD}-V_{EE}$ *1, *2	—	8 to 18	V
Operating Temperature	$T_{Op}$	—	-20 to +85	°C

\*1  $V_{DD} > V_2 > V_3 > V_{EE}$

\*2 Applies when a series resistor of  $47\Omega$  or more is connected as shown below.



## ELECTRICAL CHARACTERISTICS

### DC Characteristics

( $V_{DD} = 5V \pm 10\%$ ,  $T_a = -20$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	$V_{IH}$ *1	—	$0.8V_{DD}$	—	$V_{DD}$	V
"L" Input Voltage	$V_{IL}$ *1	—	$V_{SS}$	—	$0.2V_{DD}$	V
"H" Input Current	$I_{IH}$ *1	$V_I = V_{DD}$	—	—	1	$\mu\text{A}$
"L" Input Current	$I_{IL}$ *1	$V_I = 0V$	—	—	-1	$\mu\text{A}$
"H" Output Voltage	$V_{OH}$ *2	$I_O = -0.4\text{mA}$	$V_{DD}-0.4$	—	—	V
"L" Output Voltage	$V_{OL}$ *2	$I_O = 0.4\text{mA}$	—	—	0.4	V
ON Resistance	$R_{ON}$ *4	$V_{DD}-V_{EE} = 10V$ $ V_N - V_O  = 0.25V$ *3	—	3.5	7	$k\Omega$
Supply Current	$I_{DD}$	Connect all inputs to $V_{DD}$ or $V_{SS}$ $V_{DD}-V_{EE} = 18V$ , No load	—	—	100	$\mu\text{A}$

\*1 Applicable to LOAD, CP, DI<sub>1</sub>, DI<sub>21</sub>, DF

\*2 Applicable to DO<sub>20</sub>, DO<sub>40</sub>

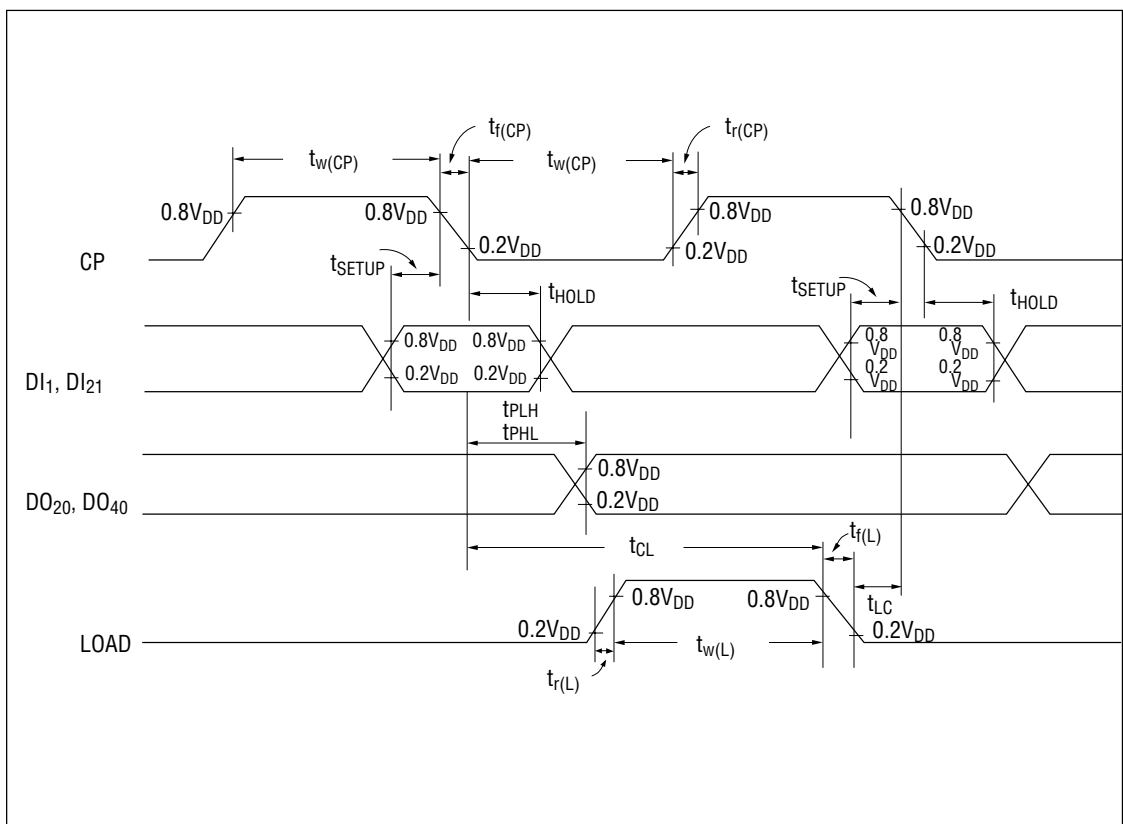
\*3  $V_N = V_{DD}$  to  $V_{EE}$ ,  $V_3 = \frac{2}{9} (V_{DD}-V_{EE})$ ,  $V_2 = \frac{7}{9} (V_{DD}-V_{EE})$

\*4 Applicable to O<sub>1</sub> - O<sub>40</sub>

# Switching Characteristics

( $V_{DD} = 5V \pm 10\%$ ,  $T_a = -20$  to  $+85^\circ\text{C}$ ,  $C_L = 15\text{pF}$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H", "L" Propagation Delay Time	$t_{PLH}$ $t_{PHL}$	—	—	—	250	ns
Clock Frequency	$f_{CP}$	DUTY = 50%	—	—	3.3	MHz
Clock Pulse Width	$t_{W(CP)}$	—	125	—	—	ns
LOAD Pulse Width	$t_{W(L)}$	—	125	—	—	ns
Data Setup Time DI $\rightarrow$ CP	$t_{SETUP}$	—	50	—	—	ns
CP $\rightarrow$ LOAD Time	$t_{CL}$	—	250	—	—	ns
LOAD $\rightarrow$ CP Time	$t_{LC}$	—	0	—	—	ns
Data Hold Time DI $\rightarrow$ CP	$t_{HOLD}$	—	50	—	—	ns
CP Rise/Fall Time	$t_{r(CP)}$ $t_{f(CP)}$	—	—	—	50	ns
LOAD Rise/Fall Time	$t_{r(L)}$ $t_{f(L)}$	—	—	—	1	$\mu\text{s}$



## FUNCTIONAL DESCRIPTION

### Pin Functional Description

- **DI<sub>1</sub>**

The data input pin for the 20-bit shift register (from 1st to 20th bit). The display data is input to the data pin in synchronization with a clock pulse.

- **CP**

Clock pulse input pin for the two 20-bit shift registers. The data is shifted in the two 20-bit shift registers at the falling edge of the clock pulse. Data setup time ( $t_{\text{SETUP}}$ ) and data hold time ( $t_{\text{HOLD}}$ ) are required each between DI<sub>1</sub>, DI<sub>21</sub> and CP. Refer to the Switching Characteristics.

- **DO<sub>20</sub>**

The 20th output bit of the shift register.

The data which is input from DI<sub>1</sub> is clocked out with the delay in the number of bits of the shift register (20). A 40-bit shift register can be configured by connecting the output of this pin to DI<sub>21</sub> pin.

- **DI<sub>21</sub>**

The data input pin for the 20-bit shift register (from 21st to 40th bit).

Connecting the DO<sub>20</sub> pin and this pin allows the device to be used as a 40-bit shift register.

- **DO<sub>40</sub>**

The 40th output bit of the shift register.

The data which is input from DI<sub>1</sub> is clocked out with the delay in the number of the bits of the shift register (20).

When extending the number of characters, this pin is used to cascade connect the next MSM5839B.

- **DF**

Alternate signal input pin for LCD driving waveform.

- **V<sub>DD</sub>(V<sub>1</sub>), V<sub>SS</sub>**

Supply voltage pins. V<sub>DD</sub> should be 4.5 to 5.5V.

V<sub>SS</sub> is the ground pin (V<sub>SS</sub> = 0V).

- **V<sub>2</sub>, V<sub>3</sub>, V<sub>EE</sub>(V<sub>4</sub>)**

Bias supply voltage pins to drive the LCD. Bias voltage is supplied from an external source.

- **LOAD**

The signal for latching the shift register contents is input from this pin.

When LOAD pin is set at "H", the shift register contents are transferred to the 40-bit 4-level driver. When LOAD pin is set at "L", the last display output data (O<sub>1</sub> to O<sub>40</sub>), which was transferred when LOAD pin was at "H", is held.



- **O<sub>1</sub> to O<sub>40</sub>**

Display data output pins which correspond to each data bit in the latch.

One of V<sub>DD</sub>, V<sub>2</sub>, V<sub>3</sub> or V<sub>EE</sub> (V<sub>4</sub>) is selected as a display driving voltage source based on the combination of latched data level and DF signal. Refer to the Truth Table below.

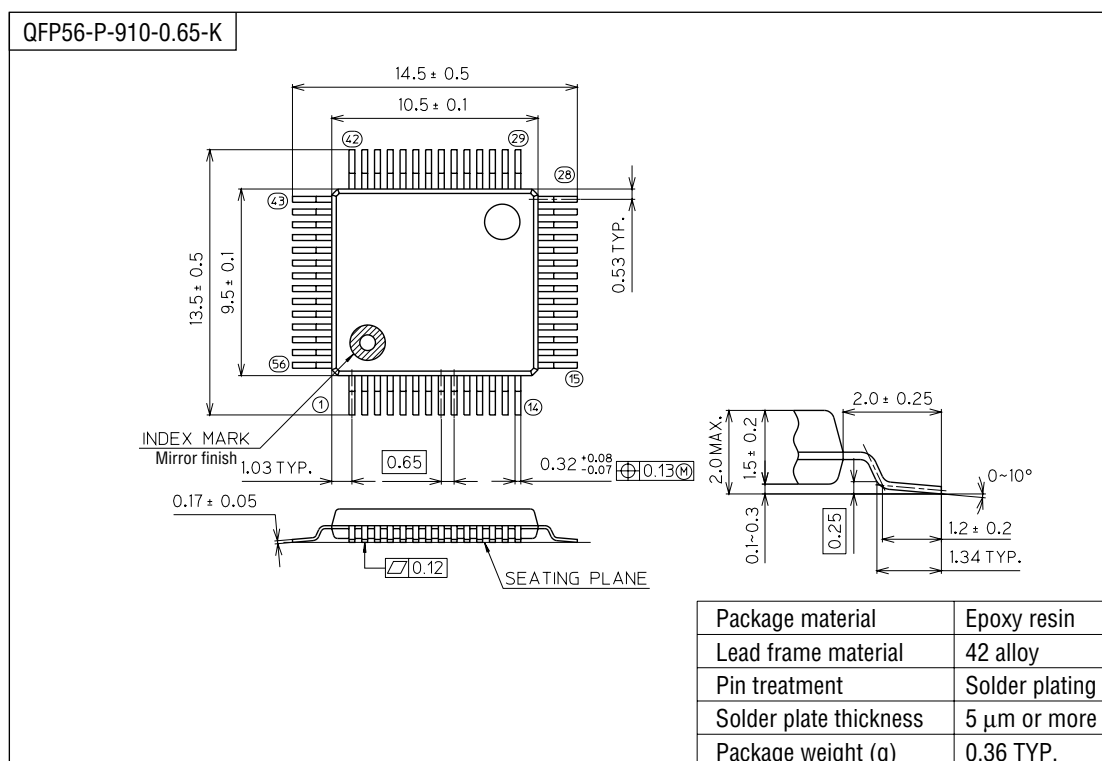
These pins should be connected to the SEGMENT side of the LCD panel.

**Truth Table**

Latched data	DF	LCD driver output
H	H	V <sub>EE</sub> (V <sub>4</sub> )
	L	V <sub>DD</sub> (V <sub>1</sub> )
L	H	V <sub>3</sub>
	L	V <sub>2</sub>

## PACKAGE DIMENSIONS

(Unit : mm)

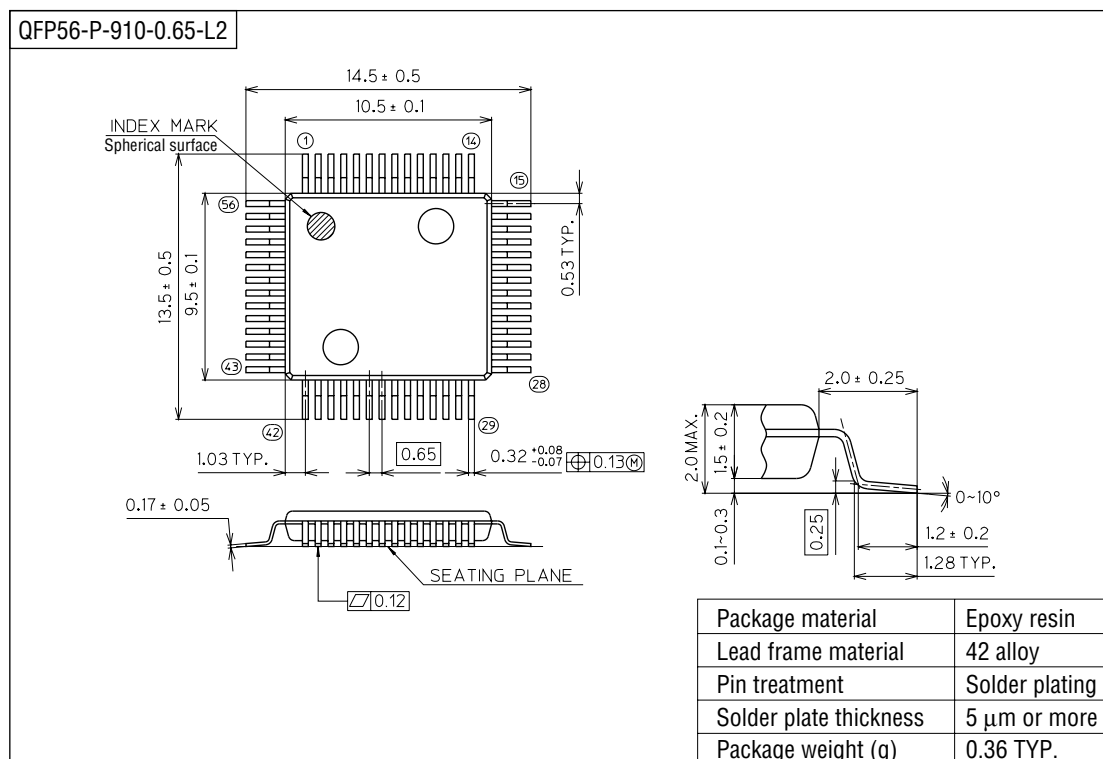


## Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

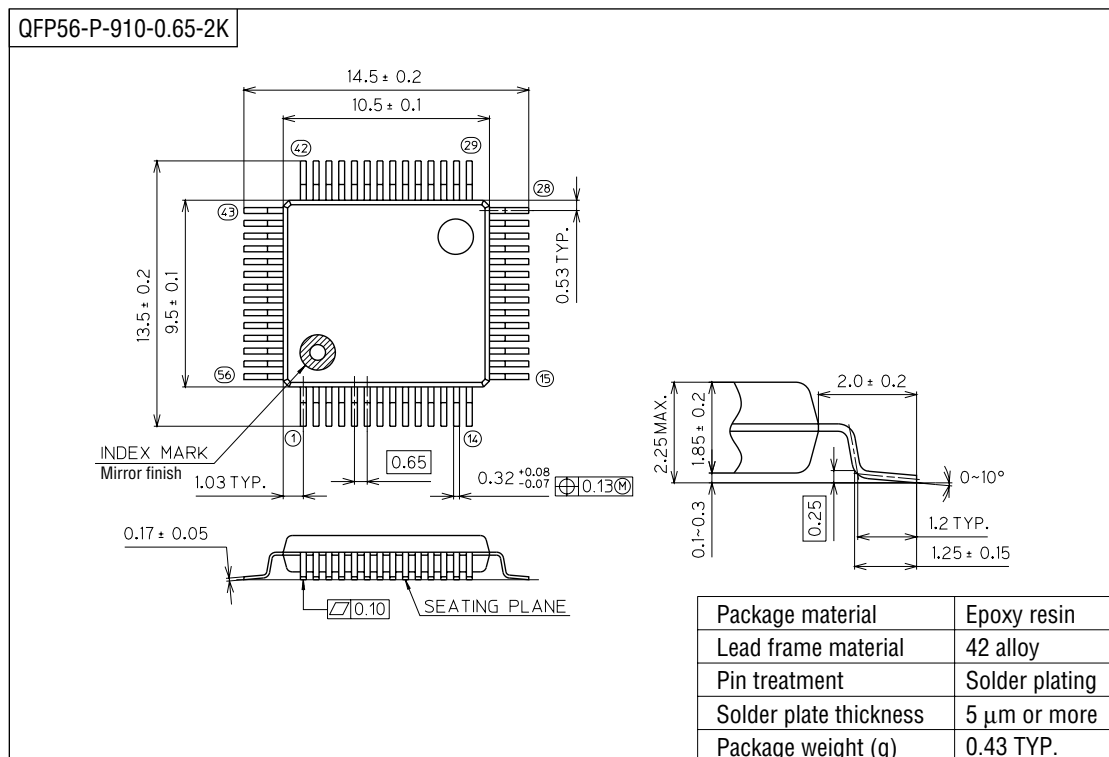
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