



Integrated Device Technology, Inc.

# 512K (64K x 8) SYNCHRONOUS STATIC RAM PLASTIC SIP MODULE

IDT 7MP6025

## FEATURES:

- 64K x 8 fully synchronous memory
- High-speed – 20MHz read cycle time
- 16-bit synchronous address input
- 8-bit synchronous data input
- Synchronous chip select and write enable
- Separate clock enable for each register
- Low standby power
- Onboard decoupling capacitors
- Available in 43-pin SIP (single in-line package) configuration
- 2 Ground and 2 V<sub>CC</sub> pins

## DESCRIPTION:

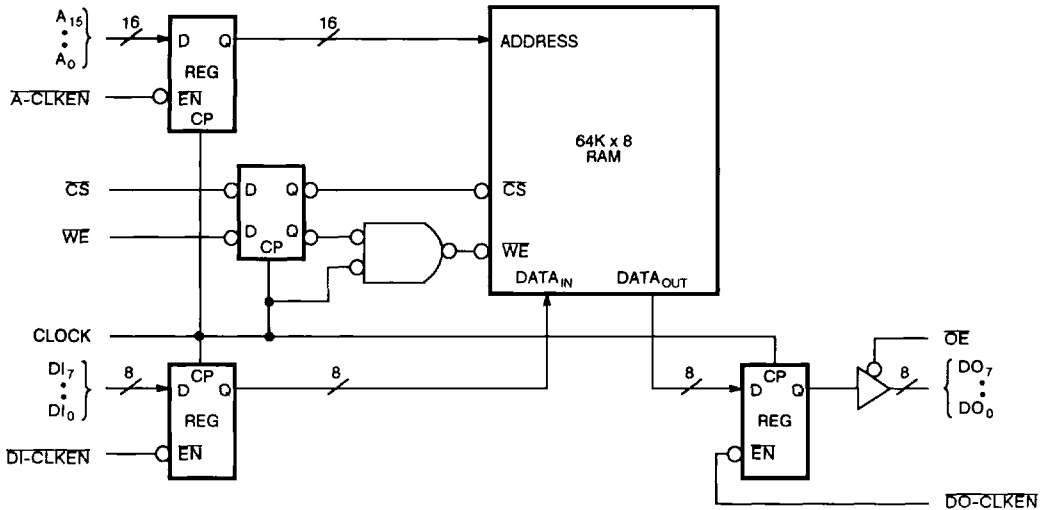
The IDT7MP6025 is a 64K x 8 synchronous RAM with edge triggered registers on the address lines, data-in bus, data-out bus, chip select and write enable. The edge triggered register of the 16 address lines features an independent clock enable that allows the address register to be selectively loaded. The address register will be loaded on the low-to-high transition of the clock when the clock enable line is low and will hold its current contents on the low-to-high transition of the clock when the clock enable is high. Similarly, the 8-bit data-in register will be loaded with new data on the low-to-high transition of the clock when the data-in clock enable is low and will hold its contents when the data-in clock enable is high. The data-out register will receive new data from the 64K x 8 RAM when the clock enable line is low and will hold its data when the clock enable line is high at the low-to-high transition of the clock. All

clock enables, as well as address and data inputs, must meet the appropriate set-up and hold times with respect to the clock.

The eight data output bits are enabled when the output enable is low and are in the high-impedance state when the output enable is high. The chip select and write enable signals are also registered in D flip-flops. These two flip-flops are loaded with new data on each low-to-high transition of the clock. The chip select is passed directly from the Q output of the D-type flip-flop to the 64K x 8 RAM. The write enable signal is gated with the clock signal to generate a delayed write enable pulse. In essence, this gives the output of the address register time to settle and internally select the appropriate byte of RAM before the write enable goes low to write new data into the RAM. Thus, the low-to-high transition of the clock causes the chip select and write enable flip-flops to be loaded with new data and immediately deselects a previous write by means of the clock going high. The data lines to the RAM and the address lines to the RAM may indeed change to new values based on the low-to-high transition of the clock. When the clock goes from high-to-low, if the chip select is low and the write enable is low, a write cycle is begun and the data at the RAM data inputs will be written into the selected address. If the write enable is high or the chip enable is high, data will not be written into the memory.

One of the features of this configuration of memory that has registers on all of the address lines, data input lines and data output lines as well as the control lines, is to provide the highest possible clock rate in the system. All that is necessary is that the data, address, chip select, write enable and clock enables signals meet the required set-up and hold time with respect to the clock. In this manner, fully asynchronous operation is achieved. The IDT7MP6025 is offered as a compact, cost-effective 43-pin plastic SIP module.

## FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGE

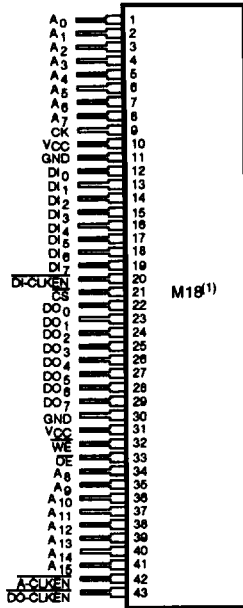
JANUARY 1989

© 1989 MIPS Computer Systems, Inc. All Rights Reserved.

S13-189

OSC-7031/-

**PIN CONFIGURATION**



**SIP  
 SIDE VIEW**

**NOTE:**

1. For module dimension, please refer to module drawing M18 in the packaging section.

**PIN NAMES**

A <sub>0-15</sub>	Addresses
CK	Clock
DI <sub>0-7</sub>	Data Input
DO <sub>0-7</sub>	Data Output
DI-CLKEN	Data Input Clock Enable
A-CLKEN	Address Clock Enable
DO-CLKEN	Data Output Clock Enable
V <sub>CC</sub>	Power
GND	Ground
CS	Chip Select
WE	Write Enable
OE	Output Enable

**ABSOLUTE MAXIMUM RATINGS**

SYMBOL	RATING	COMMERCIAL	UNIT
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature	0 to +70	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	°C
I <sub>OUT</sub>	DC Output Current	50	mA

**NOTE:**

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	-	6.0	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	-	0.8	V

**NOTE:**

1. V<sub>IL</sub> (min.) = -3.0V for pulse width less than 20ns.

**RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE**

GRADE	AMBIENT TEMPERATURE	GND	V <sub>CC</sub>
Commercial	0°C to +70°C	0V	5.0V ± 10%

**DC ELECTRICAL CHARACTERISTICS**

V<sub>CC</sub> = 5V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
I <sub>I1</sub>	Input Leakage (Address & Control)	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND to V <sub>CC</sub>	-	5	µA
I <sub>I2</sub>	Input Leakage (Data)	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND to V <sub>CC</sub>	-	5	µA
I <sub>I3</sub>	Output Leakage	V <sub>CC</sub> = Max., CS = V <sub>OUT</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>	-	10	µA
V <sub>OL</sub>	Output Low Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8mA	-	0.4	V
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4mA	2.4	-	V

**DC ELECTRICAL CHARACTERISTICS**

V<sub>CC</sub> = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS	MAX.	UNIT
I <sub>CC1</sub>	Operating Current	f = 0, CS = V <sub>IL</sub> , V <sub>CC</sub> = Max., Output Open	725	mA
I <sub>CC2</sub>	Dynamic Operating Current	V <sub>CC</sub> = Max., CS = V <sub>IL</sub> ; f = f <sub>MAX</sub> , Output Open	950	mA
I <sub>SB1</sub>	Standby Power Supply Current	CS ≥ V <sub>CC</sub> - 0.2V V <sub>IN</sub> > V <sub>CC</sub> - 0.2V or < 0.2V	125	mA

**CAPACITANCE** (T<sub>A</sub> = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER <sup>(1)</sup>	CONDITIONS	TYP.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	20	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	22	pF

**NOTE:**

1. This parameter is sampled and not 100% tested.

**AC ELECTRICAL CHARACTERISTICS**

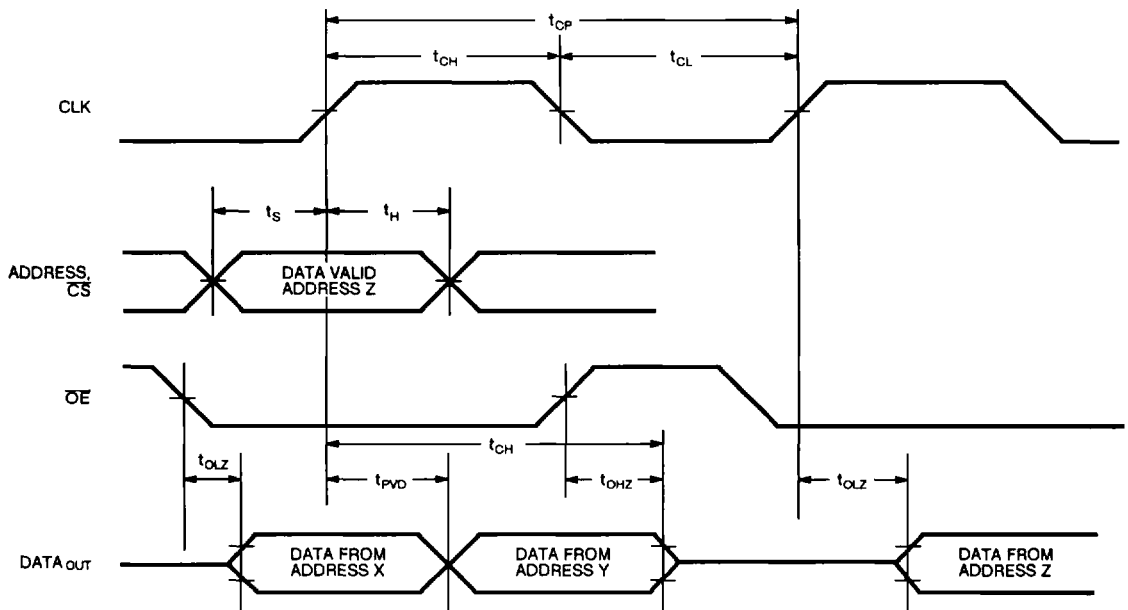
V<sub>CC</sub> = 5V ±10%

SYMBOL	PARAMETER	7MP6025S35		7MP6025S45		7MP6025S55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
<b>READ CYCLE</b>								
t <sub>CP</sub>	Read Cycle Time	35	—	45	—	55	—	ns
t <sub>CH</sub>	Clock High Time	10	—	10	—	10	—	ns
t <sub>CL</sub>	Clock Low Time	10	—	10	—	10	—	ns
t <sub>S</sub>	Address, $\overline{WE}$ , $\overline{CS}$ , $\overline{CE}$ Set Up Time	4	—	5	—	5	—	ns
t <sub>H</sub>	Address, $\overline{WE}$ , $\overline{CS}$ , $\overline{CE}$ Hold Time	4	—	6	—	6	—	ns
t <sub>OLZ</sub> <sup>(1)</sup>	Output Low Z Time	—	10	—	15	—	15	ns
t <sub>OHZ</sub> <sup>(1)</sup>	Output High Z Time	—	8	—	11	—	11	ns
t <sub>PVD</sub>	Prop Delay to Valid Data Out	—	10	—	15	—	15	ns
<b>WRITE CYCLE</b>								
t <sub>CP</sub>	Write Cycle Time	35	—	45	—	55	—	ns
t <sub>CH</sub>	Clock High Time	10	—	10	—	10	—	ns
t <sub>CL</sub>	Clock Low Time	23	—	30	—	37	—	ns
t <sub>S</sub>	Data, Addr, $\overline{WE}$ , $\overline{CS}$ , $\overline{CE}$ Set Up Time	4	—	5	—	5	—	ns
t <sub>H</sub>	Data, Addr, $\overline{WE}$ , $\overline{CS}$ , $\overline{CE}$ Hold Time	4	—	6	—	6	—	ns

**NOTE:**

1. This parameter is guaranteed but not tested.

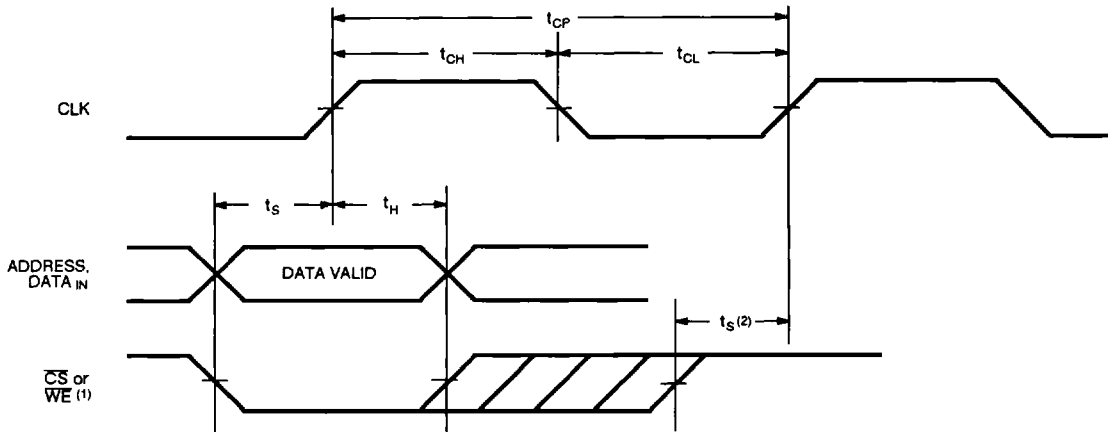
**TIMING WAVEFORM OF READ CYCLE <sup>(1)</sup>**



**NOTE:**

1. The device must be selected by a  $\overline{CS}$  level for the conditions above to take place.

**TIMING WAVEFORM OF WRITE CYCLE**



**NOTES:**

1. Either  $\overline{CS}$  or  $\overline{WE}$  can be used to trigger a write cycle, provided that the other signal is low at the same time.
2. When a write is terminated, either  $\overline{CS}$  or  $\overline{WE}$  must become high at least one  $t_s$  before the next rising edge of CLK.

**TRUTH TABLE**

MODE	$\overline{CS}$	$\overline{OE}$	CK	$\overline{DO-CLKEN}$	$\overline{DI-CLKEN}$	$\overline{A-CLKEN}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	H	↑	H	H	H	X	High Z	Standby
Read	L	L	↑	L	X	L	H	Low Z	Active
Read	L	H	↑	L	X	L	H	High Z	Active
Write	L	H	↑	H	L	L	L	High Z	Active

**AC TEST CONDITIONS**

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

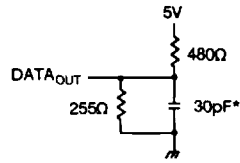


Figure 1. Output Load

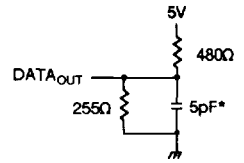


Figure 2. Output Load  
 (for  $t_{OLZ}$ ,  $t_{CHZ}$ ,  $t_{OHZ}$ ,  
 $t_{WHZ}$  and  $t_{OW}$ )

\* Including scope and jig.

**ORDERING INFORMATION**

