SMP9210, -11, -12

Dual 10-Bit Nonvolatile DAC

Preliminary

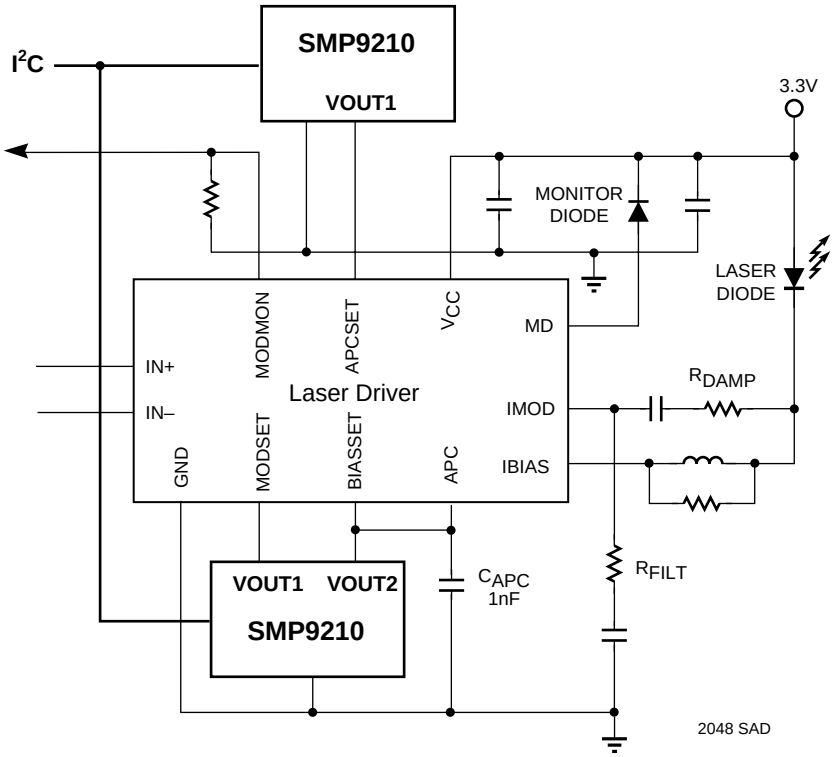
FEATURES

- Two 10-Bit Nonvolatile DACs
  - INL ±1LSB
  - DNL ±1LSB
- Programmable Configuration
- Programmable Power On Reset Options
  - Recall Full Scale Value
  - Recall Zero Scale Value
  - Recall Mid-Scale Value
  - Recall NV Register Value
- Tandem or Independent Operation of DACs
- Programmable Power Down Mode (Short VOUT to GND or Float VOUT)
- I2C Interface
- Low Noise Outputs
- 2.7V to 5.5V Operation
- –40°C to 85°C Temperature Range

APPLICATIONS

- ATE Set and Forget Calibration
- Laser Biasing
- RFPA Biasing

SIMPLIFIED APPLICATION DRAWING



INTRODUCTION

The SMP9210, -11, -12 trio are serial input, voltage output, dual 10-Bit digital to analog converters. They can operate from a single 2.7V to 5.5V supply. Internal precision buffers swing rail-to-rail with an input reference range from ground to the positive supply.

They integrate two 10-Bit DACs and their associated circuits: an enhanced unity gain operational amplifier output, a 10-Bit volatile data latch, a 10-bit nonvolatile data register and an industry standard 2-wire serial interface.

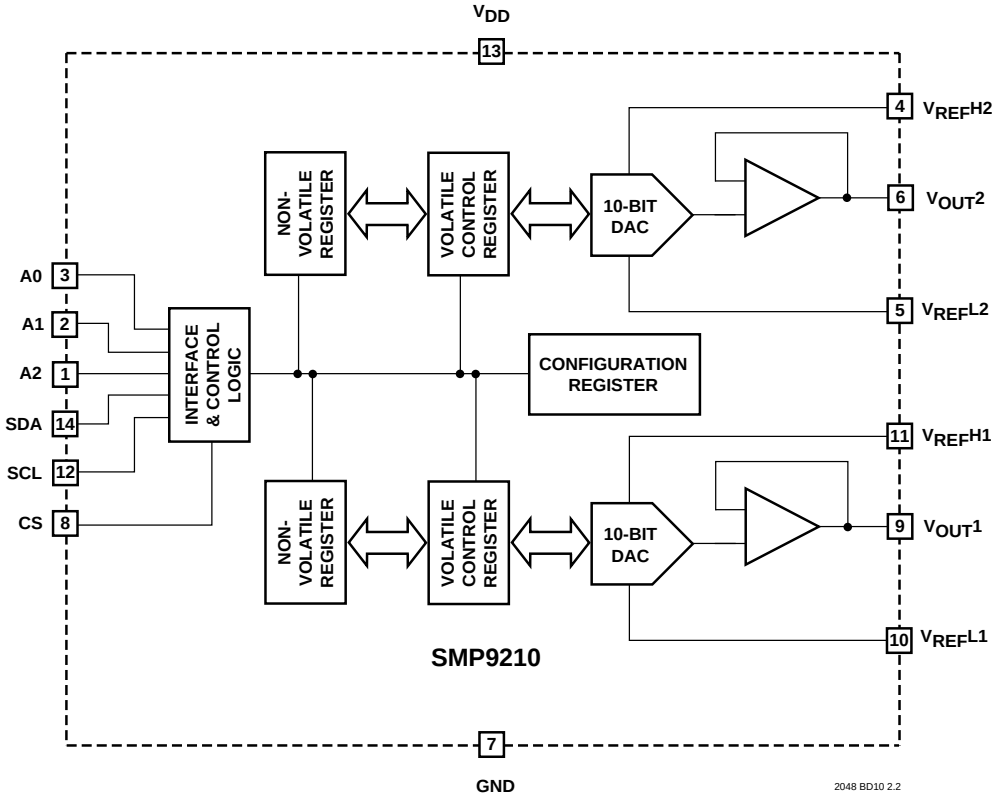
Programming of configuration, control and calibration values by the user can be simplified with the interface adapter and Windows GUI software obtainable from Summit Microelectronics.

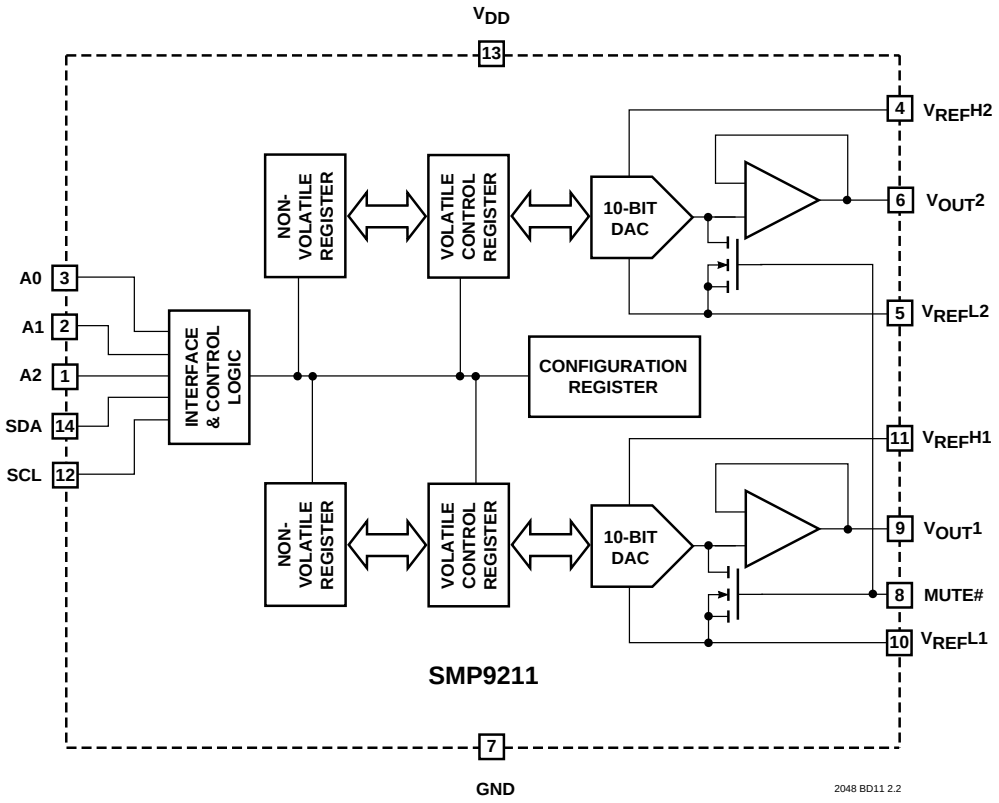
RECOMMENDED OPERATING CONDITIONS

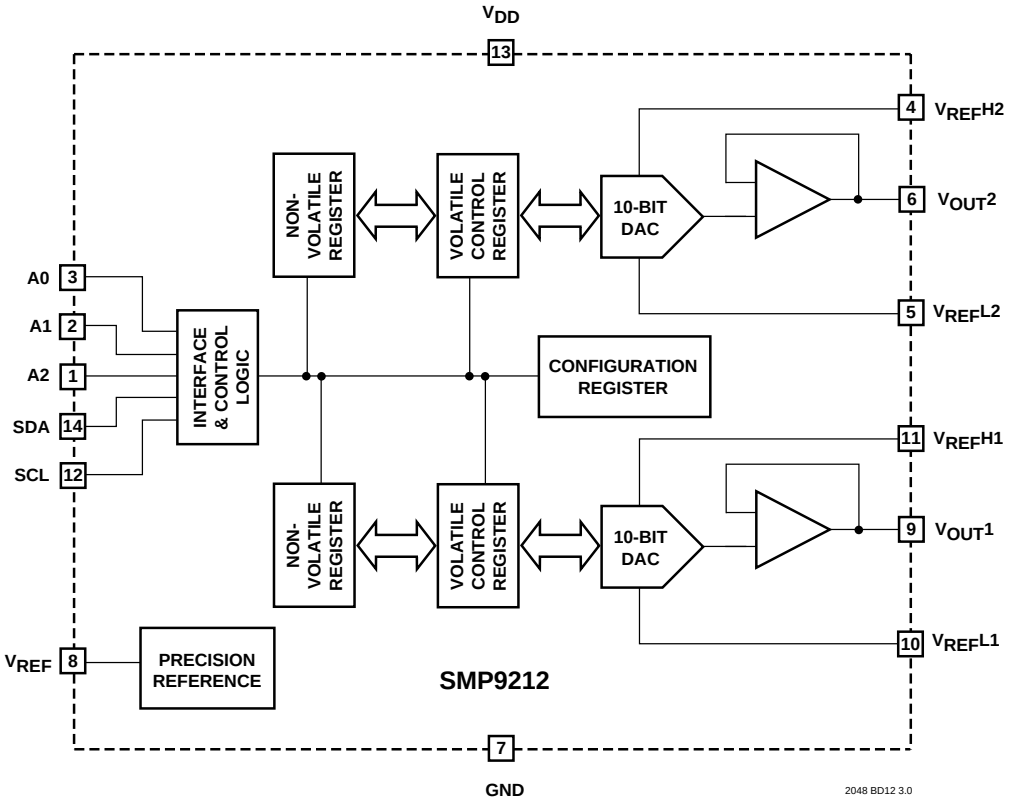
Temperature	–40°C to 85°C.
Voltage	2.7V to 5.5V

FUNCTIONAL BLOCK DIAGRAMS

Note: Pinouts for these three drawings reflect the 14 pin SOIC package.




VDD
13
4 VREFH2
6 VOUT2
5 VREFL2
11 VREFH1
9 VOUT1
8 MUTE#
10 VREFL1
A0 3
A1 2
A2 1
SDA 14
SCL 12
NON-VOLATILE REGISTER
VOLATILE CONTROL REGISTER
10-BIT DAC
INTERFACE & CONTROL LOGIC
CONFIGURATION REGISTER
NON-VOLATILE REGISTER
VOLATILE CONTROL REGISTER
10-BIT DAC
SMP9211
7
GND
2048 BD11 2.2


VDD
13
4 VREFH2
6 VOUT2
5 VREFL2
11 VREFH1
9 VOUT1
10 VREFL1
A0 3
A1 2
A2 1
SDA 14
SCL 12
VREF 8
NON-VOLATILE REGISTER
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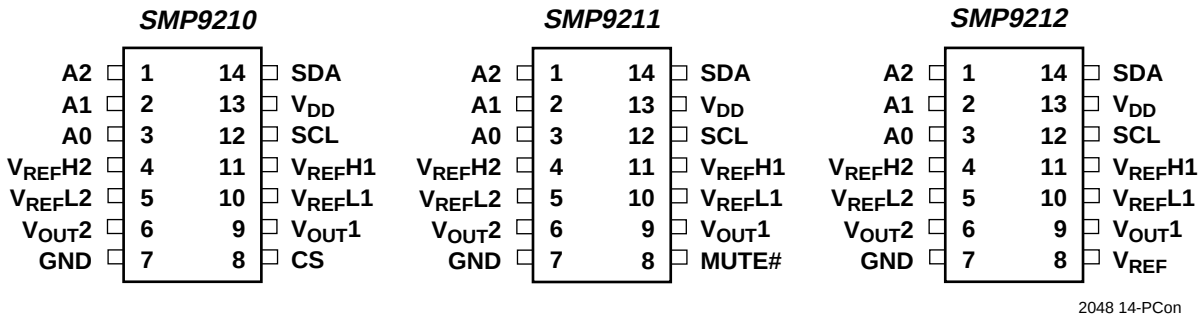
10-BIT DAC
INTERFACE & CONTROL LOGIC
CONFIGURATION REGISTER
NON-VOLATILE REGISTER
VOLATILE CONTROL REGISTER
10-BIT DAC
PRECISION REFERENCE
SMP9212
7
GND
2048 BD12 3.0

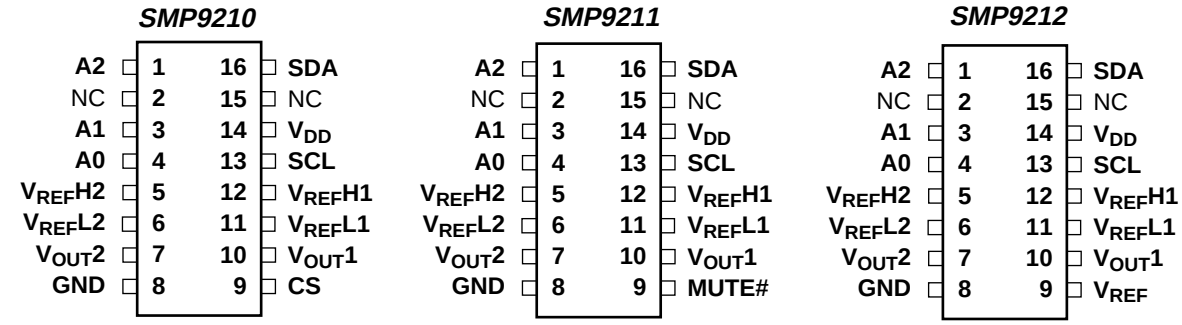
PIN CONFIGURATIONS

14-Pin SOIC



2048 14-PCon

16-Pin SSOP



2048 16-PCon

PIN DESCRIPTIONS

V_{DD}

Power supply input.

GND

Power supply return.

$V_{OUT}1$, $V_{OUT}2$

The voltage output of the DACs. It is buffered by a unity-gain follower that can slew up to 1V/µs.

$V_{REF}L1$, $V_{REF}L2$

The lower of the voltage reference inputs. $V_{REF}L$ must be equal to or greater than ground and less than $V_{REF}H$.

$V_{REF}H1$, $V_{REF}H2$

The higher of the voltage reference inputs. $V_{REF}H$ must be equal to or less than V_{CC} and greater than $V_{REF}L$.

A0, A1, A2

The address inputs for the serial interface logic. Biasing the address inputs will determine the device's bus address that is contained within the serial data stream when communicating over the serial bus.

SCL

The serial interface clock. It is used to clock the data in and out. When writing to the device data must remain stable while SCL is high. When reading from the device data is clocked out on the falling edge of SCL.

SDA

The bidirectional pin used to transfer data in and out of the device.

CS

Chip Select input (V_{IH} = selected) in the 9210. See the Block Diagrams.

MUTE#

Mute input (V_{IL} = mute) in the 9211. See the Block Diagrams.

V_{REF}

V_{REF} output (1.25V) in the 9212. See the Block Diagrams.

Note: NC pins are not connected.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to 125°C
Storage Temperature ..... –65°C to 150°C
Lead Solder Temperature (10 secs) ..... 300 °C
Terminal Voltage with Respect to GND:
V_{DD} ..... –0.3V to 6.0V
All Others ..... –0.3V to 6.0V
θJ_A ..... 14 Pin = 88, 16 pin = 115
θJ_C ..... 14 Pin = 37, 16 pin = 40

*Comment

Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

DC OPERATING CHARACTERISTICS

(**Over Recommended Operating Conditions; Voltages are relative to GND**)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Static Performance (1)						
N	Resolution		10			Bits
INL	Relative Accuracy		–2	±1	2	LSB
DNL	Differential nonlinearity	Guaranteed monotonic	–1	±0.5	1	LSB
VZSE	Zero scale error	Data = 000_{HEX}	0		20	mV
VFS	Full scale voltage	Data = $3FF_{HEX}$			$V_{REF}H$ –1LSB	V
TCV	Full scale temperature coefficient			±15		ppm
	Offset error		–0.3		0.3	%VFS
	Gain error		–0.5		0.5	%
Matching Performance						
	Linearity matching error			±5		LSB
Analog Output						
I_{OUT}	Output current	Data = 200_{HEX}, ΔV_{OUT}, 3LSB			±5	mA
LDREG	Load regulation @ halfscale	Data = 200_{HEX}, RL = 1kΩ to ∞		1	4	LSB
C_L	Capacitive load	No oscillation		500		pF
Reference Voltages						
$V_{REF}H$		$V_{REF}H > V_{REF}L$			V_{DD}	V
$V_{REF}L$		$V_{REF}L < V_{REF}H$	GND			V
$V_{REF}OUT$		SMP9212		1.25		V

(1) $V_{REF}L$ = 0.5V, $V_{REF}H$ = 4.5V

2048 Elect TableA 3.1

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Power						
I_{DD}	Power supply current	NV write V_{DD} = 5.5V			3	mA
		NV write V_{DD} = 2.7V			3	mA
	Standby or quiescent	Excluding current through DACs V_{DD} = 5.5V			1	mA
		Excluding current through DACs V_{DD} = 2.7V			1	mA
	Power down	Total current including DAC V_{DD} = 5.5V			1	mA
		Total current including DAC V_{DD} = 2.7V			1	mA
V_{DD}	Supply voltage		2.7		5.5	V
V_{IH}	SDA, SCL				$0.7 \times V_{DD}$	V
V_{IL}	SDA, SCL		$0.3 \times V_{DD}$			V
V_{OL}	SDA	I_{OL} = 3mA			0.4	V
I_{LI}	Input leakage	V_{IN} = 0 to V_{DD}		100		µA
I_{LO}	Output leakage	V_{OUT} powered down in high impedance mode			10	µA
W_{END}	Write endurance	Number of NV store operations	1×10^6			NV stores
t_{DR}	Data retention	NV data retention	100			Years

2048 Elect TableB

DEVICE OPERATION

INTRODUCTION

The device has two 10-Bit digital to analog converters that are comprised of a resistor network that converts a digital input into an equivalent analog output voltage in proportion to the applied reference voltage. The voltage differential between each of the $V_{REF}L$ and $V_{REF}H$ input pairs sets the full-scale output voltage for their respective DAC.

Each DAC has a 10-Bit volatile register that holds the current digital value. The register can be set to any value by the serial interface; commanded to load the zero scale value, full scale value or mid-scale value; or can recall a preset value stored in a nonvolatile register.

Each DAC has a 10-Bit nonvolatile register that can hold a 'set-and-forget' value that can be recalled whenever the device is powered-on.

The device also has a nonvolatile configuration register that is accessible over the 2-wire bus. The configuration register is used to select the device type identifier, the function of pin 8 and the DAC power-on state.

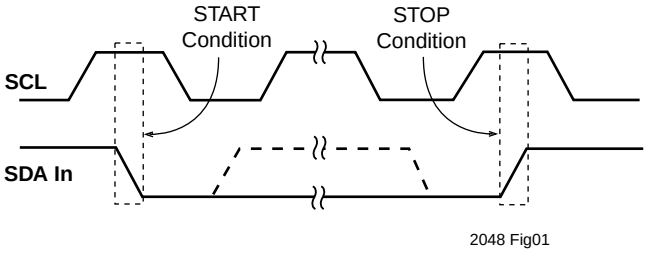


Figure 1. START and STOP Timing

ACCESSING THE DACS

The device uses the industry standard 2-wire serial protocol. The bus is designed for two-way, two-line serial communication between different integrated circuits. The two lines are the SCL (serial clock) and SDA (serial data) and both lines must be tied to the positive supply through a pull-up resistor. The protocol defines devices as being either Masters or Slaves. The SMP9210, -11, or -12 will always be a Slave because it does not initiate any communications or provide a clock output.

Data transfers are initiated when a Master issues a Start condition, which is a high to low transition on SDA while SCL is high (see Figure 1). The Start is immediately followed by an eight bit transmission: bits 7 through 1 comprise the device type identifier and bus device bus address; bit 0 is the Read/Write bit indicating the action to follow. If the intended device receives the byte and recognizes its address it will return an Acknowledge during the 9th clock cycle. Some data transfers will be concluded with a Stop condition, which is a low to high transition on SDA while SCL is high. Note: a Stop condition must be performed for all nonvolatile Write operations. Timing for all I^2C operations are summarized in Figure 2 and Table 1.

The DAC device type identifier default is 0101_{BIN}. In order to accommodate more than eight devices on a single bus the device type identifier can be modified by the end user by writing to the Configuration Registers. (See page 10)

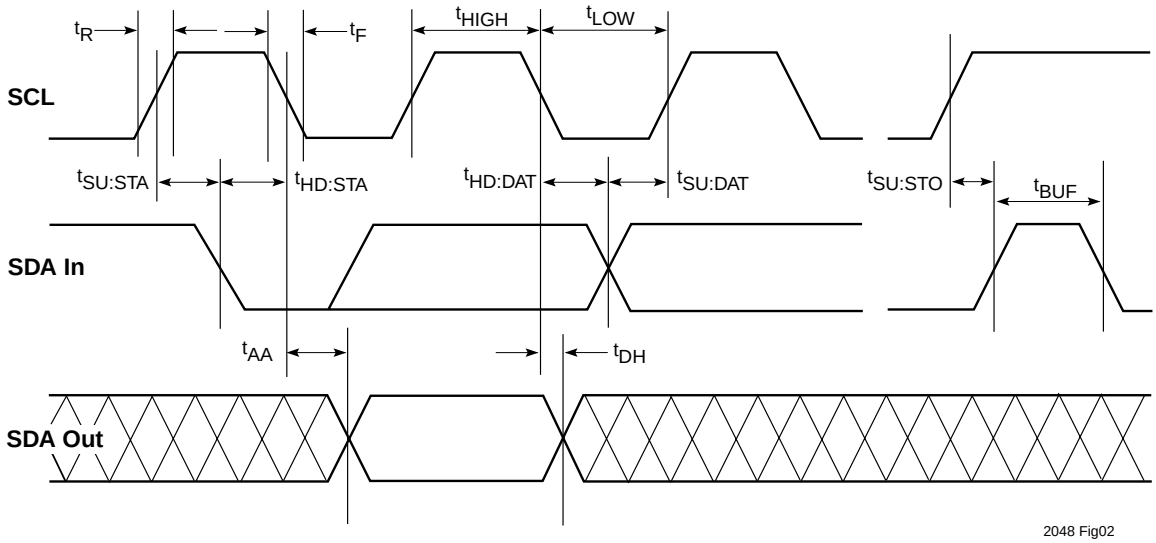


Figure 2. Data/Clock Timing

Symbol	Parameter	Conditions	Min.	Max.	Units
f_{SCL}	SCL clock frequency		0	100	kHz
t_{LOW}	Clock low period		4.7		µs
t_{HIGH}	Clock high period		4.0		µs
t_{BUF}	Bus free time (1)	Before new transmission	4.7		µs
$t_{SU:STA}$	Start condition setup time		4.7		µs
$t_{HD:STA}$	Start condition hold time		4.0		µs
$t_{SU:STO}$	Stop condition setup time		4.7		µs
t_{AA}	Clock edge to valid output (1)	SCL low to valid SDA (cycle n)	0.3	3.5	µs
t_{DH}	Data Out hold time (1)	SCL low (cycle n+1) to SDA change	0.3		µs
t_R	SCL and SDA rise time (1)			1000	ns
t_F	SCL and SDA fall time (1)			300	ns
$t_{SU:DAT}$	Data In setup time (1)		250		ns
$t_{HD:DAT}$	Data In hold time (1)		0		ns
TI	Noise filter SCL and SDA (1)	Noise suppression		100	ns
t_{WR}	Write cycle time			5	ms

Note (1) These values are guaranteed by design.

2048 Table01 2.0

Table 1. Data/Clock Timing

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	Command	Function
1	**0**	**0**	**1**	x	x	**D9**	**D8**	Write DAC1	Write 10-Bit value to DAC1
1	**0**	**1**	**0**	x	x	**D9**	**D8**	Write DAC2	Write 10-Bit value to DAC2
1	**0**	**1**	**1**	x	x	**D9**	**D8**	Write both DACs	Write 10-Bit value to both DACs
1	**1**	**0**	**1**	**1**	**1**	**1**	**0**	3F DAC2	Set DAC2 to full scale ($V_{REF}H$)
1	**1**	**0**	**1**	**1**	**1**	**0**	**1**	3F DAC1	Set DAC1 to full scale ($V_{REF}H$)
1	**1**	**0**	**1**	**1**	**1**	**1**	**1**	3F both DACs	Set both DACs to full scale ($V_{REF}H$)
1	**1**	**1**	**0**	**1**	**1**	**1**	**0**	Zero DAC2	Set DAC2 to zero scale ($V_{REF}L$)
1	**1**	**1**	**0**	**1**	**1**	**0**	**1**	Zero DAC1	Set DAC1 to zero scale ($V_{REF}L$)
1	**1**	**1**	**0**	**1**	**1**	**1**	**1**	Zero both DACs	Set both DACs to zero scale ($V_{REF}L$)
1	**1**	**1**	**1**	x	x	**1**	**0**	Recall DAC2	Recall E^2 to DAC2
1	**1**	**1**	**1**	x	x	**0**	**1**	Recall DAC1	Recall E^2 to DAC1
1	**1**	**1**	**1**	x	x	**1**	**1**	Recall both DACs	Recall E^2 to both DACs
1	**0**	**0**	**0**	x	x	**1**	**0**	PD DAC2	Power down DAC2 (V_{OUT} to GND)
1	**0**	**0**	**0**	x	x	**0**	**1**	PD DAC1	Power down DAC1 (V_{OUT} to GND)
1	**0**	**0**	**0**	x	x	**1**	**1**	PD both DACs	Power down both DACs (V_{OUT} to GND)

2048 Table02 3.0

Table 2. Command Structure

The command structure is illustrated in Table 2. Of special note is the ability to write individually to either of the two DACs, or write to them both. The first three commands are three bytes in length and can either be volatile or nonvolatile.

ACK and NACK

A device that is receiving data will respond with an Acknowledge by pulling the SDA line low (ACK) after each byte is transmitted. The transmitting device will recognize this and continue to transmit. When the Master has received the data it expects it will hold the SDA line high (NACK) and the transmitting device will end transmission.

Sequence

The sequence is to issue a Start, followed by the device type and bus address with the Read/Write bit set to zero. The device will respond with an Acknowledge and the Master will then issue the command and follow-on data. In Figure 3 the Write is to DAC1 where the command = 1001_{BIN}; D9 and D8 are the MSBs of the DAC value being written. The device will then respond with an Acknowledge followed by the Master writing the last eight bits. If no Stop is generated after the device Acknowledge the Write is only to the register. If the device Acknowledge is followed by a Stop the data is written to both the DAC register and to the nonvolatile register.

Reading the Device

Reading the DACs requires setting the R/W bit to one. Then the host supplies clocks and the device will output data as shown in Figure 4. PD is the Power Down mode indicator: 1 = power down, 0= DAC active. Both DACs provide their data for a single Read operation.

Special Configurations

The SMP9210 can be configured by the end user or by Summit prior to shipment (see page 10). Reading the configuration register can also be performed if it has not already been locked. See Figure 5. There is one configuration register and it is accessed through the serial interface using 1001_{BIN} as the device type address, consequently the DAC address should never be set to 1001_{BIN}. The register is shown in Table 3.

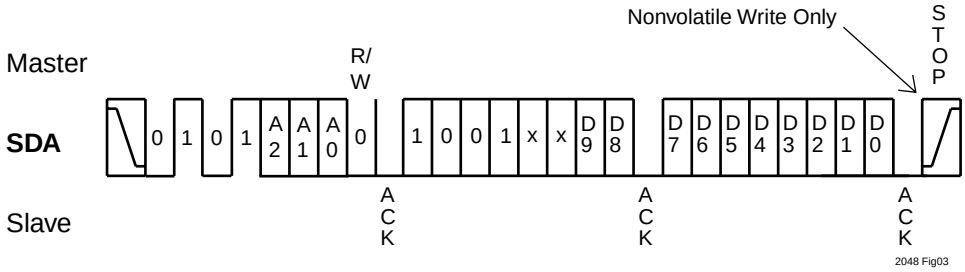


Figure 3. DAC1 Write Operation (see Table 2)

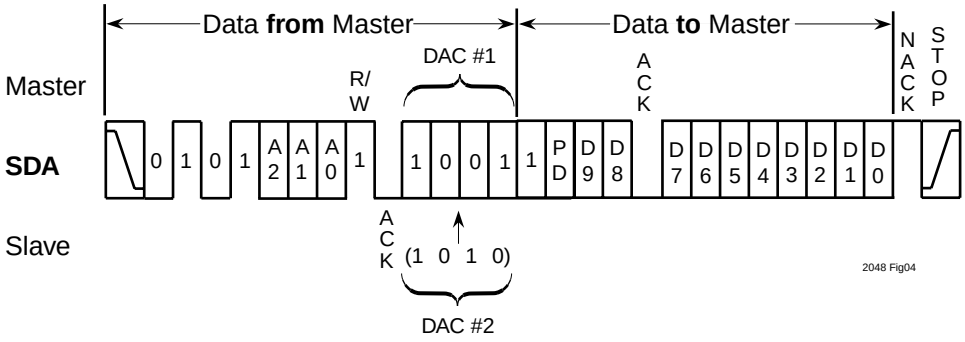


Figure 4. Read DAC1 (See DAC2 Differentiator & Table 2)

CONFIGURATION REGISTER

Note: All parts are normally shipped with the Configuration Register locked. Unlocked user configurable parts are available on a special order basis. Contact the factory.

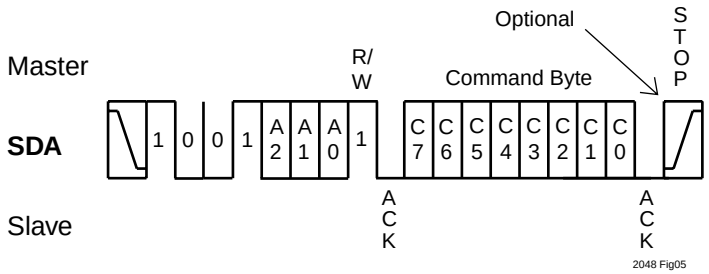


Figure 5. Configuration Register (see Table 3)

MSB C7	C6	C5	C4	C3	C2	C1	LSB C0	Function
x	x	x	x	x	x	x	**0**	Configuration register accessible
					x	x	**1**	Configuration register locked
					0	**0**	x	Power on recall: DACs set to all 0s
					0	**1**		Power on recall: DACs set to all 1s
					1	**0**		Power on recall: DACs set to mid scale
					1	**1**		Power on recall: DACs set to NV register
				0	x	x		At power down V_{OUT} = low impedance
				1				At power down V_{OUT} = high impedance
PDA3*	**PDA2***	**PDA1***	**PDA0***	x				Programmble DAC address

* Note: Never set the DAC address to 1001_{BIN}. The Slave address for the configuration register is 1001_{BIN}, and a collision will occur on the I^2C bus.

2048 Table03 3.1

Table 3. Configuration Register

PROGRAMMING CONNECTION

HARDWARE

The end user can use the summit SMX3200 programming cable and software that have been developed to operate with a standard personal computer. The programming cable interfaces directly between a PC's parallel port and the target application. The application's values are entered via an intuitive graphical user interface employing drop-down menus.

After the desired settings for the application are determined the software will generate a hex file that can be transferred to the target device or downloaded to Summit. If it is downloaded to Summit a customer part number will be assigned and the file will be used to customize the devices during the final electrical test operations.

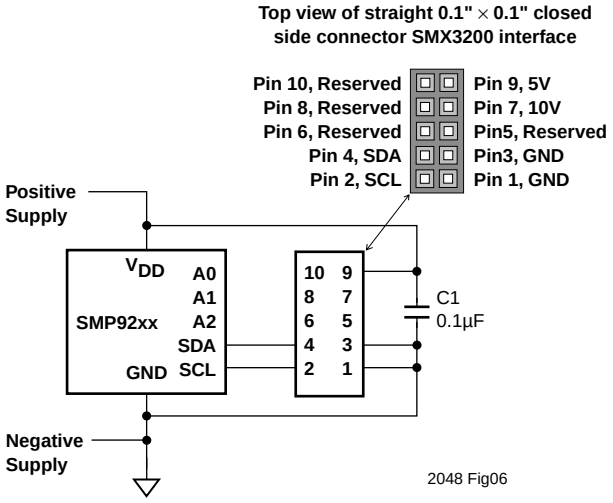
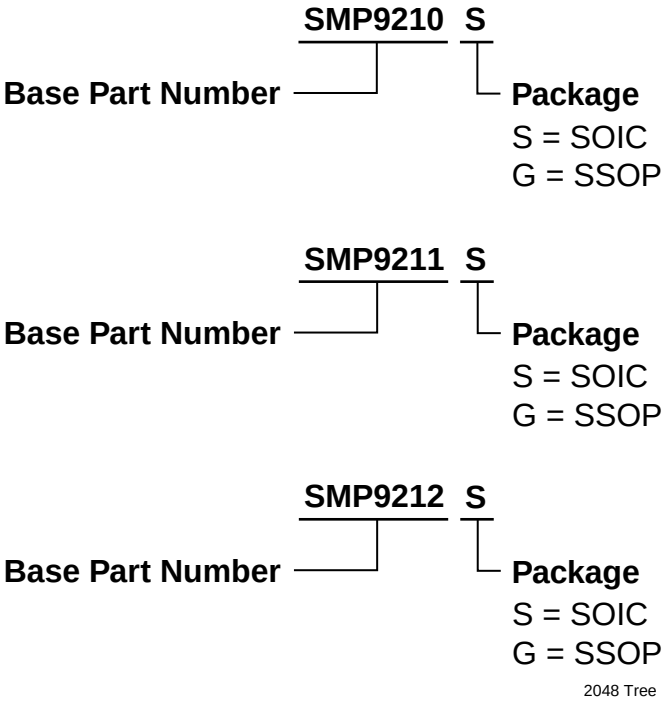


Figure 6. Programming Connection

ORDERING INFORMATION

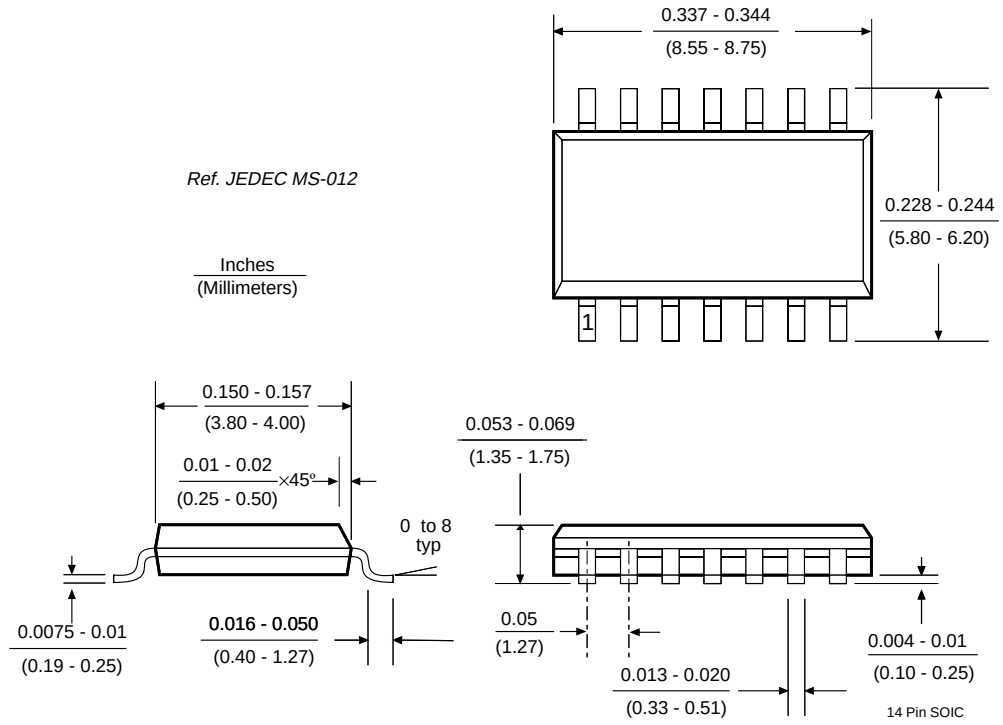


PACKAGES

14 PIN SOIC PACKAGE

Ref. JEDEC MS-012

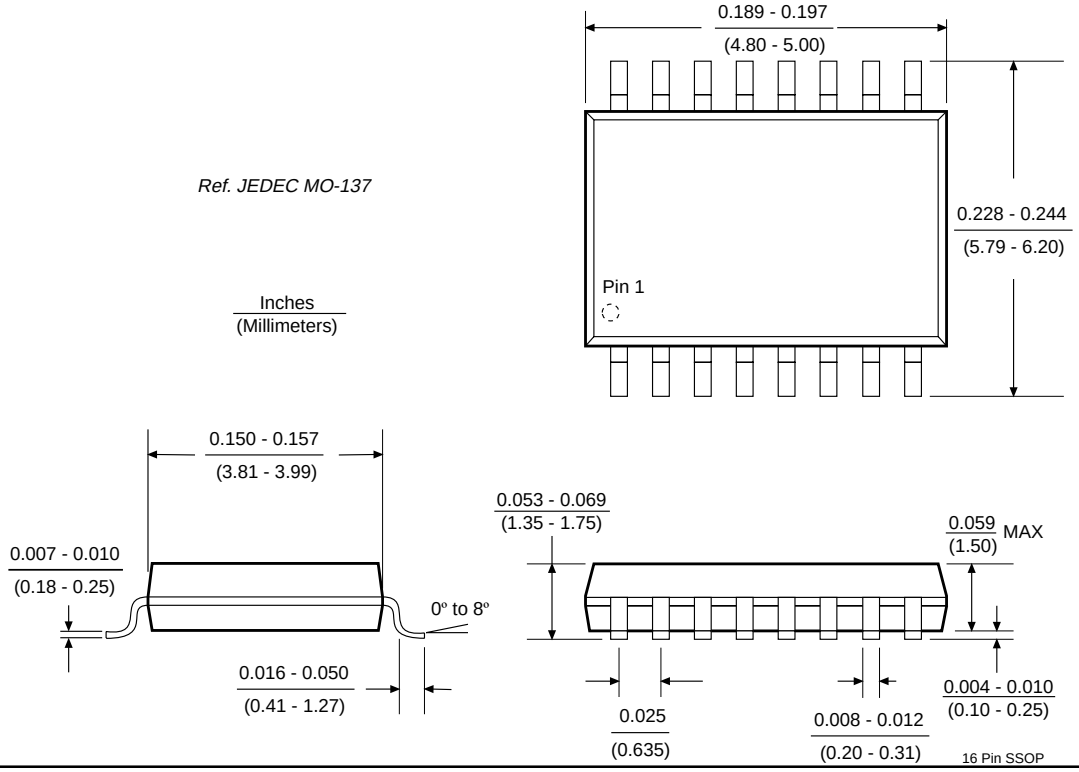
Inches
(Millimeters)



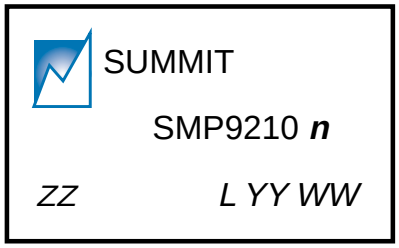
16 PIN SSOP PACKAGE

Ref. JEDEC MO-137

Inches
(Millimeters)



PART MARKING



n = Package type (P or S)
L = Lot number
YY = Year
WW = Work Week
9210: *ZZ* = blank
9211: *ZZ* = 11
9212: *ZZ* = 12

This Document supersedes all previous versions.