SL28EB742

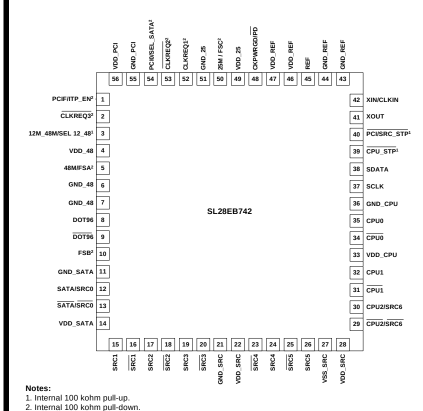
INTEL® CEDARVIEW EMBEDDED CLOCK GENERATOR

Features

- Low power push-pull type differential output buffers
- No termination resistors required on differential clocks
- 3-bits slew rate control on single-ended clocks
- Differential CPU clocks with pins selectable frequency
- 100 MHz Differential SRC clocks
- Selectable Differential SATA or SRC clock
- 96 MHz Differential DOT clock
- 48 MHz USB clock
- Selectable 12 or 48 MHz clock
- 25 MHz clock
- Buffered Reference Clock 14.318 MHz
- 14.318 MHz Crystal Input or Clock input
- I^2C support with readback capabilities
- Triangular Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- Extended Temperature: –40 to 85 °C
- 3.3 V power supply
- 56-pin QFN package

Ordering Information:
See page 37

Pin Assignments



Patents pending

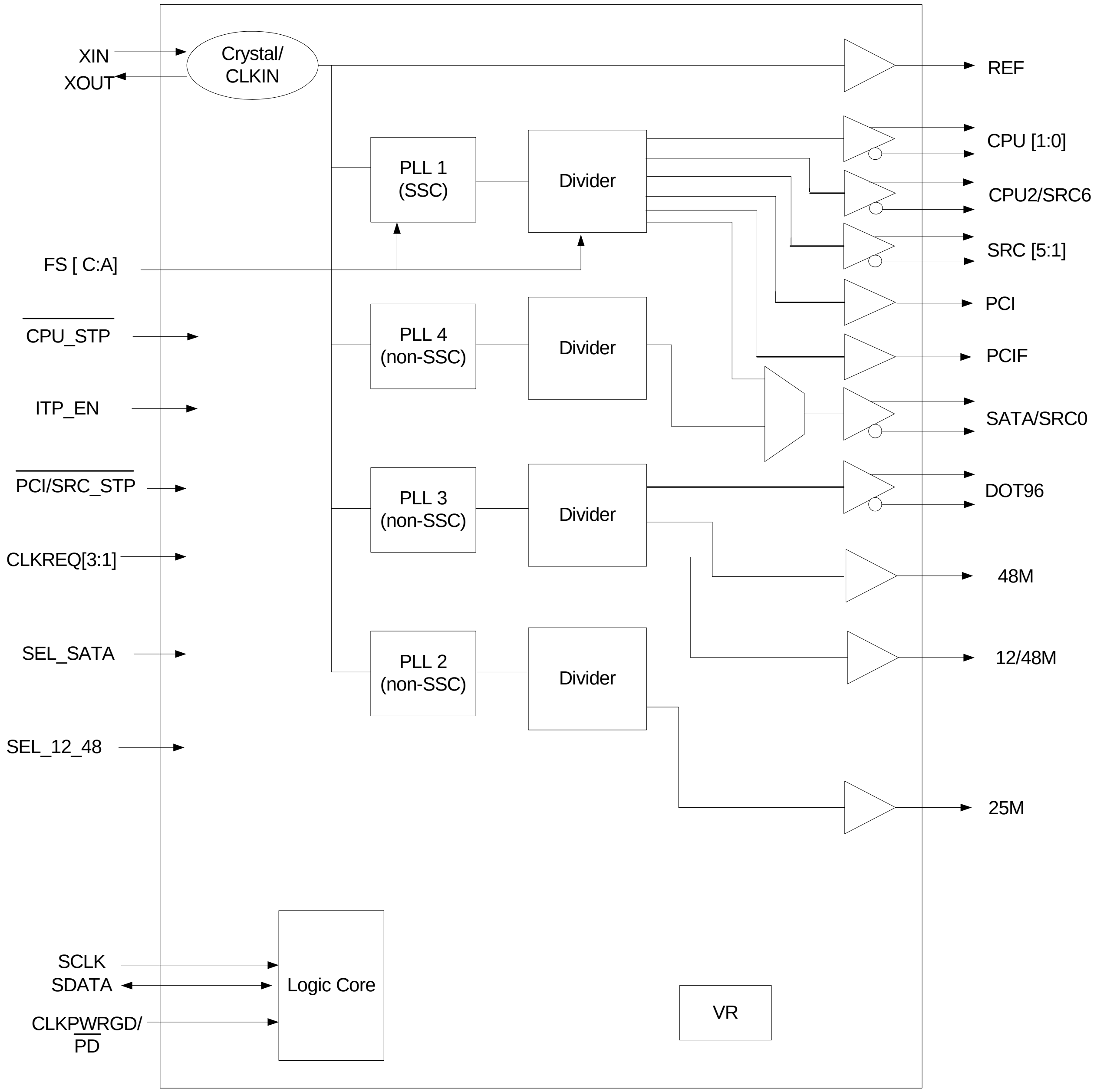
Selectable Differential SRC or CPU Clock

CPU	CPU/ SRC	SRC	SATA/ SRC	DOT96	48M	48M/ 12M	33M	25M	14.318M
x2	x1	x5	x 1	x1	x1/2	x1	x2	x1	x1

Description

The SL28EB742 is a high-performance clock generator for supporting Intel Cedarview platforms. The SL28EB742 is rated to support extended grade temperature. Utilizing an inexpensive 14.318 MHz crystal, it is capable of supporting multiple frequencies from four PLLs. The CPU clock can support a frequency range from 83.33 to 166 MHz by configuration of two strap pins. With a combination of strap pins and an I^2C, the device allows maximum configurability.

Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

(VDD = 3.3 V, T_A = 25 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage (extended)	$VDD_{(extended)}$	3.3 V ±5%	3.13	3.3	3.46	V
Supply Voltage (commercial)	$VDD_{(commercial)}$	3.3 V ±10%	2.97	3.3	3.63	V

Table 2. DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Max	Unit
3.3 V Input High Voltage (SE)	V_{IH}		2.0	V_{DD} + 0.3	V
3.3 V Input Low Voltage (SE)	V_{IL}		V_{SS} – 0.3	0.8	V
Input High Voltage	V_{IHI2C}	SDATA, SCLK	2.2	—	V
Input Low Voltage	V_{ILI2C}	SDATA, SCLK	—	1.0	V
FS Input High Voltage	V_{IH_FS}		0.7	V_{DD}+ 0.3	V
FS Input Low Voltage	V_{IL_FS}		V_{SS} – 0.3	0.35	V
Input High Leakage Current	I_{IH}	Except internal pull-down resistors, $0 < V_{IN} < V_{DD}$	—	5	µA
Input Low Leakage Current	I_{IL}	Except internal pull-up resistors, $0 < V_{IN} < V_{DD}$	–5	—	µA
3.3 V Output High Voltage (SE)	V_{OH}	I_{OH} = –1 mA	2.4	—	V
3.3 V Output Low Voltage (SE)	V_{OL}	I_{OL} = 1 mA	h	0.4	V
High-impedance Output Current	I_{OZ}		–10	10	µA
Input Pin Capacitance	C_{IN}		1.5	5	pF
Output Pin Capacitance	C_{OUT}			6	pF
Pin Inductance	L_{IN}		—	7	nH
Power Down Current	$IDD_{\_PD}$		—	1	mA
Dynamic Supply Current	$I_{DD\_3.3 V}$	All outputs enabled. SE clocks with 5” traces and 4 pF load. Differential clocks with 5” traces and 2 pF load.	—	120	mA

Table 3. AC Electrical Specifications

Parameter	Symbol	Condition	Min	Max	Unit
Crystal					
Long-term Accuracy	L_{ACC}	Measured at V_{DD}/2 differential	—	250	ppm
Clock Input					
CLKIN Duty Cycle	T_{DC}	Measured at VV_{DD}/2	47	53	%
CLKIN Rising/Falling Slew Rate	T_R/T_F	Measured between 0.2 V_{DD} and 0.8 V_{DD}	0.5	4.0	V/ns
CLKIN Cycle to Cycle Jitter	T_{CCJ}	Measured at V_{DD}/2	—	250	ps
CLKIN Long Term Jitter	T_{LTJ}	Measured at V_{DD}2	—	350	ps
Input High Voltage	V_{IH}	XIN / CLKIN pin	2	V_{DD}+0.3	V
Input Low Voltage	V_{IL}	XIN / CLKIN pin	—	0.8	V
Input High Current	I_{IH}	XIN / CLKIN pin, VIN = V_{DD}	—	35	µA
Input Low Current	I_{IL}	XIN / CLKIN pin, 0 < VIN <0.8	-35	–	µA
CPU at 0.7 V					
Duty Cycle	T_{DC}	Measured at 0 V differential	45	55	%
Cycle to Cycle Jitter	T_{CCJ}	Measured at 0 V differential	—	85	ps
Cycle to Cycle Jitter for CPU 2	$T_{CCJ\ (CPU2)}$	Measured at 0 V differential	—	125	ps
CPU0 to CPU1 Skew	T_{skew}	Measured at 0 V differential	—	100	ps
Long-term Accuracy	L_{ACC}	Measured at 0 V differential	—	100	ppm
Rising/Falling Slew Rate	T_R / T_F	Measured differentially from ±150 mV	2.5	8	V/ns
Rise/Fall Matching	T_{RFM}	Measured single-endedly from ±75 mV	—	20	%
Voltage High	V_{HIGH}			1.15	V
Voltage Low	V_{LOW}		–0.3	—	V
Crossing Point Voltage at 0.7 V Swing	V_{OX}		300	550	mV
SRC at 0.7 V					
Duty Cycle	T_{DC}	Measured at 0 V differential	45	55	%
Any SRC Clock Skew from the Earliest Bank to the Latest Bank	T_{SKEW}	Measured at 0 V differential	—	3.0	ns
Cycle to Cycle Jitter	T_{CCJ}	Measured at 0 V differential	—	85	ps
Long Term Accuracy	L_{ACC}	Measured at 0 V differential	—	100	ppm
Rising/Falling Slew Rate	T_R / T_F	Measured differentially from ±150 mV	2.5	8	V/ns
Rise/Fall Matching	T_{RFM}	Measured single-endedly from ±75 mV	—	20	%
Voltage High	V_{HIGH}			1.15	V

Table 3. AC Electrical Specifications (Continued)

Parameter	Symbol	Condition	Min	Max	Unit
Voltage Low	V_{LOW}		–0.3	—	V
Crossing Point Voltage at 0.7 V Swing	V_{OX}		300	550	mV
DOT96 at 0.7 V					
Duty Cycle	T_{DC}	Measured at 0 V differential	45	55	%
Cycle to Cycle Jitter	T_{CCJ}	Measured at 0 V differential at 1 clock	—	250	ps
Long Term Accuracy	L_{ACC}	Measured at 0 V differential at 1 clock	—	100	ppm
Rising/Falling Slew Rate	T_R / T_F	Measured differentially from ±150 mV	2.5	8	V/ns
Rise/Fall Matching	T_{RFM}	Measured single-endedly from ±75 mV	—	20	%
Voltage High	V_{HIGH}			1.15	V
Voltage Low	V_{LOW}		–0.3	—	V
Crossing Point Voltage at 0.7 V Swing	V_{OX}		300	550	mV
SATA at 0.7 V					
Duty Cycle	T_{DC}	Measured at 0 V differential	45	55	%
Cycle to Cycle Jitter	T_{CCJ}	Measured at 0 V differential at 1 clock	–	125	ps
Long Term Accuracy	L_{ACC}	Measured at 0 V differential at 1 clock	–	100	ppm
Rising/Falling Slew Rate	T_R / T_F	Measured differentially from ±150 mV	2.5	8	V/ns
Rise/Fall Matching	T_{RFM}	Measured single-endedly from ±75 mV	—	20	%
Voltage High	V_{HIGH}			1.15	V
Voltage Low	V_{LOW}		–0.3	—	V
Crossing Point Voltage at 0.7 V Swing	V_{OX}		300	550	mV
PCI/PCIF at 3.3 V					
Duty Cycle	T_{DC}	Measurement at 1.5 V	45	55	%
Rising/Falling Slew Rate	T_R / T_F	Measured between 0.8 V and 2.0 V	1.0	4.0	V/ns
Any PCI Clock to Any PCI Clock Skew	T_{SKEW}	Measurement at 1.5V	—	1000	ps
48M, 12_48M at 3.3 V					
Duty Cycle	T_{DC}	Measurement at 1.5 V	45	55	%
Rising/Falling Slew Rate	T_R / T_F (48M)	Measured between 0.8 V and 2.0 V	1.0	2.0	V/ns
Rising/Falling Slew Rate	T_R / T_F (12_48M)	Measured between 0.8 V and 2.0 V	1.0	2.0	V/ns
Cycle to Cycle Jitter	T_{CCJ}	Measurement at 1.5 V	—	300	ps

Table 3. AC Electrical Specifications (Continued)

Parameter	Symbol	Condition	Min	Max	Unit
48M Long Term Accuracy	L_{ACC}	Measurement at 1.5 V	—	100	ppm
25M at 3.3 V					
Duty Cycle	T_{DC}	Measurement at 1.5 V	45	55	%
Rising/Falling Slew Rate	T_R / T_F	Measured between 0.8 V and 2.0 V	1.0	4.0	V/ns
Cycle to Cycle Jitter	T_{CCJ}	Measurement at 1.5 V	—	300	ps
Long Term Accuracy	L_{ACC}	Measured at 1.5 V	—	100	ppm
14.318M at 3.3 V					
Duty Cycle	T_{DC}	Measurement at 1.5 V	45	55	%
Rising/Falling Slew Rate	T_R / T_F	Measured between 0.8 V and 2.0 V	1.0	4.0	V/ns
Cycle to Cycle Jitter	T_{CCJ}	Measurement at 1.5 V	—	500	ps
Long Term Accuracy	L_{ACC}	Measurement at 1.5 V	—	100	ppm
Enable/Disable and Set-Up					
Clock Stabilization from Powerup	T_{STABLE}		—	1.8	ms
Stopclock Set-up Time	T_{SS}		10.0	—	ns

Table 4. Thermal Conditions

Parameter	Symbol	Condition	Min	Max	Unit
Temperature, Storage	T_S	Non-functional	–65	150	°C
Temperature, Operating Ambient, Extended	T_A	Functional	–40	85	°C
Temperature, Operating Ambient, Commercial	T_A	Functional	0	70	°C
Temperature, Junction	T_J	Functional	—	150	°C
Dissipation, Junction to Case	$Ø_{JC}$	JEDEC (JESD 51)	—	20	°C/W
Dissipation, Junction to Ambient	$Ø_{JA}$	JEDEC (JESD 51)	—	60	°C/W
Note: For multiple supplies, the voltage on any input or I/O pin cannot exceed the power pin during powerup. Power supply sequencing is not required.					

Table 5. Absolute Maximum Limits

Parameter	Symbol	Condition	Min	Max	Unit
Main Supply Voltage	$V_{DD\_3.3V}$	Functional	—	4.6	V
Input Voltage	V_{IN}	Relative to V_{SS}	–0.5	4.6	V_{DC}
ESD Protection (Human Body Model)	ESD_{HBM}	JEDEC (JESD 22 - A114)	2000	—	V
Flammability Rating	UL-94	UL (Class)	V–0		
Note: For multiple supplies, the voltage on any input or I/O pin cannot exceed the power pin during powerup. Power supply sequencing is not required.					

2. Functional Description

2.1. Powerdown (PD) Clarification

The CKPWRGD/PD pin is a dual-function pin. During initial powerup, the pin functions as CKPWRGD. Once CKPWRGD has been sampled high by the clock chip, the pin assumes PD functionality. The PD pin is an asynchronous active low input used to shut off all clocks cleanly before shutting off power to the device. This signal is synchronized internally to the device before powering down the clock synthesizer. PD is also an asynchronous input for powering up the system. When PD is asserted low, clocks are driven to a low value and held before turning off the VCOs and the crystal oscillator.

2.2. Powerdown (PD) Assertion

When PD is sampled low by two consecutive rising edges of CPUC, all single-ended outputs clocks will be held low on their next high-to-low transition and differential clocks will be held low. When powerdown mode is desired as the initial power on state, PD must be asserted low in less than 10 µs after asserting CKPWRGD.

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Table 6. Output Driver Status during CPU_STP and PCIS_STP

		CPU_STP Asserted	**PCI_STP Asserted**	**CLKREQ Asserted**	**I^2C OE Disabled**
Single-ended Clocks	Stoppable	Running	Driven low	Running	Driven low
	Non-stoppable	Running	Running	Running	
Differential Clocks	Stoppable	Clock driven high	Clock driven high	Clock driven low	Clock driven low
		Clock driven low	Clock driven low	Clock driven low	
	Non-stoppable	Running	Running	Running	

Table 7. Output Driver Status

	All Single-ended Clocks		**All Differential Clocks**	
	w/o Strap	**w/ Strap**	**Clock**	**Clock#**
PD = 0 (Powerdown)	Low	Hi-z	Low	Low

2.3. Powerdown ($\overline{PD}$) Deassertion

The powerup latency is less than 1.8 ms. This is the time from the deassertion of the $\overline{PD}$ pin or the ramping of the power supply until the time that stable clocks are generated from the clock chip. All differential outputs stopped in a three-state condition resulting from powerdown are driven high in less than 300 µs of $\overline{PD}$ deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs are enabled within a few clock cycles of each clock. Figure 2 is an example showing the relationship of clocks coming up.

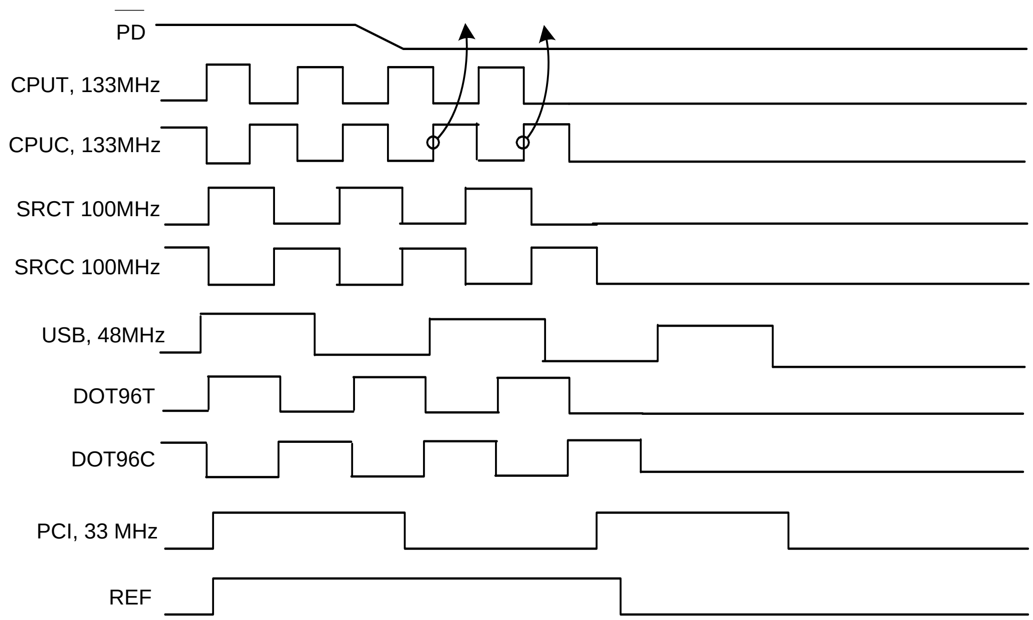


Figure 1. Powerdown Assertion Timing Waveform

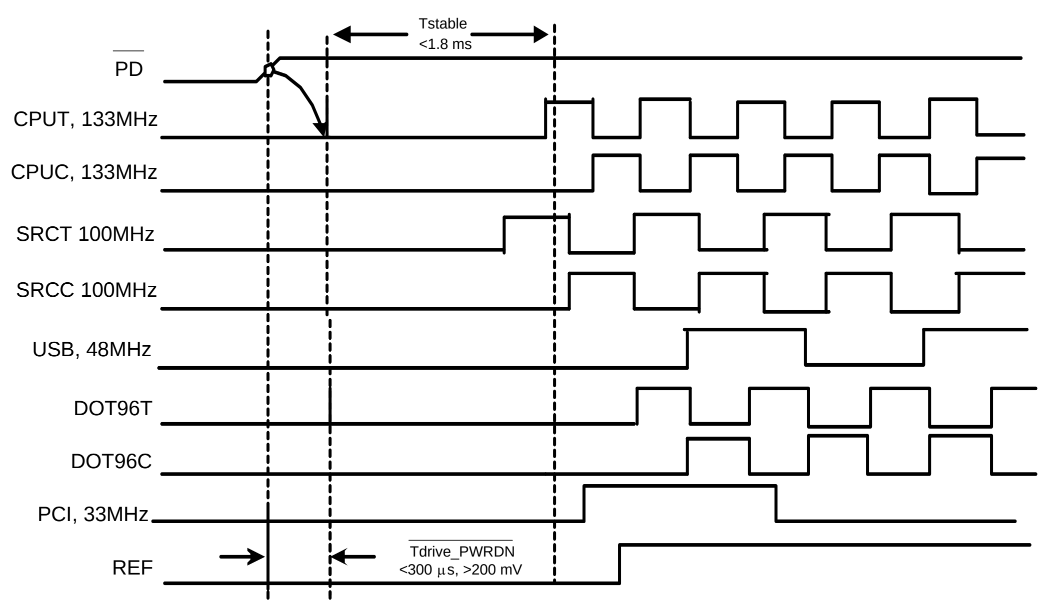


Figure 2. Powerdown Deassertion Timing Waveform

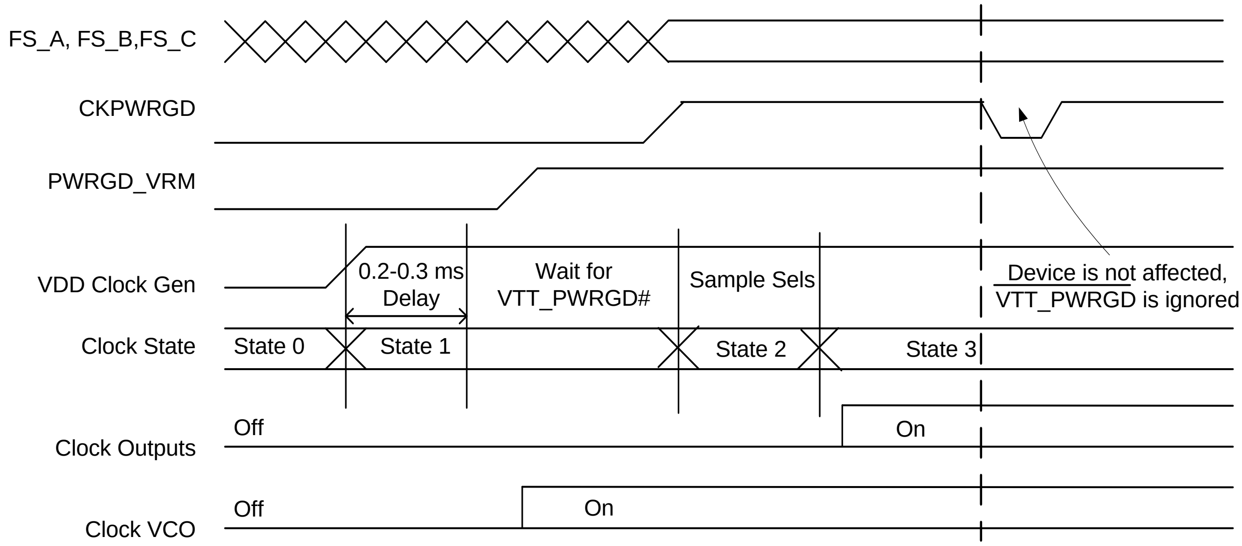


Figure 3. CKPWRGD Timing Diagram

2.4. CPU_STP Assertion

The CPU_STP signal is an active LOW input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function. When the CPU_STP pin is asserted, all CPU outputs that are set with the I^2C configuration to be stoppable are stopped within two to six CPU clock periods after being sampled by two rising edges of the internal CPUC clock. The final states of the stopped CPU signals are CPUT = High and CPUC = Low.

2.5. CPU_STP Deassertion

The deassertion of the CPU_STP signal causes all stopped CPU outputs to resume normal operation in a synchronous manner. No short or stretched clock pulses are produced when the clock resumes. The maximum latency from the deassertion to active outputs is no more than two CPU clock cycles.

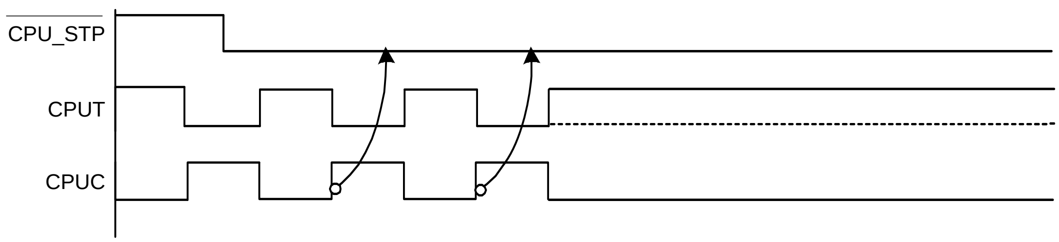


Figure 4. CPU_STP Assertion Waveform

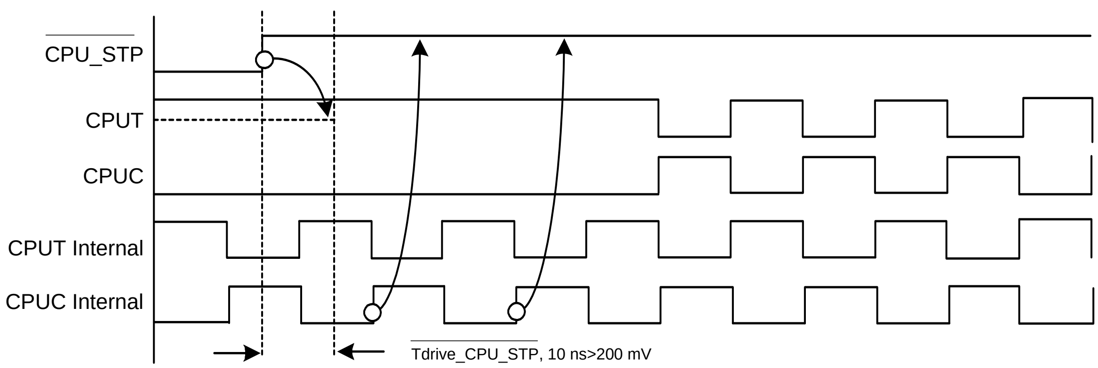


Figure 5. CPU_STP Deassertion Waveform

2.6. PCI/SRC_STP Assertion

The PCI/SRC_STP signal is an active low input used for synchronously stopping and starting the PCI outputs while the rest of the clock generator continues to function. The set-up time for capturing PCI/SRC_STP going low is 10 ns (t_{SU}) (refer to Figure 6). The PCIF and SRC clocks are affected by the PCI/SRC pin if their corresponding control bit in the I^2C register is set to allow them to be free running. For SRC clocks assertion description, refer to the CPU_STP descriptions in Section 2.4 and Section 2.5.

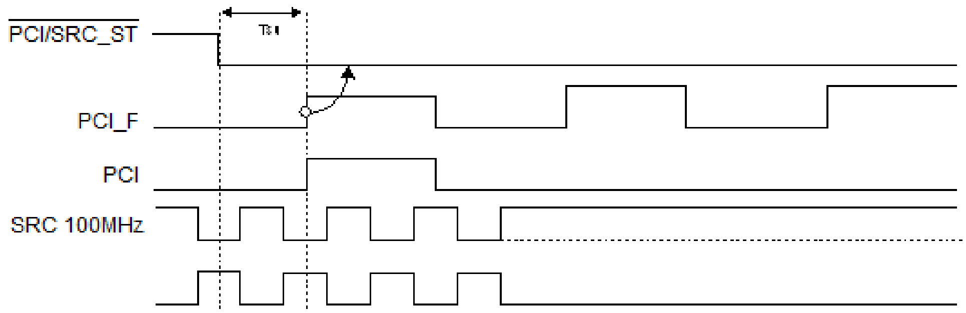


Figure 6. PCI/SRC_STP Assertion Waveform

2.7. PCI/SRC_STP Deassertion

The deassertion of the PCI/SRC_STP signal causes all PCI and stoppable PCIF to resume running in a synchronous manner within two PCI clock periods and after PCI/SRC_STP transitions to a high level. Similarly, PCI/SRC_STP deassertion will cause stoppable SRC clocks to resume running. For an SRC clocks deassertion description, refer to the CPU_STP description Section 2.4 and Section 2.5.

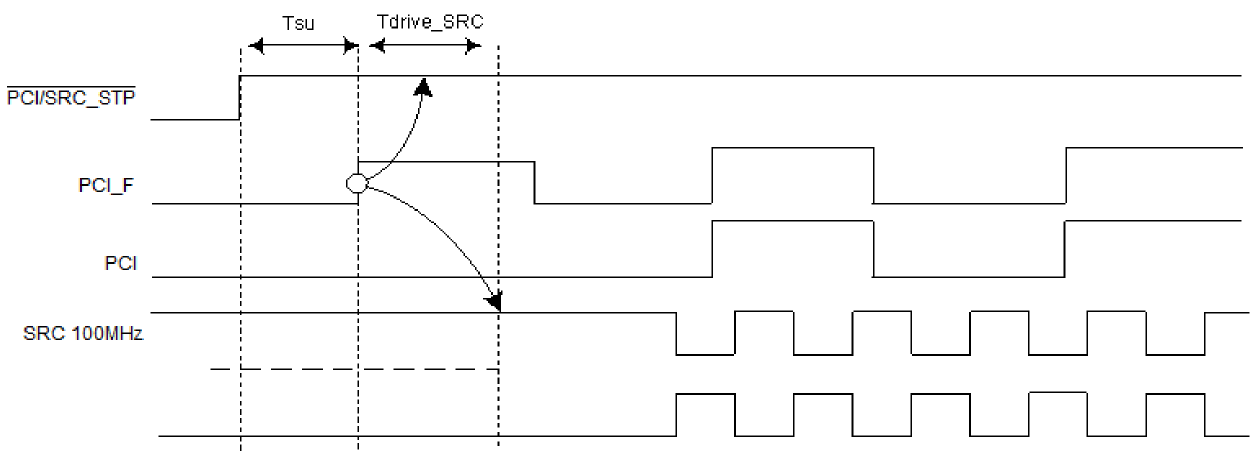


Figure 7. PCI/SRC_STP Deassertion Waveform

3. Test and Measurement Setup

3.1. Single-ended Clocks

Figure 8 shows the test load configuration for the single-ended output signals.

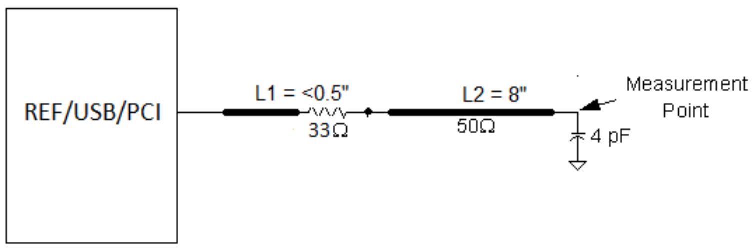


Figure 8. Single-ended Clocks Single Load Configuration

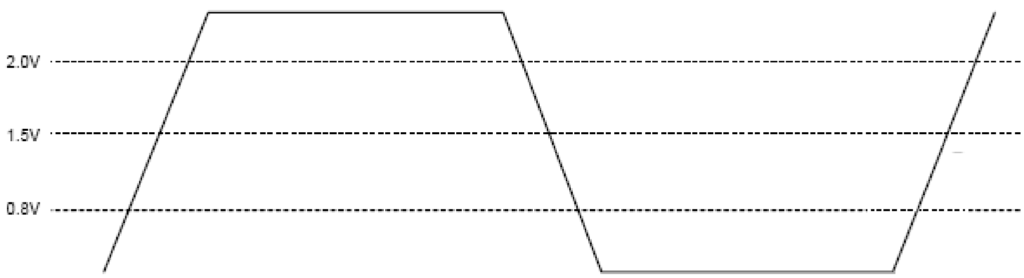


Figure 9. Single-ended Output Signals (for AC Parameters Measurement)

3.2. Differential Clock Signals

Figure 10 shows the test load configuration for the differential clock signals.

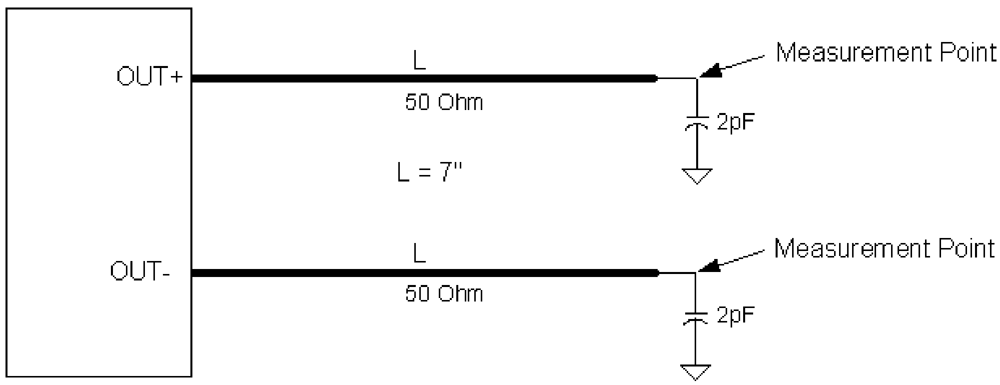


Figure 10. 0.7 V Differential Load Configuration

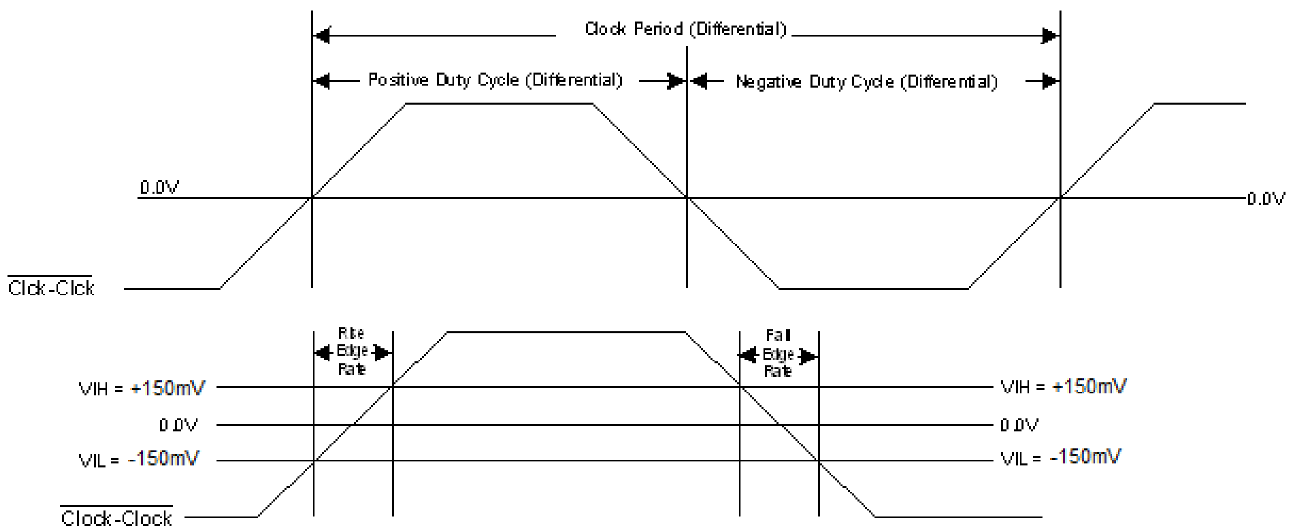


Figure 11. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)

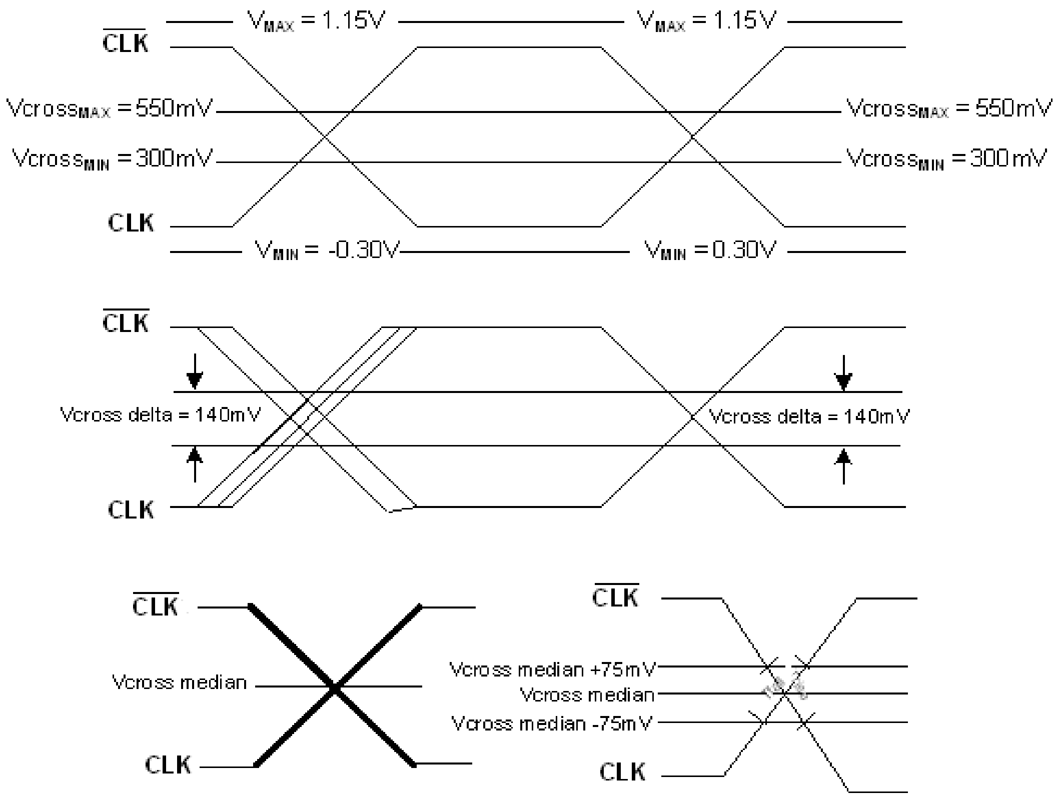


Figure 12. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

4. Control Registers

4.1. Frequency Select Pin FS

Apply the appropriate logic levels to FS inputs before CKPWRGD assertion to achieve host clock frequency selection. When the clock chip sampled HIGH on CKPWRGD and indicates that VTT voltage is stable, then FS input values are sampled. This process employs a one-shot functionality and, once the CKPWRGD samples a valid HIGH, all other FS and CKPWRGD transitions are ignored except in test mode.

Table 8. Frequency Select Pin (FS)

SEL_SATA	FSC	FSB	FSA	CPU	SRC	SATA	PCI
0	0	0	0	100.00	100.00	100.00	33.33
0	0	0	1	100.00	100.00	100.00	33.33
0	0	1	0	83.33	100.00	100.00	33.33
0	0	1	1	83.33	100.00	100.00	33.33
0	1	0	0	133.33	100.00	100.00	33.33
0	1	0	1	133.33	100.00	100.00	33.33
0	1	1	0	166.67	100.00	100.00	33.33
0	1	1	1	166.67	100.00	100.00	33.33
1	0	0	0	100.00	100.00	100.00	33.33
1	0	0	1	100.00	100.00	100.00	33.33
1	0	1	0	83.33	100.00	100.00	33.33
1	0	1	1	83.33	100.00	100.00	33.33
1	1	0	0	133.33	100.00	100.00	33.33
1	1	0	1	133.33	100.00	100.00	33.33
1	1	1	0	166.67	100.00	100.00	33.33
1	1	1	1	166.67	100.00	100.00	33.33

4.2. I^{2}C Interface

To enhance the flexibility and function of the clock synthesizer, an I^{2}C interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, are individually enabled or disabled. The registers associated with the I^{2}C interface initialize to their default setting at powerup. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required.

4.3. Data Protocol

The clock I^{2}C serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes.

The block write and block read protocol is outlined in Table 10, while Table 11 outlines byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 9. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation.
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'.

Table 10. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count–8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address–7 bits
36:29	Data byte 1–8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2–8 bits	37:30	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave–8 bits
....	Data Byte N–8 bits	47	Acknowledge

Table 10. Block Read and Block Write Protocol (Continued)

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
....	Acknowledge from slave	55:48	Data byte 2 from slave–8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave / Acknowledge
		....	Data Byte N from slave–8 bits
		....	NOT Acknowledge
		....	Stop

Table 11. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

Control Register 0. Byte 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			Spread Enable	SEL_SATA		FSC	FSB	FSA
Type	R/W	R/W	R/W	R	R/W	R	R	R

Reset settings = 000x0xxx

Bit	Name	Function
7:6	Reserved	
5	Spread Enable	Enable spread for CPU/SRC/PCI outputs 0 = Disable, 1 = –0.5%
4	SEL_SATA	See Table 9 for SATA/SRC selection.
3	Reserved	
2	FSC	See Table 9 for CPU Frequency Selection Table.
1	FSB	
0	FSA	

Register 1. Byte 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DOT96_OE	SATA/ SRC0_OE	CPU2/ SRC6_OE	SRC2	SRC1			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 1111110

Bit	Name	Function
7	DOT96_OE	**Output enable for DOT96.** 0 = Output Disabled, 1 = Output Enabled
6	SATA/SRC0_OE	**Output enable for SATA/SRC0.** 0 = Output Disabled, 1 = Output Enabled
5	CPU2/SRC6_OE	**Output enable for CPU2/SRC6.** 0 = Output Disabled, 1 = Output Enabled
4	SRC2	**Output enable for SRC2.** 0 = Output Disabled, 1 = Output Enabled
3	SRC1	**Output enable for SRC1.** 0 = Output Disabled, 1 = Output Enabled
2:0	Reserved	

Register 2. Byte 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	48M_OE		25M_OE	REF_OE	12_48M_OE	PCI0_OE	PCIF_OE	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 10111110

Bit	Name	Function
7	48M_OE	**Output Enable for DIFF2.** 0: Output disabled. 1: Output enabled.
6	Reserved	
5	25M_OE	**Output ENABLE for 25M.** 0 = Output Disabled, 1 = Output Enabled
4	REF_OE	**Output Enable for REF.** 0 = Output Disabled, 1 = Output Enabled
3	12_48M_OE	**Output Enable for 12_48M.** 0 = Output Disabled, 1 = Output Enabled
2	PCI0_OE	**Output Enable for PCI0.** 0 = Output Disabled, 1 = Output Enabled
1	PCIF_OE	**Output Enable for PCIF.** 0 = Output Disabled, 1 = Output Enabled
0	Reserved	

Register 3. Byte 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CPU1_OE	CPU0_OE	CLKREQ#_3	CLKREQ#_3	CLKREQ#_2	CLKREQ#_2	CLKREQ#_1	CLKREQ#_1
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 1100000

Bit	Name	Function
7	CPU1_OE	**Output Enable for CPU1.** 0 = Output Disabled, 1 = Output Enabled
6	CPU0_OE	**Output Enable for CPU0.** 0 = Output Disabled, 1 = Output Enabled
5	CLKREQ#_3	**Clock Request for SRC2.** 0 = Not controlled, 1 = Controlled
4	CLKREQ#_3	**Clock Request for SRC6 (does not apply to CPU clock).** 0 = Not controlled, 1 = Controlled
3	CLKREQ#_2	**Clock Request for SRC2.** 0 = Not controlled, 1 = Controlled
2	CLKREQ#_2	**Clock Request for SATA75M/SRC0.** 0 = Not controlled, 1 = Controlled
1	CLKREQ#_1	**Clock Request for SRC1.** 0 = Not controlled, 1 = Controlled
0	CLKREQ#_1	**Clock Request for SATA75M/SRC0.** 0 = Not controlled, 1 = Controlled

Register 4. Byte 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		CPU1	12_48M	CPU2	ITP_EN		CPU0	
Type	R/W	R/W	R	R/W	R	R/W	R/W	R/W

Reset settings = 00x0x000

Bit	Name	Function
7	Reserved	
6	CPU1	**CPU1 Free Run Control.** 0 = Free Running, 1 = Stoppable
5	12_48M	**Selectable 12_48M Status.** 0 = 48M, 1 = 12M
4	CPU2	**CPU2 Free Run Control.** 0 = Free Running, 1 = Stoppable
3	ITP_EN	**Selectable CPUe_ITP/ SRC6 Status.** 0 = SRC6, 1 = CPU2
2	Reserved	
1	CPU0	**CPU0 Free Run Control.** 0 = Free Running, 1 = Stoppable
0	Reserved	

Control Register 5. Byte 5

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				SATA75/SRC0	SRC6	SRC2	SRC1	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00010000

Bit	Name	Function
7:5	Reserved	
4	SATA75/SRC0	**SATA75/SRC0 Free Run Control.** 0 = Free Running, 1 = Stoppable
3	SRC6	**SRC6 Free Run Control.** 0 = Free Running, 1 = Stoppable
2	SRC2	**SRC2 Free Run Control.** 0 = Free Running, 1 = Stoppable
1	SRC1	**SRC1 Free Run Control.** 0 = Free Running, 1 = Stoppable
0	Reserved	

Control Register 6. Byte 6

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CPU_AMP		SRC_AMP		DOT96_AMP		SATA_AMP	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 01010101

Bit	Name	Function
7:6	CPU_AMP	**CPU Amplitude Adjustment.** 00 = 70 0mV, 01 = 800 mV, 10 = 900 mV, 11 = 1000 mV
5:4	SRC_AMP	**SRC Amplitude Adjustment.** 00 = 70 0mV, 01 = 800 mV, 10 = 900 mV, 11 = 1000 mV
3:2	DOT96_AMP	**DOT96 Amplitude Adjustment.** 00 = 70 0mV, 01 = 800 mV, 10 = 900 mV, 11 = 1000 mV
1:0	SATA_AMP	**SATA75/SRC0 Amplitude Adjustment.** 00 = 70 0mV, 01 = 800 mV, 10 = 900 mV, 11 = 1000 mV

Control Register 7. Byte 7

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Rev Code Bit 3	Rev Code Bit 2	Rev Code Bit 1	Rev Code Bit 0	Vendor ID Bit 3	Vendor ID Bit 2	Vendor ID Bit 1	Vendor ID Bit 0
Type	R	R	R	R	R	R	R	R

Reset settings = 00011000

Bit	Name	Function
7	Rev Code Bit 3	Revision Code Bit 3
6	Rev Code Bit 2	Revision Code Bit 2
5	Rev Code Bit 1	Revision Code Bit 1
4	Rev Code Bit 0	Revision Code Bit 0
3	Vendor ID Bit 3	Vendor ID Bit 3
2	Vendor ID Bit 2	Vendor ID Bit 2
1	Vendor ID Bit 1	Vendor ID Bit 1
0	Vendor ID Bit 0	Vendor ID Bit 0

Control Register 8. Byte 8

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00001111

Bit	Name	Function
7	BC7	Byte count register for block read operation. The default value for Byte count is 15. In order to read beyond Byte 15, the user should change the byte count limit to or beyond the byte that is desired to be read.
6	BC6	
5	BC5	
4	BC4	
3	BC3	
2	BC2	
1	BC1	
0	BC0	

Control Register 9. Byte 9

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SRC5	SRC4	SRC3	SRC5	SRC4	SRC3	PCI0	PCIF
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 11100001

Bit	Name	Function
7	SRC5	**Output Enable for SRC5.** 0 = Output Disabled, 1 = Output Enabled
6	SRC4	**Output Enable for SRC4.** 0 = Output Disabled, 1 = Output Enabled
5	SRC3	**Output Enable for SRC3.** 0 = Output Disabled, 1 = Output Enabled
4	SRC5	**SRC5 Free Run Control.** 0 = Free Running, 1 = Stoppable
3	SRC4	**SRC4 Free Run Control.** 0 = Free Running, 1 = Stoppable
2	SRC3	**SRC3 Free Run Control.** 0 = Free Running, 1 = Stoppable
1	PCI0	**PCI0 Free Run Control.** 0 = Free Running, 1 = Stoppable
0	PCIF	**PCIF Free Run Control.** 0 = Free Running, 1 = Stoppable

Control Register 10. Byte 10

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00000000

Bit	Name	Function
7:0	Reserved	

Control Register 11. Byte 11

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	14M_Bit2	14M_Bit1	14M_Bit0	25M_Bit2	25M_Bit1	25M_Bit0	12_48M_ Bit2	12_48M_ Bit0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 10110111

Bit	Name	Function
7	14M_Bit2	Drive Strength Control - Bit[2:0] Normal mode default '101' Wireless Friendly Mode default to '111' ,
6	14M_Bit1	
5	14M_Bit0	
4	25M_Bit2	
3	25M_Bit1	
2	25M_Bit0	
1	12_48M_Bit2	
0	12_48M_Bit0	

Mode	Bit2	Bit1	Bit0	Buffer Strength
	0	0	0	Strong
	0	0	1	
	0	1	0	
	0	1	1	
	1	0	0	
Default	1	0	1	
	1	1	0	
Wireless Friendly	1	1	1	Weak

Control Register 12. Byte 12

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	48M_Bit2	48M_Bit1	48M_Bit0	PCI0_Bit2	PCI0_Bit1	PCI0_Bit0		12_48M_Bit1
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 10110100

Bit	Name	Function
7	48M_Bit2	Drive Strength Control - Bit[2:0] Normal mode default '101' Wireless Friendly Mode default to '111' ,
6	48M_Bit1	
5	48M_Bit0	
4	PCI0_Bit2	
3	PCI0_Bit1	
2	PCI0_Bit0	
1	Reserved	
0	12_48M_Bit1	

Mode	Bit2	Bit1	Bit0	Buffer Strength
	0	0	0	Strong
	0	0	1	↓
	0	1	0	
	0	1	1	
	1	0	0	
Default	1	0	1	
	1	1	0	
Wireless Friendly	1	1	1	Weak

Control Register 13. Byte 13

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PCIF_Bit2	PCIF_Bit1	PCIF_Bit0					Wireless Friendly Mode
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 10100000

Bit	Name	Function
7	PCIF_Bit2	Drive Strength Control—Bit[2:0] Normal mode default 101 Wireless Friendly Mode default to ‘111’ ’
6	PCIF_Bit1	
5	PCIF_Bit0	
4:1	Reserved	
0	Wireless Friendly Mode	**Wireless Friendly Mode.** 0 = Disabled, Default all single-ended clocks slew rate config bits to 101 1 = Enabled, Default all single-ended clocks slew rate config bits to 111

Mode	Bit2	Bit1	Bit0	Buffer Strength
	0	0	0	Strong
	0	0	1	↓
	0	1	0	
	0	1	1	
	1	0	0	
Default	1	0	1	
	1	1	0	
Wireless Friendly	1	1	1	Weak

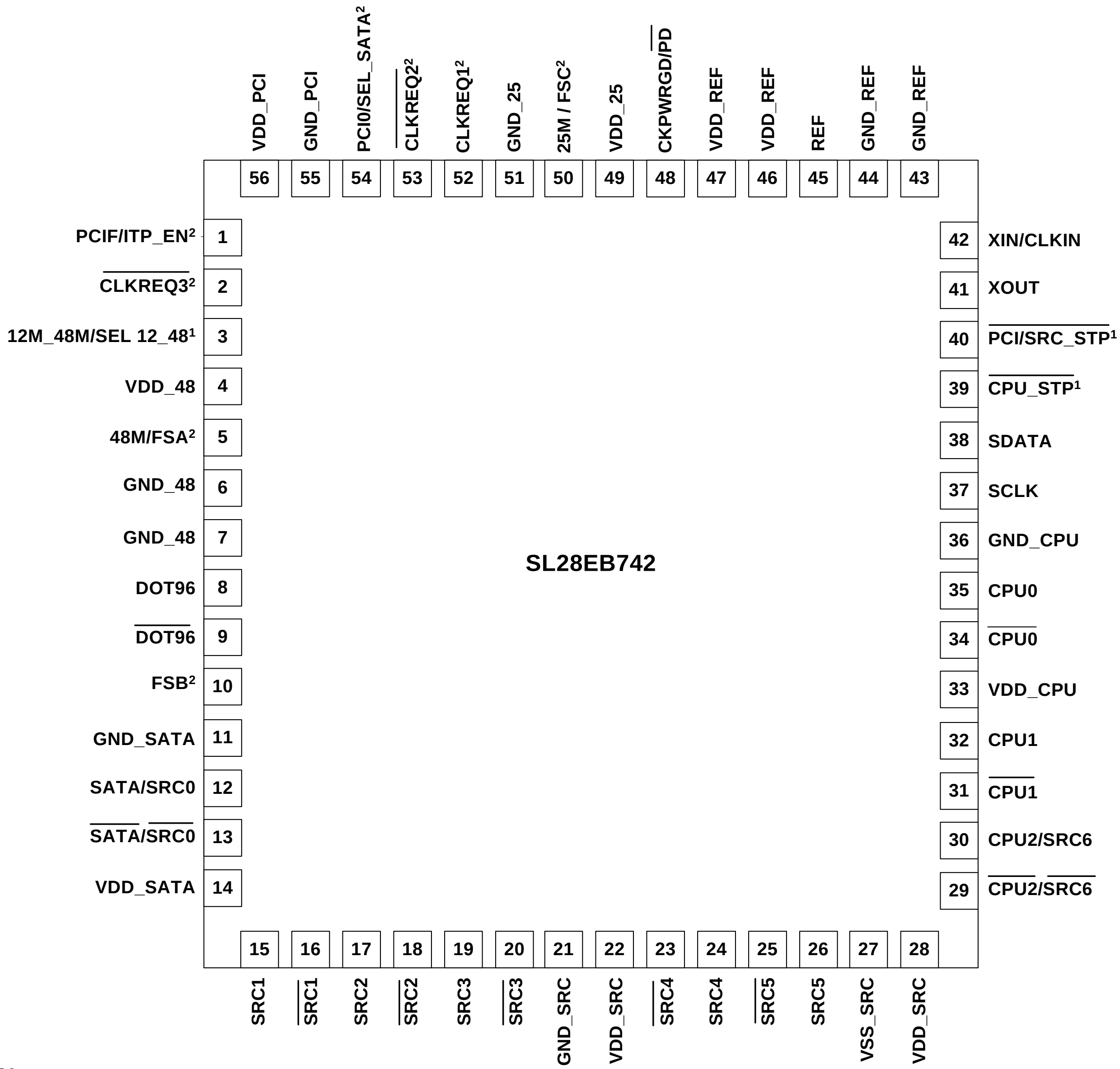
Control Register 14. Byte 14

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				OTP_4	OTP_3	OTP_2	OTP_1	OTP_0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 10101000

Bit	Name	Function
7:5	Reserved	
4	OTP_4	**OTP_ID.** Identification for programmed device
3	OTP_3	
2	OTP_2	
1	OTP_1	
0	OTP_0	

5. Pin Descriptions: 56-Pin QFN



Notes:
1. Internal 100 kohm pull-up.
2. Internal 100 kohm pull-down.

Table 12. 56-QFN Pin Definitions

Pin #	Name	Type	Description
1	PCIF/ITP_EN	I/O, SE, PD	33 MHz free running clock output/3.3 V LVTTL input to enable SRC6 or CPU2_ITP (sampled on the CKPWRGD assertion). 0 = SRC6, 1 = CPU2
2	$\overline{\text{CLKREQ3}}$	I, PD	Active low input pin enables SRC3 (internal 100 kΩ pull-down).
3	12_48M / SEL12_48	I/O, SE PU	12/48 MHz Clock output/3.3 V-tolerance input for 12 MHz or 48 MHz selection (Sampled at CKPWRGD assertion) (internal 100 kΩ pull-up). 0 = 48M, 1 = 12M
4	VDD_48	PWR	3.3 V Power supply
5	48M/FSA	I/O PD	Fixed 48 MHz clock output/3.3 V-tolerant input for CPU frequency selection (internal 100 kΩ pull-down).
6	GND_48	GND	Ground.
7	GND_48	GND	Ground.
8	DOT96	O, DIF	Fixed true 96 MHz clock output.
9	$\overline{\text{DOT96}}$	O, DIF	Fixed complement 96 MHz clock output.
10	FSB	I, PD	3.3 V-tolerant input for CPU frequency selection (internal 100 kΩ pull-down).
11	GND_SATA	GND	Ground.
12	SATA/SRC0	O, DIF	100 MHz True differential serial reference clock.
13	SATA/$\overline{\text{SRC0}}$	O, DIF	100 MHz Complement differential serial reference clock.
14	VDD_SATA	PWR	3.3 V Power supply.
15	SRC1	O, DIF	100 MHz True differential serial reference clock.
16	$\overline{\text{SRC1}}$	O, DIF	100 MHz Complement differential serial reference clock.
17	SRC2	O, DIF	100 MHz True differential serial reference clock.
18	$\overline{\text{SRC2}}$	O, DIF	100 MHz Complement differential serial reference clock.
19	SRC3	O, DIF	100 MHz True differential serial reference clock.
20	$\overline{\text{SRC3}}$	O, DIF	100 MHz Complement differential serial reference clock.
21	GND_SRC	GND	Ground.
22	VDD_SRC	PWR	3.3 V Power supply.
23	$\overline{\text{SRC4}}$	O, DIF	100 MHz Complement differential serial reference clock.
24	SRC4	O, DIF	100 MHz True differential serial reference clock.
25	$\overline{\text{SRC5}}$	O, DIF	100 MHz Complement differential serial reference clock.

Table 12. 56-QFN Pin Definitions (Continued)

Pin #	Name	Type	Description
26	SRC5	O, DIF	100 MHz True differential serial reference clock.
27	GND_SRC	GND	Ground.
28	VDD_SRC	PWR	3.3 V Power supply.
29	$\overline{\text{SRC6}}$/$\overline{\text{CPU2\_ITP}}$	O, DIF	Selectable complementary differential CPU or SRC clock output. ITP_EN = 0 @ CKPWRGD assertion = $\overline{\text{SRC6}}$ ITP_EN = 1 @ CKPWRGD assertion = $\overline{\text{CPU2}}$
30	SRC6/CPU2_ITP	O, DIF	Selectable True differential CPU or SRC clock output. ITP_EN = 0 @ CKPWRGD assertion = SRC6 ITP_EN = 1 @ CKPWRGD assertion = CPU2
31	$\overline{\text{CPU1}}$	O, DIF	Complement differential CPU clock output.
32	CPU1	O, DIF	True differential CPU clock output.
33	VDD_CPU	PWR	3.3 V Power supply.
34	$\overline{\text{CPU0}}$	O, DIF	Complement differential CPU clock output.
35	CPU0	O, DIF	True differential CPU clock output.
36	GND_CPU	GND	Ground.
37	SCLK	I	I^2C compatible SCLOCK.
38	SDATA	I/O	I^2C compatible SDATA.
39	$\overline{\text{CPU\_STP}}$	I, PU	3.3 V-tolerant input for stopping CPU outputs (internal 100 kΩ pull-up).
40	$\overline{\text{PCI/SRC\_STP}}$	I, PU	3.3 V-tolerant input for stopping PCI and SRC outputs (internal 100 kΩ pull-up).
41	XOUT	O	14.318 MHz Crystal output, Float XOUT if using only CLKIN (Clock input).
42	XIN/CLKIN	I	14.318 MHz Crystal input or 3.3 V, 14.318 MHz Clock Input
43	GND_REF	GND	Ground for REF clock.
44	GND_REF	GND	Ground for REF clock.
45	REF	O	14.318 MHz reference output clock.
46	VDD_REF	PWR	3.3 V Power Supply for REF clock.
47	VDD_REF	PWR	3.3 V Power Supply for REF clock.
48	CKPWRGD/$\overline{\text{PD}}$	I	3.3 V LVTTL input. This pin is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. After latch inputs are latched, this pin becomes a real-time active low input for asserting power down ($\overline{\text{PD}}$); asynchronous active low input pin that stops all outputs except free running.

Table 12. 56-QFN Pin Definitions (Continued)

Pin #	Name	Type	Description
49	VDD_25	PWR	3.3 V Power supply.
50	25M/FSC	I/O, PD	Fixed 25 MHz clock output/3.3 V-tolerant input for CPU frequency selection (internal 100 kΩ pull-up).
51	GND_25	GND	Ground.
52	$\overline{\text{CLKREQ1}}$	I, PD	Active low input pin enables SRC1 (internal 100 kΩ pull-up).
53	$\overline{\text{CLKREQ2}}$	I, PD	Active low input pin enables SRC2 (internal 100 kΩ pull-up).
54	PCI0/SEL_SATA	I/O, SE PD	33 MHz clock output/3.3 V LVTTL input to enable 100 MHz SATA (internal 100 kΩ pull-up). 0 = SATA/SRC0 = SRC0 1 = SATA/SRC0 = SATA
55	GND_PCI	GND	Ground.
56	VDD_PCI	PWR	3.3 V Power supply.

6. Ordering Guide

Part Number	Package Type	Product Flow
Lead-free		
SL28EB742ALC	56-pin QFN	Commercial, 0 to 70 °C
SL28EB742ALCT	56-pin QFN Tape and Reel	Commercial, 0 to 70 °C
SL28EB742ALI	56-pin QFN	Extended, –40 to 85 °C
SL28EB742ALIT	56-pin QFN Tape and Reel	Extended, –40 to 85 °C

7. Package Outline

Figure 13 illustrates the package details for the SL28EB742. Table 13 lists the values for the dimensions shown in the illustration.

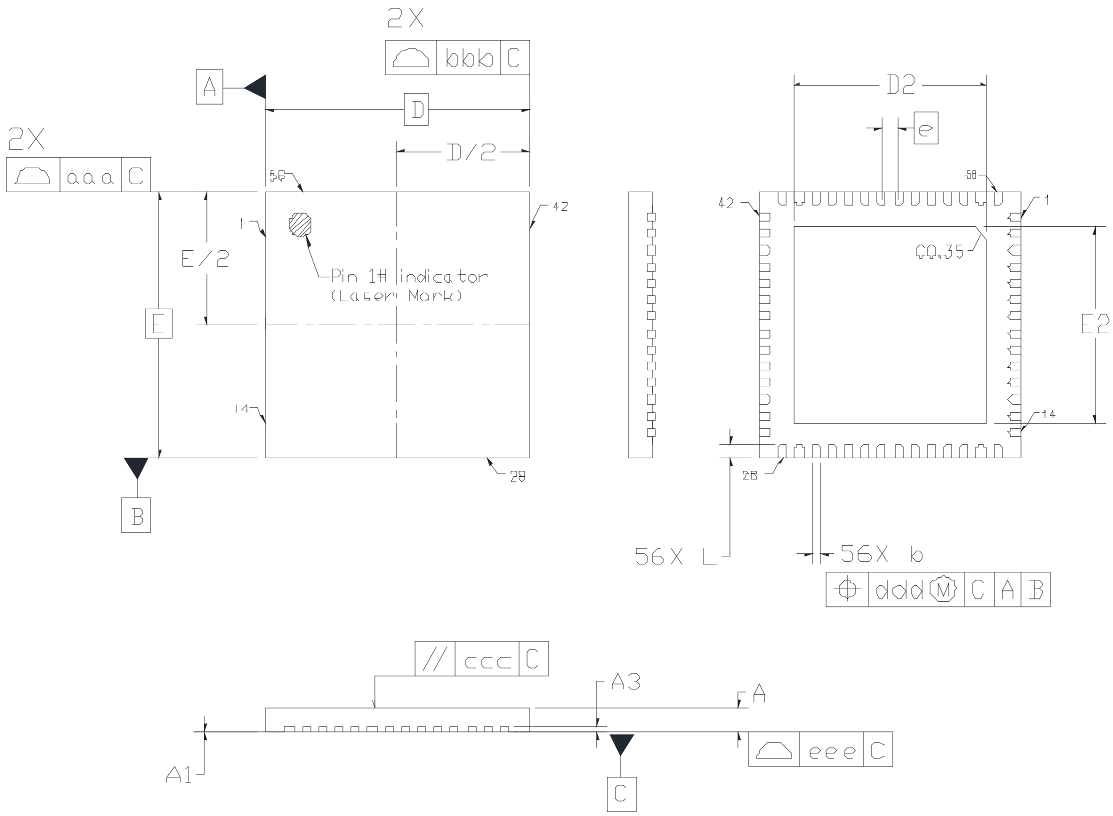


Figure 13. 56-Lead QFN Package

Table 13. Package Diagram Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.18	0.25	0.30
D	8.00 BSC		
D2	5.80	5.90	6.00
e	0.50 BSC		
E	8.00 BSC		
E2	5.80	5.90	6.00
L	0.30	0.40	0.50
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.10		
eee	0.08		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
4. This drawing conforms to the JEDEC Solid State Outline MO-220.

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