

ICE4N70D N-Channel Enhancement Mode MOSFET

RoHS
compliant
2011/65/EU



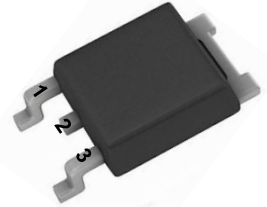
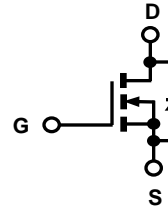
HALOGEN
FREE

Product Summary			
I_D	$T_A=25^\circ\text{C}$	4A	Max
$V_{(BR)DSS}$	$I_D=250\mu\text{A}$	700V	Min
$r_{DS(on)}$	$V_{GS}=10\text{V}$	1.0 Ω	Typ
Q_g	$V_{DS}=480\text{V}$	21nC	Typ

Features

- Low $r_{DS(on)}$
- Ultra Low Gate Charge
- High dv/dt capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems

ICEMOS AND ITS SISTER COMPANY 3D SEMI OWN THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 TO 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN & EUROPE.



T0252

Standard Metal
Heatsink

1=Gate, 2=Drain,
3=Source.

Maximum ratings^b, at $T_j=25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_c=25^\circ\text{C}$	4	A
Pulsed drain current	$I_{D, \text{pulse}}$	$T_c=25^\circ\text{C}$	12	A
Avalanche energy, single pulse	E_{AS}	$I_D=2\text{A}$	80	mJ
Avalanche current, repetitive	I_{AR}	limited by $T_j\text{max}$	2	A
MOSFET dv/dt ruggedness	dv/dt	$V_{DS}=480\text{V}$, $I_D=4\text{A}$, $T_j=125^\circ\text{C}$	50	V/ns
Gate source voltage	V_{GS}	Static	± 20	V
		AC ($f > 1\text{Hz}$)	± 30	
Power dissipation	P_{tot}	$T_c=25^\circ\text{C}$	65	W
Operating and storage temperature	T_j, T_{stg}		-55 to +150	$^\circ\text{C}$

a When mounted on 1inch square 2oz copper clad FR-4

b Preliminary Data Sheet – Specifications subject to change

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

Thermal characteristics

Thermal resistance, junction-case ^a	R_{thJC}		-	-	1.9	°C/W
Thermal resistance, junction-ambient ^a	R_{thJA}	leaded	-	-	68	
Soldering temperature, wave soldering only allowed at leads	T_{sold}	1.6mm (0.063in.) from case for 10 s	-	-	260	°C

Electrical characteristics ^b, at $T_j=25^\circ\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=250\mu\text{A}$	700	730	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.1	3	3.9	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=700\text{V}, V_{GS}=0\text{V}, T_j=25^\circ\text{C}$	-	0.1	1	μA
		$V_{DS}=700\text{V}, V_{GS}=0\text{V}, T_j=150^\circ\text{C}$	-	-	100	
Gate source leakage current	I_{GSS}	$V_{GS}=\pm 20\text{ V}, V_{DS}=0\text{V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=2\text{A}, T_j=25^\circ\text{C}$	-	1.0	1.2	Ω
		$V_{GS}=10\text{V}, I_D=2\text{A}, T_j=150^\circ\text{C}$	-	2.6	-	
Gate resistance	R_G	$f=1\text{ MHz}, \text{open drain}$	-	6.3	-	Ω

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V}, f=1\text{ MHz}$	-	630	-	μF
Output capacitance	C_{oss}		-	430	-	
Reverse transfer capacitance	C_{rss}		-	12	-	
Transconductance	g_{fs}	$V_{DS}>2 * I_D * R_{DS}, I_D=2\text{A}$	-	4	-	S
Turn-on delay time	$t_{d(on)}$	$V_{DS}=480\text{V}, V_{GS}=10\text{V}, I_D=4\text{A}, R_G=4\Omega \text{ (External)}$	-	22	-	ns
Rise time	t_r		-	5	-	
Turn-off delay time	$t_{d(off)}$		-	67	-	
Fall time	t_f		-	4.5	-	

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

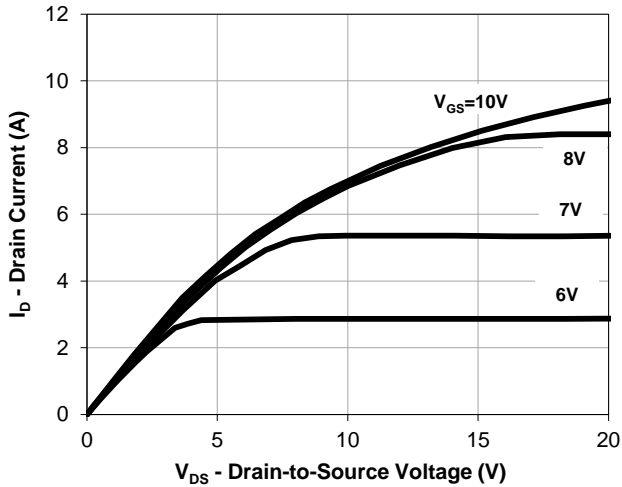
Gate charge characteristics

Gate to source charge	Q_{gs}	$V_{DS}=480\text{ V}, I_D=2\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	4.6	-	nC
Gate to drain charge	Q_{gd}		-	6.8	-	
Gate charge total	Q_g		-	21	-	
Gate plateau voltage	V_{plateau}		-	5.5	-	V

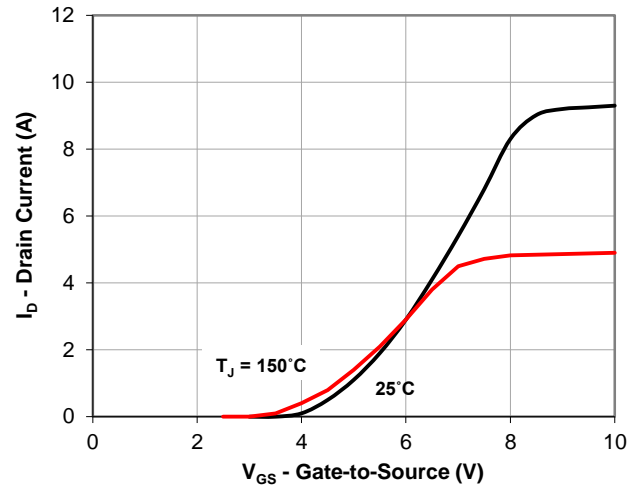
Reverse Diode

Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_S=I_F$	-	1.0	1.2	V
Reverse recovery time	t_{rr}	$V_{RR}=480\text{ V}, I_S=I_F,$ $d_{iF}/d_t=100\text{ A}/\mu\text{S}$	-	280	-	ns
Reverse recovery charge	Q_{rr}		-	3	-	μC
Peak reverse recovery current	I_{rm}		-	20	-	A

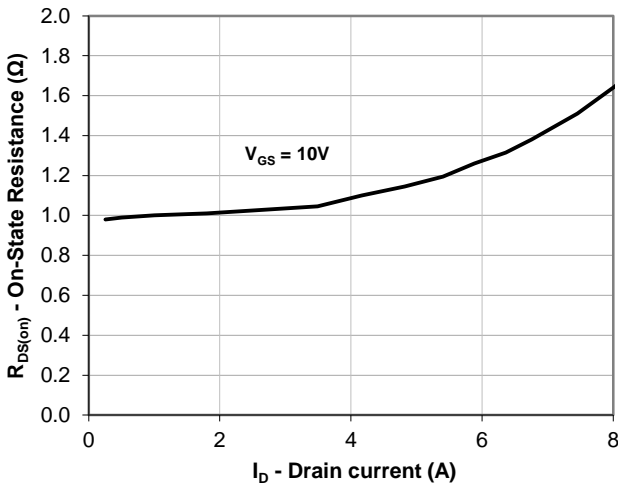
Output Characteristics



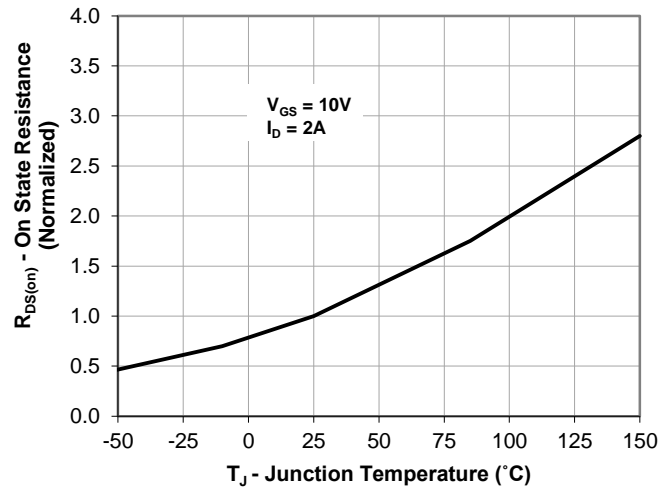
Transfer Characteristics



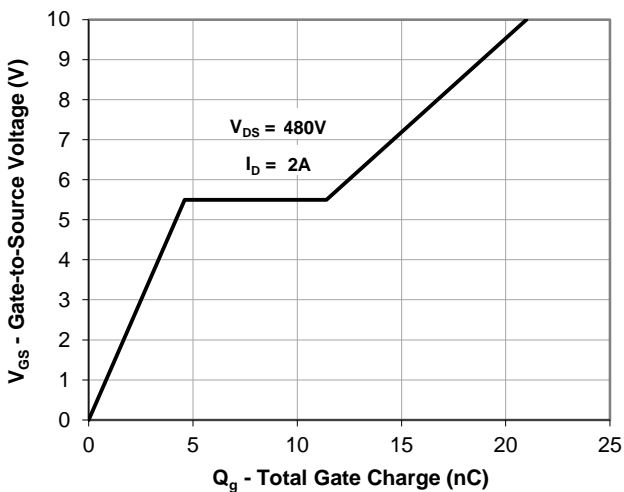
On Resistance vs Drain Current



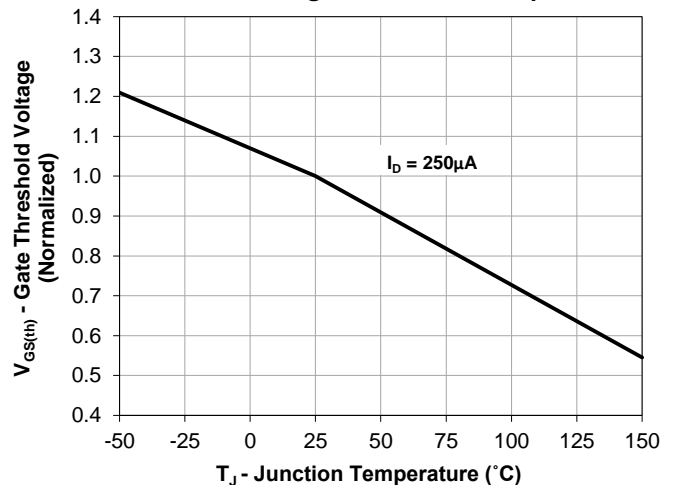
On Resistance vs Junction Temperature



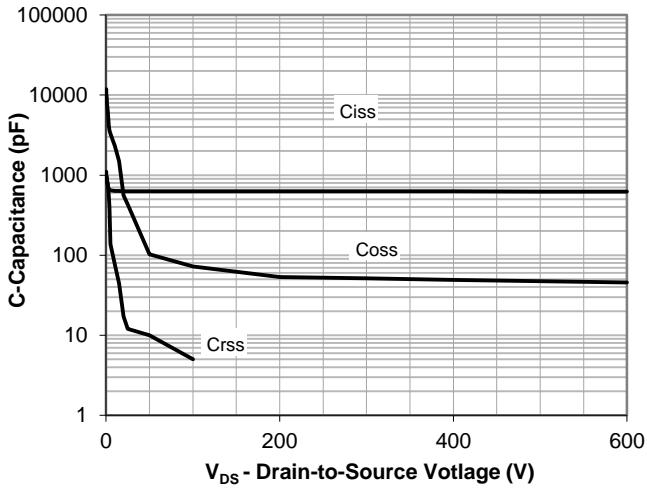
Gate Charge



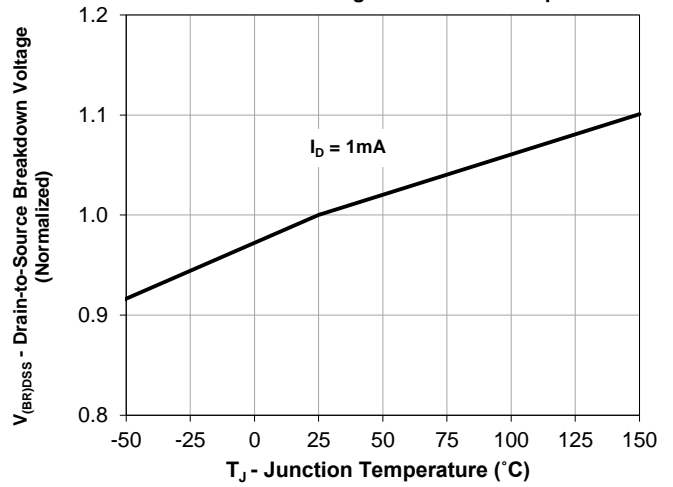
Gate Threshold Voltage vs Junction Temperature



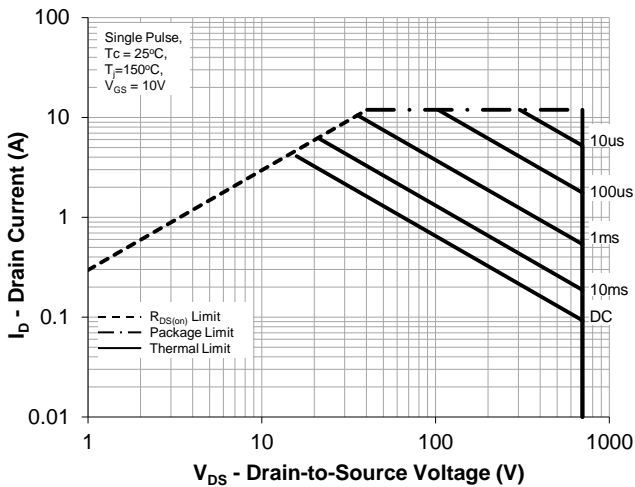
Capacitance



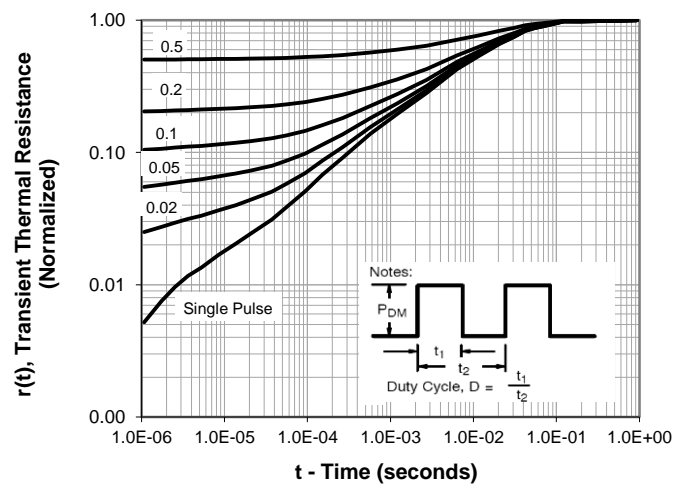
Drain-to-Source Breakdown Voltage vs. Junction Temperature

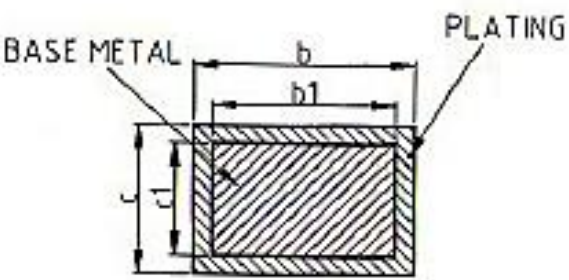
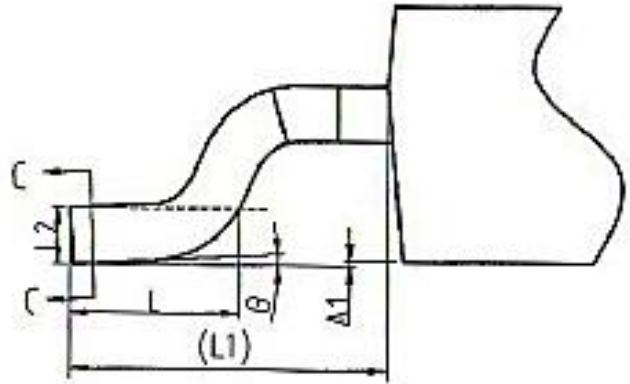
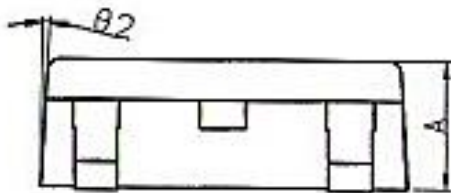
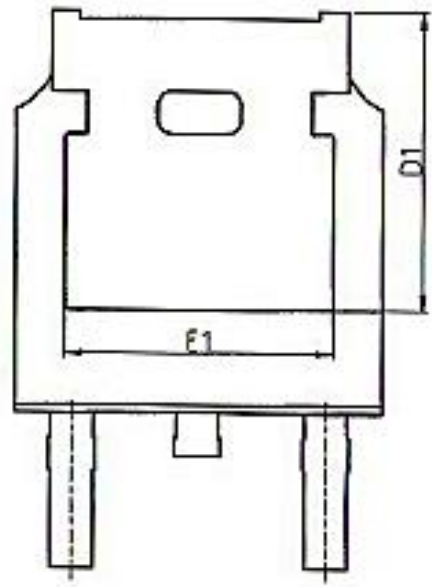
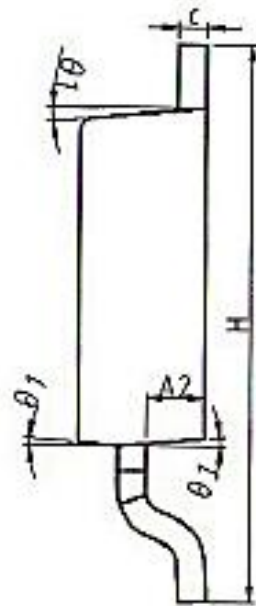
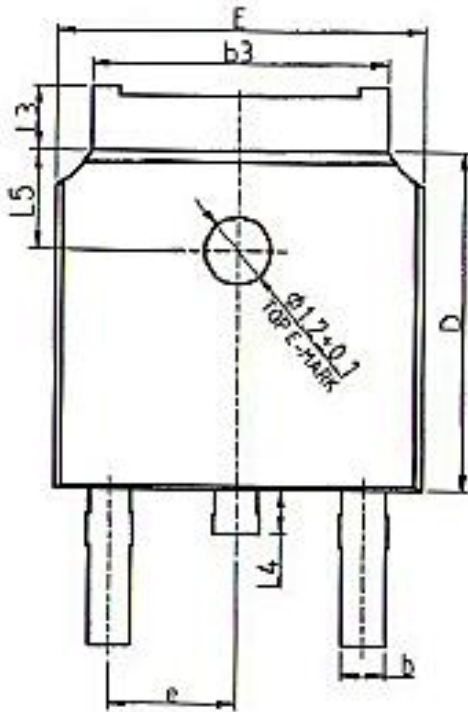


Maximum Rated Forward Biased Safe Operating Area



Transient Thermal Response, Junction-to-Case





SECTION C-C

NOTES
1 ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 AA,
DO NOT INCLUDE MOLO FLASH OR PROTRUSIONS.

COMMON DIMENSIONS

SYMBOL	mm		
	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0.00	-	0.10
A2	0.97	1.07	1.17
b	0.72	0.78	0.85
b1	0.71	0.76	0.81
b3	5.23	5.33	5.46
c	0.47	0.53	0.58
c1	0.46	0.51	0.56
D	6.00	6.10	6.20
D1	5.30 REF		
E	6.50	6.60	6.70
E1	4.70	4.83	4.92
e	2.286 BSC		
H	9.90	10.10	10.30
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.51 BSC		
L3	0.90	-	1.25
L4	0.60	0.80	1.00
L5	1.70	1.80	1.90
θ	0°	-	8°
θ1	5°	7°	9°
θ2	5°	7°	9°

ICEMOS SUPERJUNCTION PATENT PORTFOLIO

ICEMOS GRANTED PATENTS

US7,429,772
US7,439,178
US7,446,018
US7,579,607
US7,723,172
US7,795,045
US7,846,821
US7,944,018
US8,012,806
US8,030,133

3D SEMI PATENTS LICENSED TO ICEMOS

US7,041,560B2
US7,023,069B2
US7,364,994
US7,227,197B2
US7,304,944B2
US7,052,982B2
US7,339,252
US7,410,891
US7,439,583
US7,227,197B2
US6,635,906
US6,936,867
US7,015,104
US9,109,110
US7,271,067
US7,354,818
US7,052,982,
US7,199,006B2

Note: additional patents in China, Korea, Japan, Taiwan, Europe have also been granted to IceMOS and 3D Semi for Superjunction MOSFETs with 70 additional Patent applications in process in the USA and the above listed countries.

Marking Information

YY = Last two digits of the year

WW = Work week calendar on Icemos subcon assembly & test house

***** = Initial for Icemos subcon assembly and test house

XXXXXX = Lot ID

ICE4N70 = ICE is Icemos logo and 4N70 is a designated device part number

