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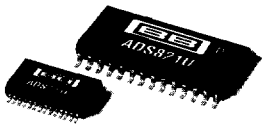


ADS821

www.burr-brown.com/databook/ADS821.html

SpeedPlus™ 10-Bit, 40MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- NO MISSING CODES
- INTERNAL REFERENCE
- LOW POWER: 380mW
- HIGH SNR: 58dB
- INTERNAL TRACK/HOLD
- PACKAGE: 28-Lead SOIC and SSOP

APPLICATIONS

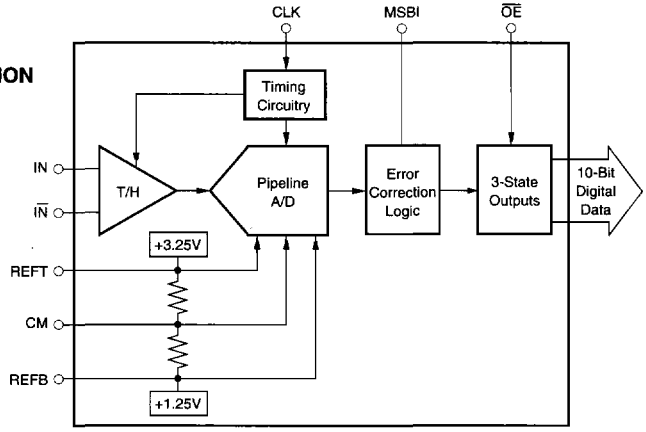
- VIDEO DIGITIZING
- ULTRASOUND IMAGING
- GAMMA CAMERAS
- SET-TOP BOXES
- CABLE MODEMS
- CCD IMAGING
  - Color Copiers
  - Scanners
  - Camcorders
  - Security Cameras
  - Fax Machines
- IF AND BASEBAND DIGITIZATION
- TEST INSTRUMENTATION

DESCRIPTION

The ADS821 is a low power, monolithic 10-bit, 40MHz analog-to-digital converter utilizing a small geometry CMOS process. This COMPLETE converter includes a 10-bit quantizer with internal track/hold, reference, and a power down feature. It operates from a single +5V power supply and can be configured to accept either differential or single-ended input signals.

The ADS821 employs digital error correction to provide excellent Nyquist differential linearity performance for demanding imaging applications. Its low distortion, high SNR and high oversampling capability give it the extra margin needed for telecommunications and video applications.

This high performance converter is specified for AC and DC performance at a 40MHz sampling rate. The ADS821 is available in 28-lead SOIC and SSOP packages.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

PARAMETER	CONDITIONS	TEMP	ADS821U (SOIC) MIN	ADS821U (SOIC) TYP	ADS821U (SOIC) MAX	ADS821E (SSOP) MIN	ADS821E (SSOP) TYP	ADS821E (SSOP) MAX	UNITS
Resolution				10			*		Bits
Specified Temperature Range	$T_{AMBIENT}$		–40		+85	*[1]		*	°C
ANALOG INPUT									
Differential Full Scale Input Range			+1.25		+3.25	*		*	V
Common-Mode Voltage				+2.25			*		V
Analog Input Bandwidth (–3dB)									
Small Signal	–20dBFS[2] Input	+25°C		400			*		MHz
Full Power	0dBFS Input	+25°C		65			*		MHz
Input Impedance				1.25 ll 4			*		MΩ ll pF
DIGITAL INPUT									
Logic Family				TTL/HCT Compatible CMOS			TTL/HCT Compatible CMOS		
Convert Command	Start Conversion			Falling Edge			Falling Edge		
ACCURACY[3]									
Gain Error		+25°C		±0.6	±1.5		*	*	%
		Full		±1.1	±2.5		*	*	%
Gain Drift				±85			*		ppm/°C
Power Supply Rejection of Gain	Delta $+V_S$ = ±5%	+25°C		0.01	0.15		*	*	%FSR/%
Input Offset Error		Full		±2.1	±3.5		*	*	%
Power Supply Rejection of Offset	Delta $+V_S$ = ±5%	+25°C		0.02	0.15		*	*	%FSR/%
CONVERSION CHARACTERISTICS									
Sample Rate			10k		40M	*		*	Sample/s
Data Latency				6.5			*		Convert Cycle
DYNAMIC CHARACTERISTICS									
Differential Linearity Error	t_H = *13ns*[4]								
f = 500kHz		+25°C		±0.5	±1.0		*	*	LSB
		0°C to +70°C		±0.6	±1.0		*	*	LSB
f = 12MHz		+25°C		±0.5	±1.0		*	*	LSB
		0°C to +70°C		±0.6	±1.0		*	*	LSB
No Missing Codes		0°C to +70°C		Guaranteed			*		
Integral Linearity Error at f = 500kHz		0°C to +70°C		±0.5	±2.0		*	*	LSB
Spurious-Free Dynamic Range (SFDR)									
f = 500kHz (–1dBFS input)		+25°C	60	70		*	*		dBFS
		Full	54	67		*	*		dBFS
f = 12MHz (–1dBFS input)		+25°C	58	63		*	*		dBFS
		Full	54	62		*	*		dBFS
Two-Tone Intermodulation Distortion (IMD)[5]									
f = 4.4MHz and 4.5MHz (–7dBFS each tone)		+25°C		–61			*		dBc
		Full		–60			*		dBc
Signal-to-Noise Ratio (SNR)									
f = 500kHz (–1dBFS input)		+25°C	57	59		55	*		dB
		Full	55	59		53	*		dB
f = 12MHz (–1dBFS input)		+25°C	56	58		54	*		dB
		Full	54	58		52	*		dB
Signal-to-(Noise + Distortion) (SINAD)									
f = 500kHz (–1dBFS input)		+25°C	56	58.5		*	*		dB
		Full	52	58		*	*		dB
f = 12MHz (–1dBFS input)		+25°C	53	57		*	*		dB
		Full	50	56		*	*		dB
Differential Gain Error	NTSC or PAL	+25°C		0.5			*		%
Differential Phase Error	NTSC or PAL	+25°C		0.1			*		degrees
Effective Bits[6]	f_{IN} = 3.58MHz	+25°C		9.3			*		Bits
Aperture Delay Time		+25°C		2			*		*ns*
Aperture Jitter		+25°C		7			*		ps rms
Overvoltage Recovery Time[7]	1.5x Full Scale Input	+25°C		2			*		ns

NOTE: (1) An asterisk (*) indicates same specifications as the ADS821U. (2) dBFS refers to dB below Full Scale. (3) Percentage accuracies are referred to the internal A/D Full Scale Range of 4Vp-p. (4) Refer to Timing Diagram footnotes for the differential linearity performance conditions for the SOIC and SSOP packages. (5) IMD is referred to the larger of the two input signals. If referred to the peak envelope signal (=0dB), the intermodulation products will be 7dB lower. (6) Based on (SINAD – 1.76)/6.02. (7) No "rollover" of bits.

SPECIFICATIONS (CONT)

At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

PARAMETER	CONDITIONS	TEMP	ADS821U (SOIC) MIN	ADS821U (SOIC) TYP	ADS821U (SOIC) MAX	ADS821E (SSOP) MIN	ADS821E (SSOP) TYP	ADS821E (SSOP) MAX	UNITS
OUTPUTS									
Logic Family				TTL/HCT Compatible CMOS			TTL/HCT Compatible CMOS		
Logic Coding	Logic Selectable			SOB or BTC			SOB or BTC		
Logic Levels	Logic "LO", C_L = 15pF max	Full	0		0.4	*		*	V
	Logic "HI", C_L = 15pF max	Full	+2.5		$+V_S$	*		*	V
3-State Enable Time				20	40		*	*	ns
3-State Disable Time		Full		2	10		*	*	ns
POWER SUPPLY REQUIREMENTS									
Supply Voltage: $+V_S$	Operating	Full	+4.75	+5	+5.25	*	*	*	V
Supply Current: $+I_S$	Operating	+25°C		76	88		*	*	mA
	Operating	Full		78	90		*	*	mA
Power Consumption	Operating	+25°C		380	440		*	*	mW
	Operating	Full		390	450		*	*	mW
Thermal Resistance, θ_{JA}				75			50		°C/W

* Specifications same as ADS821U.

ABSOLUTE MAXIMUM RATINGS

$+V_S$	+6V
Analog Input	0V to ($+V_S$ + 300mV)
Logic Input	0V to ($+V_S$ + 300mV)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+125°C
External Top Reference Voltage (REFT)	+3.4V max
External Bottom Reference Voltage (REFB)	+1.1V min

NOTE: Stresses above these ratings may permanently damage the device.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
ADS821U	28-Lead SOIC	217	–40°C to +85°C
ADS821E	28-Lead SSOP	324	–40°C to +85°C

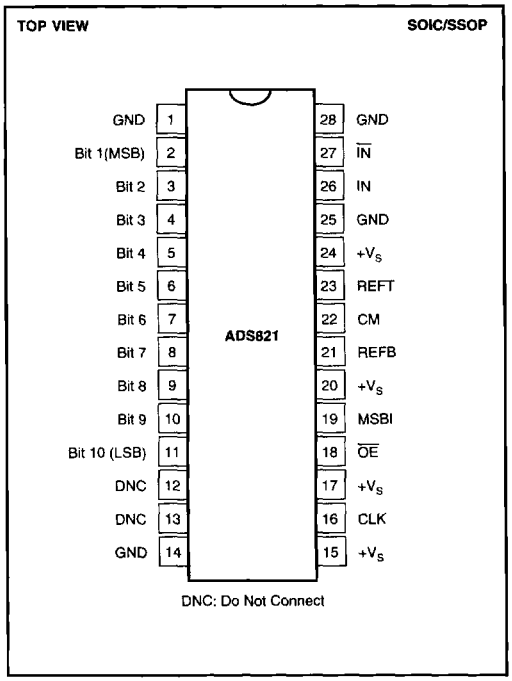
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

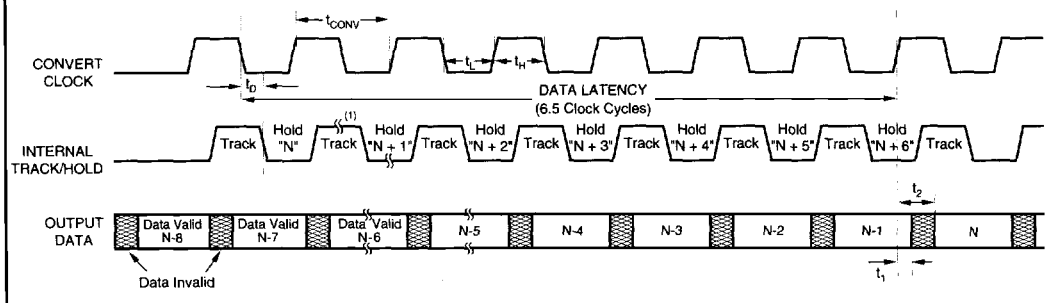
PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1	GND	Ground
2	B1	Bit 1, Most Significant Bit
3	B2	Bit 2
4	B3	Bit 3
5	B4	Bit 4
6	B5	Bit 5
7	B6	Bit 6
8	B7	Bit 7
9	B8	Bit 8
10	B9	Bit 9
11	B10	*Bit 10, Least Significant Bit*
12	DNC	Do not connect.
13	DNC	*Do not connect.*
14	GND	Ground
15	$+V_S$	+5V Power Supply
16	CLK	Convert Clock Input, 50% Duty Cycle
17	$+V_S$	+5V Power Supply
18	$\overline{OE}$	HI: High Impedance State. LO or Floating: Normal Operation. Internal pull-down resistor.
19	MSBI	Most Significant Bit Inversion, HI: MSB inverted for complementary output. LO or Floating: Straight output. Internal pull-down resistor.
20	$+V_S$	+5V Power Supply
21	REFB	Bottom Reference Bypass. For external bypassing of internal +1.25V reference.
22	CM	*Common-Mode Voltage. It is derived by (REFT + REFB)/2.*
23	REFT	Top Reference Bypass. For external bypassing of internal +3.25V reference.
24	$+V_S$	+5V Power Supply
25	GND	Ground
26	$\underline{IN}$	Input
27	$\overline{IN}$	Complementary Input
28	GND	Ground

TIMING DIAGRAM



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	25		100µs	ns
t_L	Clock Pulse Low	12	12.5		ns
t_H	Clock Pulse High	12(2)	12.5		ns
t_D	Aperture Delay		2		ns
t_1	Data Hold Time, C_L = 0pF	3.9			ns
t_2	New Data Delay Time, C_L = 15pF max			12.5	ns

NOTE: (1) "§" indicates the portion of the waveform that will stretch out at slower sample rates. (2) t_H must be 13ns minimum if no missing codes is desired only for the conditions of t_{CONV} ≤28ns and f_{IN} <2MHz for the SOIC package. For best performance in the SSOP package, t_H must be 13ns minimum for all input frequencies and t_{CONV} ≤28ns. Refer to the Clock Requirements for a possible clock skew circuit for this condition.