# MN1237A, MN1237AD

CMOS LSIs for CRT Interface

■ Outline

The MN1237A and MN1237AD are high-performance CMOS LSIs for highly efficient CRT interface, which can display times, channels, programs, etc. up to 60 characters(12 characters×5Lines) on the CRT screens of video equipment such as video cameras, color TV sets, VTRs, video disks, etc., using alphabets, numerals, symbols, etc.

■ Features

- Displays up to 60 characters(12 characters×5 lines).
- 44 Kinds of characters(5×7 dots) (with rounding function); A-Z, 0-9, ., :, •, —, ?,(background),__(blank)
- Black background to display characters clearly
- Character size selectable out of 4 types, depending on programs.
- Display position selectable out of 57 horizontal directions and 64 vertical direction, depending on programs.
- Available for various controls because 4-bit general purpose output latches are porvided.
- +5V singie power supply
- CMOS process

■ Pin Configuration

② 22-DIP

⑬ 42-QFP

■ Block Diagam
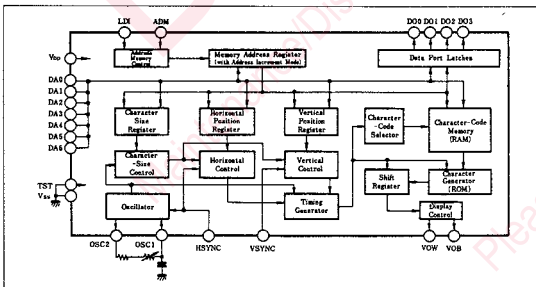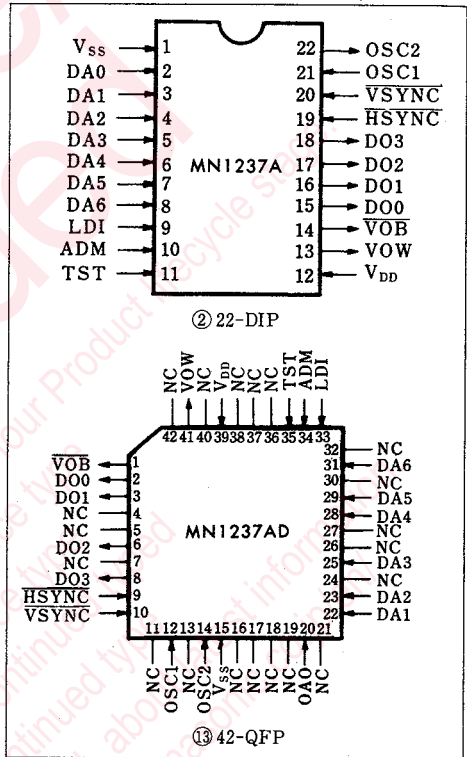
■ Absolute Maximum Ratings (V$_{ss}$=0 V, Ta=25°C)

Item	Symbol	Rating	Unit
Supply voltage	V$_{DD}$	$-0.3 \sim +8$	V
Input voltage	V$_I$	$-0.3 \sim$ V$_{DD}$+0.3	V
Output voltage	V$_O$	$-0.3 \sim$ V$_{DD}$+0.3	V
Power Dissipation	P$_D$	100	mW
Operating ambient temperature	T$_{opr}$	$-20 \sim +70$	°C
Storage temperature	T$_{stg}$	$-50 \sim +120$	°C

■ Operating Conditions (Ta=25°C)

Item	Symbol	Condition	min.	typ.	max.	Unit
Supply voltage	V$_{DD}$	V$_{ss}$=0V	4.5	5	5.5	V
Self-oscillation						
Self-oscillation frequency	f$_{osc}$	R=1~3kΩ, R$_{fix}$=1kΩ, C=22pF	4.5	5	5.5	MHz

*1 Recommended self-oscillator circuit
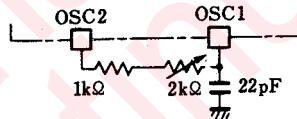
■ Electrical Characteristics (V$_{DD}$=5 V±5%, V$_{ss}$=0 V, Ta=0 to +70°C)

### ● DC Characteristics

Item	Symbol	Condition	min.	typ.	max.	Unit
Supply current	I$_{DD}$	V$_{DD}$=5V, Output terminal open		5	8	mA
Power consumption	P$_{tot}$				40	mW
Input pin 1(DAO-6, ADM, TST)						
Input voltage high level	V$_{IH}$	V$_{DD}$=5V	3			V
Input voltage low level	V$_{IL}$				0.8	V
Input leakage current	I$_{LI}$	V$_I$=V$_{DD}$			30	μA
Input pin 2(LDI, HSYNC, VSYNC)						
Input voltage high level	V$_{IHS}$	V$_{DD}$=5V	3			V
Input voltage low level	V$_{ILS}$				0.8	V
Input leakage current	I$_{LI}$	V$_I$=V$_{DD}$			30	μA
Output pin(DOO-3, VOW, VOB)						
Output voltage high level	V$_{OH}$	V$_{DD}$=5V, I$_{OH}$=300μA	3.2			V
Output volyage low level	V$_{OL}$	V$_{DD}$=5V, I$_{OL}$=2mA			0.5	V

● AC Characteristics

| Item	Symbol	Condition	min.	typ.	max.	Unit	Note
Address setup time	t$_{Sua}$	V$_{DD}$=5.0V V$_{IH}$=4.0V V$_{IL}$=0.8V V$_{IHS}$=4.0V V$_{ILS}$=0.8V	4			μs	Fig.1
Address hold time	t$_{ha}$		7			μs	
Data setup time	t$_{ud}$		4			μs	
Data hold time	t$_{hd}$		8			μs	
VSYNC pulse width	t$_{WVSYNC}$	V$_{DD}$=5.0V	6			μs	Fig.2
HSYNC pulse width	t$_{WHSYNC}$		3			μs	
DOO-3 output delay time	t$_{aDO}$	V$_{DD}$=5.0V	5			μs	Fig.3

■ Timing Diagrams

Fig.1

Fig.2

Fig.3
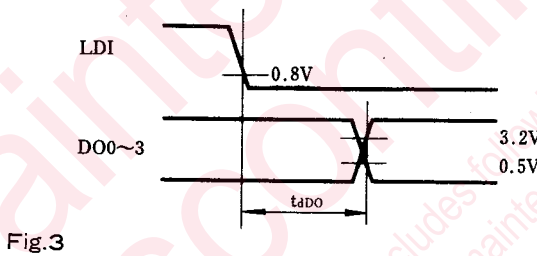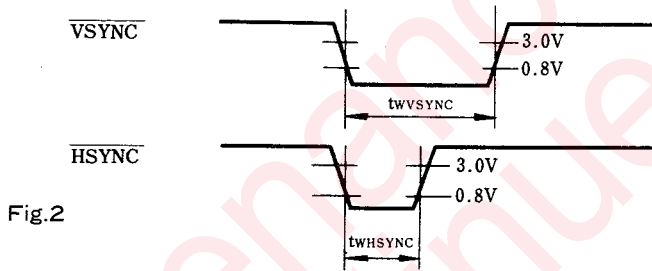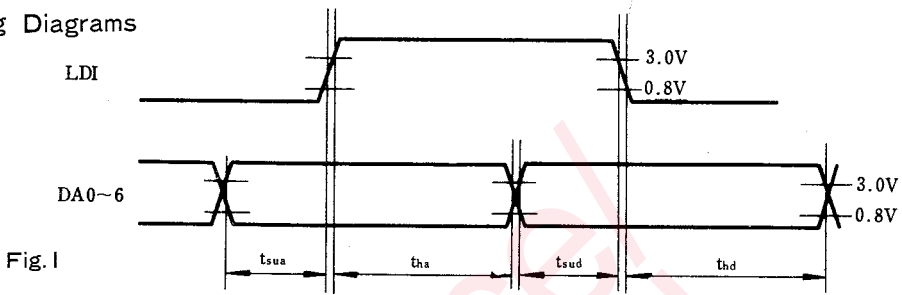
■ Pins Description

Symbol	Pin	Description
V$_{DD}$	V$_{DD}$ power supply	Connects to the V$_{DD}$ supply voltage(+5V).
V$_{SS}$	V$_{SS}$ power supply	Connects to the V$_{SS}$ supply voltage.(0V).
OSC1~2	Self-oscillation pin	Pins to connect C and R for determining a self-oscillation frequency.
TST	Test input	Set to the "L" level in other cases than chip test.
$\overline{VSYNC}$	Vert. sync. pulse input	Pin to input a TV vertical sync. A sync. signal is active at the "L" level.
$\overline{HSYNC}$	Hor. sync pulse input	Pin to input a horizontal sync. signal. A sync. signal is active at the "L" level.
DA0~6	Data bus input	7-bit data input pin. Active at the "H" level
ADM	Address mode select input	Input pin for a signal which selects an address setting mode.
LDI	Strobe pulse input	Input pin for a strobe signal which latches an address and data
VOW	Video signal output(W)	Video signal output pin. A white signal is outputted at the "H" level.(character output)
$\overline{VOB}$	Video signal output(B)	Video signal output pin. A black signal is outputted at the "L" level.(background output)
DO0~3	Output with general purpose latch	4-bit general purpose output pin.

■ Description of Operation

1. Screen Configuration

The MN1237A and MN1237AD can display up to 60 characters; 12 characters per line × 5 lines. Each character has a 5 × 7 dot matrix. There is a 1-dot space between each character, and a 2-dot space between each line.
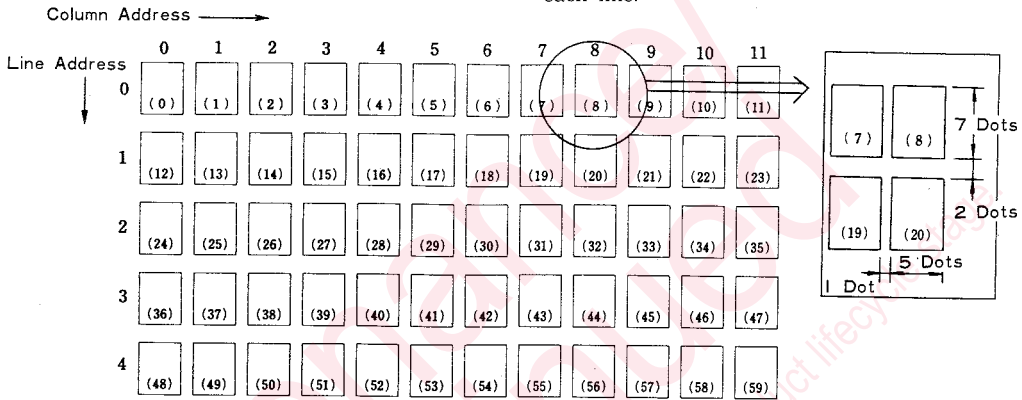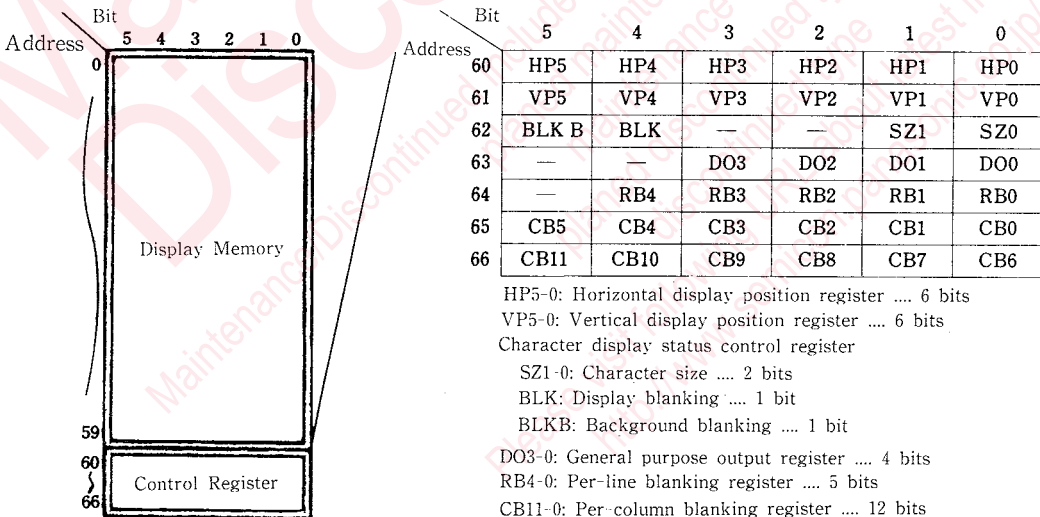

Note Numerals 0 through 59 in frames indicate display memory addresses.

Fig.4 Relations between Screen Configuration and Display Memory Addresses

2. Memory Configuration

A memory address consists of 7 bits. Addresses 0(0000000) through 59(0111011) are display data memory. Fig.4 shows its relations with the screen.

Addresses 60(0111100) through 66(1000010) are display control register. Fig.5 shows a memory map.

Address	Bit 5	4	3	2	1	0
60	HP5	HP4	HP3	HP2	HP1	HP0
61	VP5	VP4	VP3	VP2	VP1	VP0
62	BLK B	BLK	—	—	SZ1	SZ0
63	—	—	DO3	DO2	DO1	DO0
64	—	RB4	RB3	RB2	RB1	RB0
65	CB5	CB4	CB3	CB2	CB1	CB0
66	CB11	CB10	CB9	CB8	CB7	CB6

HP5-0: Horizontal display position register .... 6 bits
VP5-0: Vertical display position register .... 6 bits
Character display status control register
   SZ1-0: Character size .... 2 bits
   BLK: Display blanking .... 1 bit
   BLKB: Background blanking .... 1 bit
DO3-0: General purpose output register .... 4 bits
RB4-0: Per-line blanking register .... 5 bits
CB11-0: Per-column blanking register .... 12 bits

Fig.5 Memory Map

[Supplement: Differences between MN1237 and MN1227]

The MN1237 is a pin compatible CMOS LSI with the MN1227. As it uses a precharge system at RAM write/read time along with a CMOS-oriented trend, precharge may affect read RAM data under the following circumstances.

In writing a character code at the RAM address "n", display data may be affected by precharge when displaying the data of the same address, within a period of 3μs from a rise edge of the LDI signal.

3. Character Codes and Their Patterns

The MN1237A/MN1237AD incorporates a 5×7-dot ROM type character generator. Each character corresponds to the codes shown in Table 1.

Table 1 Character Codes List

Lower 4 Bits \ Upper 2 Bits	0	1	2
0	A	N	0
1	B	O	1
2	C	P	2
3	D	Q	3
4	E	R	4
5	F	S	5
6	G	T	6
7	H	U	7
8	I	V	8
9	J	W	9
10	K	X	:
11	L	Y	. (Period)
12	M	Z	—
13	(Dot)	?	/
14	■	■	■
15	�	�	�

Fig.6 shows character patterns registered in the ROM. Since the MN1237A/MN1237AD has a rounding function, corners of each characters are rounded to display characters more naturally, compared with a general 5×7-dot display.
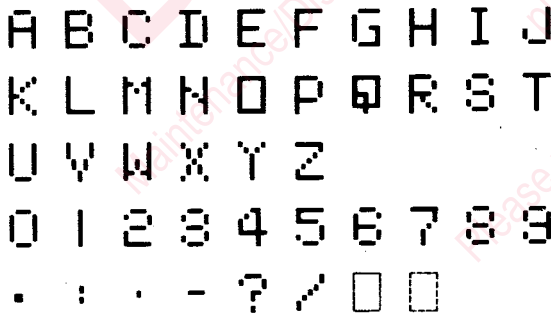

Fig.6 Character Types

(Character patterns registered in ROM: 44 types, 1 character: 5×7 dots)

4. Display Memory Configuration

The display memory is a 60×6-bits RAM. Bits 5-0 specify character codes. Fig.7 shows a configuration of one word of the display memory. Character codes are shown in Table 1.
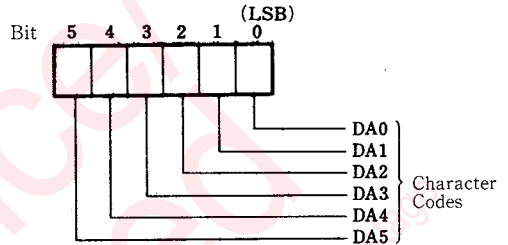

Fig.7 Configuration of One Word of Display Memory

5. Control Registers

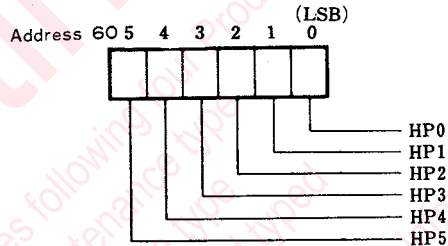### (1) Horizontal display position register (HP5-0)

Fig.8 Horizontal Display Position Register

This register specifies a display start position in the horizontal direction on the CRT.

HP5-0 are not allowed to be(000000) through(000110).

For a horizontal display start position, see Fig.10.

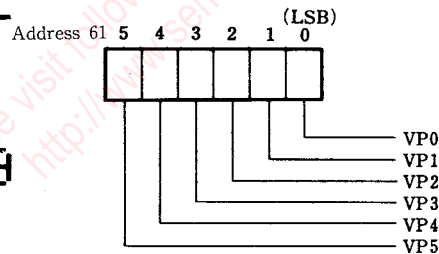### (2) Vertical display position register (VP5-0)

Fig.9 Vertical display Position Register

This register specifies a display start position in the vertical direction on the CRT screen.

For a vertical display start position, see Fig.10.

[Horizontal and Vertical Disply Start Positions]

Horizontal and vertical display start positions on the CRT screen are specified by specifying a black background display position in accordance with values of HP5-0 and those of VP5-0. (See Fig. 10) Assuming that the horizontal and vertical display start positions are HL and VL, respectively, they can be obtained by the following formulas, where an oscillation cycle is t [s] and H is one cycle of a horizontal sync. signal when an oscillation frequency is fosc [Hz].

$$HL = t \times \{4(HP5 \times 2^5 + HP4 \times 2^4 + HP3 \times 2^3 + HP2 \times 2^2 + HP1 \times 2 + HPO) + A\}$$

$$VL = H \times 4(VP5 \times 2^5 + VP4 \times 2^4 + VP3 \times 2^3 + VP2 \times 2^2 + VP1 \times 2 + VPO)$$

Note) The value of A changes as shown in Table 2, depending on character sizes(SZ1 0).

t=1/fosc: Oscillation frequency(5 MHz typ.)

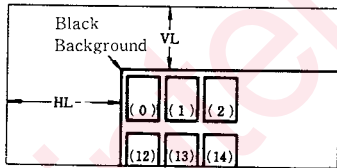H: Horizontal sync. signal cycle(63.5μs typ.)

Fig.10 Display Start Position

Table 2 Relations between Character Size(SZ1-0) and A

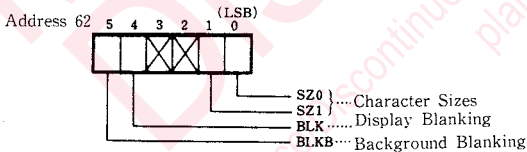| SZ1	SZ0	A
0	0	8
0	1	10
1	0	11
1	1	12

(3) Character display status control register

Address 62

SZ0 } Character Sizes
SZ1 }
BLK ...... Display Blanking
BLKB ... Background Blanking

Fig.11 Character Display State Control Register

① Character size(SZ1-0)

SZ1 and SZ0 are bits to specify a character size. One of four types of character sizes shown in Table 3 can be selected depending on data in SZ1-SZ0.

Fig.12 shows a 5×7 dot matrix configuration.

Table 3

Code		Character Size(1-dot Size) H: Hor. Line	
SZ1	SZ0	Vert.	Hor.
0	0	14H (2H)	2μs(0.4μs)
0	1	28H (4H)	4μs(0.8μs)
1	0	42H (6H)	6μs(1.2μs)
1	1	56H (8H)	8μs(1.6μs)

Hor.
5 Dots

Vert.
7 Dots

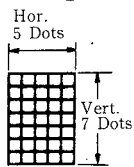Fig.12

Notes) ● H means a horizontal line; H=63.5(μs).
● Values in the Hor. column are when the oscillation frequency fosc is 5 MHz.

② Display blanking(BLK)

This bit specifies a display screen state. When BLK is "1", all the display is suppressed regardless of other date. To display, it is necessary to reset BLK to "0". The BLK status is indefinite when power is turned on.

③ Background blanking(BLKB)

This bit specifies a background display state. When BLKB is "1", background output(VOB) is suppressed regardless of other data. To display the background, it is necessary to reset BLKB to "0". The BLKB status is indefinite when power is turned on.

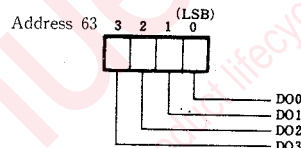(4) General purpose register(DO3-0)

Address 63

Fig.13 General Purpose Output Register

This is an output with 4-bits latch, and data written in DO3-0 is outputted to output pins(DO3-DO0).
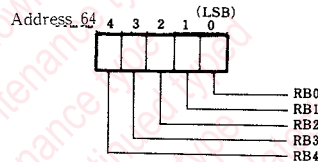
(5) Per-line blanking register(RB4-0)

Address 64

Fig.14 Per-line Blanking Register

These bits specify a per-line display state. If one of RB0-RB4 is set to "1", a display of the line corresponding to that bit is suppressed.

When displaying a line, therefore, it is necessary to reset the bit corresponding to that line to "0". The status of RB0-4 is indefinite when power is turned on.

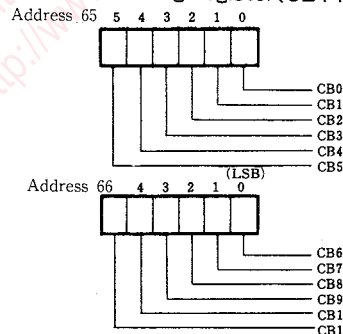(6) Per-column blanking register(CB11-0)

Address 65

Address 66

Fig.15 Per-column Blanking Register

These bits specify a per-column display state. If one of CB0-11 is set to "1", a display of the column corresponding to that bit is suppressed. When displaying a column, therefore, it is necessary to reset the bit corresponding to that column to "0". The status of CB0-11 is indefinite when power is turned on.

6. Data Write

The MN1237A/MN1237AD has two modes for writing data in the memory.

① Direct address mode

This mode is set when ADM is at the "L" level. When a signal inputted to the LDI terminal changes from "L" to "H", the 7-bit data of DA6-DA0 is latched to the memory address register. When a signal at the LDI terminal changes from "H" to "L", the 6-bit data of DA5-DA0 is written in the memory at the address specified by the memory address register. Fig.16 shows this timing.
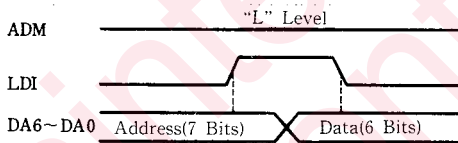

Fig.16 Direct Address Mode Timing

② Address increment mode

This mode is set when ADM is at the "H" level. When a signal inputted to the LDI terminal changes from "L" to "H", the data already latched in the memory address register is incremented. When a signal at the LDI terminal changes from "H" to "L", the 6-bit data of DA5-DA0 is written in the memory at the address specified by the memory address register which was incremented. Fig.17 shows this timing.
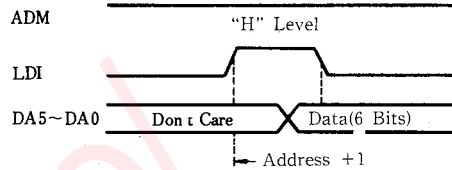
■ Applied Circuit

Fig.17 Address Increment Mode Timing

7. Rounding Function

When a character pattern on the ROM is as shown in Fig.18, the rounding function automatically adds 1 dot in the middle of opposite angles to display it. This function allows more natural display than general 5×7-dot display.
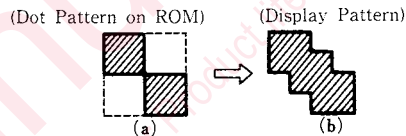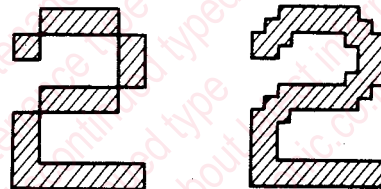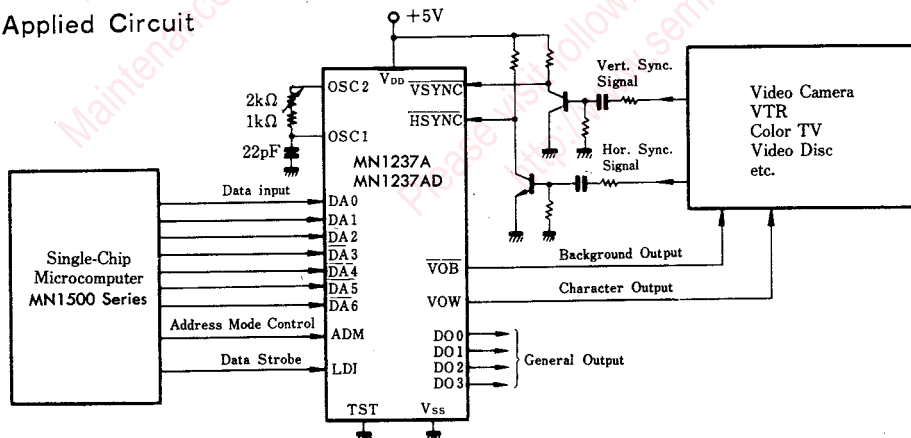
(Dot Pattern on ROM) (Display Pattern)

Fig.18 Rounding Function

(a) 5×7-dot Display   (b) Display by MN1237A/AD

Fig.19 Display Example

Request for your special attention and precautions in using the technical information and semiconductors described in this book

(1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.

(2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information described in this book.

(3) The products described in this book are intended to be used for standard applications or general electronic equipment (such as office equipment, communications equipment, measuring instruments and household appliances).
Consult our sales staff in advance for information on the following applications:
・Special applications (such as for airplanes, aerospace, automobiles, traffic control equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.
・Any applications other than the standard applications intended.

(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
 Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

(7) This book may be not reprinted or reproduced whether wholly or partially, without the prior written permission of our company.

20080805