

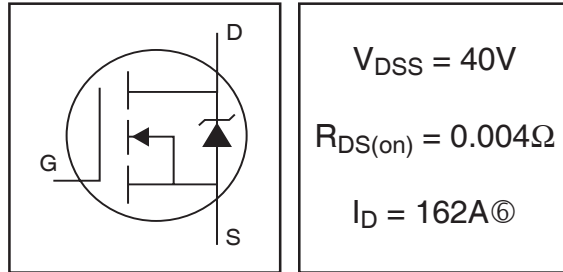


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PD-95104

IRF1404SPbF
IRF1404LPbF
HEXFET® Power MOSFET

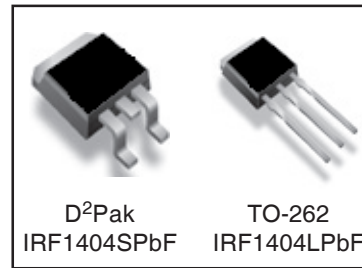
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead-Free



Description

Seventh Generation HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application. The through-hole version (IRF1404L) is available for low-profile applications.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V\text{Ⓞ}$	162Ⓞ	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V\text{Ⓞ}$	115Ⓞ	
I_{DM}	Pulsed Drain Current ①Ⓞ	650	
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation	3.8	W
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche EnergyⓄ	519	mJ
I_{AR}	Avalanche Current①	95	A
E_{AR}	Repetitive Avalanche Energy①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ③Ⓞ	5.0	V/ns
T_J	Operating Junction and	-55 to +175	°C
T_{STG}	Storage Temperature Range	-55 to +175	
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mounted, steady-state)*	—	40	



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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	40	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.036	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	0.0035	0.004	Ω	V _{GS} = 10V, I _D = 95A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = 10V, I _D = 250μA
g _{fs}	Forward Transconductance	106	—	—	S	V _{DS} = 25V, I _D = 60A ⑦
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 40V, V _{GS} = 0V
		—	—	250		V _{DS} = 32V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V _{GS} = -20V
Q _g	Total Gate Charge	—	160	200	nC	I _D = 95A
Q _{gs}	Gate-to-Source Charge	—	35	—		V _{DS} = 32V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	42	60		V _{GS} = 10V ④ ⑦
t _{d(on)}	Turn-On Delay Time	—	17	—	ns	V _{DD} = 20V
t _r	Rise Time	—	140	—		I _D = 95A
t _{d(off)}	Turn-Off Delay Time	—	72	—		R _G = 2.5Ω
t _f	Fall Time	—	26	—		R _D = 0.21Ω ④ ⑦
L _S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C _{iss}	Input Capacitance	—	7360	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	1680	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	240	—		f = 1.0MHz, See Fig. 5 ⑦
C _{oss}	Output Capacitance	—	6630	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	1490	—		V _{GS} = 0V, V _{DS} = 32V, f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance ⑤ ⑦	—	1540	—		V _{GS} = 0V, V _{DS} = 0V to 32V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	162 ⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	650		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 95A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	71	110	ns	T _J = 25°C, I _F = 95A
Q _{rr}	Reverse Recovery Charge	—	180	270	nC	di/dt = 100A/μs ④ ⑦
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting T_J = 25°C, L = 0.12mH
R_G = 25Ω, I_{AS} = 95A. (See Figure 12)
- ③ I_{SD} ≤ 95A, di/dt ≤ 150A/μs, V_{DD} ≤ V_{(BR)DSS},
T_J ≤ 175°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ C_{oss eff.} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A
- ⑦ Use IRF1404 data and test conditions.

* When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

IRF1404S/LPbF

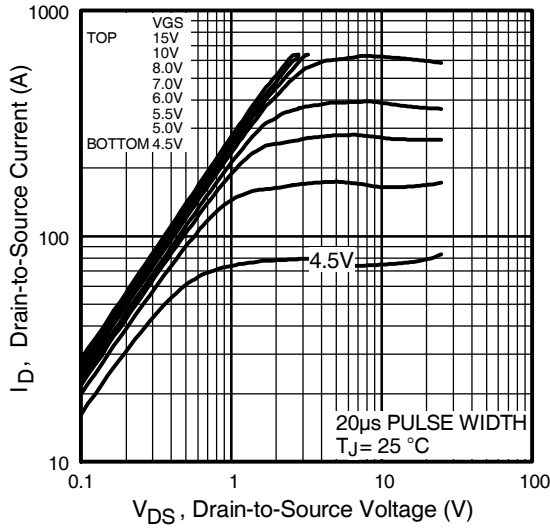


Fig 1. Typical Output Characteristics

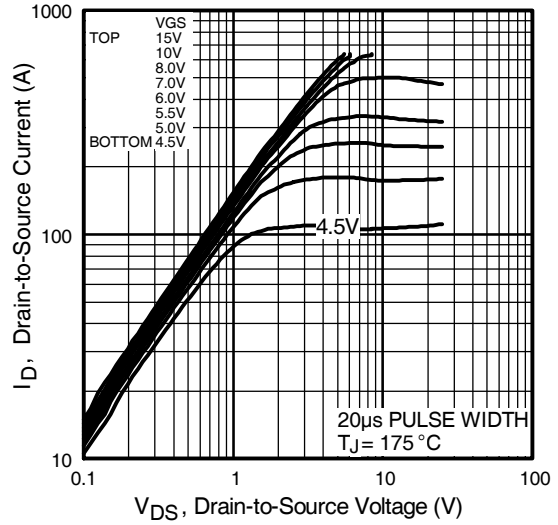


Fig 2. Typical Output Characteristics

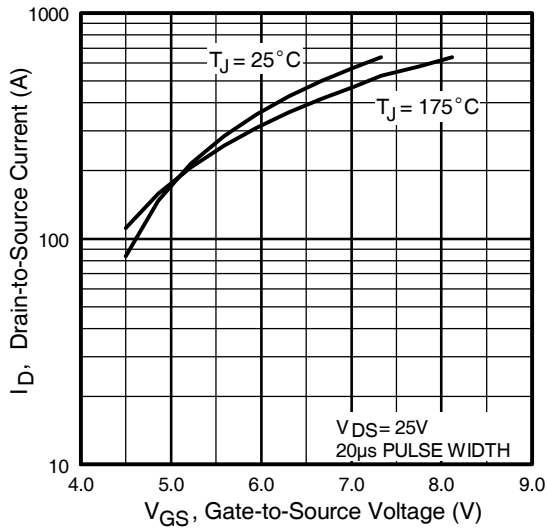


Fig 3. Typical Transfer Characteristics

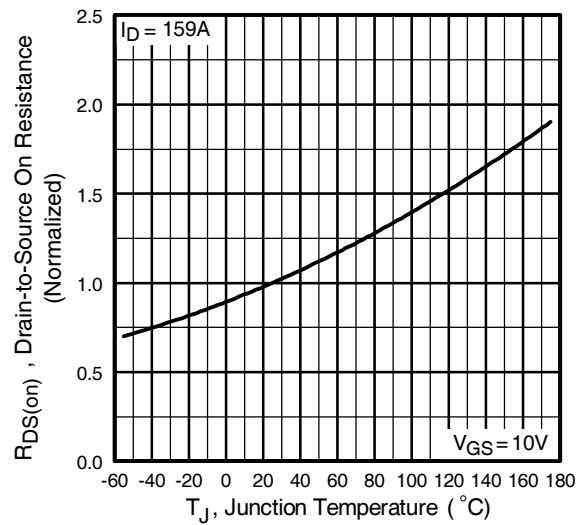


Fig 4. Normalized On-Resistance Vs. Temperature

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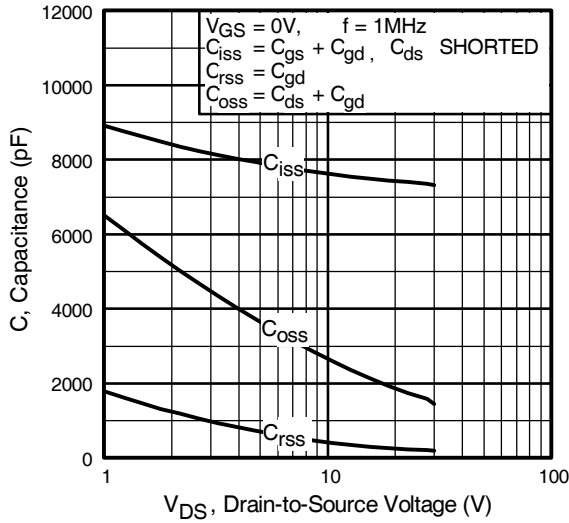


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

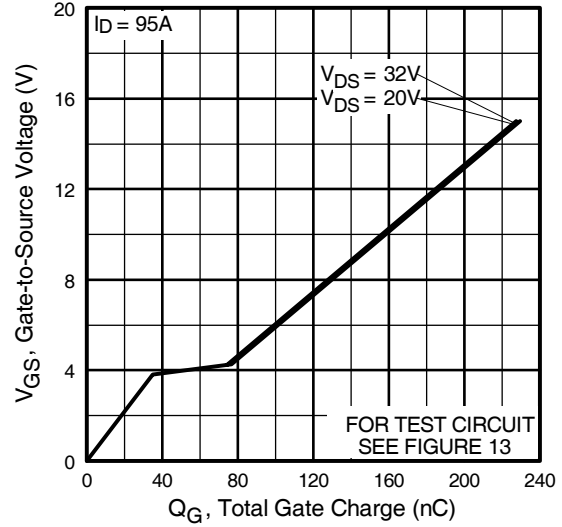


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

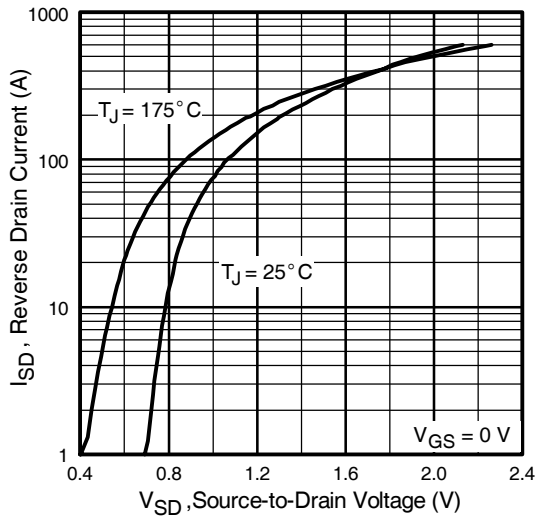


Fig 7. Typical Source-Drain Diode Forward Voltage

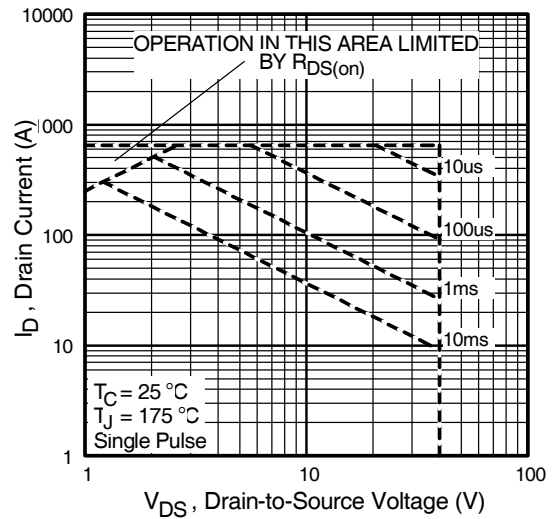


Fig 8. Maximum Safe Operating Area



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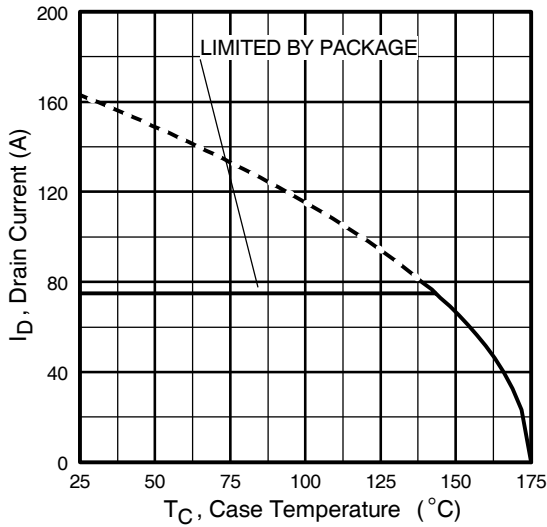


Fig 9. Maximum Drain Current Vs. Case Temperature

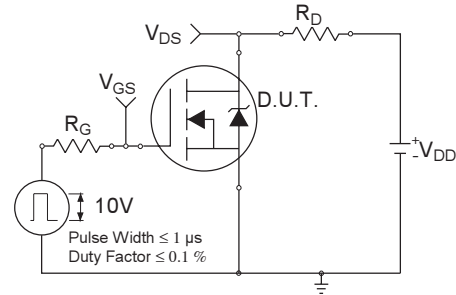


Fig 10a. Switching Time Test Circuit

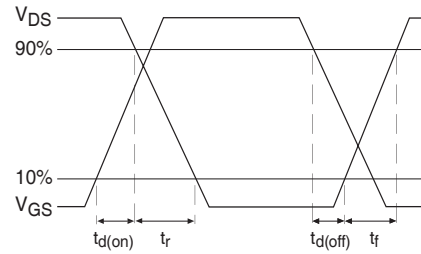


Fig 10b. Switching Time Waveforms

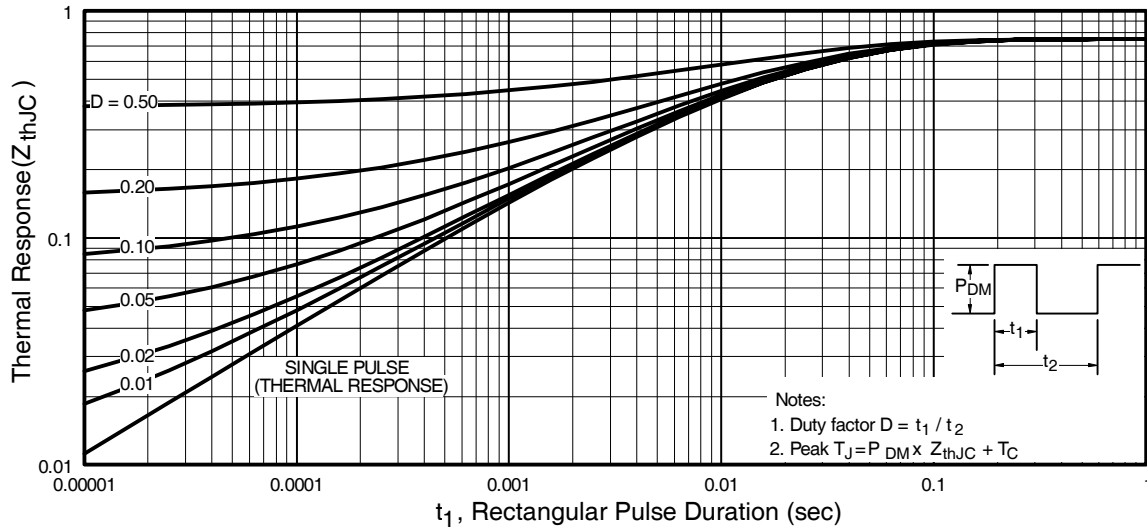


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



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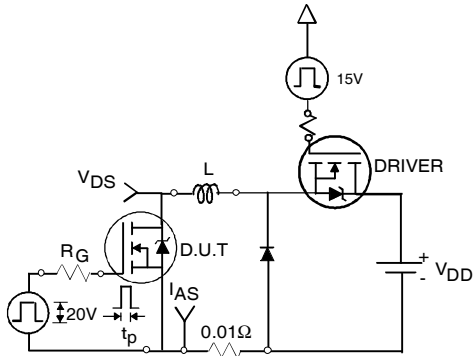


Fig 12a. Unclamped Inductive Test Circuit

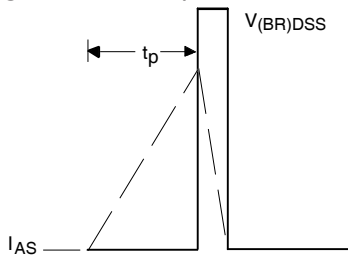


Fig 12b. Unclamped Inductive Waveforms

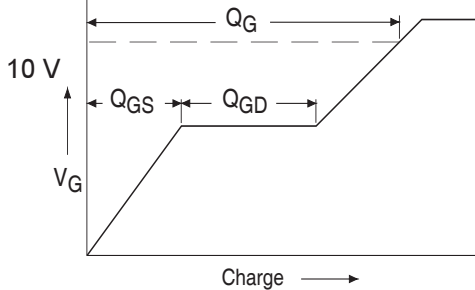


Fig 13a. Basic Gate Charge Waveform

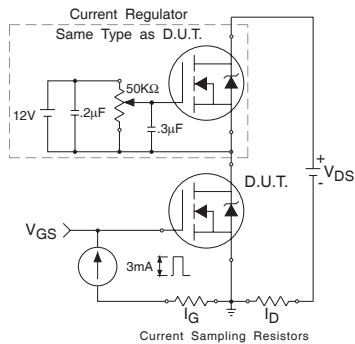


Fig 13b. Gate Charge Test Circuit

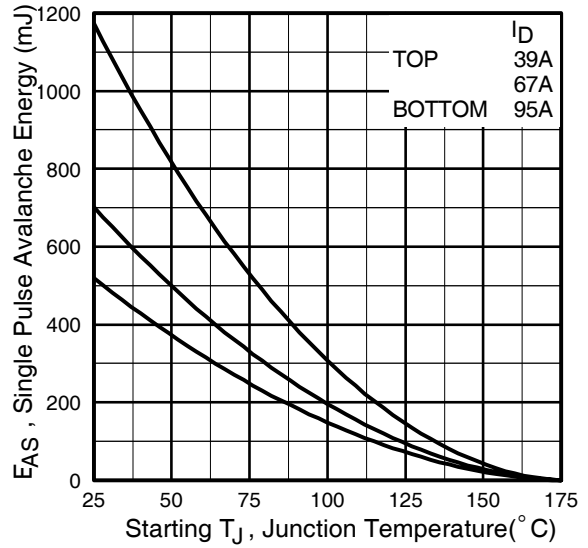


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

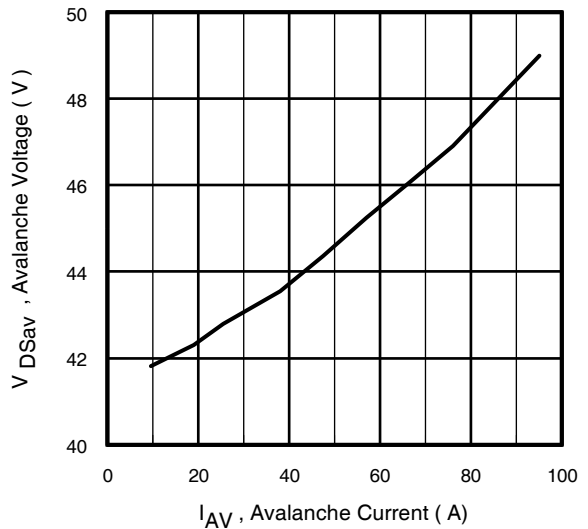


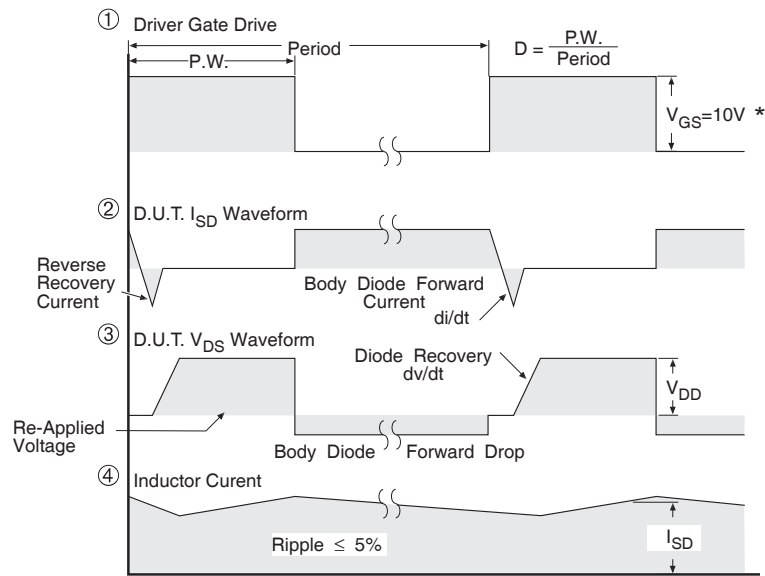
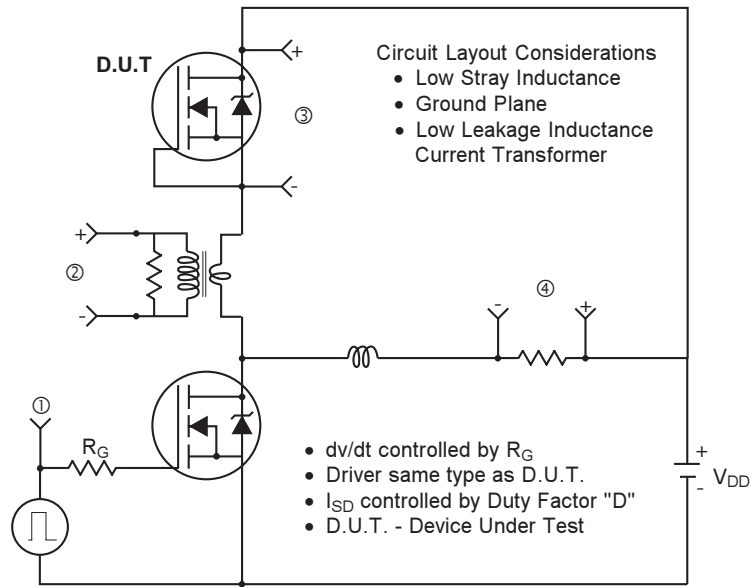
Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current



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Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-channel HEXFET® Power MOSFETs

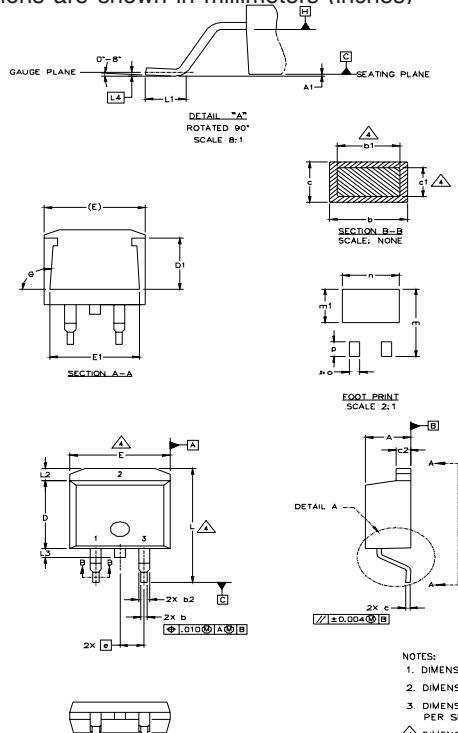


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D²Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1		0.127		.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.43	0.63	.017	.025	
c1	0.38	0.74	.015	.029	4
c2	1.14	1.40	.045	.055	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2		1.65		.065	
L3		1.27		.070	
L4	0.25 BSC		.010 BSC		
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK	DIODES
1.- GATE	1.- GATE	1.- ANODE *
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

* PART DEPENDENT.

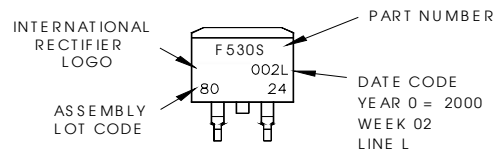
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

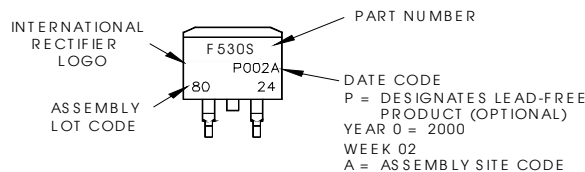
D²Pak Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line
position indicates "Lead-Free"



OR



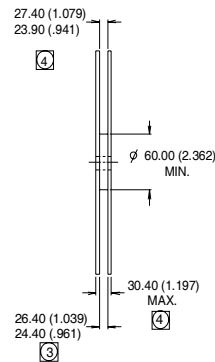
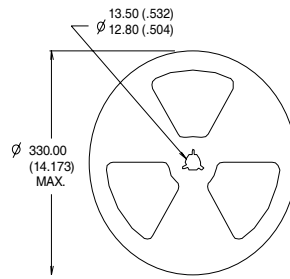
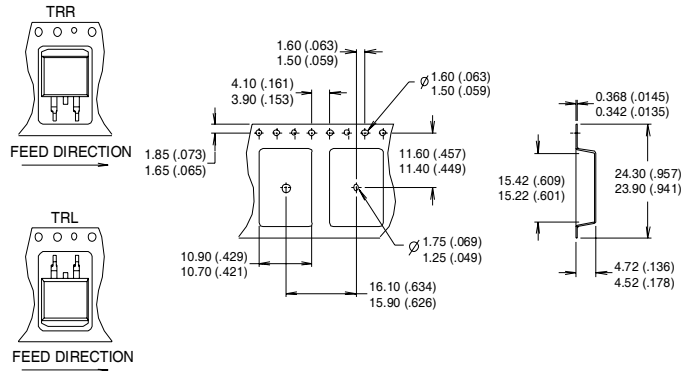


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D²Pak Tape & Reel Infomation

Dimensions are shown in millimeters (inches)



- NOTES:
1. COMFORMS TO EIA-418.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION MEASURED @ HUB.
 4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.