AO3421

General Description

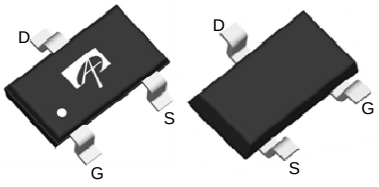
The AO3421 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications.

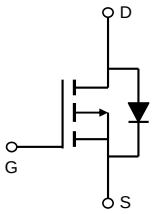
Product Summary

V_{DS}	-30V
I_D (at V_{GS}=-10V)	-2.6A
$R_{DS(ON)}$ (at V_{GS}=-10V)	< 110mΩ
$R_{DS(ON)}$ (at V_{GS}=-4.5V)	< 180mΩ

SOT23

Top View **Bottom View**





Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A=25℃	I_D	-2.6	A
	T_A=70℃		-2.2	
Pulsed Drain Current [C]		I_{DM}	-20	
Power Dissipation [B]	T_A=25℃	P_D	1.4	W
	T_A=70℃		1	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	70	90	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		100	125	℃/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	63	80	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250μA, V_{GS}=0V		-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V				-1	μA
			T_J=55℃			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V				±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250μA		-1.4	-1.9	-2.4	V
$I_{D(ON)}$	On state drain current	V_{GS}=-10V, V_{DS}=-5V		-20			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-2.6A			77	110	mΩ
			T_J=125℃		100	140	
		V_{GS}=-4.5V, I_D=-2A			125	180	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-2.6A			5		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V			-0.8	-1	V
I_S	Maximum Body-Diode Continuous Current					-1.5	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz			197	240	pF
C_{oss}	Output Capacitance				42		pF
C_{rss}	Reverse Transfer Capacitance				26	37	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		3.5	7.2	11.0	Ω
SWITCHING PARAMETERS							
Q_g(10V)	Total Gate Charge	V_{GS}=-10V, V_{DS}=-15V, I_D=-2.6A			4.3	5.2	nC
Q_g(4.5V)	Total Gate Charge				2.2	3	nC
Q_{gs}	Gate Source Charge				0.7		nC
Q_{gd}	Gate Drain Charge				1.1		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-15V, R_L=5.8Ω, R_{GEN}=3Ω			7.5		ns
t_r	Turn-On Rise Time				4.1		ns
$t_{D(off)}$	Turn-Off DelayTime				11.8		ns
t_f	Turn-Off Fall Time				3.8		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-2.6A, dI/dt=100A/μs			11.3	14	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-2.6A, dI/dt=100A/μs			4.4		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25℃. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150℃, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150℃. Ratings are based on low frequency and duty cycles to keep initialT_J=25℃.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150℃. The SOA curve provides a single pulse ratin g.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

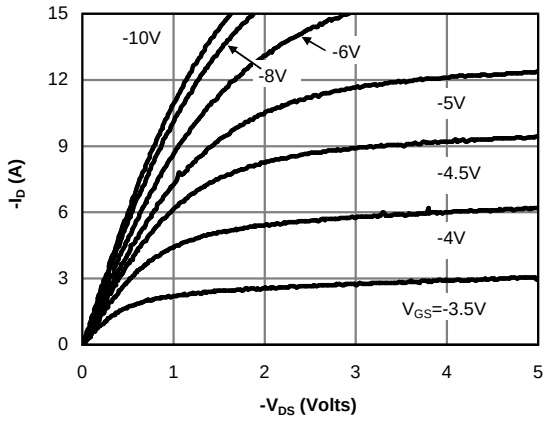


Fig 1: On-Region Characteristics (Note E)

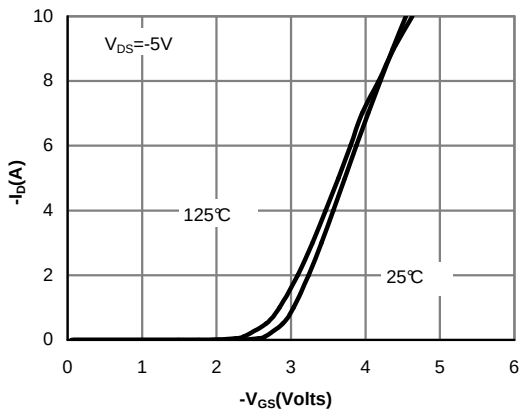


Figure 2: Transfer Characteristics (Note E)

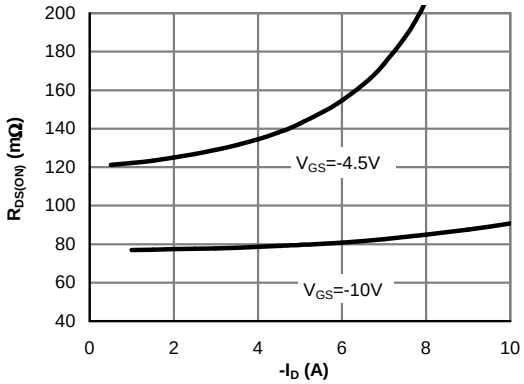


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

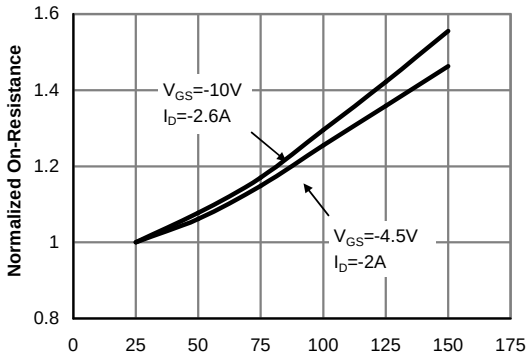


Figure 4: On-Resistance vs. Junction Temperature (Note E)

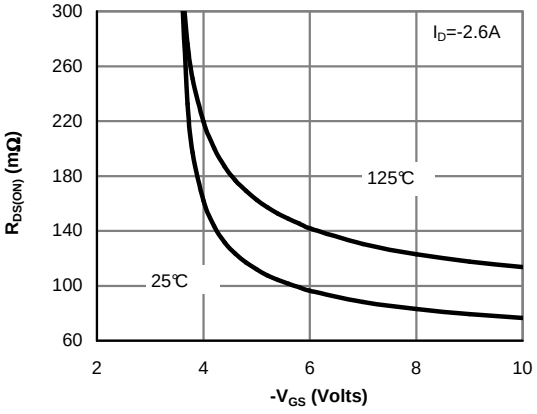


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

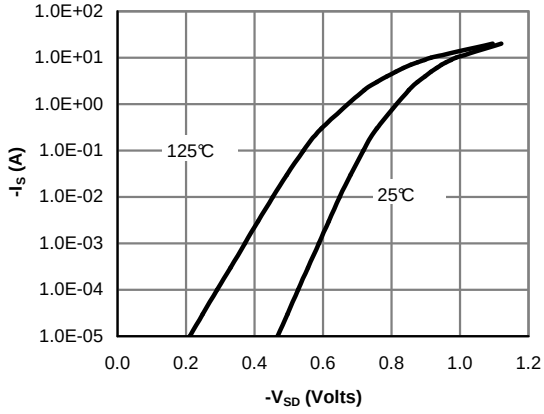


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

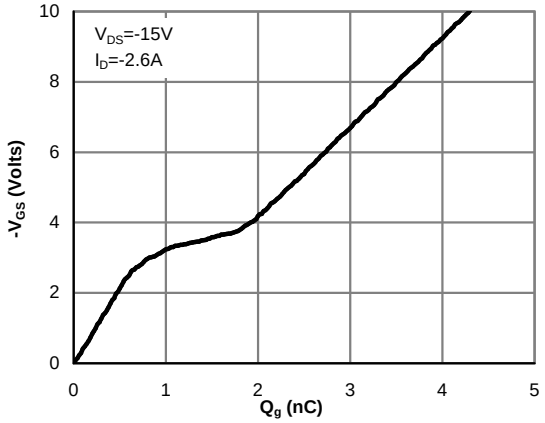


Figure 7: Gate-Charge Characteristics

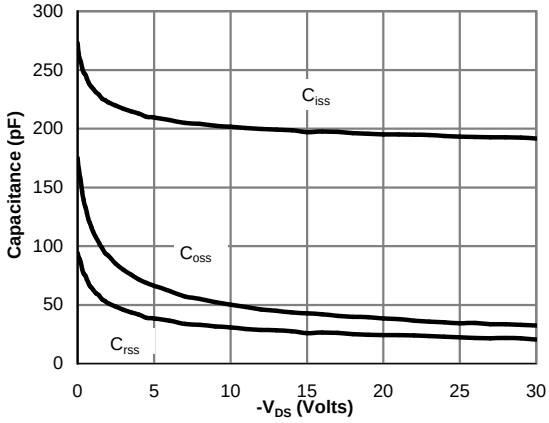


Figure 8: Capacitance Characteristics

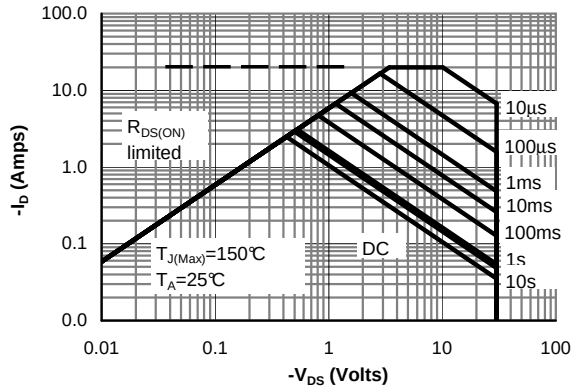


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

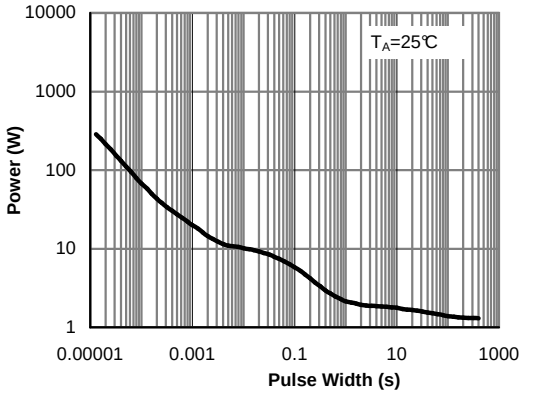


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

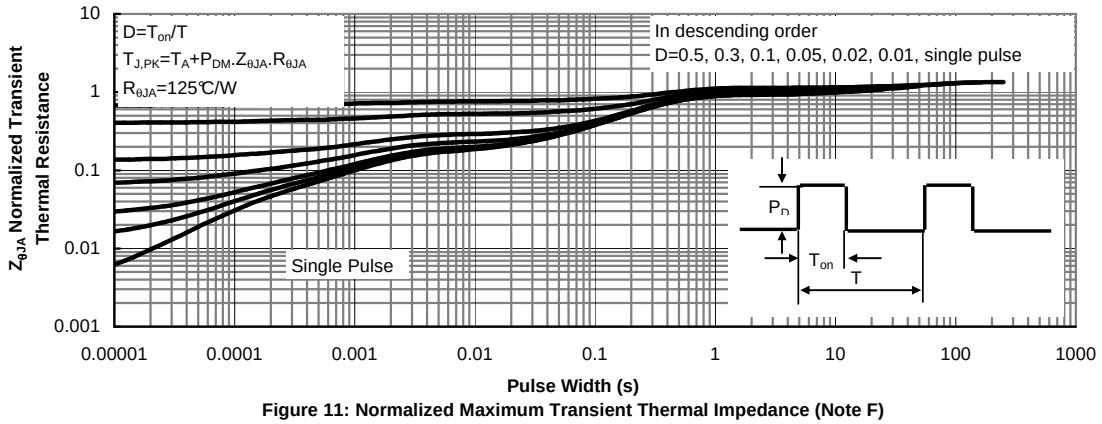
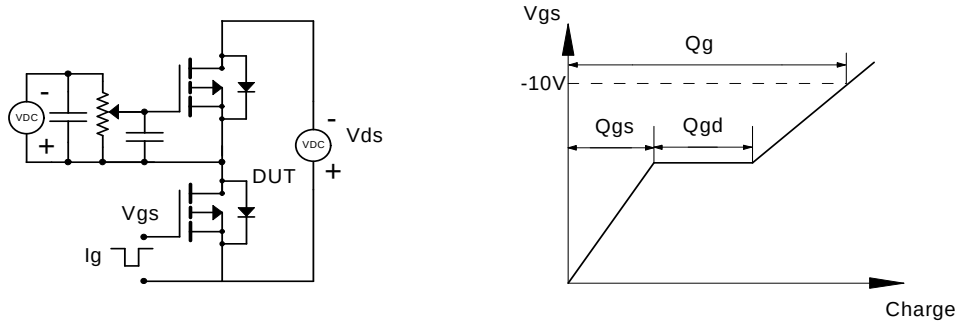
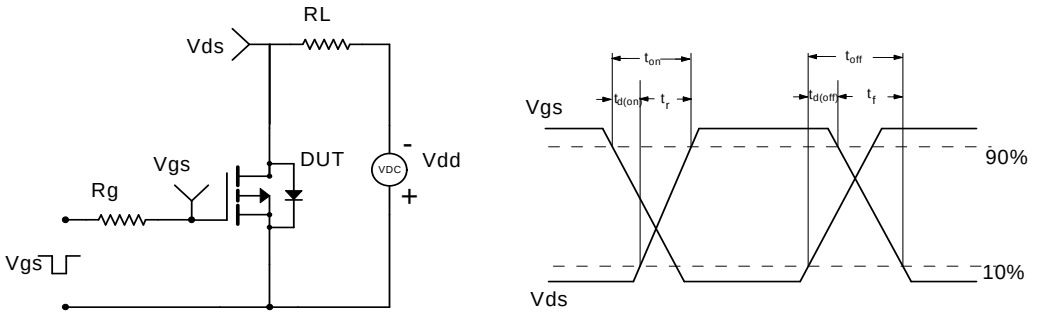


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

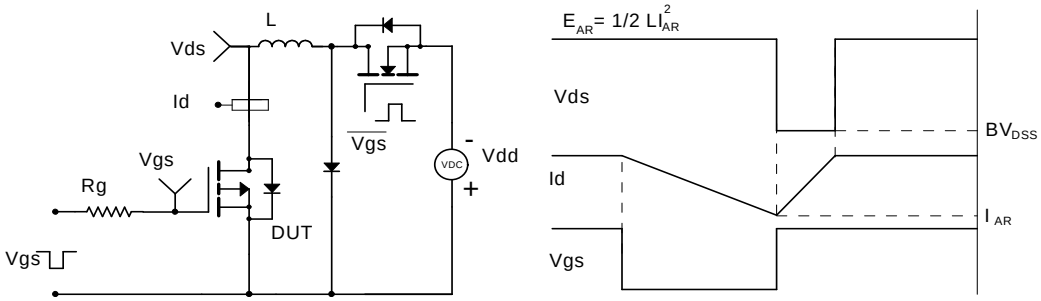
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms