NEC
NEC Electronics Inc.

μPD78C14 Family (μPD78C10A/C11A/C12A/C14/C14A/CP14) 8-Bit, Single-Chip Microcontrollers With A/D Converter

September 1993

Description

This family of microcontrollers integrates sophisticated on-chip peripheral functions normally provided by external components. Their internal 16-bit ALU and data paths, combined with a powerful instruction set and addressing, make the devices appropriate in data processing as well as control applications.

The devices integrate a 16-bit ALU, 4K, 8K, or 16K-byte ROM, 256-byte RAM, an eight-channel A/D converter, a multifunction 16-bit timer/event counter, two 8-bit timers, a USART, and two zero-cross detect inputs on a single die, allowing their use in fast, high-end processing applications. This involves analog signal interface and processing.

The μPD78C14 family includes: 4K, 8K, and 16K-byte mask ROM devices, embedded with a custom customer program; ROMless devices for use with up to 64K-bytes of external memory; and 16K-byte EPROM or OTP ROM devices for prototyping and low-volume production. The μPD78C11A/C12A/C14A also have mask optional pullup resistors available on ports A, B, and C.

Features

- CMOS technology
  - 25 mA operating current (78C10A/C11A/C12A)
  - 30 mA operating current (78C14/C14A)
- Complete single-chip microcontroller
  - 16-bit ALU
  - 4K, 8K, or 16K x 8 ROM
  - 256-byte RAM
- 44 I/O lines
- Mask optional pullup resistors
  - Ports A, B, and C (μPD78C11A/C12A/C14A only)
- Two zero-cross detect inputs
- Two 8-bit timers
- Expansion capabilities
  - 8085A-like bus
  - 60K-byte external memory address range
- Eight-channel, 8-bit A/D converter
  - Autoscan mode
  - Channel select mode
- Full-duplex USART
  - Synchronous and asynchronous
- 159 instructions
  - 16-bit arithmetic, multiply, and divide
  - HALT and STOP instructions
- 0.8-μs instruction cycle time (15-MHz operation)
- Prioritized interrupt structure
  - Three external
  - Eight internal
- Standby function
- On-chip clock generator

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Ordering Information

Part Number (Note 1)	Package	Package Drawing	Quality Grade (Note 3)
ROMless			
μPD78C10ACW	64-pin SDIP	P64C-70-750A, C	Standard
AGF-3BE	64-pin QFP (Note 2)	P64GF-100-3B8, 3BE-1	Standard
AGF(A)-3BE			Special
AGQ-36	64-pin QUIP	P64GQ-100-36	Standard
AGQ(A)-36			Special
AL	68-pin PLCC	P68L-50A1-1	Standard
AL(A)			Special
4K Mask ROM			
μPD78C11ACW-xxx	64-pin SDIP	P64C-70-750A, C	Standard
AGF-xxx-3BE	64-pin QFP (Note 2)	P64GF-100-3B8, 3BE-1	Standard
AGF(A)-xxx-3BE			Special
AGQ-xxx-36	64-pin QUIP	P64GQ-100-36	Standard
AGQ(A)-xxx-36			Special
AGQ-xxx-37	64-pin QUIP (straight)	P64GQ-100-37	Standard
AL-xxx	68-pin PLCC	P68L-50A1-1	Standard
AL(A)-xxx			Special
8K Mask ROM			
μPD78C12ACW-xxx	64-pin SDIP	P64C-70-750A, C	Standard
AG-xxx-37	64-pin QUIP (straight)	P64GQ-100-37	Standard
AG-xxx-36	64-pin QUIP	P64GQ-100-36	Standard
AG(A)-xxx-36			Special
AGF-xxx-3BE	64-pin QFP (Note 2)	P64GF-100-3B8, 3BE-1	Standard
AL-xxx	68-pin PLCC	P68L-50A1-1	Standard
AL(A)-xxx			Special
16K Mask ROM			
μPD78C14AG-xxx-AB8	64-pin QFP	P64GC-80-AB8-2	Standard
CW-xxx	64-pin SDIP	P64C-70-750A, C	
G-xxx-36	64-pin QUIP	P64GQ-100-36	
G-xxx-37	64-pin QUIP (straight)	P64GQ-100-37	
G-xxx-1B	64-pin QFP (Note 2)	P64G-100-12, 1B-1	
GF-xxx-3BE	64-pin QFP (Note 2)	P64GF-100-3B8, 3BE-1	
L-xxx	68-pin PLCC	P68L-50A1-1	
16K OTP ROM			
μPD78CP14CW	64-pin SDIP	P64C-70-750A, C	Standard
G-36	64-pin QUIP	P64GQ-100-36	
G-37	64-pin QUIP (straight)	P64GQ-100-37	
GF-3BE	64-pin QFP (Note 2)	P64GF-100-3B8, 3BE-1	
L	68-pin PLCC	P68L-50A1-1	

Ordering Information (cont)

Part Number (Note 1)	Package	Package Drawing	Quality Grade (Note 3)
16K UV EPROM			
μPD78CP14DW	64-pin CER SDIP w/window	P64DW-70-750A	Standard
R	64-pin CER QUIP w/window	P64RQ-100-A	
16K OTP ROM			
μPD78CP14G(A)-36	64-pin QUIP	P64GQ-100-36	Special

Notes:

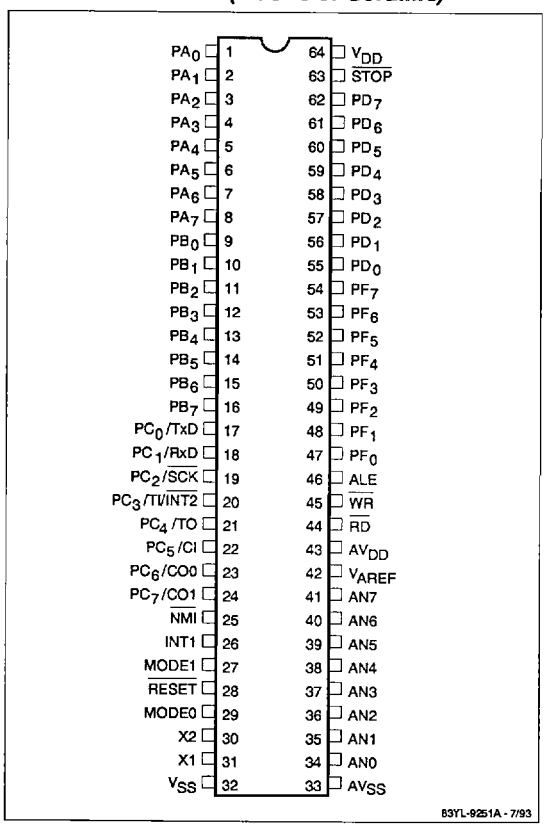
(1) xxx indicates ROM code suffix

(2) Engineering samples supplied in a ceramic QFP package

(3) Special grade devices have the symbol (A) embedded in the part number

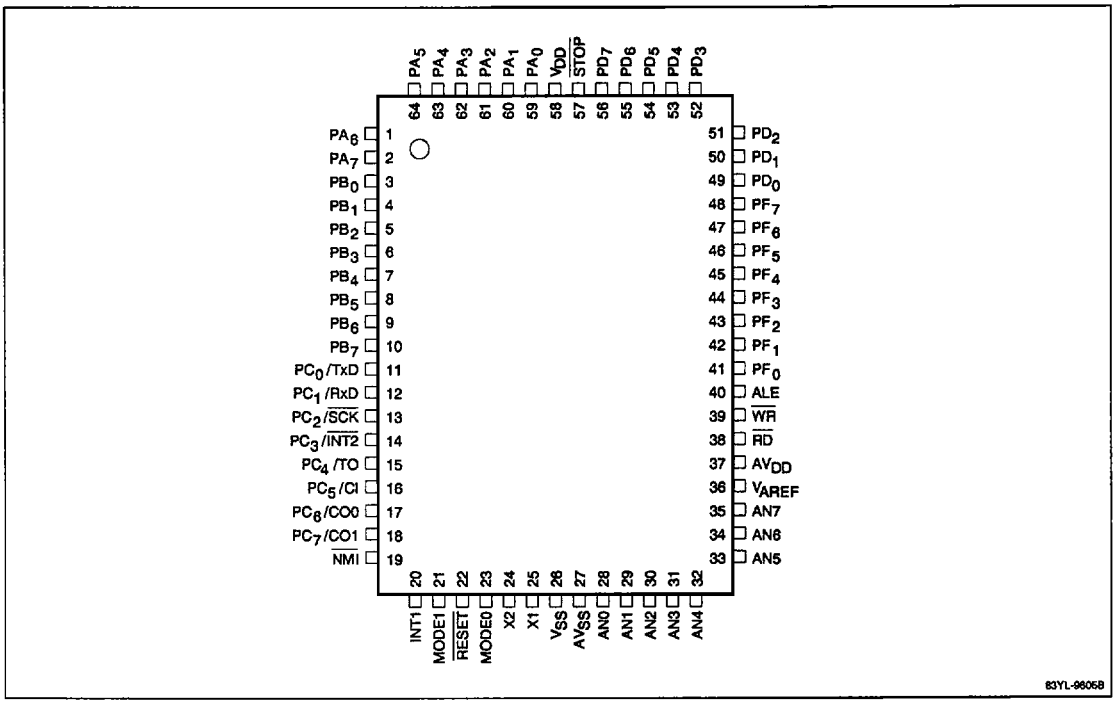
Pin Configurations

64-Pin QUIP or SDIP (Plastic or Ceramic)



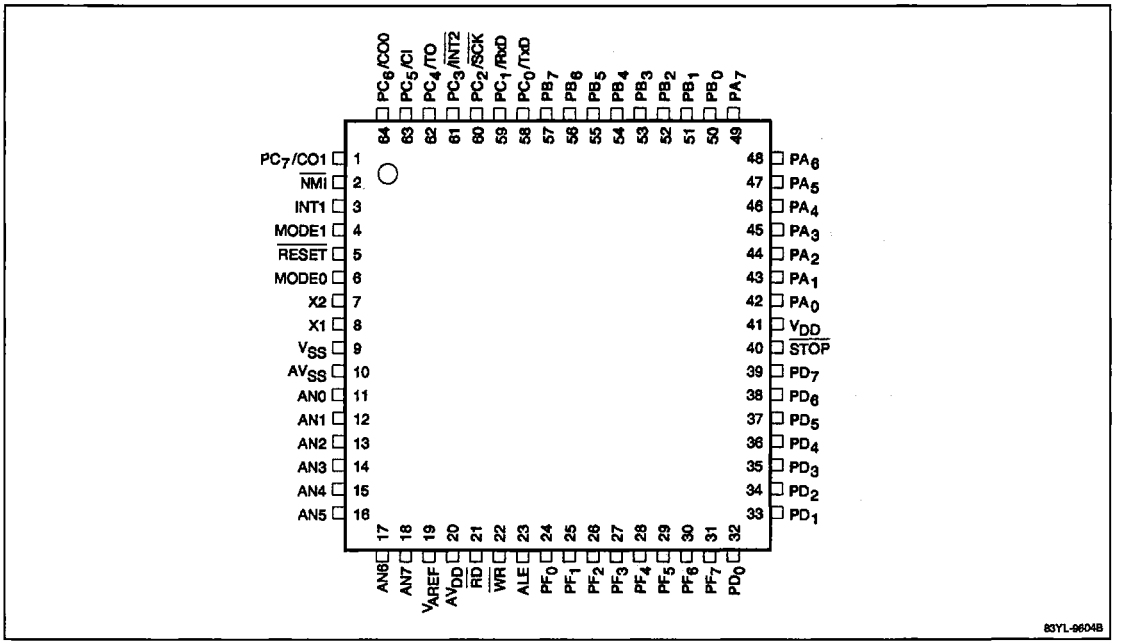
Pin Configurations (cont)

64-Pin QFP (20mm x 14mm)



Pin Configurations (cont)

64-Pin QFP (14mm x 14mm)



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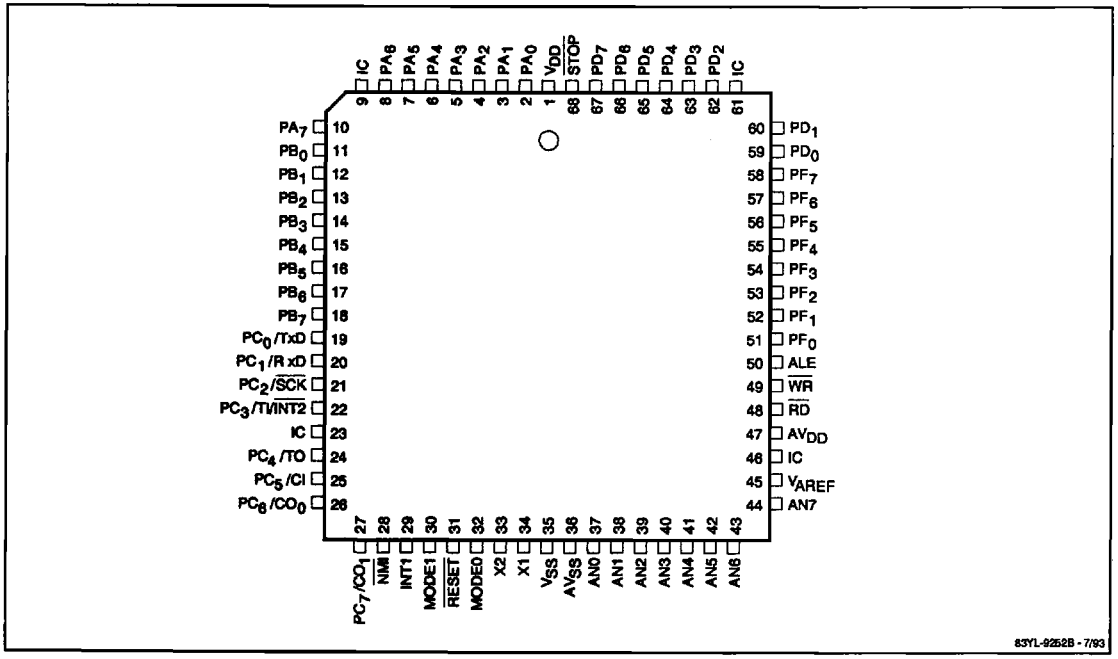
Pin Configurations (cont)

68-Pin PLCC



Pin Identification

Symbol	Function
ALE	Address latch enable output
AN0-AN7	A/D converter analog inputs 0-7
INT1	Interrupt request 1 input
MODE0	Mode 0 input; I/O memory output
MODE1	Mode 1 input
$\overline{NMI}$	Nonmaskable interrupt input
PA_0 - PA_7	Port A I/O
PB_0 - PB_7	Port B I/O
PC_0/TxD	Port C I/O line 0; transmit data output
PC_1/RxD	Port C I/O line 1; receive data input
$PC_2/\overline{SCK}$	Port C I/O line 2; serial clock I/O
PC_3/TI/$\overline{INT2}$	Port C I/O line 3; timer input; interrupt request 2 input
PC_4/TO	Port C I/O line 4; timer output
PC_5/CI	Port C I/O line 5; counter input
PC_6, PC_7/ CO_0,CO_1	Port C I/O lines 6, 7; counter outputs 0, 1
PD_0 - PD_7	Port D I/O; expansion memory address, data bus (bits AD_0 - AD_7)
PF_0 - PF_7	Port F I/O; expansion memory address, (bits AB_8 - AB_{15})
$\overline{RD}$	Read strobe output
$\overline{RESET}$	Reset input
$\overline{STOP}$	Stop mode control input
V_{AREF}	A/D converter reference voltage
$\overline{WR}$	Write strobe output
X1, X2	Crystal connections 1, 2
AV_{DD}	A/D converter power supply voltage
AV_{SS}	A/D converter power supply ground
V_{DD}	5 V power supply
V_{SS}	Ground
IC	Internal connection

PIN FUNCTIONS

ALE (Address Latch Enable). The ALE output is used to latch the address of PD_0 - PD_7 into an external latch.

AN0-AN7 (Analog Inputs). These are the eight analog inputs to the A/D converter. AN4-AN7 can also be used as a digital input for falling edge detection.

CI (Counter Input). External pulse input to timer/ event counter.

CO_0, CO_1 (Counter Outputs). Programmable waveform outputs based on timer/event counter.

INT1 (Interrupt Request 1). INT1 is a rising edge triggered, maskable interrupt input. It is also an ac-input, zero-cross detection terminal.

If the optional pullup resistor is specified for this pin on the μPD78C11A/C12A/C14A, the zero-cross detection circuitry will not function.

$\overline{INT2}$ (Interrupt Request 2). $\overline{INT2}$ is a falling edge triggered, maskable interrupt input. It is also an ac-input, zero-cross detection terminal.

MODE0, MODE1 (Mode 0, 1). The MODE0 and MODE1 inputs select the amount of external memory. MODE0 outputs the $\overline{IO}$ signal and MODE1 outputs the $\overline{M1}$ signal. An external pullup resistor to V_{DD} is required if the input is to be a logic high.

The value of this pullup resistor, R, is dependent on t_{CYC} and is calculated as follows: R in KΩ is $4 \leq R \leq 0.4\ t_{CYC}$ where t_{CYC} is in ns units.

$\overline{NMI}$ (Nonmaskable Interrupt). Falling edge, Schmitt-triggered nonmaskable interrupt input.

PA_0 - PA_7 (Port A). Port A is an 8-bit three-state port. Each bit is independently programmable as either input or output. Reset makes all lines of port A inputs. Mask optional pullup resistors are available on the μPD78C11A/C12A/C14A.

PB_0 - PB_7 (Port B). Port B is an 8-bit three-state port. Each bit is independently programmable as either input or output. Reset makes all lines of port B inputs. Mask optional pullup resistors are available on the μPD78C11A/C12A/C14A.

PC_0 - PC_7 (Port C). Port C is an 8-bit three-state port. Each bit is independently programmable as either input or output. Alternatively, the lines of port C can be used as control lines for the USART, interrupts, and timer. Reset makes all lines of port C inputs. Mask optional pullup resistors are available on the μPD78C11A/C12A/C14A.

PD_0 - PD_7 (Port D). Port D is an 8-bit three-state port. It can be programmed as either 8 bits of input or 8 bits of output. When external expansion memory is used, port D acts as the multiplexed address/data bus.

PF_0 - PF_7 (Port F). Port F is an 8-bit three-state port. Each bit is independently programmable as either input or output. When external expansion memory is used, port F outputs the high-order address bits.

$\overline{RD}$ (Read Strobe). The three-state $\overline{RD}$ output goes low to gate data from external devices onto the data bus. $\overline{RD}$ goes high during reset.

$\overline{RESET}$ (Reset). When the Schmitt-triggered $\overline{RESET}$ input is brought low, it initializes the device.

RxD (Receive Data). Serial data input terminal.

$\overline{SCK}$ (Serial Clock). Output for the serial clock when internal clock is used. Input for serial clock when external clock is used.

$\overline{STOP}$ (STOP Mode Control Input). A low-level input on $\overline{STOP}$ (Schmitt-triggered input) stops the system clock oscillator.

TI (Timer Input). Timer input terminal.

TO (Timer Output). The output of TO is a square wave with a frequency determined by the timer/counter.

TxD (Transmit Data). Serial data output terminal.

V_{AREF} (A/D Converter Reference). V_{AREF} sets the upper limit for the A/D conversion range.

$\overline{WR}$ (Write Strobe). The three-state $\overline{WR}$ output goes low to indicate that the data bus holds valid data. It is a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes high during reset.

X1, X2 (Crystal Connections). X1 and X2 are the system clock crystal oscillator terminals. X1 is the input for an external clock.

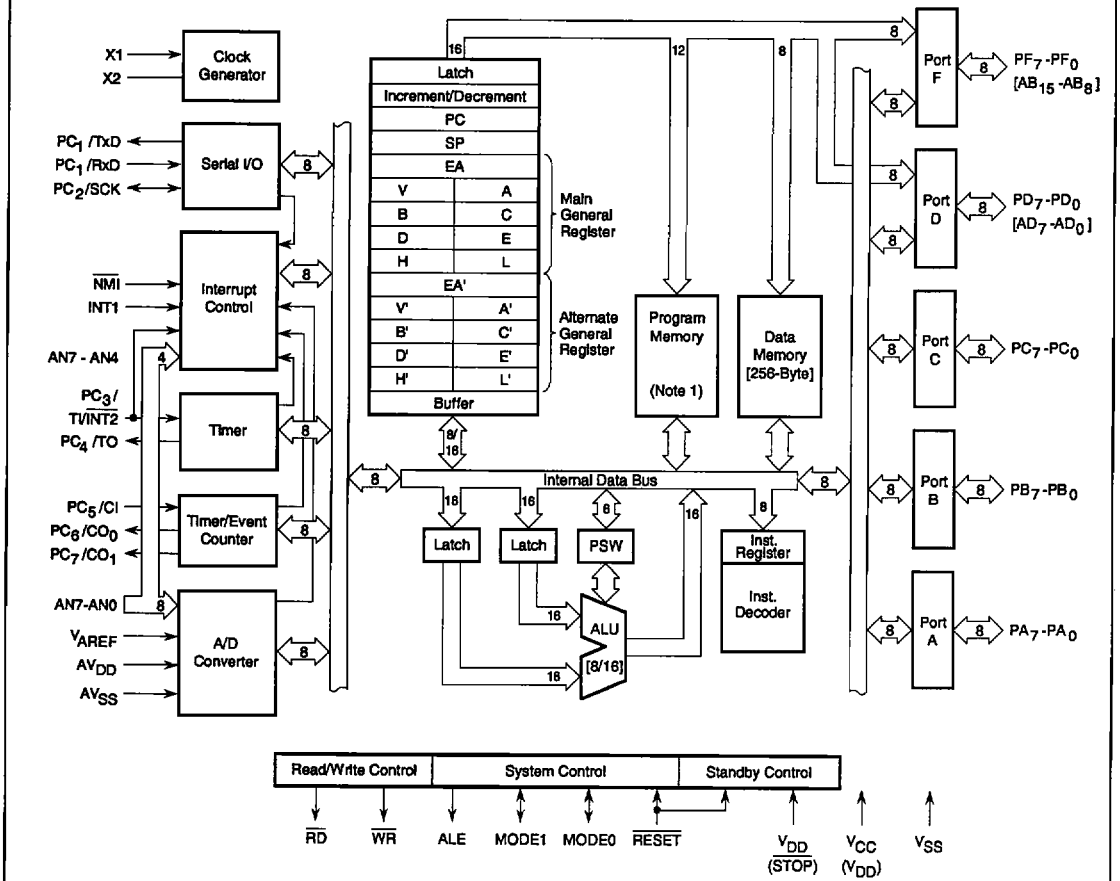
AV_{DD} (A/D Converter Power). This is the power supply voltage for the A/D converter.

AV_{SS} (A/D Converter Power Ground). AV_{SS} is the ground potential for the A/D converter power supply.

V_{DD} (Power Supply). V_{DD} is the +5-volt power supply.

V_{SS} (Ground). Ground potential.

Block Diagram



Note:

1. On-Chip ROM
   - 78C10A : 0
   - 78C11A : 4096 Bytes
   - 78C12A : 8192 Bytes
   - 78C14/C14A: 16384 Bytes
   - 78CP14 : 16384 Bytes EPROM/OTP ROM

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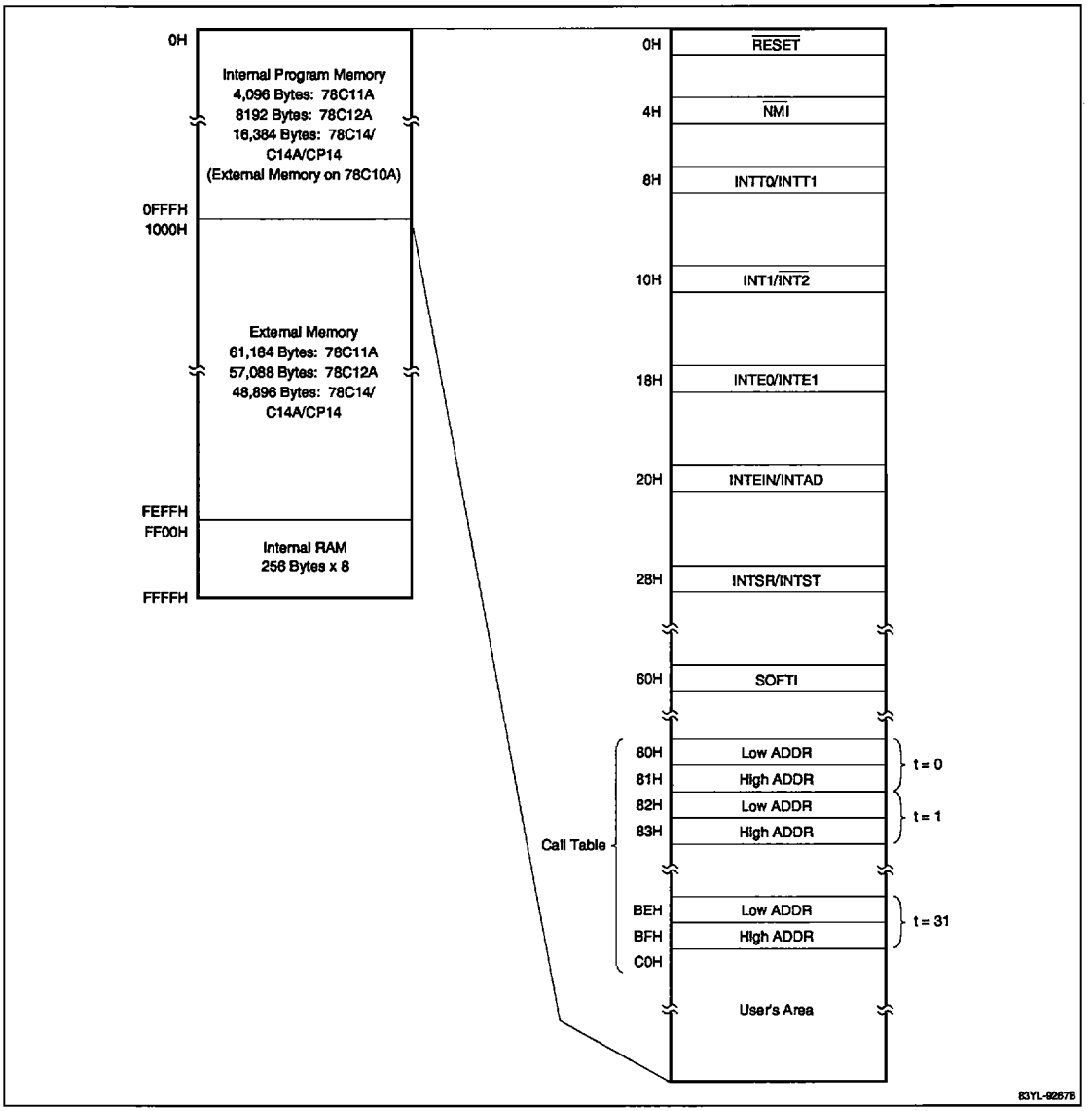
Figure 1. Memory Map



FUNCTIONAL DESCRIPTION

Memory Map

The μPD78C14 family can directly address up to 64K bytes of memory. Except for the on-chip ROM (or PROM) and RAM (FF00H-FFFFH), any memory location can be used as ROM or RAM. The memory map, figure 1, defines the 0 to 64K-byte memory space for the μPD78C14 family.

The μPD78CP14 can be programmed in software to have 4K, 8K, or 16K-bytes of internal program memory. This programming is transparent to the ROM-based device, allowing easy transfer of code to a ROM-based device.

Input/Output

The μPD78C14 family has 44 digital I/O lines, five 8-bit ports (ports A, B, C, D, F), and four digital input lines (AN4-AN7).

Analog Input Lines. AN0-AN7 are configured as analog input lines for the on-chip A/D converter. Lines AN4-AN7 can be used as digital input lines for falling-edge detection.

Port A, Port B, Port C, Port F. Each line of these ports can be individually programmed as an input or output. When used as I/O ports, all have latched outputs and high-impedance inputs. On the μPD78C11A/C12A/C14A, mask optional pullup resistors are available for ports A, B, and C.

Port D. Port D can be programmed as a byte input or a byte output.

Control Lines. Under software control, each line of port C can be configured individually as a control line for the serial interface, timer, and timer/counter or as an I/O port.

Memory Expansion. In addition to the single-chip operation mode, the μPD78C14 family has four memory expansion modes. Under software control, port D can provide a multiplexed low-order address and data bus; port F can provide a high-order address bus. Table 1 shows the relation between memory expansion modes and the pin configurations of port D and port F.

Table 1. Memory Expansion Modes and Port Configurations

Memory Expansion	Port	Port Configuration
None	Port D	I/O port
	Port F	I/O port
256 bytes	Port D	Multiplexed address/data bus
	Port F	I/O port
4K bytes	Port D	Multiplexed address/data bus
	Port F (PF_0-PF_3)	Address bus
	Port F (PF_4-PF_7)	I/O port
16K bytes	Port D	Multiplexed address/data bus
	Port F (PF_0-PF_5)	Address bus
	Port F (PF_6-PF_7)	I/O port
60K bytes	Port D	Multiplexed address/data bus
	Port F	Address bus

Timers

The two 8-bit timers may be programmed independently or cascaded as a 16-bit timer. The timer can be software set to increment at intervals of four machine cycles (0.8 μs at 15-MHz operation) or 128 machine cycles (25.6 μs at 15 MHz), or to increment on receipt of a pulse at TI. Figure 2 is the block diagram for the timer.

Timer/Event Counter

The 16-bit multifunctional timer/event counter (figure 3) can be used for the following operations:

- Interval timer
- External event counter
- Frequency measurement
- Pulse-width measurement
- Programmable frequency and duty cycle waveform output
- Single-pulse output

8-Bit A/D Converter

- Eight input channels
- Four conversion result registers
- Two powerful operation modes
  — Autoscan mode
  — Channel select mode
- Successive approximation technique
- Absolute accuracy: 0.6% FSR ± 1/2 LSB
- Conversion range: 0 to 5 V
- Conversion time: 38.4 μs
- Interrupt generation

Figure 2. Timer Block Diagram

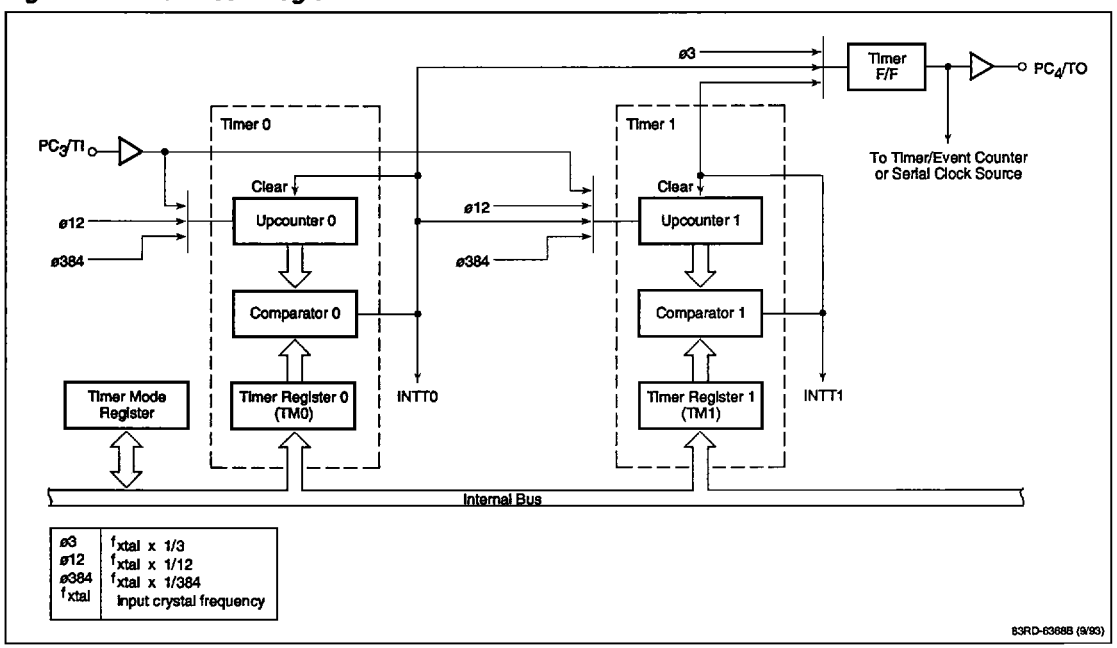


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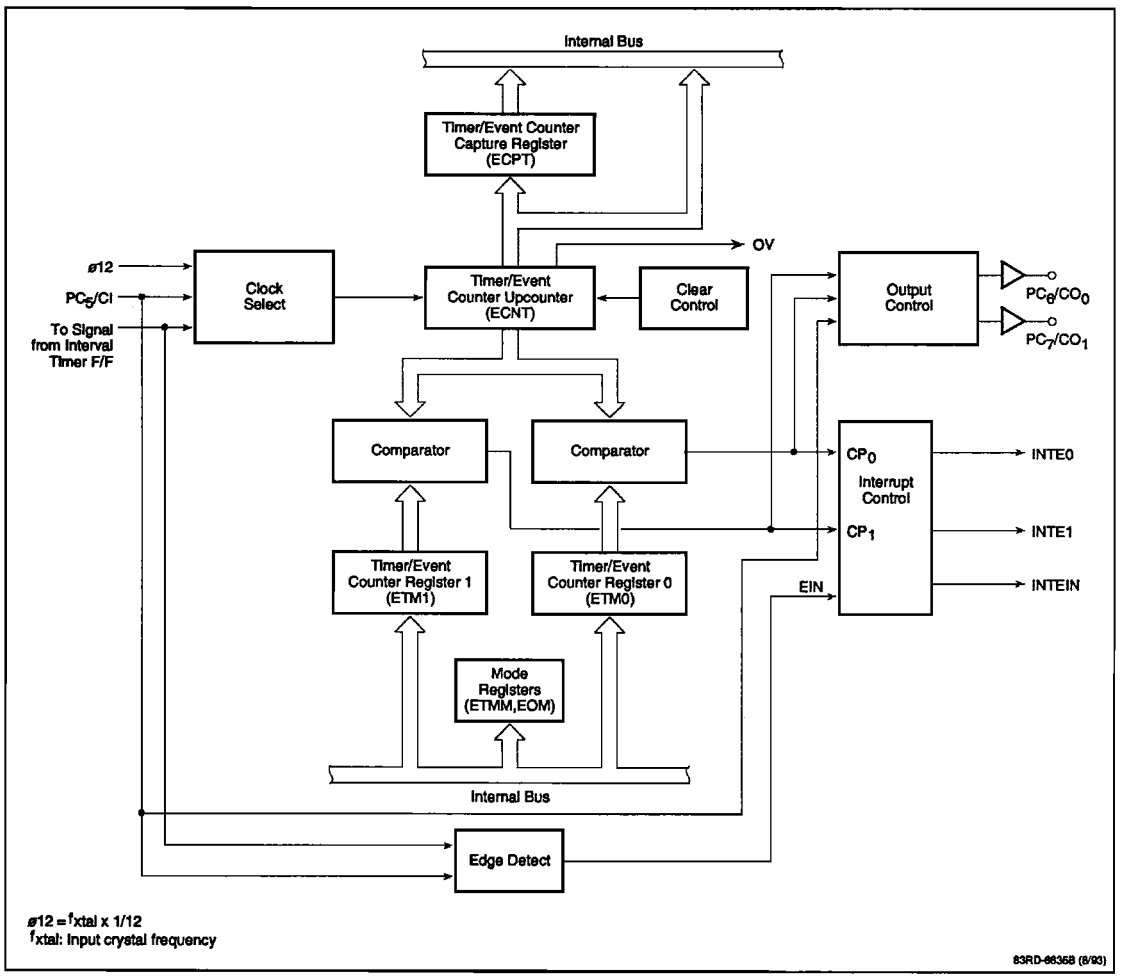
Figure 3. Block Diagram for the Timer/Event Counter



Analog/Digital Converter

The μPD78C14 family features an 8-bit, high-speed, high accuracy A/D converter. The A/D converter is made up of a 256-resistor ladder and a successive approximation register (SAR). There are four conversion result registers (CR0-CR3).

The eight-channel analog input may be operated in either of two modes. In the select mode, the conversion value of one analog input is sequentially stored in CR0-CR3. In the scan mode, either the upper four channels or the lower four channels may be specified. Then those four channels will be consecutively selected and the conversion results stored sequentially in the four conversion result registers.

Figure 4 is the block diagram for the A/D converter. To stop the operation of the A/D converter and thus reduce power consumption, set V_{AREF} = 0 V.

Interrupt Structure

There are 12 interrupt sources in the μPD78C14 family of chips. Three are external interrupts and nine are internal. Table 2 shows 11 interrupt sources divided into seven priority levels where IRQ0 is the highest and IRQ6 is the lowest. See figure 5.

Figure 4. A/D Converter Block Diagram

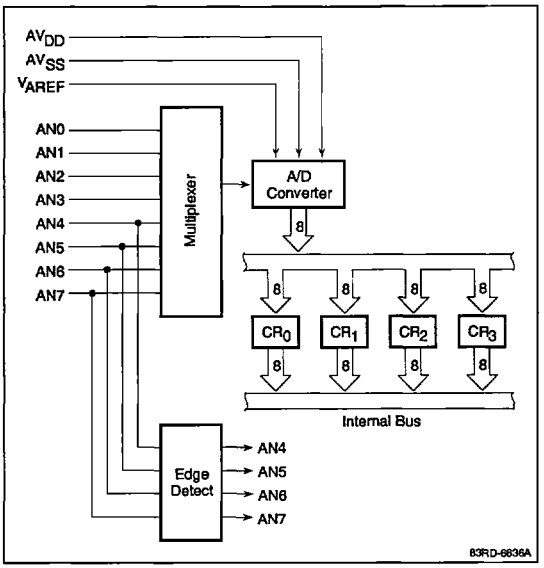
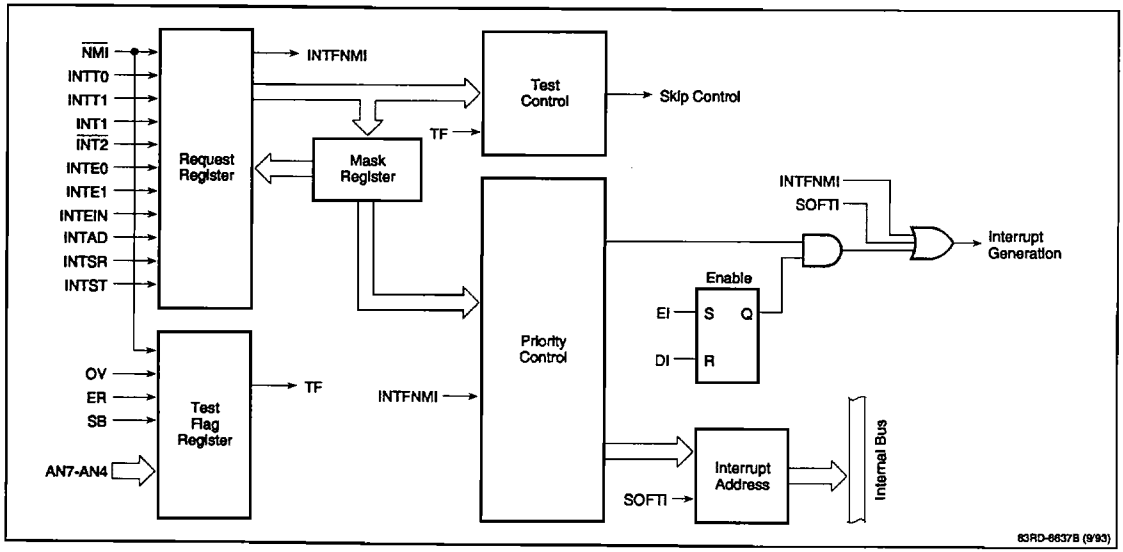


Table 2. Interrupt Sources

Interrupt Request	Interrupt Address	Type of Interrupt	Internal/External
IRQ0	4	$\overline{NMI}$ (Nonmaskable interrupt)	External
IRQ1	8	INTT0, INTT1 (Coincidence signals from timers 0, 1)	Internal
IRQ2	16	INT1, $\overline{INT2}$ (Maskable interrupts)	External
IRQ3	24	INTE0, INTE1 (Coincidence signals from timer/event counter)	Internal
IRQ4	32	INTEIN (Falling signal of CI or TO into the timer/event counter)	Internal or External
		INTAD (A/D converter interrupt)	Internal
IRQ5	40	INTSR (Serial receive interrupt)	Internal
		INST (Serial send interrupt)	
IRQ6	96	SOFTI instruction	Internal

Figure 5. Interrupt Structure Block Diagram



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Standby Functions

The μPD78C14 family has two standby modes: HALT and STOP. The HALT mode reduces power consumption to 50% of normal operating requirements, while maintaining the contents of on-chip registers, RAM, and control status. The system clock and on-board peripherals continue to operate, but the CPU stops executing instructions. The HALT mode is initiated by executing the HLT instruction. The HALT mode can be released by any nonmasked interrupt or by $\overline{\text{RESET}}$.

The STOP mode reduces power consumption to less than 0.1% of normal operating requirements. There are two STOP modes: type A and type B.

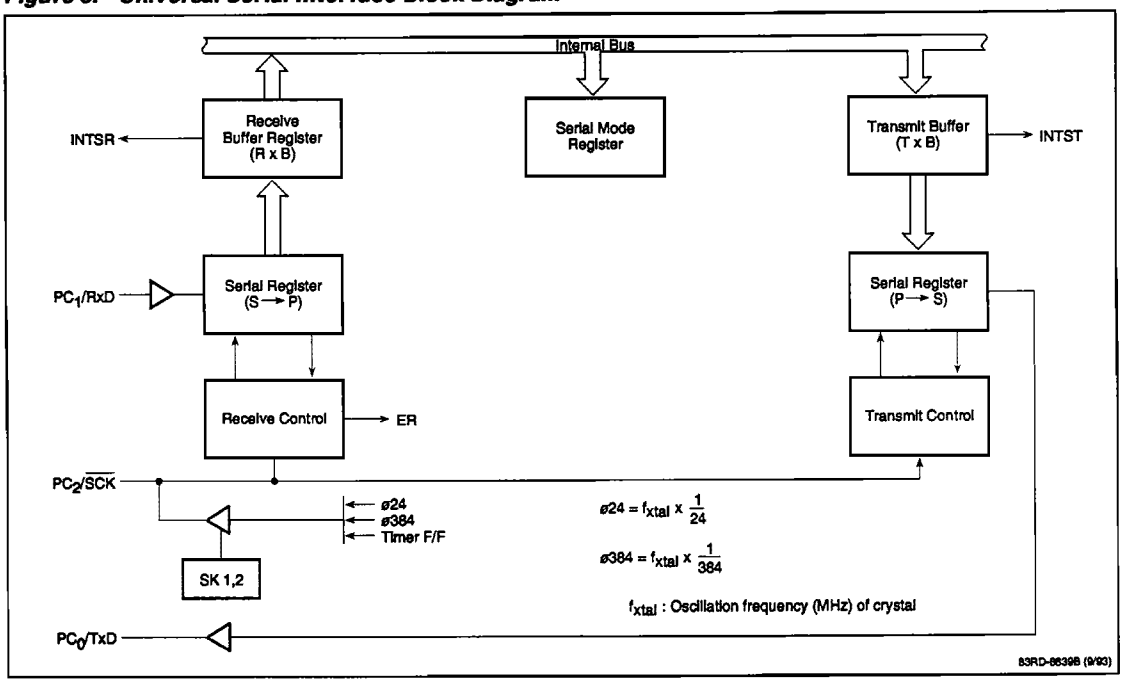
Type A is initiated by executing a STOP instruction. If V_{DD} is held above 2.5 V, the on-board RAM is saved. The oscillator is stopped. The STOP mode can be released by an input on $\overline{\text{NMI}}$ or $\overline{\text{RESET}}$. The user can program oscillator stabilization time up to 52.4 ms via timer 1. By checking the standby flag (SB), the user can determine whether the processor has been in the standby mode or has been powered up.

Type B is initiated by inputting a low level on the $\overline{\text{STOP}}$ input. The RAM contents are saved if V_{DD} is held above 2.5 V. The oscillator is stopped. The STOP mode is released by raising $\overline{\text{STOP}}$ to a high level. The oscillator stabilization time is fixed at 52.4 ms; 52.4 ms after $\overline{\text{STOP}}$ is raised, instruction execution will automatically begin at location 0. The stabilization time can be increased by holding $\overline{\text{RESET}}$ low for the required time period.

Universal Serial Interface

The serial interface can operate in one of three modes: synchronous, asynchronous, and I/O interface. The I/O interface mode transfers data MSB first, for easy interfacing to certain NEC peripheral devices. Synchronous and asynchronous modes transfer data LSB first. Synchronous operation offers two modes of data reception: search and nonsearch. In the search mode, data is transferred one bit at a time from the serial register to the receive buffer. This allows a software search for a sync character. In the nonsearch mode, data transfer from the serial register to the transmit buffer occurs eight bits at a time. Figure 6 shows the universal serial interface block diagram.

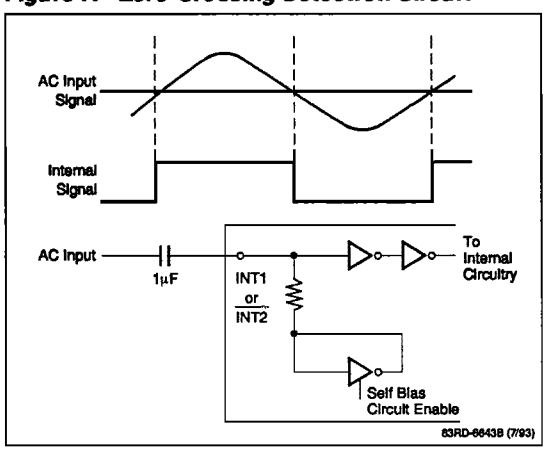
Figure 6. Universal Serial Interface Block Diagram



Zero-Crossing Detector

The INT1 and $\overline{INT2}$ terminals (used common to TI and PC_3) can detect the zero-crossing point of low-frequency AC signals. When driven directly, these pins respond as a normal digital input. Figure 7 shows the zero-crossing detection circuitry.

Figure 7. Zero-Crossing Detection Circuit



The zero-crossing detection capability allows you to make the 50-60 Hz power signal the basis for system timing and to control voltage phase-sensitive devices.

To use the zero-cross detection mode, an AC signal of 1.0 to 1.8 V (peak-to-peak) and a maximum frequency of 1 kHz is coupled through an external capacitor to the INT1 and $\overline{INT2}$ pins.

For the INT1 pin, the internal digital state is sensed as a 0 until the rising edge crosses the average DC level, when it becomes a 1 and an INT1 interrupt is generated.

For the $\overline{INT2}$ pin, the state is sensed as a 1 until the falling edge crosses the average DC level, when it becomes a 0 and $\overline{INT2}$ is generated.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

T_A = 25°C

Power supply voltage, V_{DD}	−0.5 to +7.0 V
Power supply voltage, AV_{DD}	AV_{SS} to V_{DD} + 0.5 V
Power supply voltage, AV_{SS}	−0.5 to + 0.5 V
Power supply voltage, V_{PP} (μPD78CP14 only)	−0.5 to +13.5 V
Input voltage, V_I	−0.5 to V_{DD} + .5 V
$\overline{STOP}$ pin (μPD78CP14 only)	−0.5 to +13.5 V
Output voltage, V_O	−0.5 to V_{DD} + .5 V
Output current, low; I_{OL}	
Each output pin	4.0 mA
Total	100 mA
Output current, high; I_{OH}	
Each output pin	−2.0 mA
Total	−50 mA
Reference input voltage, VA_{REF}	−0.5 to AV_{DD} + 0.3 V
Operating temperature, T_{OPR} $f_{XTAL} \leq$ 15 MHz	−40 to +85°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; V_{DD} = V_{SS} = 0 V

Parameter	Symbol	Max	Unit	Conditions
Input capacitance	C_I	10	pF	f_c = 1 MHz; unmeasured pins returned to 0 V
Output capacitance	C_O	20	pF	
I/O capacitance	C_{IO}	20	pF	

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Oscillation Characteristics

T_A = −40 to 85°C; V_{DD} = AV_{DD} = 5 V ± 10% (±5% μPD78CP14); V_{SS} = AV_{SS} = 0 V; V_{DD} − 0.8 V ≤ AV_{DD} ≤ V_{DD}; 3.4 V ≤ V_{AREF} ≤ AV_{DD}

Resonator	Recommended Circuit	Parameter	Min	Typ	Max	Unit	Conditions
Ceramic resonator (Note 1) or crystal oscillator (XTAL) (Note 4)	(Note 2)	Oscillation frequency (f_{XX})	4		15	MHz	A/D converter not used
			5.8		15	MHz	A/D converter used
			6		15	MHz	μPD78CP14 only
External clock	(Note 3)	X1 input frequency (f_X)	4		15	MHz	A/D converter not used
			5.8		15	MHz	A/D converter used
			6		15	MHz	μPD78CP14 only
		X1 input, rise, fall time (t_r, t_f)	0		20	ns	
		X_1 input low- and high-level width ($t_{\phi L}$, $t_{\phi H}$)	20		250	ns	
			20		167	ns	μPD78CP14

Notes:

(1) Refer to the Resonator and Capacitance Requirements table for the recommended ceramic resonators.

(2) For XTAL, see the Recommended XTAL or Ceramic Resonator Oscillation Circuit Diagram.

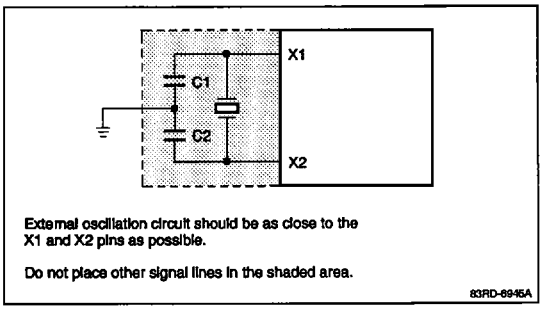
(3) See the following recommended external clock diagram.

(4) When using a crystal oscillator, it should be a parallel-resonant, fundamental mode, "AT cut" crystal. Capacitors C1 and C2 are required for frequency stability. The values of C1 and C2 (C1 = C2) can be calculated from the load capacitance (C_L), specified by the crystal manufacturer:

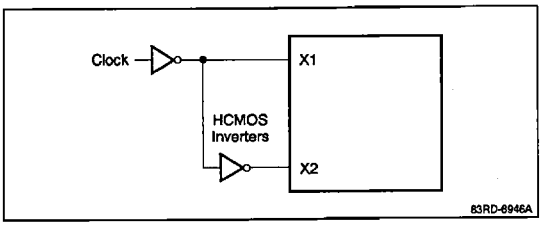
$$C_L = \frac{C1 \times C2}{C1 + C2} + C_S$$

Where C_S is any stray capacitance in parallel with the crystal such as the μPD78C10A, μPD78C11A, or μPD78C14/14A input capacitance between X1 and X2.

Recommended XTAL or Ceramic Resonator Oscillation Circuit Diagram



Recommended External Clock Diagram



Resonator and Capacitance Requirements

T_A = −40 to +85°C

Manufacturer	Product Number	C1, C2 (pF)	Conditions
Murata	CSA15.0MX3	22	μPD78C14/C14A
	CSA10.0MT	30	
	CST10.0MT	Not required	
	CSA6.00MG	30	
	CST6.00MG	Not required	
	CSA12.0MT	30	μPD78C10A/C11A/C12A/C14/C14A
	CST12.0MT	Not required	
	CSA15.00MX001	15	μPD78C10A/C11A/C12A
	CSA7.37MT	30	
	CST7.37MT	Not required	
TDK	FCR12.9MC	Not required	μPD787C14/C14A

DC Characteristics

T_A = −40 to +85°C; V_{SS} = 0 V; V_{DD} = +5.0 V ±10% (μPD78C10A/C11A/C12A/C14/C14A); V_{DD} = +5.0 V ± 5% (μPD78CP14 only)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input voltage, low	V_{IL1}	0		0.8	V	All except Note 1 inputs
	V_{IL2}	0		0.2 V_{DD}	V	Note 1 inputs
Input voltage, high	V_{IH1}	2.2		V_{DD}	V	All except X1, X2, and Note 1 inputs
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	X1, X2, and Note 1 inputs
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output voltage, high	V_{OH}	V_{DD} − 1.0			V	I_{OH} = 1.0 mA
		V_{DD} − 0.5			V	I_{OH} = −100 μA
Data retention voltage	V_{DDDR}	2.5			V	STOP mode
Input current	I_{I1}			±200	μA	INT1 (Note 2); TI (PC_3) (Note 3); 0 V ≤ V_I ≤ V_{DD}
Input current (μPD78C14 only)	I_{I2}			±200	μA	INT1 (Note 2); TI (PC_3) (Note 3); 0 V ≤ V_I ≤ V_{DD}
Input current (μPD78C14 only)	I_{I3}			−300	μA	I_0–I_7 (upper input pin); V_I = 0
Input leakage current	I_{LI}			±10	μA	All except INT1, TI (PC_3), 0 V ≤ V_I ≤ V_{DD}
				±1	μA	AN7-0, 0 V ≤ V_1 ≤ V_{DD} (μPDC10A(A)/C11A(A)/C12A(A)/CP14A(A) only)
Output leakage current	I_{LO}			±10	μA	0 V ≤ V_O ≤ V_{DD}
AV_{DD} supply current	AI_{DD1}		0.5	1.3	mA	f = 15 MHz
	AI_{DD2}		10	20	μA	STOP mode
V_{DD} supply current	I_{DD1}		13	25	mA	Normal operation; f = 15 MHz; (μPD78C10A/C11A/C12A only)
	I_{DD2}		7	13	mA	HALT mode; f = 15 MHz; (μPD78C10A/C11A/C12A only)
	I_{DD3}		16	30	mA	Normal operation; f = 15 MHz (μPD78C14/C14A)
	I_{DD4}			32	mA	Normal operation; f = 15 MHz; (μPD78CP14 only)
	I_{DD5}		8	15	mA	HALT mode; f = 15 MHz; (μPD78C14/C14A/CP14 only)
Data retention current	I_{DDDR}		1	15	μA	V_{DDDR} = 2.5 V (Note 4)
				300		(μPD78CP14 only-Note 4)
			10	50	μA	V_{DDDR} = 5.0 V ±10% (Note 4)
				1	mA	(μPD78CP14 only-Note 4)
Pullup resistor	R_L	17	27	75	KΩ	Ports A, B, C; 3.5 V ≤ V_{DD} ≤ 5.5 V; V_I = 0 V (μPD78C11A/C12A/C14A only)

Notes:

(1) Inputs $\overline{\text{RESET}}$, $\overline{\text{STOP}}$, $\overline{\text{NMI}}$, $\overline{\text{SCK}}$, INTP1, TI, and AN4-AN7.

(2) Assuming ZCM register is set to self-bias.

(3) Assuming ZCM register is set to self-bias and the MCC register is set to control mode.

(4) Hardware/software STOP mode and assuming ZCM register is set to self-bias not selected.

AC Characteristics

T_A = −40 to +85°C; V_{SS} = 0 V; V_{DD} = +5.0 V ±10% (μPD78C10A/C11A/C12A/C14/C19A); V_{DD} = +5.0 V ± 5% (μPD78CP14 only)

Parameter	Symbol	Min	Max	Unit	Conditions
$\overline{RESET}$ pulse width high, low	t_{RSH}, t_{RSL}	10		μs	
$\overline{NMI}$ pulse width high, low	t_{NIH}, t_{NIH}	10		μs	
X1 input cycle time	t_{CYC}	66	250	ns	
			167	ns	(Note 1)
Address setup to ALE ↓	t_{AL}	30		ns	(Notes 2, 3)
Address hold to ALE ↓	t_{LA}	35		ns	(Notes 2, 3)
Address to $\overline{RD}$ ↓ delay time	t_{AR}	100		ns	(Notes 2, 3)
$\overline{RD}$ ↓ to address floating	t_{AFR}		20	ns	(Note 2)
Address to data input	t_{AD}		250	ns	(Notes 2, 3)
ALE ↓ to data input	t_{LDR}		135	ns	(Notes 2, 3)
$\overline{RD}$ ↓ to data input	t_{RD}		120	ns	(Notes 2, 3)
ALE ↓ to $\overline{RD}$ ↓ delay time	t_{LR}	15		ns	(Notes 2, 3)
Data hold time $\overline{RD}$ ↑	t_{RDH}	0		ns	(Note 2)
$\overline{RD}$ ↑ to ALE ↑ delay time	t_{RL}	80		ns	(Notes 2, 3)
$\overline{RD}$ width low	t_{RR}	215		ns	Data read (Notes 2, 3)
		415		ns	Opcode fetch (Notes 2, 3)
ALE width high	t_{LL}	90		ns	(Notes 2, 3)
$\overline{M1}$ setup time to ALE ↓	t_{ML}	30		ns	(Note 3)
$\overline{M1}$ hold time after ALE ↓	t_{LM}	35		ns	(Note 3)
$\overline{IO}$/M setup time to ALE ↓	t_{IL}	30		ns	(Note 3)
$\overline{IO}$/M hold time after ALE ↓	t_{LI}	35		ns	(Note 3)
Address to $\overline{WR}$ ↓ delay	t_{AW}	100		ns	(Notes 2, 3)
ALE ↓ to data output	t_{LDW}		180	ns	(Notes 2, 3)
$\overline{WR}$ ↓ to data output	t_{WD}		100	ns	(Note 2)
ALE ↓ to $\overline{WR}$ ↓ delay time	t_{LW}	15		ns	(Notes 2, 3)
Data setup time to $\overline{WR}$ ↑	t_{DW}	165		ns	(Notes 2, 3)
Data hold time to $\overline{WR}$ ↑	t_{WDH}	60		ns	(Notes 2, 3)
$\overline{WR}$ ↑ to ALE ↑ delay time	t_{WL}	80		ns	(Notes 2, 3)
$\overline{WR}$ width low	t_{WW}	215		ns	(Notes 2, 3)
Address to data input	t_{ACC}		250	ns	(Notes 2, 3)
Data hold time from address	t_{IH}	0		ns	(Note 2)

Notes:

(1) Applies to μPD78CP14 only.

(2) Load capacitance C_L = 150 pF.

(3) Values are for 15-MHz operation. For operation at other frequencies, refer to the Bus Timing Dependent on t_{CYK} table.

Serial Operation

Parameter	Symbol	Min	Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{CYK}	0.8		μs	$\overline{SCK}$ input (Notes 1, 3)
		0.4		μs	$\overline{SCK}$ input (Note 2)
		1.6		μs	$\overline{SCK}$ output (Note 3)

Serial Operation (cont)

Parameter	Symbol	Min	Max	Unit	Conditions
$\overline{SCK}$ width low	t_{KKL}	335		ns	$\overline{SCK}$ input (Notes 1, 3)
		160		ns	$\overline{SCK}$ input (Note 2)
		700		ns	$\overline{SCK}$ output (Note 3)
$\overline{SCK}$ width high	t_{KKH}	335		ns	$\overline{SCK}$ input (Notes 1, 3)
		160		ns	$\overline{SCK}$ input (Note 2)
		700		ns	$\overline{SCK}$ output (Note 3)
RxD setup time to $\overline{SCK}$ ↑	t_{RXK}	80		ns	(Note 1)
RxD hold time after $\overline{SCK}$ ↑	t_{KRX}	80		ns	(Note 1)
$\overline{SCK}$ ↓ TxD delay time	t_{KTX}		210	ns	(Note 1)

Notes:

(1) 1 x baud rate in synchronous or I/O interface mode.

(2) 16 x baud rate or 64 x baud rate in asynchronous mode.

(3) f_{XTAL} = 15 MHz.

Zero-Cross Characteristics

Parameter	Symbol	Min	Max	Unit	Condition
Zero-cross detection input	V_{ZX}	1	1.8	VAC_{p-p}	AC-coupled 60-Hz sine wave
Zero-cross accuracy	A_{ZX}		±135	mV	
Zero-cross detection input frequency	f_{ZX}	0.05	1	kHz	

A/D Converter Characteristics

T_A = −40 to +85°C; V_{DD} = +5.0 V ±10% (±5% on μPD78CP14); V_{SS} = AV_{SS} 0 V;
V_{DD} −0.5 V ≤ AV_{DD} ≤ V_{DD}; 3.4 V ≤ V_{AREF} ≤ AV_{DD}

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Resolution		8			bits	
Absolute accuracy (Note 1)				±0.4	%FSR	T_A = −10 to +70°C; 66 ns ≤ t_{CYC} ≤ 170 ns; 4.0 V ≤ V_{AREF} ≤ AV_{DD}
				±0.6	%FSR	66 ns ≤ t_{CYC} ≤ 170 ns; 4.0 V ≤ V_{AREF} ≤ AV_{DD}
				±0.8	%FSR	66 ns ≤ t_{CYC} ≤ 170 ns; 3.4 V ≤ V_{AREF} ≤ AV_{DD}
Conversion time	t_{CONV}	576			t_{CYC}	66 ns ≤ t_{CYC} ≤ 110 ns
		432			t_{CYC}	110 ns ≤ t_{CYC} ≤ 170 ns
Sampling time	t_{SAMP}	96			t_{CYC}	66 ns ≤ t_{CYC} ≤ 110 ns
		72			t_{CYC}	110 ns ≤ t_{CYC} ≤ 170 ns
Analog input voltage	V_{IAN}	0		V_{AREF}	V	
Analog input impedance	R_{AN}		1000		MΩ	
Reference voltage	V_{AREF}	3.4		AV_{DD}	V	
V_{AREF} current	I_{AREF1}		1.5	3.0	mA	Operation mode
	I_{AREF2}		0.7	1.5	mA	STOP mode
AV_{DD} supply current	AI_{DD1}		0.5	1.3	mA	Operation mode
	AI_{DD2}		10	20	μA	STOP mode

Notes:

(1) Quantizing error (±1/2 LSB) is not included.

(2) FSR = Full-scale resolution.

Bus Timing Dependent on t_{CYK}

Symbol	Min/Max (ns)	Calculation Formula
t_{TIH}, t_{TIL}	Min	6T (TI input - PC_3)
t_{CI1H}, t_{CI1L} (Note 2)	Min	6T (TI input - PC_5)
t_{CI2H}, t_{CI2L} (Note 3)	Min	48T (TI input - PC_5)
t_{I1H}, t_{I1L}	Min	36T (INT1)
t_{I2H}, t_{I2L}	Min	36T ($\overline{INT2}$)
t_{ANH}, t_{ANL}	Min	36T (AN4-AN7)
t_{AL}	Min	2T – 100
t_{LA}	Min	T – 30
t_{AR}	Min	3T – 100
t_{AD}	Max	7T – 220
t_{LDR}	Max	5T – 200
t_{RD}	Max	4T – 150
t_{LR}	Min	T – 50
t_{RL}	Min	2T – 50
t_{RR}	Min	4T – 50 (Data read)
	Min	7T – 50 (Opcode fetch)
t_{LL}	Min	2T – 40
t_{ML}	Min	2T – 100
t_{LM}	Min	T – 30
t_{IL}	Min	2T – 100

Symbol	Min/Max (ns)	Calculation Formula
t_{LI}	Min	T – 30
t_{AW}	Min	3T – 100
t_{LDW}	Max	T + 110
t_{LW}	Min	T – 50
t_{DW}	Min	4T – 100
t_{WDH}	Min	2T – 70
t_{WL}	Min	2T – 50
t_{WW}	Min	4T – 50
t_{CYK}	Min	12T ($\overline{SCK}$ input) (Note 1)
	Min	24T ($\overline{SCK}$ output)
t_{KKL}	Min	5T + 5 ($\overline{SCK}$ input) (Note 1)
	Min	12T – 100 ($\overline{SCK}$ output)
t_{KKH}	Min	5T + 5 ($\overline{SCK}$ input) (Note 1)
	Min	12T – 100 ($\overline{SCK}$ output)

Notes:

(1) 1 x baud rate in synchronous or I/O interface mode; T = t_{CYC} = $1/f_{XTAL}$.
The items not included in this list are independent of oscillator frequency.

(2) Event counter mode.

(3) Pulse-width measurement mode.

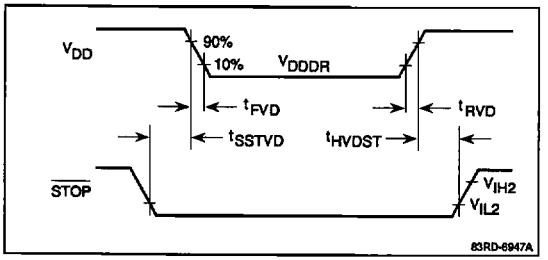
Data Memory STOP Mode Data Retention Characteristics

T_A = −40 to 85°C

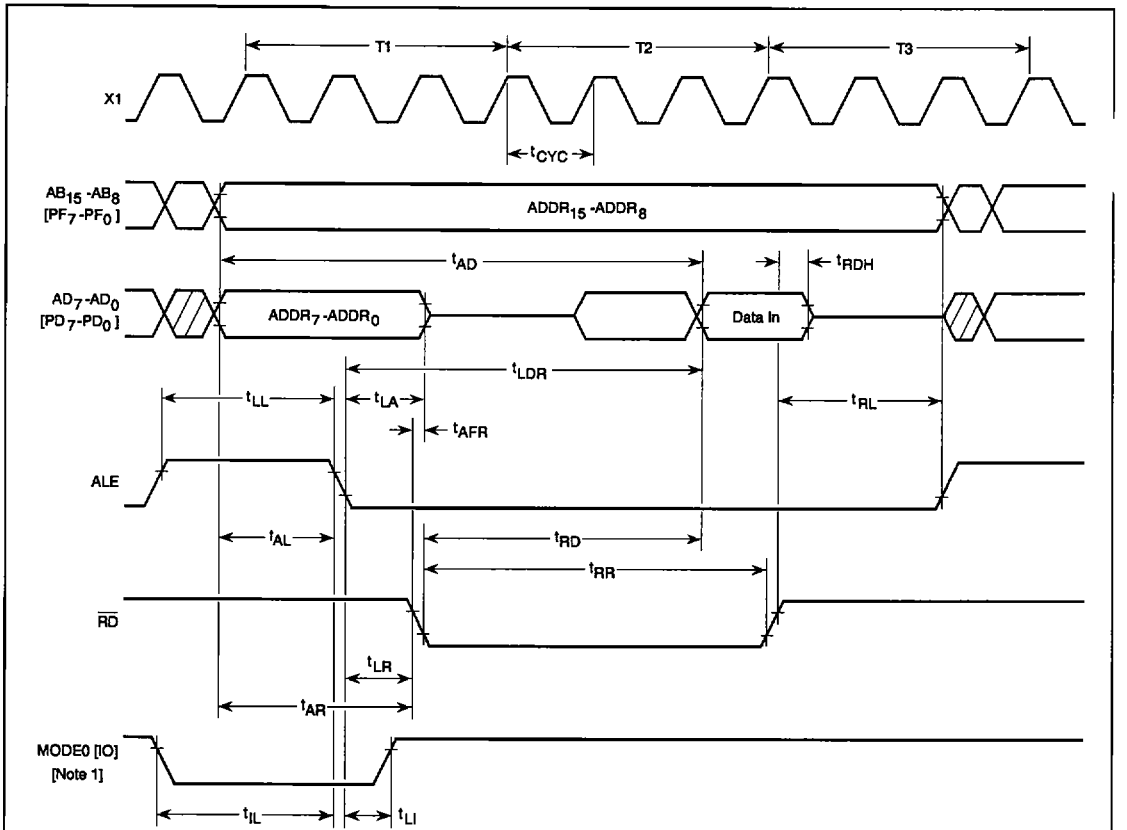
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Data retention power supply voltage	V_{DDDR}	2.5		5.5	V	
Data retention power supply current	I_{DDDR}		1	15	μA	V_{DDDR} = 2.5 V
			15	50	μA	V_{DDDR} = 5.0 V ±10%
				300	μA	V_{DDDR} = 2.4 V (μPD78CP14)
				1	mA	V_{DDDR} = 5.0 V ±5% (μPD78CP14)
V_{DD} rise, fall time	t_{RVD}, t_{FVD}	200			μs	
$\overline{STOP}$ setup time to V_{DD}	t_{SSTVD}	12T+0.5			μs	
$\overline{STOP}$ hold time from V_{DD}	t_{HVDST}	12T+0.5			μs	

Timing Waveforms

Data Retention



Read Operation



Note:

[1] $\overline{IO}$ signal is output to the MODE0 pin [if MODE0 is pulled up to V_{DD}] during a read or write of special registers sr-sr2 or a write to register MM or MF. Refer to description of Port Emulation Mode [PEM] in the User's Manual for further explanation. This signal is not output on the μPD78CP14.

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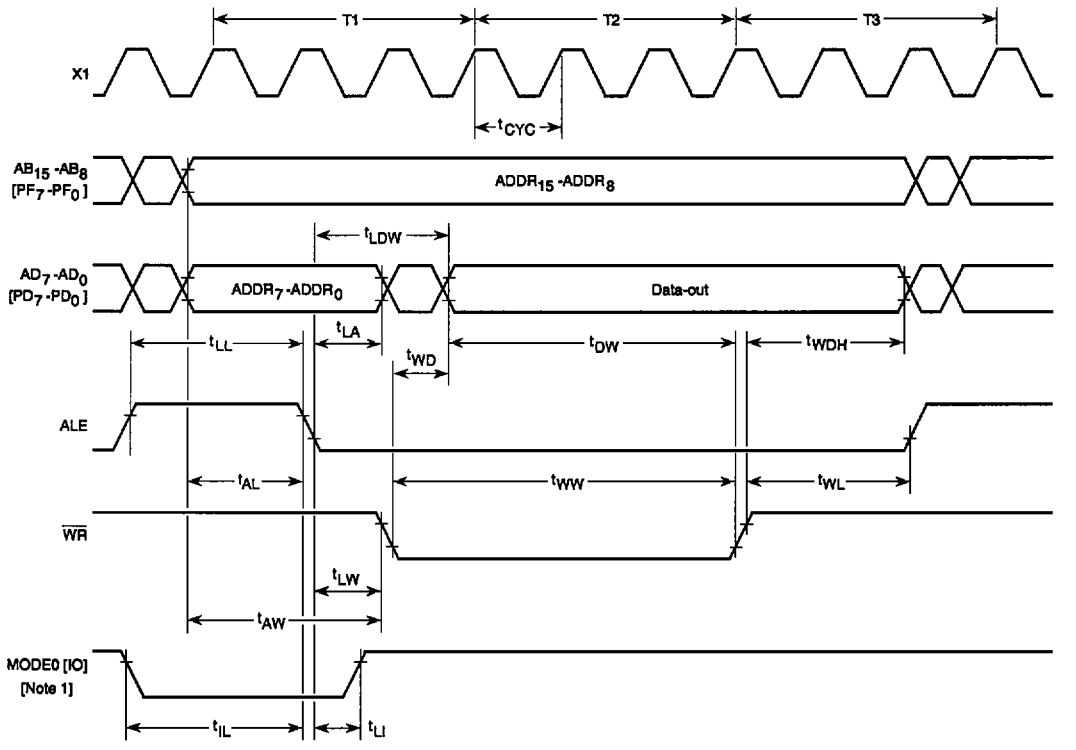
Timing Waveforms (cont)

Write Operation



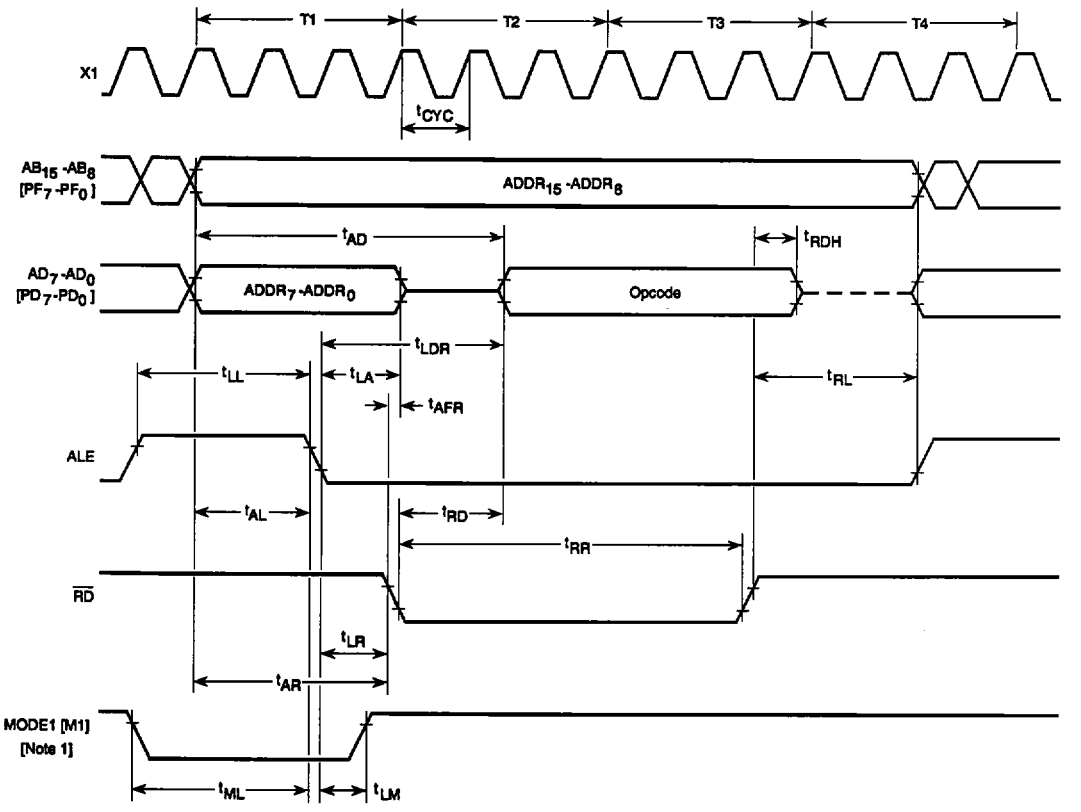
Note:

[1] $\overline{IO}$ signal is output to the MODE0 pin [if MODE0 is pulled up to V_{DD}] during a read or write of special registers sr-sr2 or a write to register MM or MF. Refer to description of Port Emulation Mode [PEM] in the User's Manual for further explanation. This signal is not output on the μPD78CP14.

83YL-9254B

Timing Waveforms (cont)

Opcode Fetch Operation



Note:

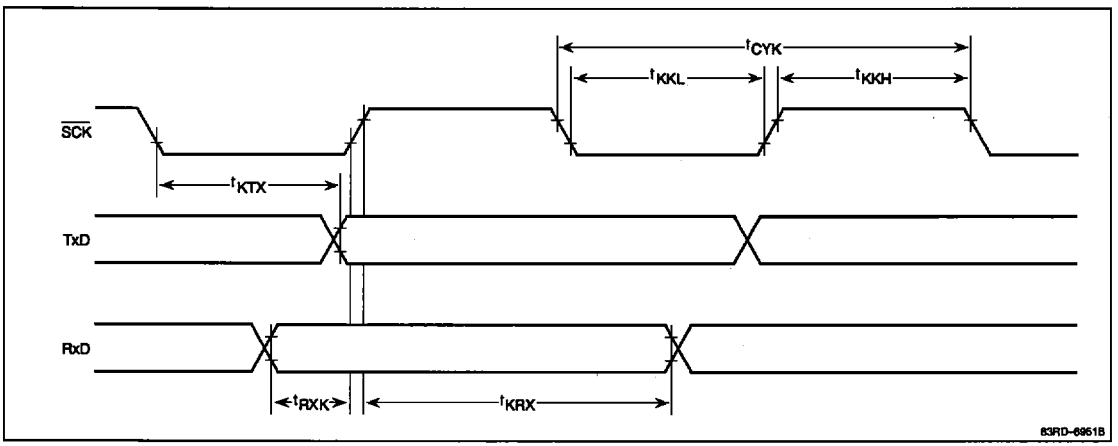
[1] $\overline{M1}$ signal is output to the MODE1 pin during every Opcode Fetch if MODE1 pin is pulled up to V_{DD}. This signal is not output on the μPD78CP14.

83YL-9256B

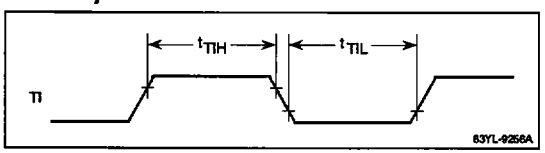
2a

Timing Waveforms (cont)

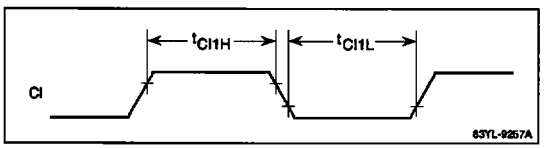
Serial Operation Transmit/Receive



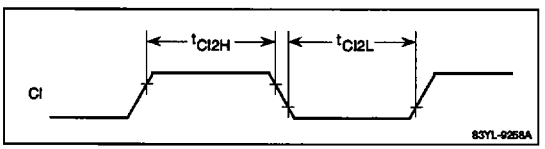
Timer Input



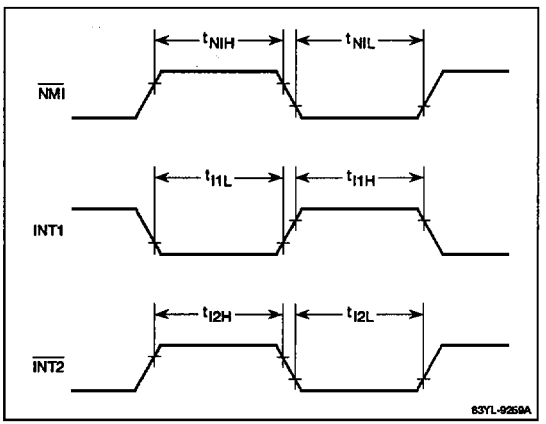
Timer/Event Counter Input: Event Counter Mode



Timer/Event Counter Input: Pulse-Width Measurement Mode

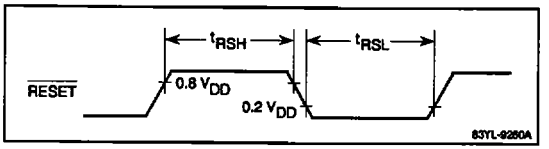


Interrupt Input

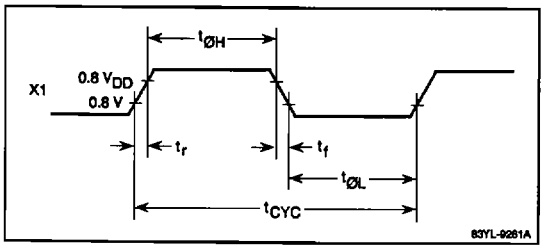


Timing Waveforms (cont)

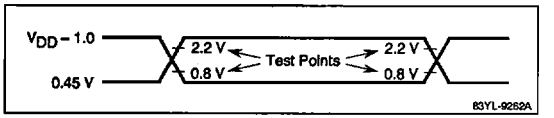
$\overline{RESET}$ Input



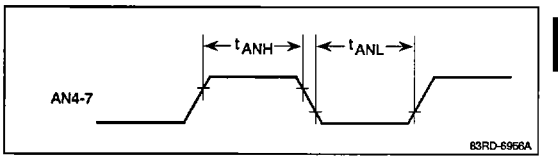
External Clock



AC Timing Test Points



AN4-AN7 Edge Detection



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μPD78CP14 PROGRAMMING

In the μPD78CP14, the mask ROM of the μPD78C14 family is replaced by a one-time programmable ROM (OTP ROM) or a reprogrammable, ultraviolet erasable ROM (UV EPROM). The ROM is 16,384 by 8 bits and can be programmed using a general-purpose PROM writer with a μPD27C256A programming mode. Refer to tables 3 through 5 and the DC and AC Programming Characteristics tables for specific information applicable to programming the μPD78CP14.

Table 3. Pin Functions during EPROM Programming

Pin	Function	Description
PA_0 - PA_7	A_0 - A_7	Low-order 8-bit address
PF_0	A_8	High-order 7-bit address
$\overline{NMI}$	A_9	
PF_2 - PF_6	A_{10} - A_{14}	
PD_0 - PD_7	D_0 - D_7	Data input/output
PB_6	$\overline{CE}$	Chip enable input
PB_7	$\overline{OE}$	Output enable input
$\overline{RESET}$	$\overline{RESET}$	PROM programming mode requires a low voltage on this pin
Mode 0	Mode 0	Enter PROM programming mode by applying a high voltage to this pin
Mode 1	Mode 1	Enter PROM programming mode by applying a low voltage to this pin
$\overline{STOP}$	V_{PP}	High-voltage input (write/verify) high level (read)

Table 4. Summary of Operation Modes for EPROM Programming

Operation Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{DD}	$\overline{RESET}$	MODE0	MODE1	A_{14}
Program write	L	H	+12.5 V	+6 V	L	H	L	L
Program verify	H	L	+12.5 V	+6 V	L	H	L	L
Program inhibit	H	H	+12.5 V	+6 V	L	H	L	L
Read	L	L	+5 V	+5 V	L	H	L	L
Output disable	L	H	+5 V	+5 V	L	H	L	L
Standby	H	L/H	+5 V	+5 V	L	H	L	L

Notes:

(1) The $\overline{CE}$, $\overline{OE}$, V_{pp}, and V_{DD} pins are all compatible with the μPD27C256A pins.

Caution: When Vpp is set to +12.5 V and V_{DD} is set to +6 V, you cannot set both $\overline{CE}$ and $\overline{OE}$ to low level (L).

Table 5. Recommended Connections for Unused Pins (EPROM Programming Mode)

Pin	Recommended Connection Method
INT1	Connect to V_{SS}
X1	Connect to V_{SS}
X2	Leave this pin disconnected
AN0-AN7	Connect to V_{SS}
VA_{REF}	Connect to V_{SS}
AV_{DD}	Connect to V_{SS}
AV_{SS}	Connect to V_{SS}
Remaining pins	Connect each pin via a resistor to V_{SS}

PROM Write Procedure

(1) Connect the $\overline{\text{RESET}}$ pin, the MODE1 pin, and A_{14} pin to a low level and connect the MODE0 pin to a high level. Connect all unused pins as recommended in Table 5.

(2) Apply +6 V to the V_{DD} pin and +12.5 V to the V_{pp} pin.

(3) Provide the initial address.

(4) Provide write data.

(5) Provide 1-ms program pulse (active low) to the $\overline{\text{CE}}$ pin.

(6) This bit is now verified with a pulse (active low) to the $\overline{\text{OE}}$ pin. If the data has been written, proceed to step 8; if not, repeat steps 4 to 6. If the data cannot be correctly written after 25 attempts, go to step 7.

(7) Classify as defective and stop write operation.

(8) Provide write data and supply program pulse (for additional writing) for 3 ms times the number of repeats performed between steps 4 to 6.

(9) Increment the address.

(10) Repeat steps 4 to 9 until the end address.

PROM Read Procedure

(1) Connect the $\overline{\text{RESET}}$ pin, the MODE1 pin, and A_{14} pin to a low level and connect the MODE0 pin to a high level.

(2) Apply +5 V to the V_{DD} and V_{pp} pins.

(3) Input the address of the data to be read to pins A_0 - A_{14}.

(4) Read mode is entered with a pulse (active low) on both the $\overline{\text{CE}}$ and $\overline{\text{OE}}$ pins.

(5) Data is output to the D_0 - D_7 pins.

EPROM Erasure

Data in an EPROM is erased by exposing the quartz window in the ceramic package to light having a wavelength shorter than 400 nm, including ultraviolet rays, direct sunlight, and fluorescent light. To prevent unintentional erasure, mask the window.

Typically, data is erased by 254-nm ultraviolet rays. A minimum lighting level of 15W-s/cm^2 (ultraviolet ray intensity x exposure time) is required to completely erase written data. Erasure by an ultraviolet lamp rated at 12 mW/cm^2 takes approximately 15 to 20 minutes. Remove any filter on the lamp and place the device within 2.5 cm of the lamp tubes.

μPD78CP14 DC Programming Characteristics

T_A = 25 ±5°C; MODE1 = V_{IL}; MODE0 = V_{IH}; V_{SS} = 0 V

Parameter	Symbol	Symbol*	Min	Typ	Max	Unit	Condition
High-level input voltage	V_{IH}	V_{IH}	2.2		V_{DDP}+ 0.3	V	
Low-level input voltage	V_{IL}	V_{IL}	−0.3		0.8	V	
Input leakage current	I_{LIP}	I_{LI}			±10	μA	$0 \le V_I \le V_{DDP}$
High-level output voltage	V_{OH}	V_{OH}	V_{DD} − 1.0			V	I_{OH} = −1.0 mA
Low-level output voltage	V_{OL}	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output leakage current	I_{LO}				±10	μA	$0 \le V_O \le V_{DDP}$; $\overline{OE}$ = V_{IH}
V_{DDP} power voltage	V_{DDP}	V_{CC}	5.75	6.0	6.25	V	Program memory write mode
			4.5	5.0	5.5	V	Program memory read mode
V_{PP} power voltage	V_{PP}	V_{PP}	12.2	12.5	12.8	V	Program memory write mode
				V_{PP} = V_{DDP}		V	Program memory read mode
V_{DDP} power current	I_{DD}	I_{CC}			30	mA	Program memory write mode
					30	mA	Program memory read mode; $\overline{CE}$ = V_{IL}; V_I = V_{IH}
V_{PP} power current	I_{PP}	I_{PP}			30	mA	Program memory read mode; $\overline{CE}$ = V_{IL}; $\overline{OE}$ = V_{IH}
				1	100	μA	Program memory write mode

* Corresponding symbols of the μPD27C256A.

μPD78CP14 AC Programming Characteristics

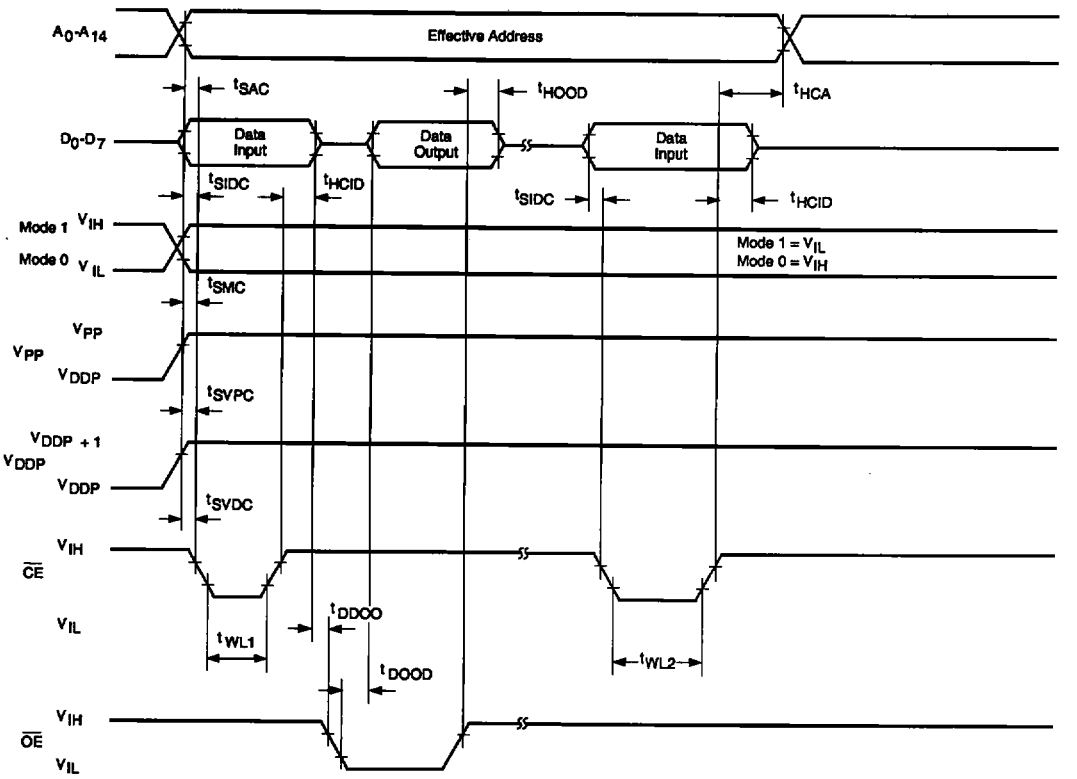
T_A = 25 ±5°C; MODE1 = V_{IL}; V_{SS} = 0 V

Parameter	Symbol	Symbol*	Min	Typ	Max	Unit	Condition
Address setup time to $\overline{CE}$ ↓	t_{SAC}	t_{AS}	2			μs	
Data to $\overline{OE}$ ↓ delay time	t_{DDOO}	t_{OES}	2			μs	
Input data setup time to $\overline{CE}$ ↓	t_{SIDC}	t_{DS}	2			μs	
Address hold time from $\overline{CE}$ ↑	t_{HCA}	t_{AH}	2			μs	
Input data hold time from $\overline{CE}$ ↑	t_{HCID}	t_{DH}	2			μs	
Output data hold time from $\overline{OE}$ ↑	t_{HOOD}	t_{DF}	0		130	ns	
V_{PP} setup time to $\overline{CE}$ ↓	t_{SVPC}	t_{VPS}	2			μs	
V_{DDP} setup time to $\overline{CE}$ ↓	t_{SVDC}	t_{VDS}	2			μs	
Initial program pulse width	t_{WL1}	t_{PW}	0.95	1.0	1.05	ms	
Additional program pulse width	t_{WL2}	t_{OPW}	2.85		78.75	ms	
MODE0/MODE1 setup time vs. $\overline{CE}$ ↓	t_{SMC}		2			μs	MODE1 = V_{IL} and MODE0 = V_{IH}
Address to data output time	t_{DAOD}	t_{ACC}			2	μs	$\overline{OE}$ = V_{IL}
$\overline{CE}$ ↓ to data output time	t_{DCOD}	t_{CE}			1	μs	
$\overline{OE}$ ↓ to data output time	t_{DOOD}	t_{OE}			1	μs	
Data hold time from $\overline{OE}$ ↑ or $\overline{CE}$ ↑	t_{HCOD}	t_{DF}	0		130	ns	
Data hold time from address	t_{HAOD}	t_{OH}	0			ns	$\overline{OE}$ = V_{IL}

* Corresponding symbols of the μPD27C256A.

PROM Timing Diagrams

μPD78CP14 PROM Write Mode



Notes:
(1) V_{DDP} must be applied before applying V_{PP}. It should be removed after removing V_{PP}.
(2) V_{PP} must not exceed +13 V, including overshoot.

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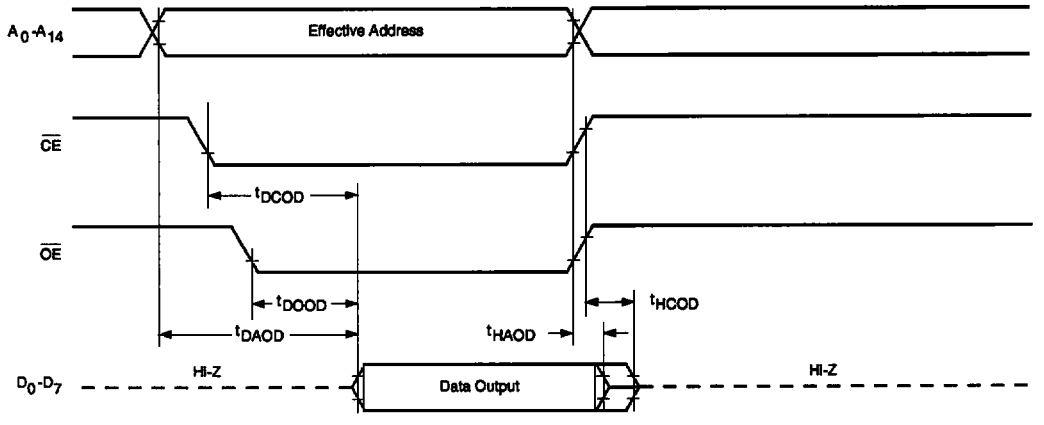
PROM Timing Diagrams (cont)

μPD78CP14 PROM Read Mode



Notes:

(1) To read PROM within the t_{DAOD} range, the delay of $\overline{OE}\downarrow$ from $\overline{CE}\downarrow$ must be within t_{DAOD}- t_{DOOD}.

(2) t_{HCOD} is the time from the state in which either $\overline{OE}$ or $\overline{CE}$ first becomes V_{IH}.

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