11. ELECTRICAL SPECIFICATIONS

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (1/26)

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{REF}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00-P04, P10-P17, P20-P27, P30-P37, P40-P47 P50-P57, P64-P67, X1, X2, XT2, $\overline{RESET}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P60-P63	Open-drain	–0.3 to +16	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10-P17	Analog input pin	AV_{SS} – 0.3 to AV_{REF} + 0.3	V
Output current high	I_{OH}	1 pin		–10	mA
		P10-P17, P20-P27, P30-P37 total		–15	mA
		P01-P03, P40-P47, P50-P57, P60-P67 total		–15	mA
Output current low	I_{OL} Note	1 pin	Peak value	30	mA
			rms	15	mA
		P40-P47, P50-P55 total	Peak value	100	mA
			rms	70	mA
		P01-P03, P56, P57, P60-P67 total	Peak value	100	mA
			rms	70	mA
		P01-P03, P64-P67 total	Peak value	50	mA
			rms	20	mA
		P10-P17, P20-P27, P30-P37 total	Peak value	50	mA
			rms	20	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note rms should be calculated as follows: [rms] = [peak value] × $\sqrt{duty}$

Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximuam ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

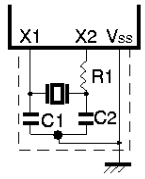
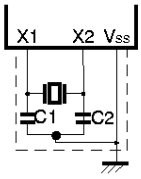
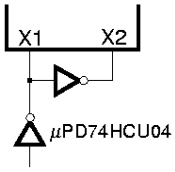
● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (2/26)

Capacitance (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P01-P03, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67			15	pF
			P60-P63			20	pF

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

Main System Clock Oscillation Circuit Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (fx) Note 1	2.7 V ≤ V_{DD} ≤ 5.5 V	1		10	MHz
			1.8 V ≤ V_{DD} < 2.7 V	1		5	
		Oscillation stabilization time Note 2	After V_{DD} reaches oscillator voltage range MIN.			4	ms
Crystal resonator		Oscillator frequency (fx) Note 1	2.7 V ≤ V_{DD} ≤ 5.5 V	1		10	MHz
			1.8 V ≤ V_{DD} < 2.7 V	1		5	
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (fx) Note 1		1.0		10.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		45		500	ns

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

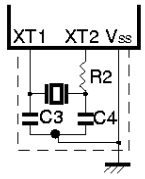
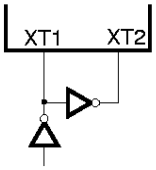
Cautions 1. When using the main system clock oscillator, wirinin the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (3/26)

Subsystem Clock Oscillation Circuit Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillator frequency (f_{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 6.0 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT}) Note 1		32		100	kHz
		XT1 input high/low level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillator voltage MIN.

Cautions 1. When using the subsystem clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. The subsystem clock oscillation circuit is a circuit with a low amplification level, more prone to misoperation due to noise than the main system clock. Particular care is therefore required with the wiring method when the subsystem clock is used.

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (4/26)

Recommended Oscillation Circuit Constant

Recommended oscillation circuit constant differs depending on the model.

(1) μPD78011F(A), 78012F(A), 78013F(A), 78014F(A)

(a) Main system clock: ceramic resonator (T_A = –40 to +85 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant		Oscillation Voltage Range		Remark
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
TDK Corp.	CCR4.0MC3	4.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, surface-mount type
	FCR4.0MC5	4.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, insertion type
	CCR4.19MC3	4.19	Built-in	Built-in	1.8	5.5	Capacitor on chip, surface-mount type
	FCR4.19MC5	4.19	Built-in	Built-in	1.8	5.5	Capacitor on chip, insertion type
	CCR5.00MC3	5.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, surface-mount type
	FCR5.00MC5	5.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, insertion type
	CCR8.00MC	8.00	Built-in	Built-in	2.7	5.5	Capacitor on chip, surface-mount type
	FCR8.00MC5	8.00	Built-in	Built-in	2.7	5.5	Capacitor on chip, insertion type
	CCR8.38MC	8.38	Built-in	Built-in	2.7	5.5	Capacitor on chip, surface-mount type
	FCR8.38MC5	8.38	Built-in	Built-in	2.7	5.5	Capacitor on chip, insertion type
	CCR10.00MC	10.00	Built-in	Built-in	2.7	5.5	Capacitor on chip, surface-mount type
	FCR10.00MC5	10.00	Built-in	Built-in	2.7	5.5	Capacitor on chip, insertion type
Murata Mfg. Co. Ltd.	CSA4.00MG	4.00	30	30	1.8	5.5	Insertion type
	CST4.00MGW	4.00	Built-in	Bkuilt-in	1.8	5.5	Capacitor on chip, insertion type
	CSA4.19MG	4.19	30	30	1.8	5.5	Insertion type
	CST4.19MGW	4.19	Built-in	Built-in	1.8	5.5	Capacitor on chip, insertion type
	CSA5.00MG	5.00	30	30	1.8	5.5	Insertion type
	CST5.00MGW	5.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, insertion type
	CSA8.00MTZ	8.00	30	30	2.7	5.5	Insertion type
	CST8.00MTW	8.00	Built-in	Built-in	2.7	5.5	Capacitor on chip, insertion type
	CSA8.38MTZ	8.38	30	30	2.7	5.5	Insertion type
	CST8.38MTW	8.38	Built-in	Built-in	2.7	5.5	Capacitor on chip, insertion type
	CSA10.00MTZ	10.00	30	30	2.7	5.5	Insertion type
	CST10.00MTW	10.00	Built-in	Built-in	2.7	5.5	Capacitor on chip, insertion type

Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee the accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency of the resonator in the application circuit. For this, it is necessary to directly contact manufacturer of the resonator being used.

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (5/26)

(b) Main system clock: ceramic resonator (T_A = –20 to +80 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant		Oscillation Voltage Range		Remark
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
Kyocera Corp.	PBRC4.00A	4.00	33	33	1.8	5.5	Surface-mount type
	RBRC4.00B	4.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, surface-mount type
	KBR-4.00MSA	4.00	33	33	1.8	5.5	Insertion type
	KBR-4.00MKS	4.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, insertion type
	PBRC5.00A	5.00	33	33	1.8	5.5	Surface-mount type
	RBRC5.00B	5.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, surface-mount type
	KBR-5.00MSA	5.00	33	33	1.8	5.5	Insertion type
	KBR-5.00MKS	5.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, insertion type
	KBR-8M	8.00	33	33	2.7	5.5	Insertion type
	KBR-10M	10.00	33	33	2.7	5.5	Insertion type

(2) μPD78015F(A), 78016F(A)

(a) Main system clock: ceramic resonator (T_A = –40 to +85 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant			Oscillation Voltage Range		Remark
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)	
Murata Mfg. Co. Ltd.	CSB1000J	1.00	100	100	5.6	1.8	5.5	Insertion type
	CSA2.00MG040	2.00	100	100	0	1.8	5.5	Insertion type
	CST2.00MG040		Built-in	Built-in	0	1.8	5.5	Capacitor on chip, insertion type
	CSA4.00MG040	4.00	100	100	0	1.8	5.5	Insertion type
	CST4.00MGW040		Built-in	Built-in	0	1.8	5.5	Capacitor on chip, insertion type
	CSA6.00MG	6.00	30	30	0	1.8	5.5	Insertion type
	CST6.00MGW		Built-in	Built-in	0	1.8	5.5	Capatitor on chip, insertion type
	CSA10.0MTZ	10.0	30	30	0	1.8	5.5	Insertion type
	CST10.0MTW		Built-in	Built-in	0	1.8	5.5	Capatitor on chip, insertion type
TDK	FCR4.0MC5	4.0	Built-in	Built-in	2.2	1.8	5.5	Capatitor on chip, insertion type
	FCR10.0MC	10.0	Built-in	Built-in	1.0	1.8	5.5	Capatitor on chip, insertion type

Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee the accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency of the resonator in the application circuit. For this, it is necessary to directly contact manufacturer of the resonator being used.

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (6/26)

(b) Main system clock: ceramic resonator (T_A = –20 to +80 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant		Oscillation Voltage Range		Remark
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
Kyocera Corp.	PBRC4.00A	4.00	33	33	1.8	5.5	Surface-mount type
	RBRC4.00B	4.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, surface-mount type
	KBR-4.00MSA	4.00	33	33	1.8	5.5	Insertion type
	KBR-4.00MKS	4.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, insertion type
	PBRC5.00A	5.00	33	33	1.8	5.5	Surface-mount type
	RBRC5.00B	5.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, surface-mount type
	KBR-5.00MSA	5.00	33	33	1.8	5.5	Insertion type
	KBR-5.00MKS	5.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, insertion type
	KBR-8M	8.00	33	33	2.7	5.5	Insertion type
	KBR-10M	10.00	33	33	2.7	5.5	Insertion type

Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee the accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency of the resonator in the application circuit. For this, it is necessary to directly contact manufacturer of the resonator being used.

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (7/26)

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH1}	P10-P17, P21, P23, P30-P32, P35-P37, P40-P47, P50-P57, P64-67	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		V_{DD}	V
				0.8 V_{DD}		V_{DD}	V
	V_{IH2}	P00-P03, P20, P22, P24-P27, P33, P34, $\overline{RESET}$	V_{DD} = 2.7 to 5.5 V	0.8 V_{DD}		V_{DD}	V
				0.85 V_{DD}		V_{DD}	V
	V_{IH3}	P60-P63 (N-ch open drain)	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		15	V
				0.8 V_{DD}		15	V
	V_{IH4}	X1, X2	V_{DD} = 2.7 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} – 0.2		V_{DD}	V
	V_{IH5}	XT1/P04, XT2	4.5 V ≤ V_{DD} ≤ 5.5 V	0.8 V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0.9 V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V **Note**	0.9 V_{DD}		V_{DD}	V
Input voltage low	V_{IL1}	P10-P17, P21, P23, P30-P32, P35-P37, P40-P47, P50-P57, P64-67	V_{DD} = 2.7 to 5.5 V	0		0.3 V_{DD}	V
				0		0.2 V_{DD}	V
	V_{IL2}	P00-P03, P20, P22, P24-P27, P33, P34, $\overline{RESET}$	V_{DD} = 2.7 to 5.5 V	0		0.2 V_{DD}	V
				0		0.15 V_{DD}	V
	V_{IL3}	P60-P63	4.5 V ≤ V_{DD} ≤ 5.5 V	0		0.3 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.2 V_{DD}	V
				0		0.1 V_{DD}	V
	V_{IL4}	X1, X2	V_{DD} = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
	V_{IL5}	XT1/P04, XT2	4.5 V ≤ V_{DD} ≤ 5.5 V	0		0.2 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.1 V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V **Note**	0		0.1 V_{DD}	V
Output voltage high	V_{OH1}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Output voltage low	V_{OL1}	P50-P57, P60-P63	V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA		0.4	2.0	V
		P01-P03, P10-P17, P20-P27 P30-P37, P40-P47, P64-P67	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{SCK0}$	V_{DD} = 4.5 to 5.5 V, open-drain, pulled-up (R = 1 kΩ)			0.2 V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V

Note When using XT1/P04 as P04, input the inverse of P04 to XT2 using an inverter.

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (8/26)

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current high	I_{LIH1}	$V_{IN} = V_{DD}$	P00-P03, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, $\overline{RESET}$			3	μA
	I_{LIH2}		X1, X2, XT1/P04, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P60-P63			80	μA
Input leakege current low	I_{LIL1}	V_{IN} = 0 V	P00-P03, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, $\overline{RESET}$			–3	μA
	I_{LIL2}		X1, X2, XT1/P04, XT2			–20	μA
	I_{LIL3}		P60-P63			–3 Note	μA
Output leakage current high	I_{LOH1}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Mask option pull-up resistor	R_1	V_{IN} = 0 V, P60-P63		20	40	90	kΩ
Software pull-up resistor	R_2	V_{IN} = 0 V, P01-P03, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67		15	40	90	kΩ

Note For P60-P63, if pull-up resistor is not provided (specifiable by mask option) a low-level input leak current of –200 μA (MAX.) flows only during the 3 clocks (no-wait time) after an instruction has been executed to read out port 6 (P6) or port mode register 6 (PM6). Outside the period of 3 clocks following execution a read-out instruction, the current is –3 μA (MAX.).

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (9/26)

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	10.00 MHz crystal oscillation operation mode	V_{DD} = 5.0 V ± 10 % Note 2		9.0	18.0	mA
			V_{DD} = 3.0 V ± 10 % Note 3		1.3	2.6	mA
	I_{DD2}	10.00 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10 % Note 2		2.4	4.8	mA
			V_{DD} = 3.0 V ± 10 % Note 3		1.2	2.4	mA
	I_{DD3}	32.768 kHz crystal oscillation operation mode Note 4	V_{DD} = 5.0 V ± 10 %		60	120	μA
			V_{DD} = 3.0 V ± 10 %		35	70	μA
			V_{DD} = 2.0 V ± 10 %		24	48	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode Note 4	V_{DD} = 5.0 V ± 10 %		25	50	μA
			V_{DD} = 3.0 V ± 10 %		5	15	μA
			V_{DD} = 2.0 V ± 10 %		2	10	μA
	I_{DD5}	XT1 = V_{DD} STOP mode when using feedback resistor	V_{DD} = 5.0 V ± 10 %		1	30	μA
			V_{DD} = 3.0 V ± 10 %		0.5	10	μA
			V_{DD} = 2.0 V ± 10 %		0.3	10	μA
	I_{DD6}	XT1 = V_{DD} STOP mode when not using feedback resistor	V_{DD} = 5.0 V ± 10 %		0.1	30	μA
			V_{DD} = 3.0 V ± 10 %		0.05	10	μA
			V_{DD} = 2.0 V ± 10 %		0.05	10	μA

Notes 1. This current excludes the AV_{REF} current, port current, and current which flows in the built-in pull-up resistor.

2. When operating at high-speed mode (when the processor clock control register (PCC) is set to 00H)

3. When operating at low-speed mode (when the PCC is set to 04H)

4. When main system clock stopped.

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (10/26)

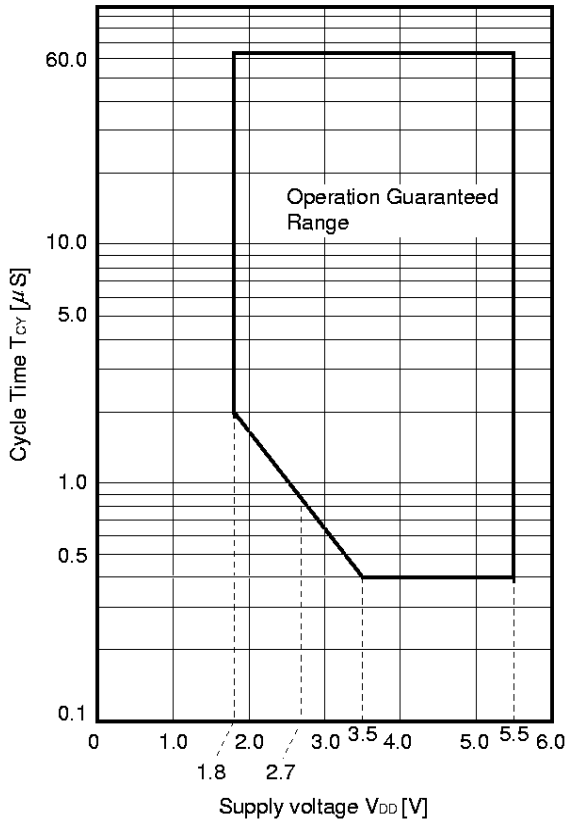
AC Characteristics

(1) Basic Operation (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating on main system clock	3.5 V ≤ V_{DD} ≤ 5.5 V	0.4		64	μs
			2.7 V ≤ V_{DD} < 3.5 V	0.8		64	μs
			1.8 V ≤ V_{DD} < 2.7 V	2.0		64	μs
		Operating on subsystem clock		40	122	125	μs
TI0 input frequency	t_{TIH0} t_{TIL0}	3.5 V ≤ V_{DD} ≤ 5.5 V		$2/f_{sam}$+0.1 Note			μs
		2.7 V ≤ V_{DD} < 3.5 V		$2/f_{sam}$+0.2 Note			μs
		1.8 V ≤ V_{DD} < 2.7 V		$2/f_{sam}$+0.5 Note			μs
TI1, TI2 input frequency	f_{TI1}	V_{DD} = 4.5 to 5.5 V		0		4	MHz
				0		275	kHz
TI1, TI2 input high/low-level width	t_{TIH1} t_{TIL1}	V_{DD} = 4.5 to 5.5 V		100			ns
				1.8			μs
Interrupt request input high/low-level width	t_{INTH} t_{INTL}	INTP0	3.5 V ≤ V_{DD} ≤ 5.5 V	$2/f_{sam}$+0.1 Note			μs
			2.7 V ≤ V_{DD} < 3.5 V	$2/f_{sam}$+0.2 Note			μs
			1.8 V ≤ V_{DD} < 2.7 V	$2/f_{sam}$+0.5 Note			μs
		INTP1-INTP3, KR0-KR7	V_{DD} = 2.7 to 5.5 V	10			μs
				20			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}	V_{DD} = 2.7 to 5.5 V		10			μs
				20			μs

Note In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register (SCS), selection of f_{sam} is possible between $fx/2^{N+1}$, fx/64 and fx/128 (when N = 0 to 4).

T_{CY} vs V_{DD} (At main system clock operation)



● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (11/26)

(2) Read/Write Operation (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.5t_{CY}$		ns
Address setup time	t_{ADS}		$0.5t_{CY}$–30		ns
Address hold time	t_{ADH}		50		ns
Data input time from address	t_{ADD1}			$(2.5+2n)t_{CY}$–50	ns
	t_{ADD2}			$(3+2n)t_{CY}$–100	ns
Data input time from $\overline{RD}$↓	t_{RDD1}			$(1+2n)t_{CY}$–25	ns
	t_{RDD2}			$(2.5+2n)t_{CY}$–100	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5+2n)t_{CY}$–20		ns
	t_{RDL2}		$(2.5+2n)$ t_{CY}–20		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{RDWT1}			$0.5t_{CY}$	ns
	t_{RDWT2}			$1.5t_{CY}$	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{WRWT}			$0.5t_{CY}$	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5+2n)t_{CY}$+10	$(2+2n)t_{CY}$	ns
Write data setup time	t_{WDS}		100		ns
Write data hold time	t_{WDH}	Load resistor ≥ 5 kΩ	20		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(2.5+2n)$ t_{CY} –20		ns
$\overline{RD}$↓ delay time from ASTB↓	t_{ASTRD}		$0.5t_{CY}$–30		ns
$\overline{WR}$↓ delay time from ASTB↓	t_{ASTWR}		$1.5t_{CY}$–30		ns
ASTB↑ delay time from $\overline{RD}$↑ in external fetch	t_{RDAST}		t_{CY}–10	t_{CY}+40	ns
Address hold time from $\overline{RD}$↑ in external fetch	t_{RDADH}		t_{CY}	t_{CY}+50	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}	V_{DD} = 4.5 to 5.5 V	$0.5t_{CY}$+5	$0.5t_{CY}$+30	ns
			$0.5t_{CY}$+15	$0.5t_{CY}$+90	ns
Write data output time from $\overline{WR}$↓	t_{WRWD}	V_{DD} = 4.5 to 5.5 V	5	30	ns
			15	90	ns
Address hold time from $\overline{WR}$↑	t_{WRADH}	V_{DD} = 4.5 to 5.5 V	t_{CY}	t_{CY}+60	ns
			t_{CY}	t_{CY}+100	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{WTRD}		$0.5t_{CY}$	$2.5t_{CY}$+80	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{WTWR}		$0.5t_{CY}$	$2.5t_{CY}$+80	ns

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates number of waits.

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (12/26)

(3) Serial Interface (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

(a) Serial Interface Channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK0}$ high/low-level width	t_{KH1}	V_{DD} = 4.5 to 5.5 V	t_{KCY1}/2–50			ns
	t_{KL1}		t_{KCY1}/2–100			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100 pF Note			300	ns

Note C is the load capacitance of $\overline{SCK0}$ and SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK0}$ high/low-level width	t_{KH2}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
	t_{KL2}	2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}			400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	C = 100 pF Note	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK0}$ rise, fall time	t_{R2} t_{F2}	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note C is the load capacitance of SO0 output line.

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (13/26)

(iii) SBI mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V_{DD} < 4.5 V		3200			ns
				4800			ns
$\overline{SCK0}$ high/low-level width	t_{KH3}	V_{DD} = 4.5 to 6.0 V		t_{KCY3}/2–50			ns
	t_{KL3}			t_{KCY3}/2–150			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK3}	4.5 V ≤ V_{DD} ≤ 5.5 V		100			ns
		2.0 V ≤ V_{DD} < 4.5 V		300			ns
				400			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI3}			t_{KCY3}/2			ns
SB0, SB1output delay time from $\overline{SCK0}$↓	t_{KSO3}	R = 1 kΩ,	V_{DD} = 4.5 to 5.5 V	0		250	ns
		C = 100 pF Note		0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R and C are the load resistors and load capacitance of the SB0, SB1 and $\overline{SCK0}$ output line.

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (14/26)

(iv) SBI mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V_{DD} < 4.5 V		3200			ns
				4800			ns
$\overline{SCK0}$ high/low-level width	t_{KH4} t_{KL4}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.0 V ≤ V_{DD} < 4.5 V		1600			ns
				2400			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK4}	4.5 V ≤ V_{DD} ≤ 5.5 V		100			ns
		2.0 V ≤ V_{DD} < 4.5 V		300			ns
				400			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI4}			t_{KCY4}/2			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO4}	R = 1 kΩ, C = 100 pF Note	V_{DD} = 4.5 to 5.5 V	0		300	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ rise, fall time	t_{R4} t_{F4}	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (15/26)

(v) 2-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF Note	2.7 V ≤ V_{DD} ≤ 5.5 V	1600			ns
			2.0 V ≤ V_{DD} < 2.7 V	3200			ns
				4800			ns
$\overline{SCK0}$ high-level width	t_{KH5}		V_{DD} = 2.7 to 5.5 V	t_{KCY5}/2–160			ns
				t_{KCY5}/2–190			ns
$\overline{SCK0}$ low-level width	t_{KL5}		V_{DD} = 4.5 to 5.5 V	t_{KCY5}/2–50			ns
				t_{KCY5}/2–100			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK5}		4.5 V ≤ V_{DD} ≤ 5.5 V	300			ns
			2.7 V ≤ V_{DD} < 4.5 V	350			ns
			2.0 V ≤ V_{DD} < 2.7 V	400			ns
				500			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI5}			600			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO5}			0		300	ns

Note R and C are the load resistors and load capacitance of the $\overline{SCK0}$, SB0 and SB1 output line.

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (16/26)

(vi) 2-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}	2.7 V ≤ V_{DD} ≤ 5.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK0}$ high-level width	t_{KH6}	2.7 V ≤ V_{DD} ≤ 5.5 V		650			ns
		2.0 V ≤ V_{DD} < 2.7 V		1300			ns
				2100			ns
$\overline{SCK0}$ low-level width	t_{KL6}	2.7 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK6}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI6}			t_{KCY6}/2			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO6}	R = 1 kΩ, C = 100 pF Note	4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			2.0 V ≤ V_{DD} < 4.5 V	0		500	ns
				0		800	ns
$\overline{SCK0}$ rise, fall time	t_{R6} t_{F6}	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (17/26)

(b) Serial Interface Channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH7}	V_{DD} = 4.5 to 5.5 V	t_{KCY7}/2–50			ns
	t_{KL7}		t_{KCY7}/2–100			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK7}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI7}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO7}	C = 100 pF Note			300	ns

Note C is the load capacitance of $\overline{SCK1}$ and SO1 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH8}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
	t_{KL8}	2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK8}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI8}			400			ns
SO0 output delay time from $\overline{SCK1}$↓	t_{KSO8}	C = 100 pF Note	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK1}$ rise, fall time	t_{R8} t_{F8}	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note C is the load capacitance of SO1 output line.

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (18/26)

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH9}	V_{DD} = 4.5 to 5.5 V	t_{KCY9}/2–50			ns
	t_{KL9}		t_{KCY9}/2–100			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK9}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI9}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO9}	C = 100 pF Note			300	ns
STB↑ from $\overline{SCK1}$↑	t_{SBD}		t_{KCY9}/2–100		t_{KCY9}/2+100	ns
Strobe signal high-level width	t_{SBW}	2.7 V ≤ V_{DD} ≤ 5.5 V	t_{KCY9}–30		t_{KCY9}+30	ns
		2.0 V ≤ V_{DD} < 2.7 V	t_{KCY9}–60		t_{KCY9}+60	ns
			t_{KCY9}–90		t_{KCY9}+90	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	200			ns
			300			ns
$\overline{SCK1}$↓ from busy inactive	t_{SPS}				2t_{KCY9}	ns

Note C is the load capacitance of $\overline{SCK1}$ and SO1 output line.

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (19/26)

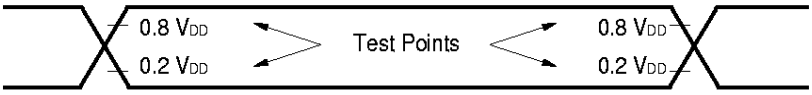
(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH10}, t_{KL10}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK10}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI10}			400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO10}	C = 100 pF Note	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK1}$ rise, fall time	t_{R10}, t_{F10}	When external device expansion function is used				160	ns
		When external device expansion function is not used				1000	ns

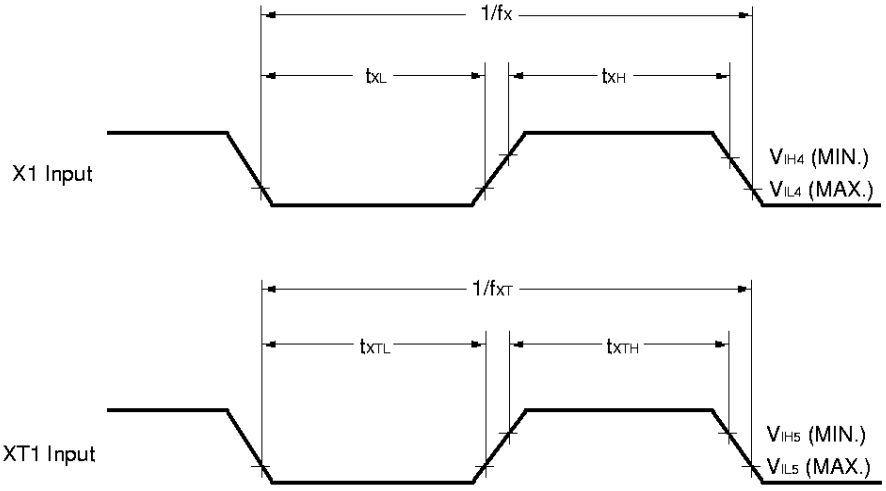
Note C is the load capacitance of the SO1 output line.

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (20/26)

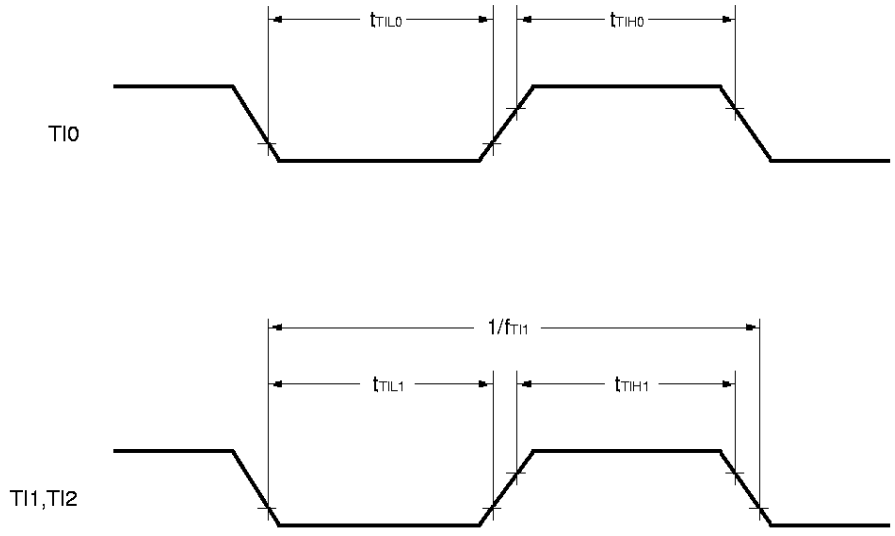
AC Timing Test Point (Excluding X1, XT1 Input)



Clock Timing



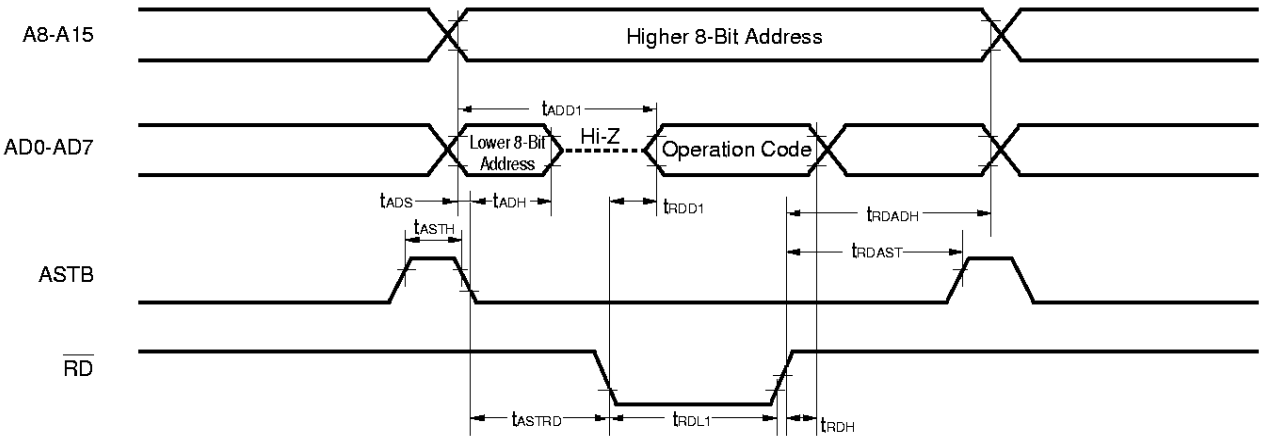
TI Timing



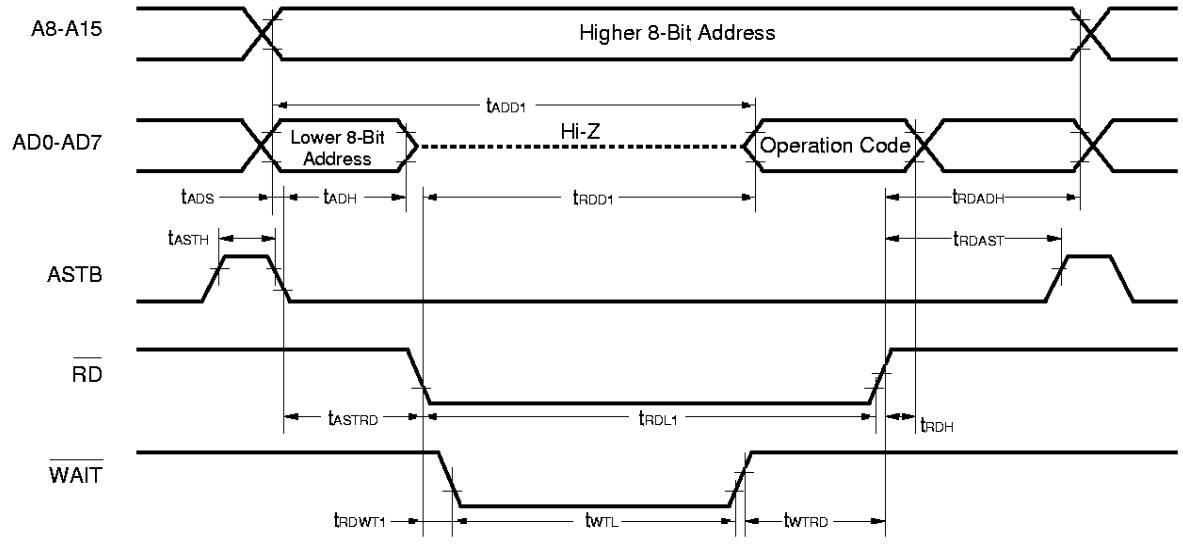
● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (21/26)

Read/Write Operation

External fetch (No wait):

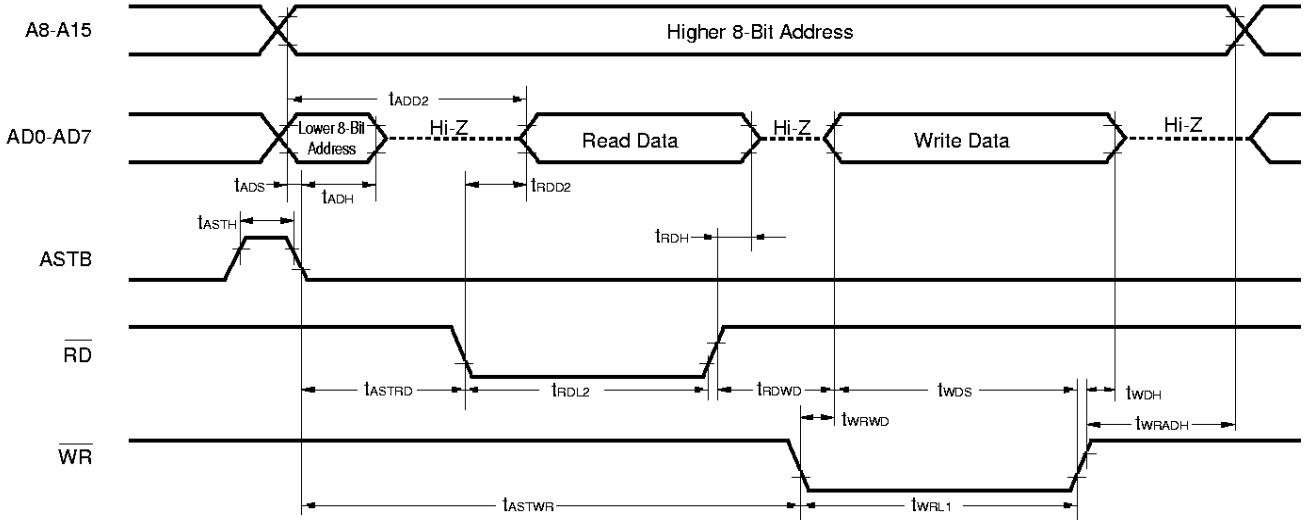


External fetch (Wait insertion):

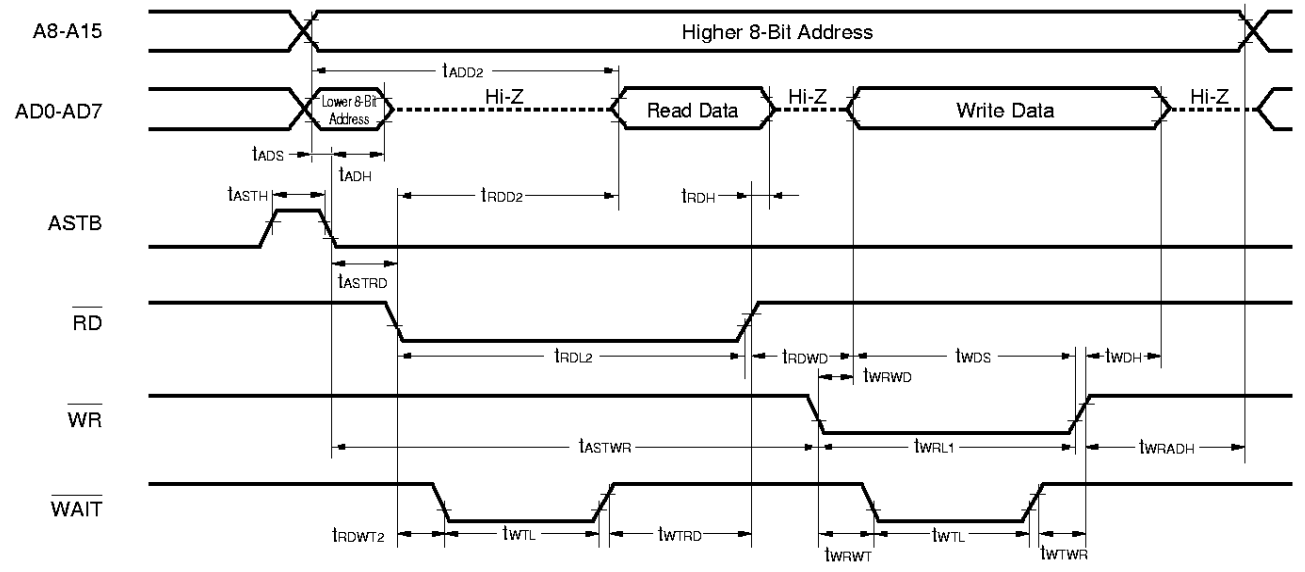


● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (22/26)

External data access (No wait):



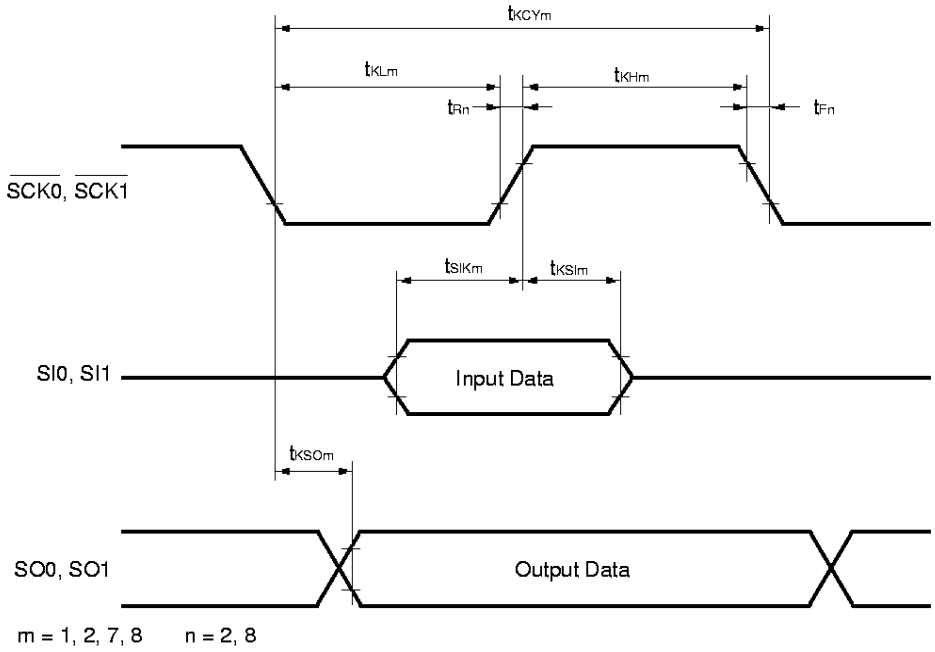
External data access (Wait insertion):



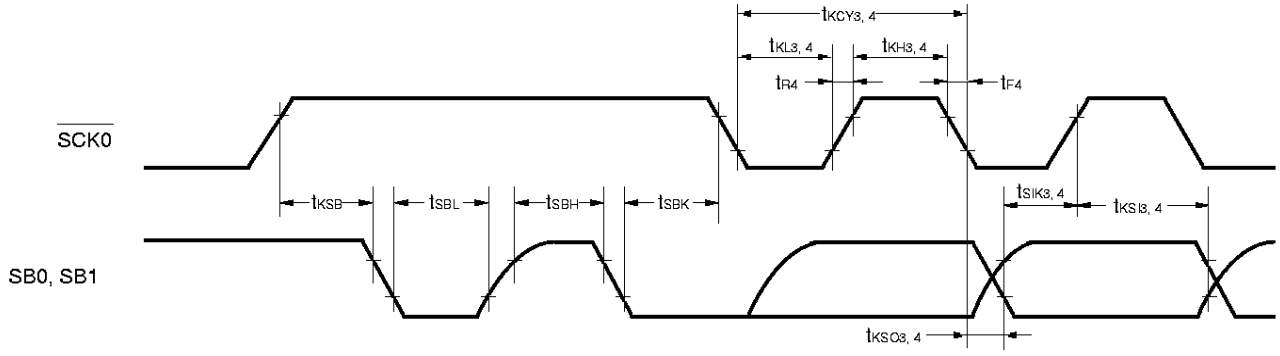
● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (23/26)

Serial Transfer Timing

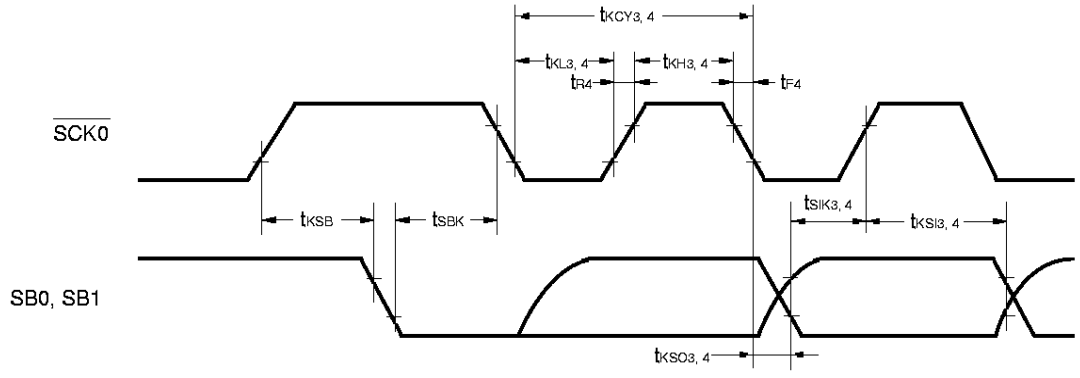
3-wire serial I/O mode:



SBI mode (Bus release signal transfer):

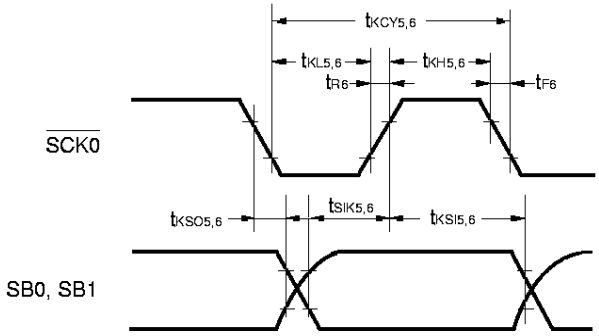


SBI Mode (command signal transfer):

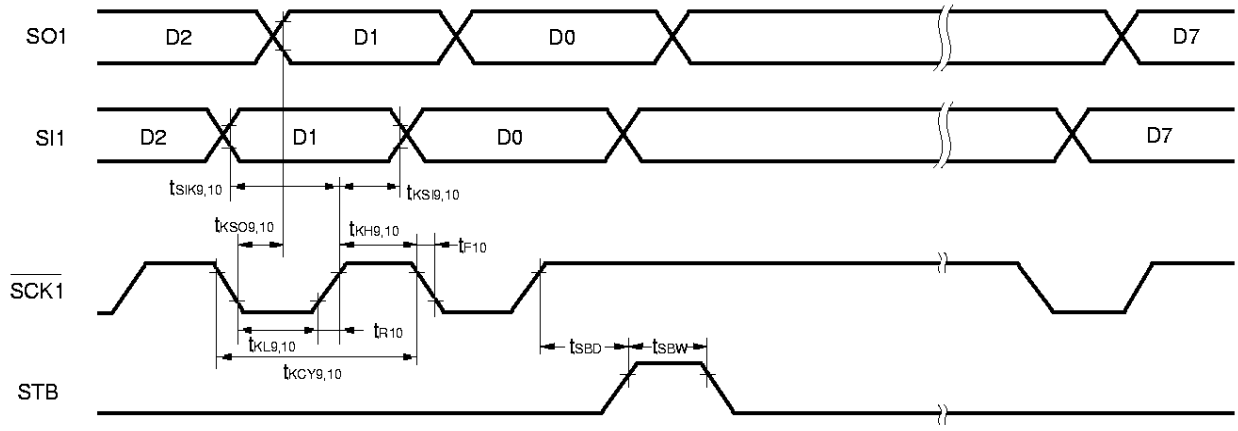


● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (24/26)

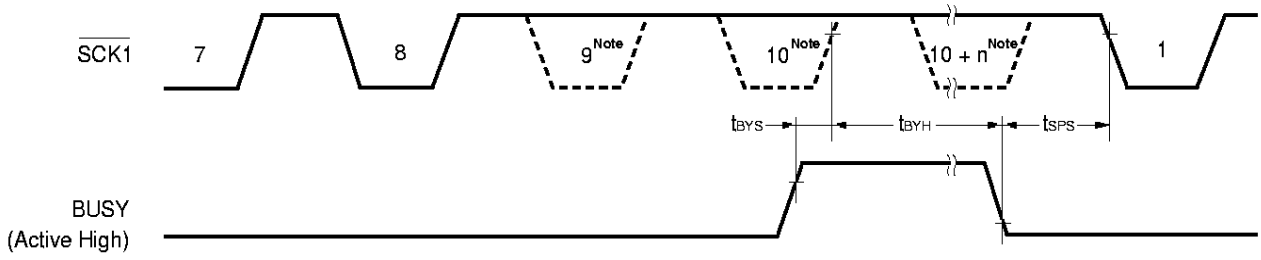
2-wire serial I/O mode:



3-wire serial I/O mode with automatic transmit/receive function:



3-wire serial I/O mode with automatic transmit/receive function (busy processing):



Note The signal is not actually driven low here; it is shown as such to indicate the timing.

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (25/26)

A/D converter characteristics (T_A = –40 to +85 °C, AV_{DD} = V_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error Note		2.7 V ≤ AV_{REF} ≤ AV_{DD}			0.6	%
		1.8 V ≤ AV_{REF} ≤ 2.7 V			1.4	%
Conversion time	t_{CONV}	2.0 V ≤ AV_{DD} < 5.5 V	19.1		200	μs
		1.8 V ≤ AV_{DD} < 2.0 V	38.2		200	μs
Sampling time	t_{SAMP}		24/fx			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
AV_{REF} resistance	R_{AIREF}		4	14		kΩ

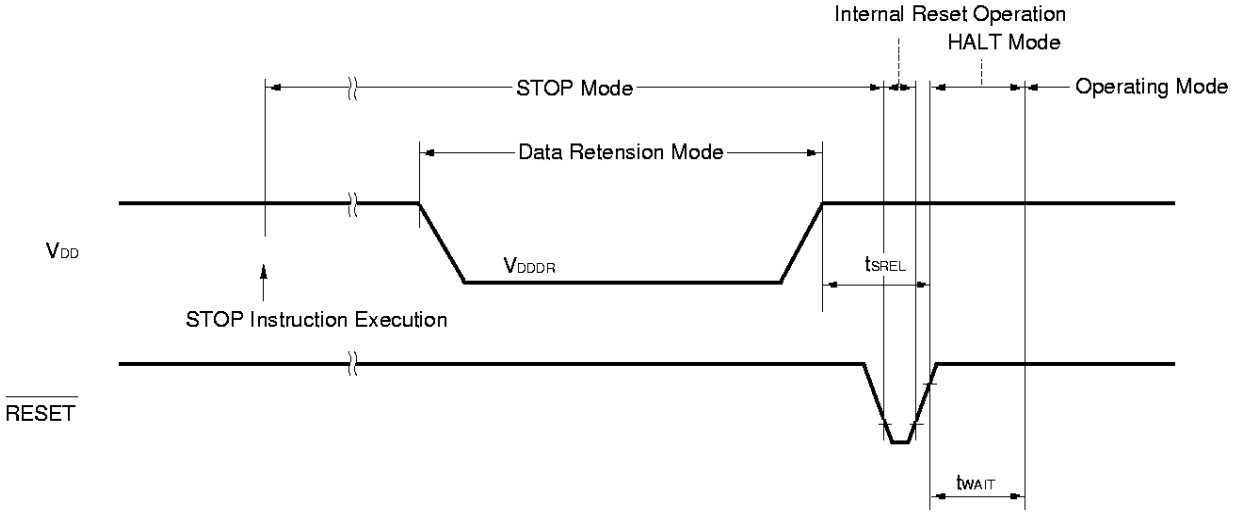
Note Overall error excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85 °C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V Subsystem clock stop and feed-back resister disconnected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		2^{18}/fx		ms
		Release by interrupt request		**Note**		ms

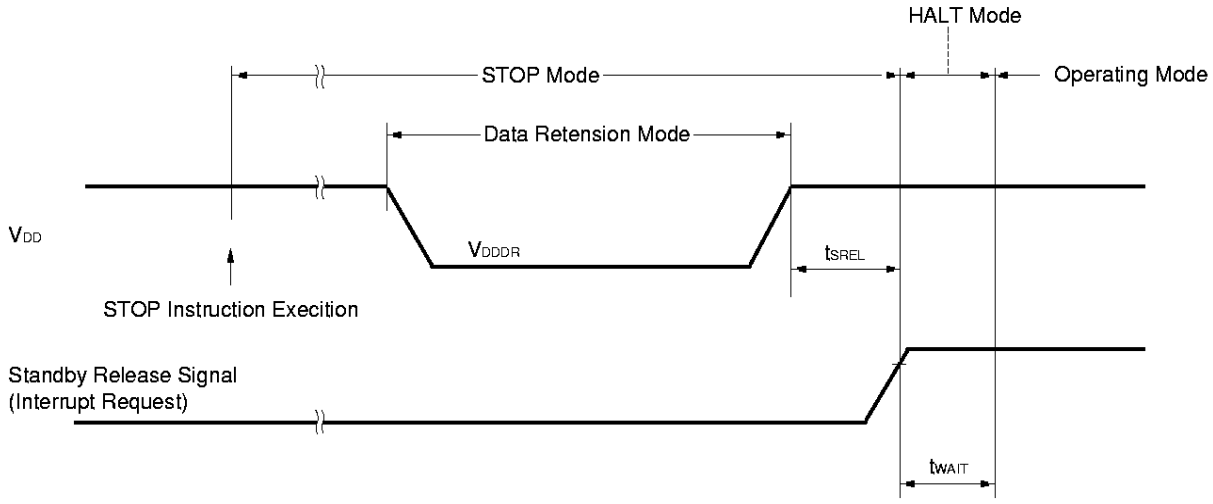
Note In combination with bit 0 to bit 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS), selection of 2^{13}/fx and 2^{15}/fx to 2^{18}/fx is possible.

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)

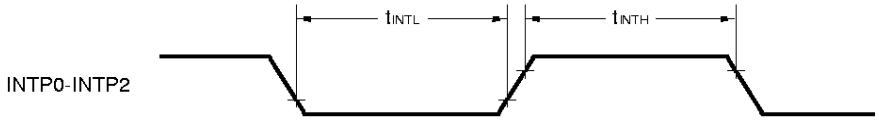


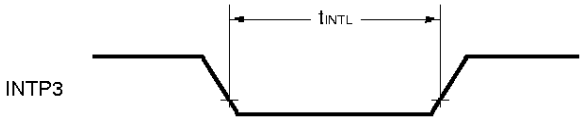
● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (26/26)

Data Retention Timing (Standby Release Signal : STOP Mode Release by Interrupt Request Signal)

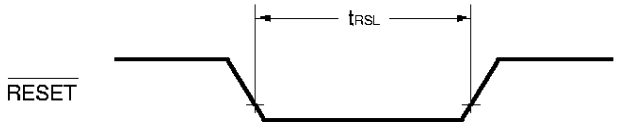


Interrupt Request Input Timing





$\overline{\text{RESET}}$ Input Timing



★ ● **Electrical Specifications of μPD78012F(A2) (1/20)**

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{REF}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00-P04, P10-P17, P20-P27, P30-P37, P40-P47 P50-P57, P64-P67, X1, X2, XT2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P60-P63	Open-drain	–0.3 to +16	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10-P17	Analog input pin	AV_{SS} – 0.3 to AV_{REF} + 0.3	V
Output current high	I_{OH}	1 pin		–10	mA
		P10-P17, P20-P27, P30-P37 total		–15	mA
		P01-P03, P40-P47, P50-P57, P60-P67 total		–15	mA
Output current low	I_{OL} Note	1 pin	Peak value	30	mA
			rms	15	mA
		P40-P47, P50-P55 total	Peak value	100	mA
			rms	70	mA
		P01-P03, P56, P57, P60-P67 total	Peak value	100	mA
			rms	70	mA
		P01-P03, P64-P67 total	Peak value	50	mA
			rms	20	mA
		P10-P17, P20-P27, P30-P37 total	Peak value	50	mA
			rms	20	mA
Operating ambient temperature	T_A			–40 to +125	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note rms should be calculated as follows: [rms] = [peak value] × $\sqrt{\text{duty}}$

Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximuam ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

● Electrical Specifications of μPD78012F(A2) (2/20)

Permissible Injection Current characteristics at overvoltage application (T_A = –40 to +125 °C, V_{DD} = 5 V ± 10 %, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions			MIN.	TYP.	MAX.	Unit
Positive direction injection current ($V_{IN} > V_{DD}$)	I_{IJH1}	1 pin	Input port other than ANIn (n = 0-7)	Peak value			2	mA
				Average value			0.2	mA
	I_{IJH2}		ANIn (n = 0-7)	Peak value			0.2	mA
				Average value			0.02	mA
	I_{IJH3}	Total for all input pins		Peak value			16	mA
				Average value			1.6	mA
	I_{IJH4}	Total for ANIn (n = 0-7)		Peak value			0.2	mA
				Average value			0.02	mA
Negative direction injection current ($V_{IN} < V_{SS}$)	I_{IJL1}	1 pin	Input port other than ANIn (n = 0-7)	Peak value			–0.1	mA
				Average value			–0.01	mA
	I_{IJL2}		ANIn (n = 0-7)	Peak value			–0.3	mA
				Average value			–0.03	mA
	I_{IJL3}	Total for all input pins		Peak value			–0.8	mA
				Average value			–0.08	mA
	I_{IJL4}	Total for ANIn (n = 0-7)		Peak value			–0.3	mA
				Average value			–0.03	mA

Cautions
1. **When injection current flows through an analog input pin (ANIn : n = 0-7), the A/D conversion result of the analog input becomes the rated value when there is no injection current ±2LSB.**
2. **When injection current flows through several analog input pins (ANIn : n = 0-7), the A/D conversion result of the analog input becomes the rated value when there is no injection current ±4LSB.**
3. **The average value (absolute value) of the pin injection current is obtained by the following formula.**

$$\text{Average value} = \left((1/T)\int_0^T |\, i(t)\,|^{3/2} dt\right)^{3/2}$$

where, i(t) indicates the pin injection current. The maximum value of | i(t) | is the peak value.

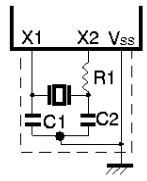
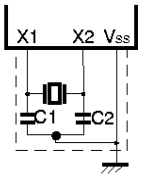
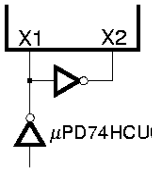
Capacitance (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P01-P03, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67			15	pF
			P60-P63			20	pF

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

● Electrical Specifications of μPD78012F(A2) (3/20)

Main System Clock Oscillation Circuit Characteristics (T_A = –40 to +125 °C, V_{DD} = 5 V ± 10 %)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (fx) Note 1		1		8	MHz
		Oscillation stabilization time Note 2	After V_{DD} reaches oscillator voltage range MIN.			10	ms
Crystal resonator		Oscillator frequency (fx) Note 1		1		8	MHz
		Oscillation stabilization time Note 2				10	ms
External clock		X1 input frequency (fx) Note 1		1.0		8.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		55		500	ns

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

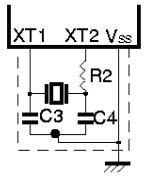
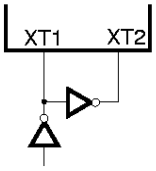
Cautions 1. When using the main system clock oscillator, wirinin the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

● **Electrical Specifications of μPD78012F(A2) (4/20)**

Subsystem Clock Oscillation Circuit Characteristics (T_A = –40 to +125 °C, V_{DD} = 5 V ± 10 %)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillator frequency (f_{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2			1.2	2	s
External clock		XT1 input frequency (f_{XT}) Note 1		32		100	kHz
		XT1 input high/low level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillator voltage MIN.

Cautions 1. When using the subsystem clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. The subsystem clock oscillation circuit is a circuit with a low amplification level, more prone to misoperation due to noise than the main system clock. Particular care is therefore required with the wiring method when the subsystem clock is used.

● **Electrical Specifications of μPD78012F(A2) (5/20)**

DC Characteristics (T_A = –40 to +125 °C, V_{DD} = 5 V ± 10%)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH1}	P10-P17, P21, P23, P30-P32, P35-P37, P40-P47, P50-P57, P64-67		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	P00-P03, P20, P22, P24-P27, P33, P34, $\overline{\text{RESET}}$		0.85 V_{DD}		V_{DD}	V
	V_{IH3}	P60-P63 (N-ch open drain)		0.7 V_{DD}		15	V
	V_{IH4}	X1, X2		V_{DD} – 0.5		V_{DD}	V
	V_{IH5}	XT1/P04, XT2		0.8 V_{DD}		V_{DD}	V
Input voltage low	V_{IL1}	P10-P17, P21, P23, P30-P32, P35-P37, P40-P47, P50-P57, P64-67		0		0.3 V_{DD}	V
	V_{IL2}	P00-P03, P20, P22, P24-P27, P33, P34, $\overline{\text{RESET}}$		0		0.18 V_{DD}	V
	V_{IL3}	P60-P63 (N-ch open drain)		0		0.3 V_{DD}	V
	V_{IL4}	X1, X2		0		0.4	V
	V_{IL5}	XT1/P04, XT2		0		0.2 V_{DD}	V
Output voltage high	V_{OH1}	I_{OH} = –1 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Output voltage low	V_{OL1}	P50-P57, P60-P63	I_{OL} = 15 mA		0.4	2.0	V
		P01-P03, P10-P17, P20-P27 P30-P37, P40-P47, P64-P67	I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	N-ch open-drain, pulled-up (R = 1 kΩ)			0.2 V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V
Input leakage current high	I_{LIH1}	V_{IN} = V_{DD}	P00-P03, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67, $\overline{\text{RESET}}$			10	μA
	I_{LIH2}		X1, X2, XT1/P04, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P60-P63			80	μA
Input leakege current low	I_{LIL1}	V_{IN} = 0 V	P00-P03, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67, $\overline{\text{RESET}}$			–10	μA
	I_{LIL2}		X1, X2, XT1/P04, XT2			–20	μA
	I_{LIL3}		P60-P63			–10 Note	μA

Note For P60-P63, if pull-up resistor is not provided (specifiable by mask option) a low-level input leak current of –200 μA (MAX.) flows only during the 3 clocks (no-wait time) after an instruction has been executed to read out port 6 (P6) or port mode register 6 (PM6). Outside the period of 3 clocks following execution a read-out instruction, the current is –10 μA (MAX.).

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

● **Electrical Specifications of μPD78012F(A2) (6/20)**

DC Characteristics (T_A = –40 to +125 °C, V_{DD} = 5 V ± 10 %)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Output leakage current high	I_{LOH}	V_{OUT} = V_{DD}			10	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V			–10	μA
Mask option pull-up resistor	R_1	V_{IN} = 0 V, P60-P63	20	40	120	kΩ
Software pull-up resistor	R_2	V_{IN} = 0 V, P01-P03, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67	15	40	120	kΩ
Supply current Note 1	I_{DD1}	8.00 MHz crystal oscillation operation mode Note 2		9.0	29.0	mA
	I_{DD2}	8.00 MHz crystal oscillation HALT mode Note 2		2.4	6.5	mA
	I_{DD3}	32.768 kHz crystal oscillation operation mode Note 3		60	1200	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode Note 3		25	1000	μA
	I_{DD5}	XT1 = V_{DD} STOP mode when using feedback resistor		1	1000	μA
	I_{DD6}	XT1 = V_{DD} STOP mode when not using feedback resistor		0.1	1000	μA

Notes 1. The current which flows in the V_{DD} pin and AV_{DD} pin. However, it does not include the current flowing in the A/D converter and built-in pull-up resistor.

2. When operating at high-speed mode (when the processor clock control register (PCC) is set to 00H)

3. When main system clock stopped.

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

● **Electrical Specifications of μPD78012F(A2) (7/20)**

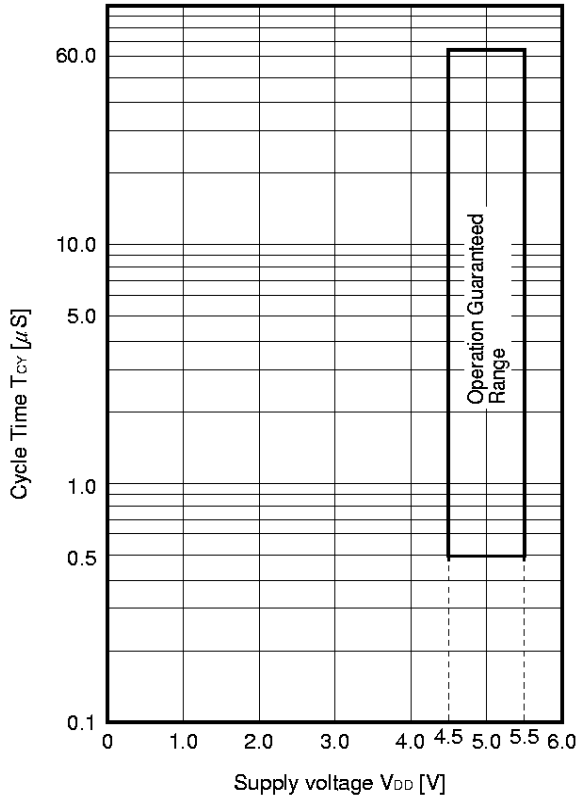
AC Characteristics

(1) Basic Operation (T_A = –40 to +125 °C, V_{DD} = 5 V ± 10 %)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating on main system clock	0.5		64	μs
		Operating on subsystem clock	40	122	125	μs
TI0 input high/low-level width	t_{TIH0} t_{TIL0}		$2/f_{sam}+0.1$ Note			μs
TI1, TI2 input frequency	f_{TI1}		0		2	kHz
TI1, TI2 input high/low-level width	t_{TIH1} t_{TIL1}		200			μs
Interrupt request input high/low-level width	t_{INTH} t_{INTL}	INTP0	$2/f_{sam}+0.1$ Note			μs
		INTP1-INTP3, KR0-KR7	10			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}		10			μs

Note In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register (SCS), selection of f_{sam} is possible between $fx/2^{N+1}$, fx/64 and fx/128 (when N = 0 to 4).

T_{CY} vs V_{DD} (At main system clock operation)



● **Electrical Specifications of μPD78012F(A2) (8/20)**

(2) Read/Write Operation (T_A = –40 to +125 °C, V_{DD} = 5 V ± 10 %)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		0.5t_{CY}		ns
Address setup time	t_{ADS}		0.5t_{CY}–30		ns
Address hold time	t_{ADH}		50		ns
Data input time from address	t_{ADD1}			(2.5+2n)t_{CY}–50	ns
	t_{ADD2}			(3+2n)t_{CY}–100	ns
Data input time from $\overline{RD}$↓	t_{RDD1}			(1+2n)t_{CY}–25	ns
	t_{RDD2}			(2.5+2n)t_{CY}–100	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(1.5+2n)t_{CY}–20		ns
	t_{RDL2}		(2.5+2n) t_{CY}–20		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{RDWT1}			0.5t_{CY}	ns
	t_{RDWT2}			1.5t_{CY}	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{WRWT}			0.5t_{CY}	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(0.5+2n)t_{CY}+10	(2+2n)t_{CY}	ns
Write data setup time	t_{WDS}		100		ns
Write data hold time	t_{WDH}	Load resistor ≥ 5 kΩ	20		ns
$\overline{WR}$ low-level width	t_{WRL1}		(2.5+2n) t_{CY}–20		ns
$\overline{RD}$↓ delay time from ASTB↓	t_{ASTRD}		0.5t_{CY}–30		ns
$\overline{WR}$↓ delay time from ASTB↓	t_{ASTWR}		1.5t_{CY}–30		ns
ASTB↑ delay time from $\overline{RD}$↑ in external fetch	t_{RDAST}		t_{CY}–10	t_{CY}+40	ns
Address hold time from $\overline{RD}$↑ in external fetch	t_{RDADH}		t_{CY}	t_{CY}+50	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}		0.5t_{CY}+5	0.5t_{CY}+30	ns
Write data output time from $\overline{WR}$↓	t_{WRWD}		5	6	ns
Address hold time from $\overline{WR}$↑	t_{WRADH}		t_{CY}	t_{CY}+60	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{WTRD}		0.5t_{CY}	2.5t_{CY}+80	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{WTWR}		0.5t_{CY}	2.5t_{CY}+80	ns

Remarks 1. t_{CY} = T_{CY}/4

2. n indicates number of waits.

● Electrical Specifications of μPD78012F(A2) (9/20)

(3) Serial Interface (T_A = –40 to +125 °C, V_{DD} = 5 V ±10 %)

(a) Serial Interface Channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}		1000			ns
$\overline{SCK0}$ high/low-level width	t_{KH1} t_{KL1}		t_{KCY1}/2–100			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}		150			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		500			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100 pF Note			400	ns

Note C is the load capacitance of $\overline{SCK0}$ and SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}			1000			ns
$\overline{SCK0}$ high/low-level width	t_{KH2} t_{KL2}			500			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}			150			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}			500			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	C = 100 pF Note				400	ns
$\overline{SCK0}$ rise, fall time	t_{R2} t_{F2}	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note C is the load capacitance of SO0 output line.

● **Electrical Specifications of μPD78012F(A2) (10/20)**

(iii) SBI mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}		1000			ns
$\overline{SCK0}$ high/low-level width	t_{KH3} t_{KL3}		$t_{KCY3}/2-100$			ns
SB0, SB1 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK3}		150			ns
SB0, SB1 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI3}		$t_{KCY3}/2$			ns
SB0, SB1output delay time from $\overline{SCK0}\downarrow$	t_{KSO3}	R = 1 kΩ, C = 100 pF Note			300	ns
SB0, SB1↓ from $\overline{SCK0}\downarrow$	t_{KSB}		t_{KCY3}			ns
$\overline{SCK0}\downarrow$ from SB0, SB1↓	t_{SBK}		t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}		t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}		t_{KCY3}			ns

Note R and C are the load resistors and load capacitance of the SB0, SB1 and $\overline{SCK0}$ output line.

(iv) SBI mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}			1000			ns
$\overline{SCK0}$ high/low-level width	t_{KH4} t_{KL4}			500			ns
SB0, SB1 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK4}			150			ns
SB0, SB1 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI4}			$t_{KCY4}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}\downarrow$	t_{KSO4}	R = 1 kΩ, C = 100 pF Note				400	ns
SB0, SB1↓ from $\overline{SCK0}\downarrow$	t_{KSB}			t_{KCY4}			ns
$\overline{SCK0}\downarrow$ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ rise, fall time	t_{R4} t_{F4}	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

● **Electrical Specifications of μPD78012F(A2) (11/20)**

(v) 2-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF Note	1600			ns
$\overline{SCK0}$ high-level width	t_{KH5}		$t_{KCY5}/2-160$			ns
$\overline{SCK0}$ low-level width	t_{KL5}		$t_{KCY5}/2-100$			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK5}		350			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI5}		600			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO5}				300	ns

Note R and C are the load resistors and load capacitance of the $\overline{SCK0}$, SB0 and SB1 output line.

(vi) 2-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}			1600			ns
$\overline{SCK0}$ high-level width	t_{KH6}			650			ns
$\overline{SCK0}$ low-level width	t_{KL6}			800			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK6}			100			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI6}			$t_{KCY6}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO6}	R = 1 kΩ, C = 100 pF Note				500	ns
$\overline{SCK0}$ rise, fall time	t_{R6} t_{F6}	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

● **Electrical Specifications of μPD78012F(A2) (12/20)**

(b) Serial Interface Channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}		1000			ns
$\overline{SCK1}$ high/low-level width	t_{KH7} t_{KL7}		$t_{KCY7}/2-100$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK7}		150			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI7}		500			ns
SO1 output delay time from $\overline{SCK1}\downarrow$	t_{KSO7}	C = 100 pF **Note**			400	ns

Note C is the load capacitance of $\overline{SCK1}$ and SO1 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}			1000			ns
$\overline{SCK1}$ high/low-level width	t_{KH8} t_{KL8}			500			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK8}			150			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI8}			500			ns
SO0 output delay time from $\overline{SCK1}\downarrow$	t_{KSO8}	C = 100 pF **Note**				400	ns
$\overline{SCK1}$ rise, fall time	t_{R8} t_{F8}	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note C is the load capacitance of SO1 output line.

● **Electrical Specifications of μPD78012F(A2) (13/20)**

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}		1000			ns
$\overline{SCK1}$ high/low-level width	t_{KH9} t_{KL9}		$t_{KCY9}/2-100$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK9}		150			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI9}		500			ns
SO1 output delay time from $\overline{SCK1}\downarrow$	t_{KSO9}	C = 100 pF Note			400	ns
STB$\uparrow$ from $\overline{SCK1}\uparrow$	t_{SBD}		$t_{KCY9}/2-100$		$t_{KCY9}/2+100$	ns
Strobe signal high-level width	t_{SBW}		$t_{KCY9}/2-30$		$t_{KCY9}/2+30$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}		150			ns
$\overline{SCK1}\downarrow$ from busy inactive	t_{SPS}				$2t_{KCY9}$	ns

Note C is the load capacitance of $\overline{SCK1}$ and SO1 output line.

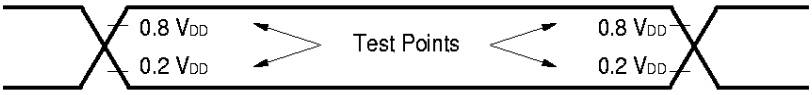
(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}			1000			ns
$\overline{SCK1}$ high/low-level width	t_{KH10}, t_{KL10}			500			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK10}			150			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI10}			500			ns
SO1 output delay time from $\overline{SCK1}\downarrow$	t_{KSO10}	C = 100 pF Note				400	ns
$\overline{SCK1}$ rise, fall time	t_{R10}, t_{FB}	When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

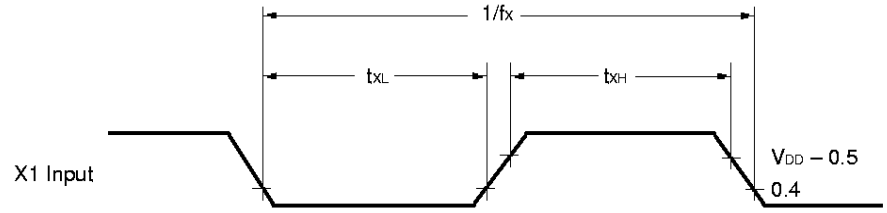
Note C is the load capacitance of the SO1 output line.

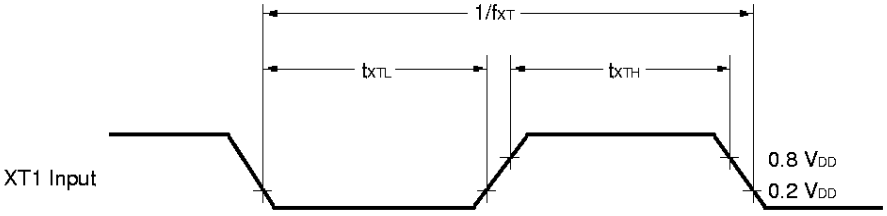
● Electrical Specifications of μPD78012F(A2) (14/20)

AC Timing Test Point (Excluding X1, XT1 Input)

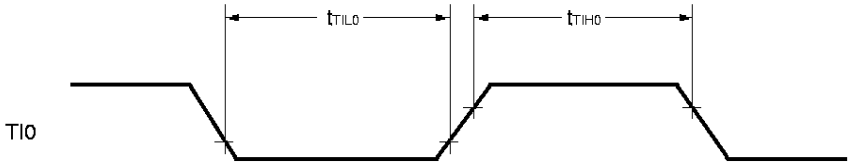


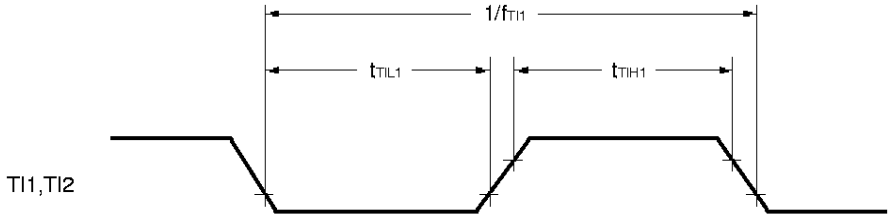
Clock Timing





TI Timing

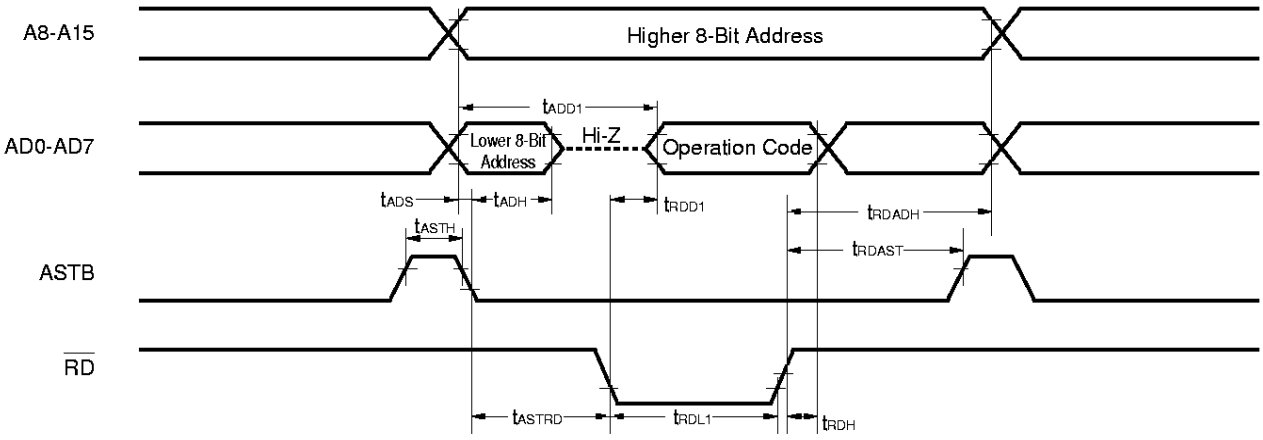




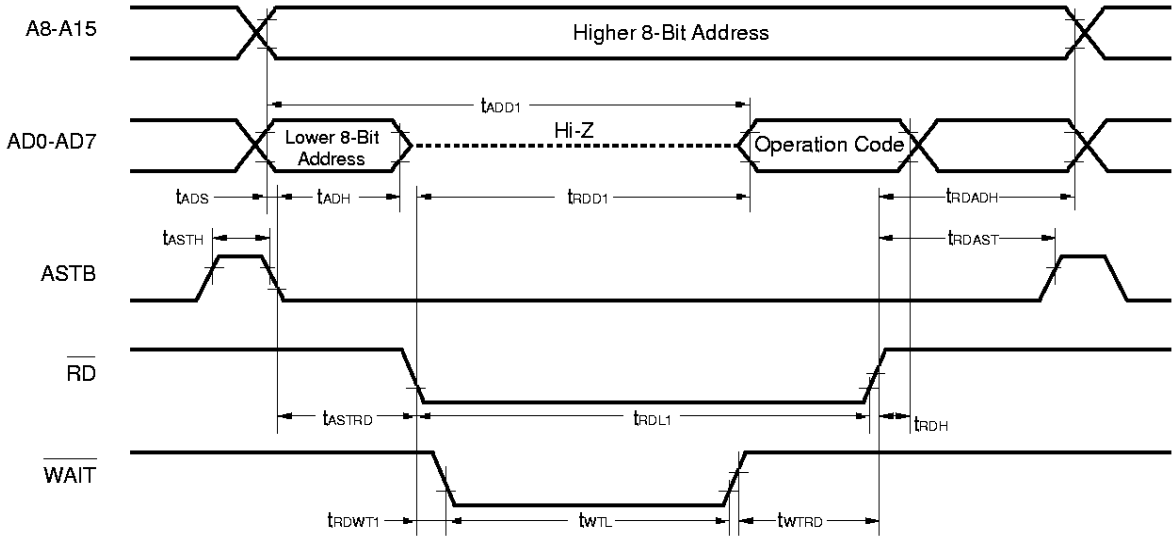
● **Electrical Specifications of μPD78012F(A2) (15/20)**

Read/Write Operation

External fetch (No wait):

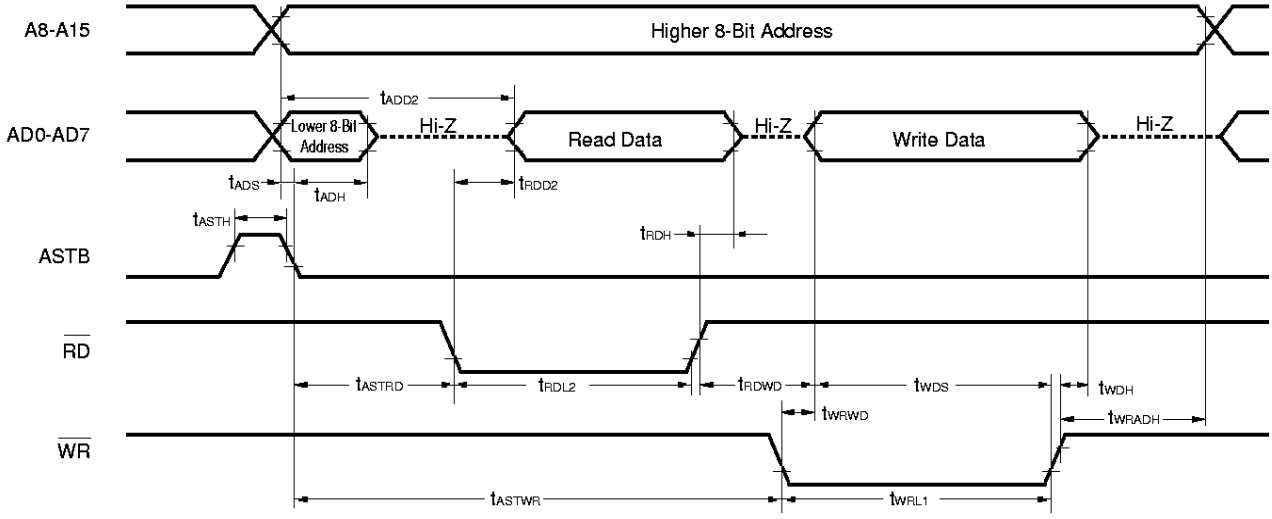


External fetch (Wait insertion):

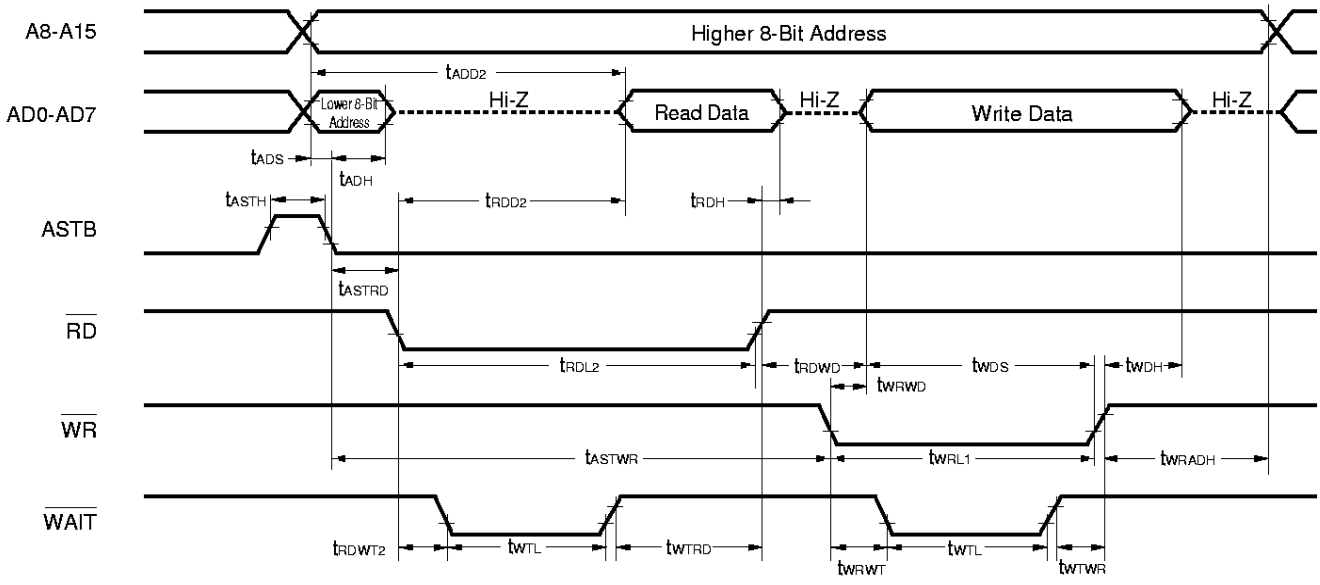


● **Electrical Specifications of μPD78012F(A2) (16/20)**

External data access (No wait):



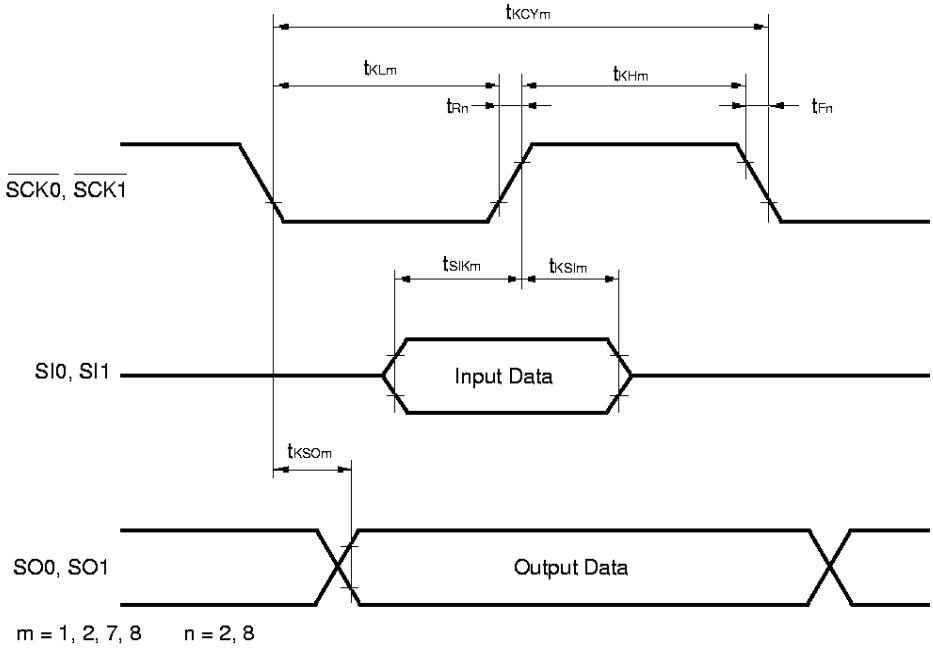
External data access (Wait insertion):



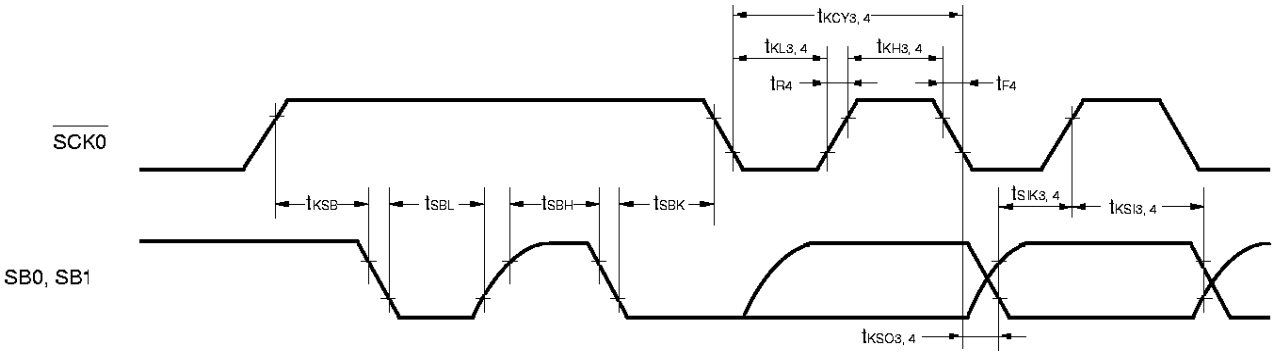
● **Electrical Specifications of μPD78012F(A2) (17/20)**

Serial Transfer Timing

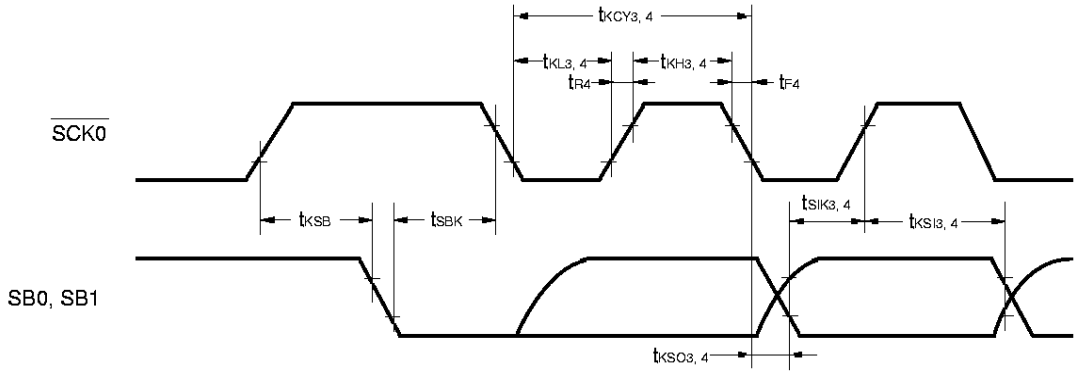
3-wire serial I/O mode:



SBI mode (Bus release signal transfer):

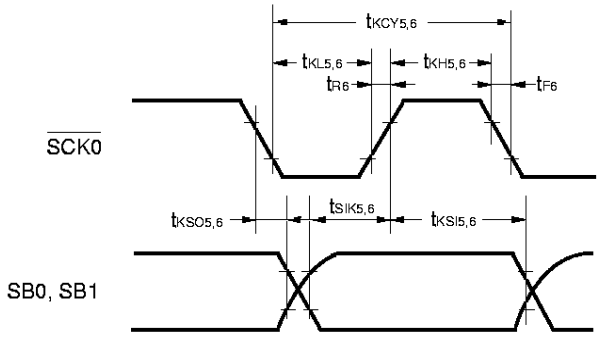


SBI Mode (command signal transfer):

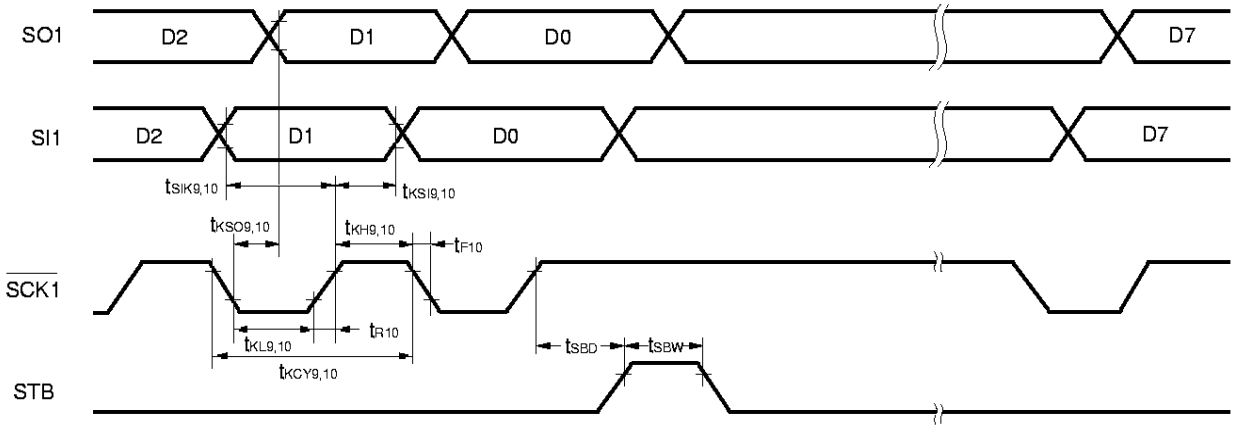


● **Electrical Specifications of μPD78012F(A2) (18/20)**

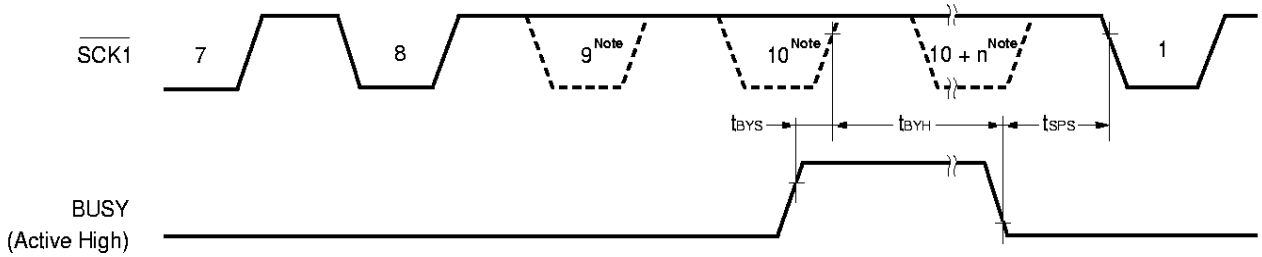
2-wire serial I/O mode:



3-wire serial I/O mode with automatic transmit/receive function:



3-wire serial I/O mode with automatic transmit/receive function (busy processing):



Note The signal is not actually driven low here; it is shown as such to indicate the timing.

● **Electrical Specifications of μPD78012F(A2) (19/20)**

A/D converter characteristics (T_A = –40 to +125 °C, AV_{DD} = V_{DD} = 5.0 V ± 10 %, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error Note		4.5 V ≤ AV_{REF} ≤ AV_{DD}			1.0	%
Conversion time	t_{CONV}	4.5 V ≤ AV_{DD} ≤ 5.5 V	23.8		200	μs
Sampling time	t_{SAMP}		24/fx			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		4.5		AV_{DD}	V
AV_{REF} resistance	R_{AIREF}		4	14		kΩ

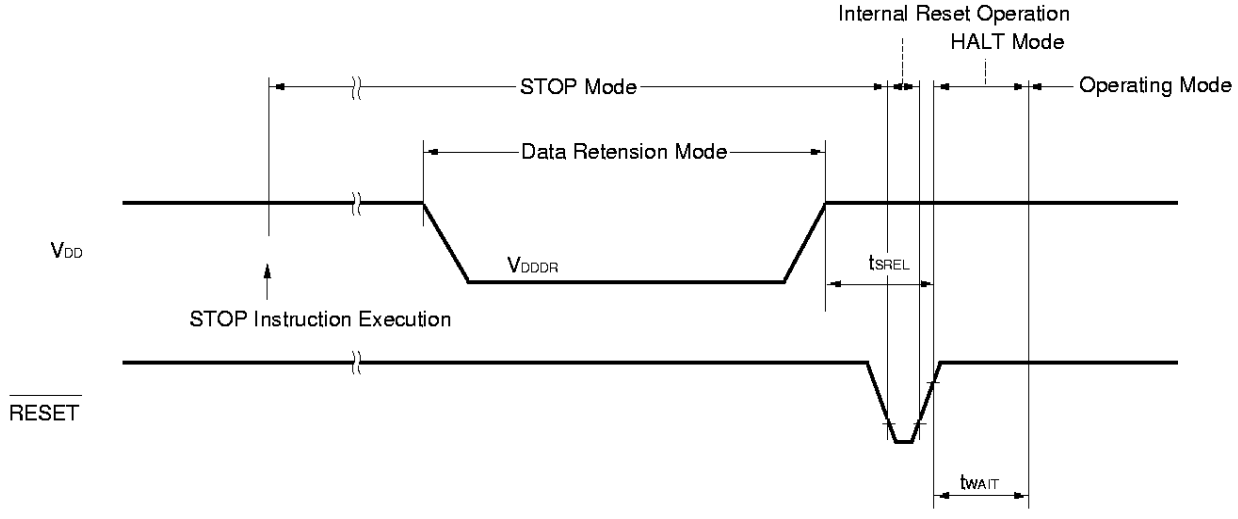
Note Overall error excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +125 °C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.7		5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.7 V Subsystem clock stop and feed-back resister disconnected		0.1	1000	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		2^{16}/fx		ms
		Release by interrupt request		**Note**		ms

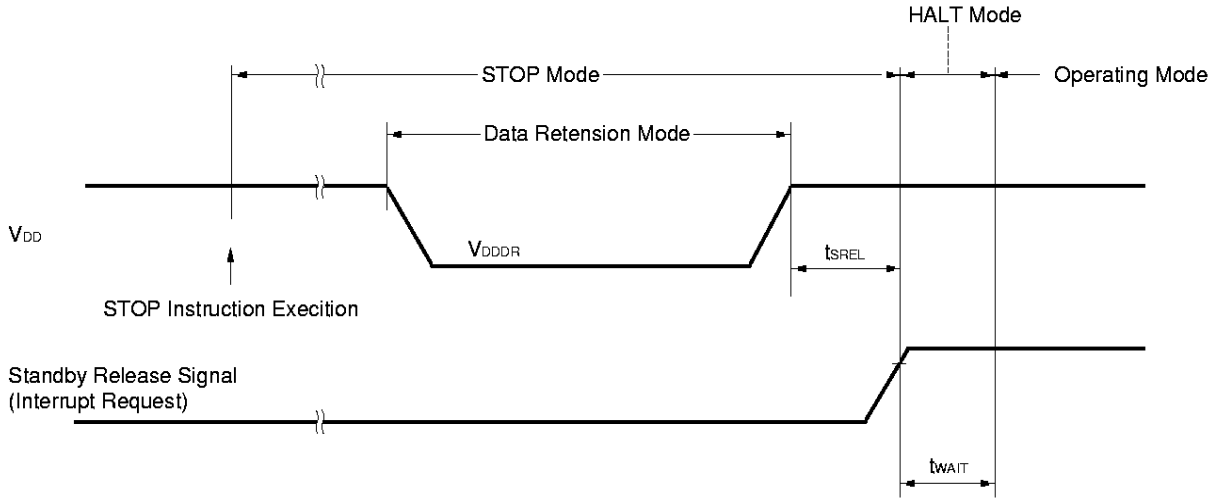
Note In combination with bit 0 to bit 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS), selection of 2^{13}/fx and 2^{15}/fx to 2^{18}/fx is possible.

Data Retention Timing (STOP Mode Release by $\overline{RESET}$)

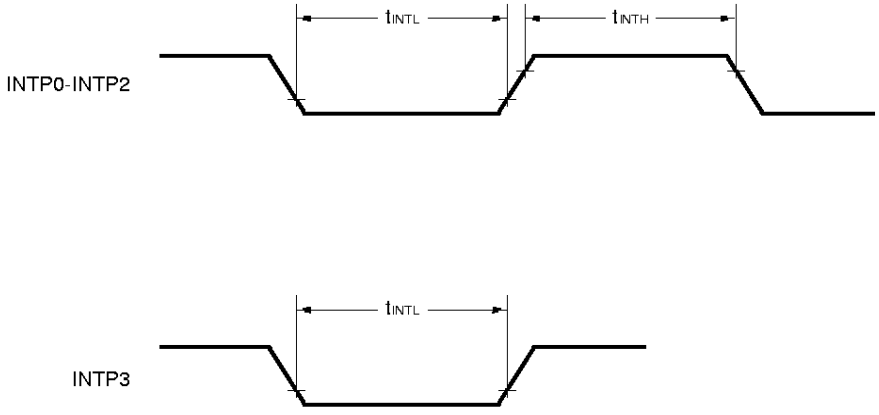


● **Electrical Specifications of μPD78012F(A2) (20/20)**

Data Retention Timing (Standby Release Signal : STOP Mode Release by Interrupt Request Signal)



Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing