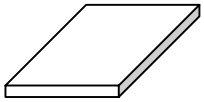
10-CHARACTER 1-LINE LCD DRIVER WITH SMOOTH SCROLL FUNCTION

■ GENERAL DESCRIPTION

The NJU6515 LCD driver can realize 10-character 1-line and max. 118 icons display. It contains voltage boost, regulator, bleeder resistor, general output ports, oscillator, microprocessor interface circuit, instruction decoder, character generator ROM/RAM and common and segment drivers.
The NJU6515 can realize display with 1-wire serial data from MPU, and its low operation voltage and low current consumption make it very suitable for the space-conscious products.

■ PACKAGE OUTLINE



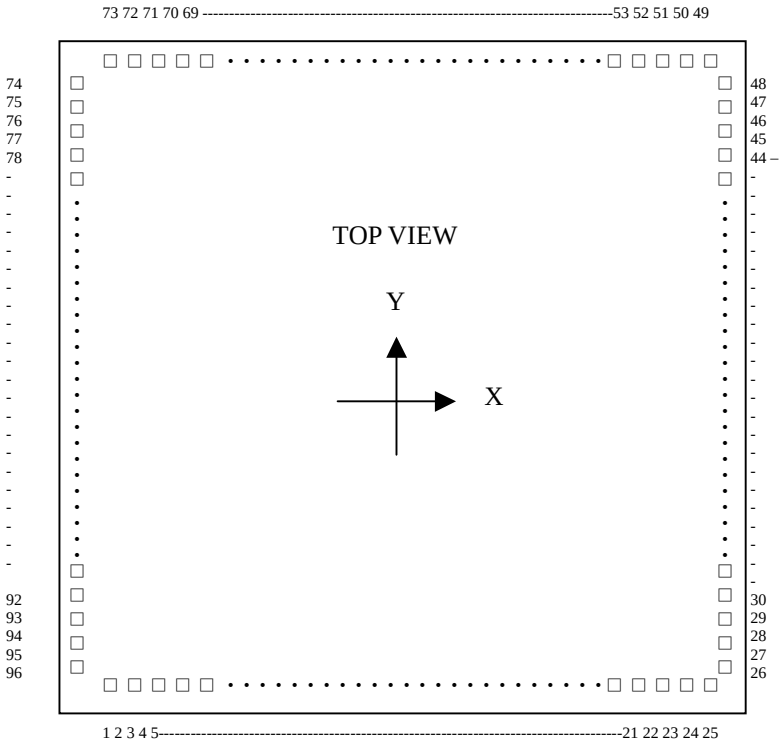
NJU6515C

■ FEATURES

- 10-character 1-line
- Maximum 118 Icon Display
- 1-wire Serial Interface
- Display Data RAM 11 x 8 bits
- Character Generator ROM 6,720 bits (192 characters for 5 x 7 dots)
- Character Generator RAM 77 x 5 bits (11 Patterns for 5 x 7 dots)
- Icon Display RAM 118 bits
- Duty Ratio 1/8, 1/9 (Programmable)
- Relocateable COM and SEG Drivers
- Various Instructions Display Clear, Return Home, Entry Mode, Duty Ratio, Display ON/OFF, Address Shift, Pattern Shift, Dot Shift, Power Control, General Ports, Electrical Volume, RAM Address, RAM Data Writing
- Voltage Boost 2-time, 3-time
- Power On Reset Function
- Voltage Regulator 8-step
- Electrical Volume 16-step
- Oscillation Circuit External Resistor and Capacitor Required
- Bleeder Resistor
- Operating Voltage +1.7 to 5.5V
- C-MOS Technology (P-sub)
- Package Outline Bare Chip (for COB)

Contents

■ PAD ALIGNMENT



Chip Size:	3.45 x 3.25mm
Chip Center:	X=0µm, Y=0µm
PAD Size:	90µm x 90µm
PAD Pitch:	117.7µm pitch
Chip Thickness:	400µm

■ PAD COORDINATES

(1) A Mode (SEL1="0", SEL2="0")

Chip Size 3.45mm x 3.25mm (Chip Center X=μ0m, Y=0μm)

PAD No.	Terminal	X= μm	Y= μm
1	RSTOUT	-1412.4	-1452.0
2	DC	-1294.7	-1452.0
3	SEL1	-1177.0	-1452.0
4	SEL2	-1059.3	-1452.0
5	IF1	-941.6	-1452.0
6	IF2	-823.9	-1452.0
7	FSEL	-706.2	-1452.0
8	SI	-588.5	-1452.0
9	REGON	-470.8	-1452.0
10	OSC1	-353.1	-1452.0
11	VDD	-235.4	-1452.0
12	VSS	-117.7	-1452.0
13	VSS	0	-1452.0
14	Vci	117.7	-1452.0
15	VREG	235.4	-1452.0
16	C1+	353.1	-1452.0
17	C1-	470.8	-1452.0
18	C2+	588.5	-1452.0
19	C2-	706.2	-1452.0
20	VOUT	823.9	-1452.0
21	VLCD1	941.6	-1452.0
22	VLCD2	1059.3	-1452.0
23	V1	1177.0	-1452.0
24	V2	1294.7	-1452.0
25	V4	1412.4	-1452.0
26	SEG59	1551.0	-1294.7
27	SEG58	1551.0	-1177.0
28	SEG57	1551.0	-1059.3
29	SEG56	1551.0	-941.6
30	SEG55	1551.0	-823.9
31	SEG54	1551.0	-706.2
32	SEG53	1551.0	-588.5
33	SEG52	1551.0	-470.8
34	SEG51	1551.0	-353.1
35	SEG50	1551.0	-235.4
36	SEG49	1551.0	-117.7
37	SEG48	1551.0	0
38	SEG47	1551.0	117.7
39	SEG46	1551.0	235.4
40	SEG45	1551.0	353.1
41	SEG44	1551.0	470.8
42	SEG43	1551.0	588.5
43	SEG42	1551.0	706.2
44	SEG41	1551.0	823.9
45	SEG40	1551.0	941.6
46	SEG39	1551.0	1059.3
47	SEG38	1551.0	1177.0
48	SEG37	1551.0	1294.7

PAD No.	Terminal	X= μm	Y= μm
49	SEG36	1412.4	1451.0
50	SEG35	1294.7	1451.0
51	SEG34	1177.0	1451.0
52	SEG33	1059.3	1451.0
53	SEG32	941.6	1451.0
54	SEG31	823.9	1451.0
55	SEG30	706.2	1451.0
56	SEG29	588.5	1451.0
57	SEG28	470.8	1451.0
58	SEG27	353.1	1451.0
59	SEG26	235.4	1451.0
60	SEG25	117.7	1451.0
61	SEG24	0	1451.0
62	SEG23	-117.7	1451.0
63	SEG22	-235.4	1451.0
64	SEG21	-353.1	1451.0
65	SEG20	-470.8	1451.0
66	SEG19	-588.5	1451.0
67	SEG18	-706.2	1451.0
68	SEG17	-823.9	1451.0
69	SEG16	-941.6	1451.0
70	SEG15	-1059.3	1451.0
71	SEG14	-1177.0	1451.0
72	SEG13	-1294.7	1451.0
73	SEG12	-1412.4	1451.0
74	SEG11	-1551.0	1294.7
75	SEG10	-1551.0	1177.0
76	SEG9	-1551.0	1059.3
77	SEG8	-1551.0	941.6
78	SEG7	-1551.0	823.9
79	SEG6	-1551.0	706.2
80	SEG5	-1551.0	588.5
81	SEG4	-1551.0	470.8
82	SEG3	-1551.0	353.1
83	SEG2	-1551.0	235.4
84	SEG1	-1551.0	117.7
85	COMMK2	-1551.0	0
86	COM7	-1551.0	-117.7
87	COM6	-1551.0	-235.4
88	COM5	-1551.0	-353.1
89	COM4	-1551.0	-470.8
90	COM3	-1551.0	-588.5
91	COM2	-1551.0	-706.2
92	COM1	-1551.0	-823.9
93	COMMK1	-1551.0	-941.6
94	P1	-1551.0	-1059.3
95	P2	-1551.0	-1177.0
96	P3	-1551.0	-1294.7

(2) B Mode (SEL1="1", SEL2="1")

Chip Size 3.45mm x 3.25mm (Chip Center X=µ0m, Y=0µm)

PAD No.	Terminal	X= µm	Y= µm
1	RSTOUT	-1412.4	-1452.0
2	DC	-1294.7	-1452.0
3	SEL1	-1177.0	-1452.0
4	SEL2	-1059.3	-1452.0
5	IF1	-941.6	-1452.0
6	IF2	-823.9	-1452.0
7	FSEL	-706.2	-1452.0
8	SI	-588.5	-1452.0
9	REGON	-470.8	-1452.0
10	OSC1	-353.1	-1452.0
11	VDD	-235.4	-1452.0
12	VSS	-117.7	-1452.0
13	VSS	0	-1452.0
14	Vci	117.7	-1452.0
15	VREG	235.4	-1452.0
16	C1+	353.1	-1452.0
17	C1-	470.8	-1452.0
18	C2+	588.5	-1452.0
19	C2-	706.2	-1452.0
20	VOUT	823.9	-1452.0
21	VLCD1	941.6	-1452.0
22	VLCD2	1059.3	-1452.0
23	V1	1177.0	-1452.0
24	V2	1294.7	-1452.0
25	V4	1412.4	-1452.0
26	SEG1	1551.0	-1294.7
27	SEG2	1551.0	-1177.0
28	SEG3	1551.0	-1059.3
29	SEG4	1551.0	-941.6
30	SEG5	1551.0	-823.9
31	SEG6	1551.0	-706.2
32	SEG7	1551.0	-588.5
33	SEG8	1551.0	-470.8
34	SEG9	1551.0	-353.1
35	SEG10	1551.0	-235.4
36	SEG11	1551.0	-117.7
37	SEG12	1551.0	0
38	SEG13	1551.0	117.7
39	SEG14	1551.0	235.4
40	SEG15	1551.0	353.1
41	SEG16	1551.0	470.8
42	SEG17	1551.0	588.5
43	SEG18	1551.0	706.2
44	SEG19	1551.0	823.9
45	SEG20	1551.0	941.6
46	SEG21	1551.0	1059.3
47	SEG22	1551.0	1177.0
48	SEG23	1551.0	1294.7

PAD No.	Terminal	X= µm	Y= µm
49	SEG24	1412.4	1451.0
50	SEG25	1294.7	1451.0
51	SEG26	1177.0	1451.0
52	SEG27	1059.3	1451.0
53	SEG28	941.6	1451.0
54	SEG29	823.9	1451.0
55	SEG30	706.2	1451.0
56	SEG31	588.5	1451.0
57	SEG32	470.8	1451.0
58	SEG33	353.1	1451.0
59	SEG34	235.4	1451.0
60	SEG35	117.7	1451.0
61	SEG36	0	1451.0
62	SEG37	-117.7	1451.0
63	SEG38	-235.4	1451.0
64	SEG39	-353.1	1451.0
65	SEG40	-470.8	1451.0
66	SEG41	-588.5	1451.0
67	SEG42	-706.2	1451.0
68	SEG43	-823.9	1451.0
69	SEG44	-941.6	1451.0
70	SEG45	-1059.3	1451.0
71	SEG46	-1177.0	1451.0
72	SEG47	-1294.7	1451.0
73	SEG48	-1412.4	1451.0
74	SEG49	-1551.0	1294.7
75	SEG50	-1551.0	1177.0
76	SEG51	-1551.0	1059.3
77	SEG52	-1551.0	941.6
78	SEG53	-1551.0	823.9
79	SEG54	-1551.0	706.2
80	SEG55	-1551.0	588.5
81	SEG56	-1551.0	470.8
82	SEG57	-1551.0	353.1
83	SEG58	-1551.0	235.4
84	SEG59	-1551.0	117.7
85	COMMK1	-1551.0	0
86	COM1	-1551.0	-117.7
87	COM2	-1551.0	-235.4
88	COM3	-1551.0	-353.1
89	COM4	-1551.0	-470.8
90	COM5	-1551.0	-588.5
91	COM6	-1551.0	-706.2
92	COM7	-1551.0	-823.9
93	COMMK2	-1551.0	-941.6
94	P1	-1551.0	-1059.3
95	P2	-1551.0	-1177.0
96	P3	-1551.0	-1294.7

(3) C Code (SEL1="1", SEL2="0")

Chip Size 3.45mm x 3.25mm (Chip Center X=µ0m, Y=0µm)

PAD No.	Terminal	X= µm	Y= µm
1	RSTOUT	-1412.4	-1452.0
2	DC	-1294.7	-1452.0
3	SEL1	-1177.0	-1452.0
4	SEL2	-1059.3	-1452.0
5	IF1	-941.6	-1452.0
6	IF2	-823.9	-1452.0
7	FSEL	-706.2	-1452.0
8	SI	-588.5	-1452.0
9	REGON	-470.8	-1452.0
10	OSC1	-353.1	-1452.0
11	VDD	-235.4	-1452.0
12	VSS	-117.7	-1452.0
13	VSS	0	-1452.0
14	Vci	117.7	-1452.0
15	VREG	235.4	-1452.0
16	C1+	353.1	-1452.0
17	C1-	470.8	-1452.0
18	C2+	588.5	-1452.0
19	C2-	706.2	-1452.0
20	VOUT	823.9	-1452.0
21	VLCD1	941.6	-1452.0
22	VLCD2	1059.3	-1452.0
23	V1	1177.0	-1452.0
24	V2	1294.7	-1452.0
25	V4	1412.4	-1452.0
26	SEG59	1551.0	-1294.7
27	SEG58	1551.0	-1177.0
28	SEG57	1551.0	-1059.3
29	SEG56	1551.0	-941.6
30	SEG55	1551.0	-823.9
31	SEG54	1551.0	-706.2
32	SEG53	1551.0	-588.5
33	SEG52	1551.0	-470.8
34	SEG51	1551.0	-353.1
35	SEG50	1551.0	-235.4
36	SEG49	1551.0	-117.7
37	SEG48	1551.0	0
38	SEG47	1551.0	117.7
39	SEG46	1551.0	235.4
40	SEG45	1551.0	353.1
41	SEG44	1551.0	470.8
42	SEG43	1551.0	588.5
43	SEG42	1551.0	706.2
44	SEG41	1551.0	823.9
45	SEG40	1551.0	941.6
46	SEG39	1551.0	1059.3
47	SEG38	1551.0	1177.0
48	SEG37	1551.0	1294.7

PAD No.	Terminal	X= µm	Y= µm
49	SEG36	1412.4	1451.0
50	SEG35	1294.7	1451.0
51	SEG34	1177.0	1451.0
52	SEG33	1059.3	1451.0
53	SEG32	941.6	1451.0
54	SEG31	823.9	1451.0
55	SEG30	706.2	1451.0
56	SEG29	588.5	1451.0
57	SEG28	470.8	1451.0
58	SEG27	353.1	1451.0
59	SEG26	235.4	1451.0
60	SEG25	117.7	1451.0
61	SEG24	0	1451.0
62	SEG23	-117.7	1451.0
63	SEG22	-235.4	1451.0
64	SEG21	-353.1	1451.0
65	SEG20	-470.8	1451.0
66	SEG19	-588.5	1451.0
67	SEG18	-706.2	1451.0
68	SEG17	-823.9	1451.0
69	SEG16	-941.6	1451.0
70	SEG15	-1059.3	1451.0
71	SEG14	-1177.0	1451.0
72	SEG13	-1294.7	1451.0
73	SEG12	-1412.4	1451.0
74	SEG11	-1551.0	1294.7
75	SEG10	-1551.0	1177.0
76	SEG9	-1551.0	1059.3
77	SEG8	-1551.0	941.6
78	SEG7	-1551.0	823.9
79	SEG6	-1551.0	706.2
80	SEG5	-1551.0	588.5
81	SEG4	-1551.0	470.8
82	SEG3	-1551.0	353.1
83	SEG2	-1551.0	235.4
84	SEG1	-1551.0	117.7
85	COMMK1	-1551.0	0
86	COM1	-1551.0	-117.7
87	COM2	-1551.0	-235.4
88	COM3	-1551.0	-353.1
89	COM4	-1551.0	-470.8
90	COM5	-1551.0	-588.5
91	COM6	-1551.0	-706.2
92	COM7	-1551.0	-823.9
93	COMMK2	-1551.0	-941.6
94	P1	-1551.0	-1059.3
95	P2	-1551.0	-1177.0
96	P3	-1551.0	-1294.7

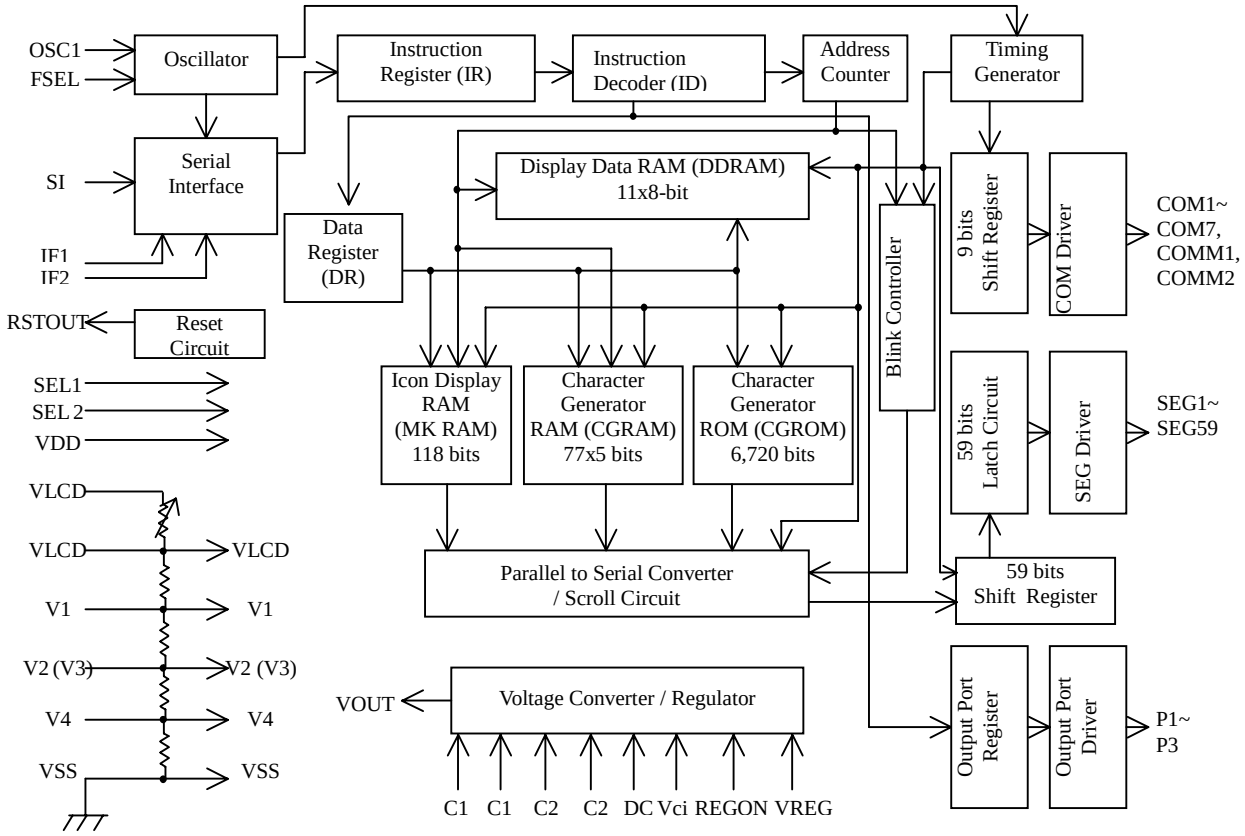
4) D Mode (SEL1="0", SEL2="1")

Chip Size 3.45mm x 3.25mm (Chip Center X=µ0m, Y=0µm)

PAD No.	Terminal	X= µm	Y= µm
1	RSTOUT	-1412.4	-1452.0
2	DC	-1294.7	-1452.0
3	SEL1	-1177.0	-1452.0
4	SEL2	-1059.3	-1452.0
5	IF1	-941.6	-1452.0
6	IF2	-823.9	-1452.0
7	FSEL	-706.2	-1452.0
8	SI	-588.5	-1452.0
9	REGON	-470.8	-1452.0
10	OSC1	-353.1	-1452.0
11	VDD	-235.4	-1452.0
12	VSS	-117.7	-1452.0
13	VSS	0	-1452.0
14	Vci	117.7	-1452.0
15	VREG	235.4	-1452.0
16	C1+	353.1	-1452.0
17	C1-	470.8	-1452.0
18	C2+	588.5	-1452.0
19	C2-	706.2	-1452.0
20	VOUT	823.9	-1452.0
21	VLCD1	941.6	-1452.0
22	VLCD2	1059.3	-1452.0
23	V1	1177.0	-1452.0
24	V2	1294.7	-1452.0
25	V4	1412.4	-1452.0
26	SEG1	1551.0	-1294.7
27	SEG2	1551.0	-1177.0
28	SEG3	1551.0	-1059.3
29	SEG4	1551.0	-941.6
30	SEG5	1551.0	-823.9
31	SEG6	1551.0	-706.2
32	SEG7	1551.0	-588.5
33	SEG8	1551.0	-470.8
34	SEG9	1551.0	-353.1
35	SEG10	1551.0	-235.4
36	SEG11	1551.0	-117.7
37	SEG12	1551.0	0
38	SEG13	1551.0	117.7
39	SEG14	1551.0	235.4
40	SEG15	1551.0	353.1
41	SEG16	1551.0	470.8
42	SEG17	1551.0	588.5
43	SEG18	1551.0	706.2
44	SEG19	1551.0	823.9
45	SEG20	1551.0	941.6
46	SEG21	1551.0	1059.3
47	SEG22	1551.0	1177.0
48	SEG23	1551.0	1294.7

PAD No.	Terminal	X= µm	Y= µm
49	SEG24	1412.4	1451.0
50	SEG25	1294.7	1451.0
51	SEG26	1177.0	1451.0
52	SEG27	1059.3	1451.0
53	SEG28	941.6	1451.0
54	SEG29	823.9	1451.0
55	SEG30	706.2	1451.0
56	SEG31	588.5	1451.0
57	SEG32	470.8	1451.0
58	SEG33	353.1	1451.0
59	SEG34	235.4	1451.0
60	SEG35	117.7	1451.0
61	SEG36	0	1451.0
62	SEG37	-117.7	1451.0
63	SEG38	-235.4	1451.0
64	SEG39	-353.1	1451.0
65	SEG40	-470.8	1451.0
66	SEG41	-588.5	1451.0
67	SEG42	-706.2	1451.0
68	SEG43	-823.9	1451.0
69	SEG44	-941.6	1451.0
70	SEG45	-1059.3	1451.0
71	SEG46	-1177.0	1451.0
72	SEG47	-1294.7	1451.0
73	SEG48	-1412.4	1451.0
74	SEG49	-1551.0	1294.7
75	SEG50	-1551.0	1177.0
76	SEG51	-1551.0	1059.3
77	SEG52	-1551.0	941.6
78	SEG53	-1551.0	823.9
79	SEG54	-1551.0	706.2
80	SEG55	-1551.0	588.5
81	SEG56	-1551.0	470.8
82	SEG57	-1551.0	353.1
83	SEG58	-1551.0	235.4
84	SEG59	-1551.0	117.7
85	COMMK2	-1551.0	0
86	COM7	-1551.0	-117.7
87	COM6	-1551.0	-235.4
88	COM5	-1551.0	-353.1
89	COM4	-1551.0	-470.8
90	COM3	-1551.0	-588.5
91	COM2	-1551.0	-706.2
92	COM1	-1551.0	-823.9
93	COMMK1	-1551.0	-941.6
94	P1	-1551.0	-1059.3
95	P2	-1551.0	-1177.0
96	P3	-1551.0	-1294.7

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	SYMBOL	I/O	FUNCTION
11	V_{DD}	-	Power Supply Terminal V_{DD}=1.7~5.5V
12,13	V_{SS}	-	Ground Terminals V_{SS}=0V
21, 22, 23,24, 25	VLCD1, VLCD2, V1, V2, V4	-	LCD Driving Voltage Supply Terminals
16,17, 18,19	C1+, C1- C2+, C2-	-	Capacitor Connecting Terminals for Voltage Boost.
14	V_{Ci}	-	Voltage Boost Input Terminal.
20	V_{OUT}	Output	Voltage Boost Output Terminal.
2	DC	Input	Voltage Boost Selection Terminal. "L": 2-time "H": 3-time
10	OSC1	Input	Resistor and Capacitor Connecting Terminal for Oscillation Circuit. (or External Clock Input Terminal.)
26~84	SEG1~ SEG59	Output	Segment Driver Output Terminals.
86~92	COM1~ COM7	Output	Common Driver Output Terminals.
85,93	COMMK1, COMMK2	Output	Common Driver Output Terminals for Icons
94~96	P1~P3	Output	General Purpose Ports
8	SI	Input	Serial Data Input Terminal
5,6	IF1, IF2	Input	Cycle Time Select Terminals
9	REGON	Input	Regulator On/Off Terminal "L": Off "H": On
15	VREG	Output	Regulator Output Terminal
7	FSEL	Input	Internal Oscillator/External Clock Select Terminal "L": Internal Oscillator "H": External Clock
1	RSTOUT	Output	Reset Signal Output Terminal
3	SEL1	Input	Select COM Drivers Scan Direction "L": COM1→COM7, COMMK1, COMMK2 "H": COMMK2, COMMK1, COM7→COM1
4	SEL2	Input	Set SEG Drivers Output Sequence "L": SEG1→SEG59 "H": SEG59→SEG1

- DC, IF1, IF2, REGON, FSEL, SEL1, SEL2 terminals should be fixed ahead

■ FUNCTION DESCRIPTION

(1) Block Description

(1-1) Register

NJU6515 has one 8-bit Instruction Register (IR) and one 8-bit Data Register (DR), IR is used to hold instructions like Display Clear, etc. DR is used to save the CPU-sending data temporally which will be eventually written to DDRAM, CGRAM, MKRAM.

Table 1 Register Select

D11	D10	D9	D8	Operation
0	0	0	0	Instruction to IR, and then executed
1	1	0	0	Set up RAM address
0	0	1	1	Display data to DR, and then to RAM

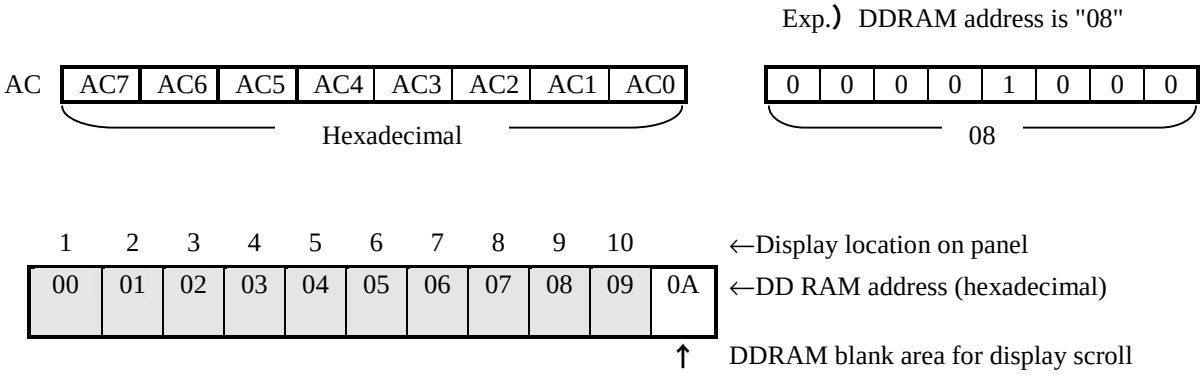
(1-2) Address Count (AC)

AC is used to count RAM address. After the RAM data writing, the AC will increase +1 or –1 automatically.

(1-3) DDRAM (Display Data RAM)

The size of DDRAM is 8x11 bits. One 8-bit data represents a code of a character. So total 11 character codes can be saved on DDRAM (a 8-bit blank area is reserved for display scroll)

The relationship between DDRAM address and display location on panel is as below, and the DDRAM address is in hex.



For shift display, the DDRAM address moves like below.

[Left shift]

(00) ← 01 02 03 04 05 06 07 08 09 0A 00

[Right shift]

0A 00 01 02 03 04 05 06 07 08 09 → (0A)

(1-4) Character Generator ROM (CGROM)

CGROM has 192 patterns of 5x7-dot characters. Every pattern can be located by an 8-bit DDRAM data. The relationship between an 8-bit code and a pattern is shown on the following Table 2.

Furthermore, if other than the following patters are requested, please contact NJRC for customized ROM. Even with customized pattern, $(20)_H$ need to be space, and $(0*)_H$, $(1*)_H$, $(8*)_H$, $(9*)_H$ shall be invalid.

Table 2 Code and pattern (ROM version 06)

LOWER 4bit(HEX) \ UPPER 4bit(HEX)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
3																
4																
5																
6																
7																
8																
9																
A																
B																
C																
D																
E																
F																

(1-5) Character Generator RAM (CGRAM)

CGRAM is used for creating patterns not included on CGROM, and totally 11 5X7-dot patterns can be written on CGRAM.

DDRAM data $(00)_H$ – $(0A)_H$ is reserved as codes of CGRAM patterns.

The relationship among DDRAM data, CGRAM address and patter data is shown on Table 3

Table 3 CGRAM Address and DDRAM data and patterns CGRAM data

DDRAM Data	CGRAM Address			CGRAM Data	
7 6 5 4 3 2 1 0	7 6 5 4 3	2 1 0		4 3 2 1 0	
0 0 0 0 0 0 0 0	1 0 0 0 0	0 0 0		1 1 1 1 0	
		0 0 1		1 0 0 0 1	
		0 1 0		1 0 0 0 1	
		0 1 1		1 1 1 1 0	Pattern (1)
		1 0 0		1 0 1 0 0	
		1 0 1		1 0 0 1 0	
		1 1 0		1 0 0 0 1	
		1 1 1		* * * * *	
0 0 0 0 0 0 0 1	1 0 0 0 1	0 0 0		1 0 0 0 1	
		0 0 1		0 1 0 1 0	
		0 1 0		1 1 1 1 1	
		0 1 1		0 0 1 0 0	Pattern (2)
		1 0 0		1 1 1 1 1	
		1 0 1		0 0 1 0 0	
		1 1 0		0 0 1 0 0	
		1 1 1		* * * * *	
		0 0 0			
		0 0 1			
•	•	•		•	
•	•	•		•	
•	•	•		•	
•	•	•		•	
•	•	•		•	
0 0 0 0 1 0 1 0	1 1 0 1 0				
		1 0 0			
		1 0 1			Pattern (11)
		1 1 0			
		1 1 1			

* Invalid

Note

1. 0~3 bits of DDRAM data is corresponding with 3~6 bits of CGRAM address.
2. 0~2 bits of CGRAM is the line address for every CGRAM pattern, and the 8th line is invalid. If CGRAM data is input continually, the 8th address of every pattern will be automatically over-passed.
3. CGRAM data has 5 bits, and bit 4 data is the left side of the pattern.
4. DDRAM data is used to specify either the CGROM patterns or CGRAM patters, for CGRAM pattern display, the upper 4 bits (4~7) of DDRAM data shall be “0”.
5. If CG RAM data ="1", corresponding pixel ON, if data =0", pixel off.
6. After power on, because CGRAM data is indefinitive, please write data into CGRAM before display on.

(1-6) Mark RAM (MKRAM)

The MKRAM can store as much as 118 data for icon display.

Only when DB1 and DB2 bits of "Display on/off" instruction are set to 1, icon display is effective. When MKRAM data=1, mark display on, data=0, mark display off.

The relationship between the address of MKRAM and marks is shown on Table 4

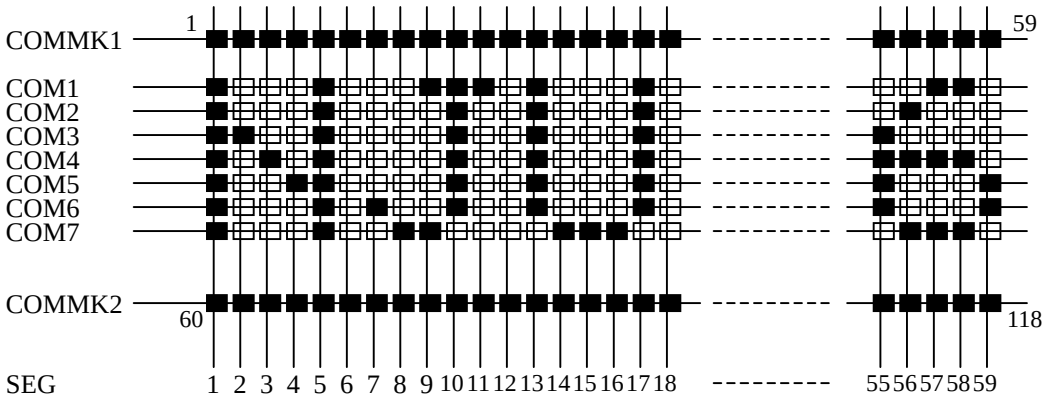


Table 4 MKRAM Address and Mark Number

MKRAM Address (COMMK1:$E0_H$〜$E9_H$) (COMMK2:EA_H〜$F3_H$)		Mark Number							
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1110 0000	$E0_H$	*	*	1	2	3	4	5	6
1110 0001	$E1_H$	*	*	7	8	9	10	11	12
1110 0010	$E2_H$	*	*	13	14	15	16	17	18
1110 0011	$E3_H$	*	*	19	20	21	22	23	24
1110 0100	$E4_H$	*	*	25	26	27	28	29	30
1110 0101	$E5_H$	*	*	31	32	33	34	35	36
1110 0110	$E6_H$	*	*	37	38	39	40	41	42
1110 0111	$E7_H$	*	*	43	44	45	46	47	48
1110 1000	$E8_H$	*	*	49	50	51	52	53	54
1110 1001	$E9_H$	*	*	55	56	57	58	59	*
1110 1010	EA_H	*	*	60	61	62	63	64	65
1110 1011	EB_H	*	*	66	67	68	69	70	71
1110 1100	EC_H	*	*	72	73	74	75	76	77
1110 1101	ED_H	*	*	78	79	80	81	82	83
1110 1110	EE_H	*	*	84	85	86	87	88	89
1110 1111	EF_H	*	*	90	91	92	93	94	95
1111 0000	$F0_H$	*	*	96	97	98	99	100	101
1111 0001	$F1_H$	*	*	102	103	104	105	106	107
1111 0010	$F2_H$	*	*	108	109	110	111	112	113
1111 0011	$F3_H$	*	*	114	115	116	117	118	*

* (Don't Care)

Note) The MKRAM is not initialized with power on. If mark display is used, write data to MKRAM first. Mark display is not affected by "Pattern Shift" instruction. When duty=1/8, the range of MKRAM address should be set between $E0_H$~$E9_H$.

(1-7) Clock Generator

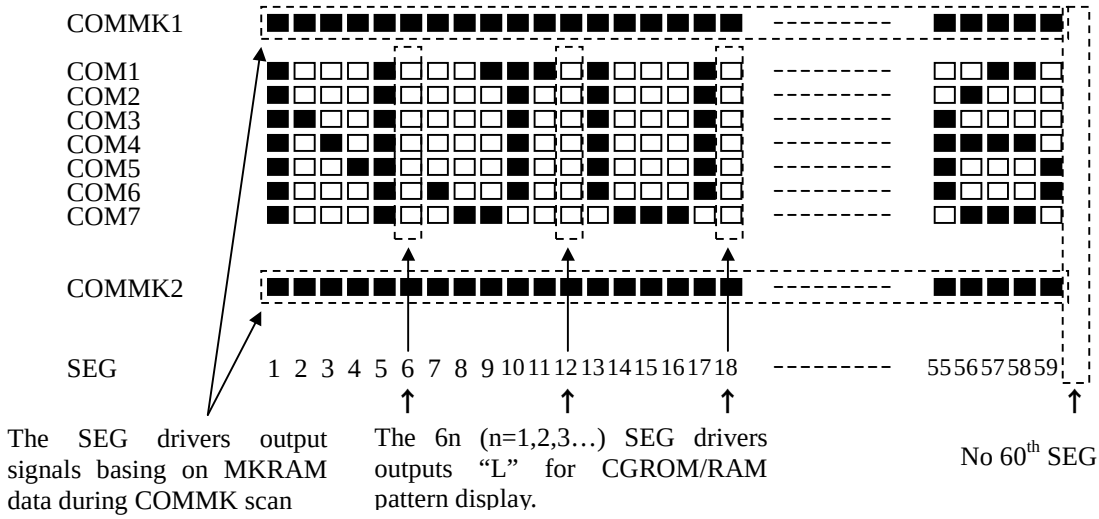
The Clock Generator outputs timing signal for DDRAM, MKRAM, CGRAM and CGROM control. The RAM data readout timing is independent from CPU access. For this reason, even during DDRAM data writing, except pixels which the corresponding data being rewritten, no blink can be observed.

(1-8) LCD Driving Circuit

The circuit consists of 9 COM drivers and 59 SEG drivers. The 59 bits display data will be latched after read in the shift register, the latched data will control the SEG drivers to output LCD driving bias voltage.

Note) LCD Display

The 6n (n=1,2,3…) SEG drivers will output "L" during CGROM/CGRAM patters display. When the "Smooth Scroll" function is used, the blank lines will shift together with the patterns, but for mark display, the 6n SEG drivers will always output signals according to MKRAM data.



(1-9) Blink Control Circuit

The circuit is used to control the display blink. When the "Blink Control" is on, the character, which address is specified by AC, will blink. For example, if the AC = $(04)_H$, the 5th character will blink.

	AC_7	AC_6	AC_5	AC_4	AC_3	AC_2	AC_1	AC_0
AC	0	0	0	0	0	1	0	0

1桁	2	3	4	5	6	7	8	9	10	←Display location
00	01	02	03	04	05	06	07	08	09	←DDRAM Address (16 Hex)

Blink character

Note) If the address of CGRAM or MKRAM is set in AC, even when the blink function is on, because no display location is corresponding with a CGRAM/MKRAM address, there is no blink character on the panel. So please set the blink function off in this case.

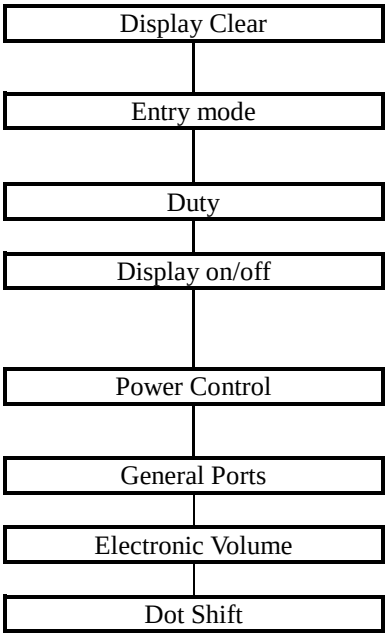
(1-10) Oscillator

The oscillation circuit use external capacitor and resistor to generate clock. If the oscillator is used, fix FSEL to "L", when external clock is used, fix FSEL to "H" and input clock from OSC1 pin.

(2) Reset Circuit

Initialization by Reset

The IC is initialized when power on. The following instruction will be executed during initialization. Please refer to (5) [Interface with CPU] for reset timing.



20H is written into DDRAM, AC is set to 00H.

I/D =1 +1(Increment)
S =0 No shift

DT =1 1/8duty

D =0 Display off
M =0 Mark off
B =0 Blink off

V =0 Voltage boost off
RE2, 1, 0 =0, 0, 0

P3, 2, 1 =0, 0, 0 General Ports off

EV3, 2, 1, 0 =0, 0, 0, 0

DS2, 1, 0 =0, 0, 0 dot shift = 0

Note) If the power supply could not meet the conditions stated in [The Power Supply Startup], the reset circuit may be malfunction.

(3) Instruction

The IC has the Instruction Register (IR) and the Data Register (DR). The data from CPU will be stored in these registers first, and then executed internally.

The MSB of data will be written in first. The RAM address shall be setup before RAM data writing.

Table 5 Instruction List

	Instruction	Start Condition				Instruction Code												Description
		DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	
a	Maker Test	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	Only for maker using
b	Display Clear	1	0	1	0	0	0	0	0	0	0	0	1	*	*	*	*	The DDRAM address 00H is set into AC by this instruction.
C	Return Home	1	0	1	0	0	0	0	0	0	0	1	0	*	*	*	*	The DDRAM address 00H is set into AC, the shifted characters return to its initial place. No change of DDRAM data.
D	Entry Mode	1	0	1	0	0	0	0	0	0	0	1	1	*	*	I/D	S	Set address increment and shift direction.
e	Duty Ratio	1	0	1	0	0	0	0	0	0	1	0	0	*	*	*	DT	Set duty ratio to 1/8 or 1/9.
f	Display On/Off	1	0	1	0	0	0	0	0	0	1	0	1	*	D	M	B	Display on/off (D), Mark on/off (M), Blink function on/off.
G	Address Shift	1	0	1	0	0	0	0	0	0	1	1	0	*	*	*	ARL	Address increment or decrement even without data writing.
h	Pattern Shift	1	0	1	0	0	0	0	0	0	1	1	1	*	*	*	DRL	Displayed character shift to the right or left
i	Dot Shift	1	0	1	0	0	0	0	0	1	0	0	0	*	DS2	DS1	DS0	0~5 bits dot shift. Combined with Pattern Shift, smooth scroll can be realized.
j	Power Control	1	0	1	0	0	0	0	0	1	0	0	1	V	RE2	RE1	RE0	Voltage boost on/off, and set regulator.
k	General Ports	1	0	1	0	0	0	0	0	1	0	1	0	*	P3	P2	P1	Set general ports (P3~P1)
l	Electronic Volume	1	0	1	0	0	0	0	0	1	0	1	1	EV3	EV2	EV1	EV0	
m	RAM Address	1	0	1	0	1	1	0	0	Address								Set the address of DDRAM, CGRAM, MKRAM
n	RAM Data Writing	1	0	1	0	0	0	1	1	Write data (DDRAM)								
										*	*	*	Write data (CGRAM)					
										*	*	Write data (MKRAM)						

I/D=1: increment I/D=0: decrement S=1: Pattern Shift
DT=1:1/8duty DT=0:1/9duty、
D=1: Display on D=0: Display off M=1: Mark on M=0: Mark off
B=1: blink on B=0:Blink off
ARL=1: address+1 ARL=0: address -1
DRL=1: right shift DRL=0: left shift
DSx: dot shift
V=1: boost on V=0: boost off REx: setting regulator
Px: General ports setting
EVx: Contrast ratio setting

*: Don't care

*1) The execution time of Power Control instruction means the time between the start of instruction processing and the power circuit reacting. Practically, power system need more time to stabilize.

*2) Do not input data other than the above shown.

(3-1) Description of Instruction

(a) Maker Test

	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Do not use this instruction.

(b) Display Clear

	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	1	0	0	0	0	0	0	0	0	1	*	*	*	*

The space font (20)H is written to all the bits of DDRAM, and the AC is set to (00)H, the ID bit of “Entry Mode” is sent to 1 (Increment), “Pattern Shift” and “Dot Shift” functions are off. The data of MK/CGRAM is unchanged.

Note) For the customized ROM, the pattern of (20)H shall be space code too.

(c) Return Home

	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	1	0	0	0	0	0	0	0	1	0	*	*	*	*

By this instruction, the AC is set to (00)H, I/D of “Entry Mode” is set to “1”, “Pattern Shift” and “Dot Shift” are initialized. DDRAM data is not changed, if Blink function used, the first Character on panel will blink.

(d) Entry Mode

	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	1	0	0	0	0	0	0	0	1	1	*	*	I/D	S

The address increment direction and Pattern Shift direction are set by this instruction.
If data is continually written to the CGRAM, invalid address will be automatically over passed.

I/D	Function
1	The address of the DDRAM, CGRAM and MKRAM increase 1.
0	The address of the DDRAM, CGRAM and MK RAM decrease 1.

S	Function
1	If I/D=1, displayed patterns move to the left, If I/D=0, display patterns move to the right. During data writing, “Pattern Shift” is invalid.
0	No Pattern Shift

(e) Duty Ratio

	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	1	0	0	0	0	0	0	1	0	0	*	*	*	DT

If duty ratio=1/9, both COMMK1 and COMMK2 drivers can be used, if duty ratio=1/8, only one COMMK driver can be used.

DT	Function
1	1/8, Max. 59 marks
0	1/9, Max.118 marks

When change duty ratio from 1/9 to 1/8, the MKRAM address need to be revised and rewrite the data for MKRAM.

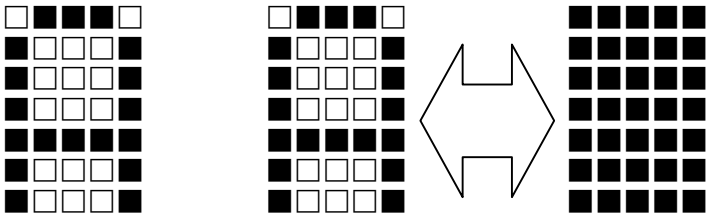
(f) Display ON/OFF

	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	1	0	0	0	0	0	0	1	0	1	*	D	M	B

D	Function
1	Display on
0	Display off, DDRAM data is remained, when set D=1 again, remained data will be shown as before. During display off, all COM or SEG drivers output "L".

M	Function
1	Mark display on (if D=0, mark display off)
0	Mark display off

B	Function
1	The pattern which address is stored at AC will blink. The blink function is realized by alternately display a font and all 5x7 dot in black at a frequency of 2.5Hz (400.16ms, f_{OSC}=380kHz, 1/9 duty ratio), or, 2.8Hz(355.71ms, f_{OSC}=380kHz, 1/8 duty ratio).
0	No blink



5X7 dot
(1) Normal display

Alternate display
(2) Blink display

(g) Address Shift

	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	1	0	0	0	0	0	0	1	1	0	*	*	*	ARL

The address of DDRAM/CGRAM/MKRAM shifts to the right or left even without data writing.

ARL	Function
1	AC+1
0	AC-1

If the CGRAM/MKRAM address is selected, the execution of "Address shift" will lead to the DDRAM. If want to write data to DDRAM after "Address Shift", it is necessary to set up DDRAM address.

(h) Pattern Shift

	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	1	0	0	0	0	0	0	1	1	1	*	*	*	DRL

Without data rewriting, the displayed pattern can move to the left or right by this instruction, but AC address will not change.

DRL	Function
1	Displayed patterns move to the right
0	Displayed patterns move to the left

(i) Dot Shift

	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	1	0	0	0	0	0	1	0	0	0	*	DS2	DS1	DS0

Using this instruction with “Pattern Shift”, smooth scroll can be realized.

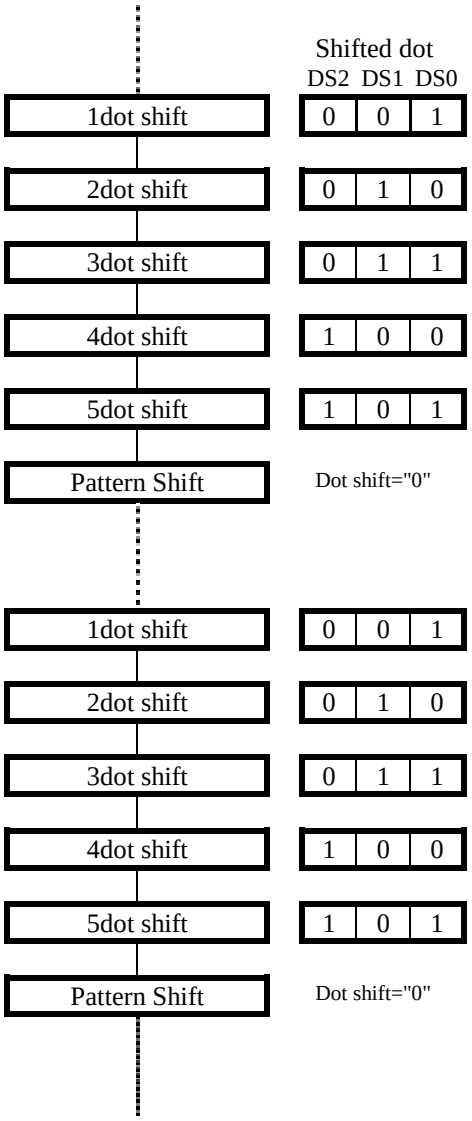
DS2	DS1	DS0	Function
0	0	0	0 dot shift (no shift)
0	0	1	1 dot shift to the left
0	1	0	2 dots shift to the left
0	1	1	3 dots shift to the left
1	0	0	4 dots shift to the left
1	0	1	5 dots shift to the left
1	1	0	Invalid
1	1	1	

Note1) If using smooth scroll mode, set I/D=1, S=0 of “Entry Mode”.
Note2) “Dot Shift” is reset to “0 dot shift” when “Pattern Shift” is executed.
Note3) Displayed marks do not shift.

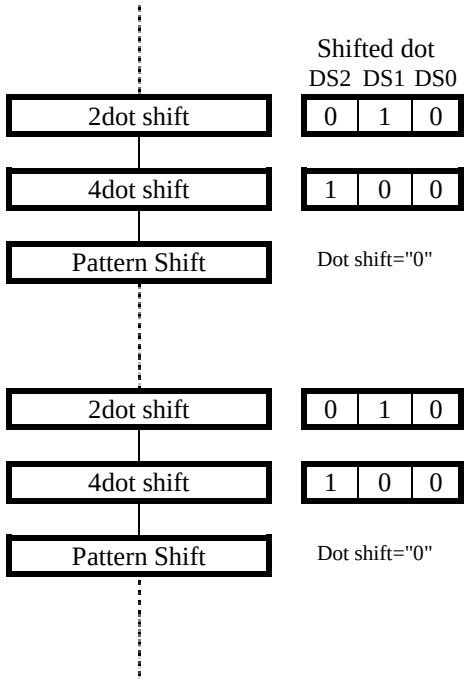
• Smooth Scroll

By setting DS2~DS0 of "Dot Shift", one of the 3 scroll patters can be selected. (1dot smooth scroll, 2-dot smooth scroll, 3-dot smooth scroll)

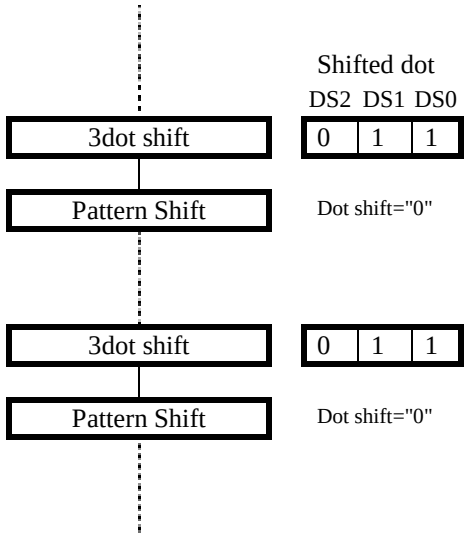
1-dot smooth scroll



2-dot smooth scroll

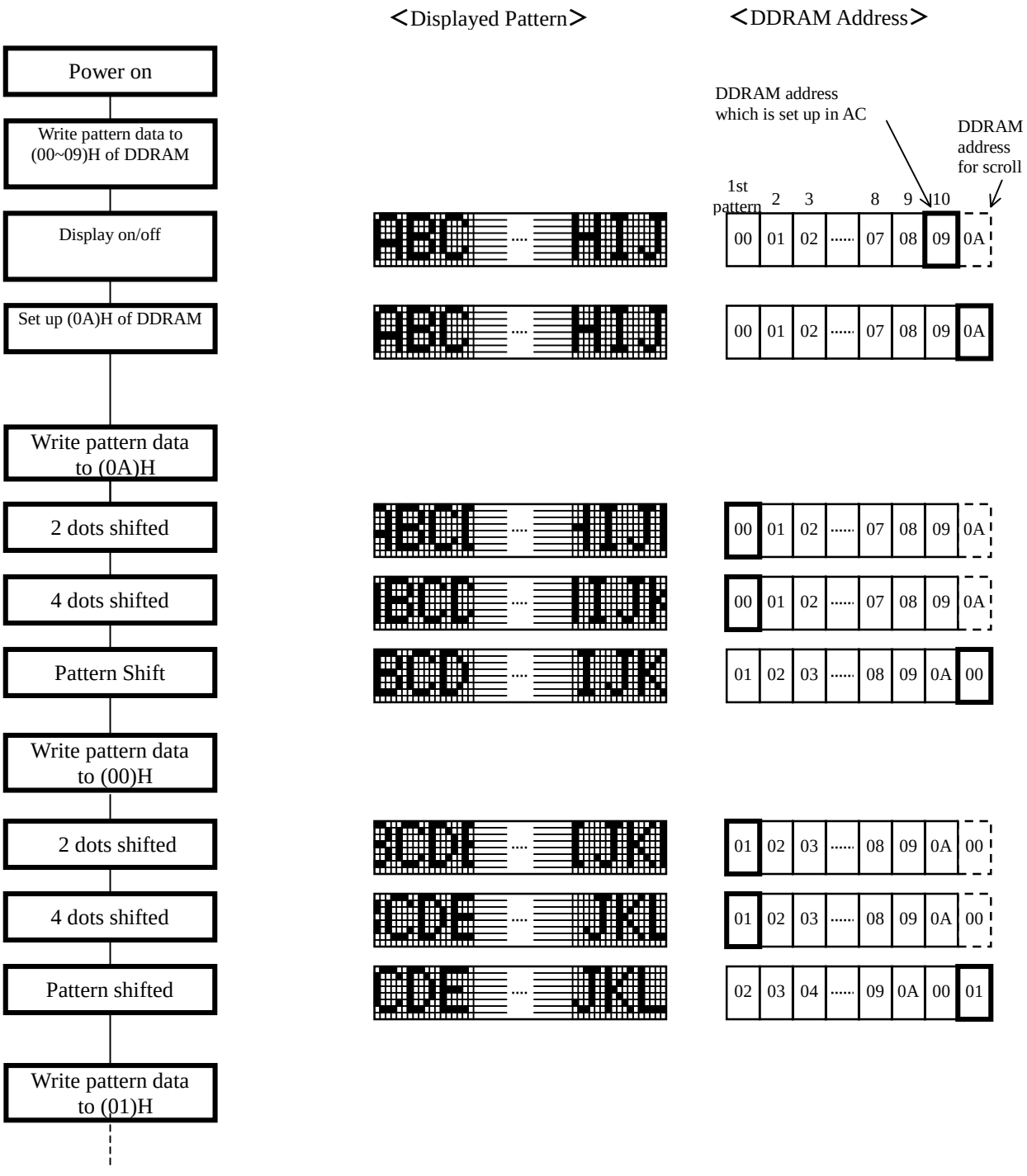


3-dot smooth scroll



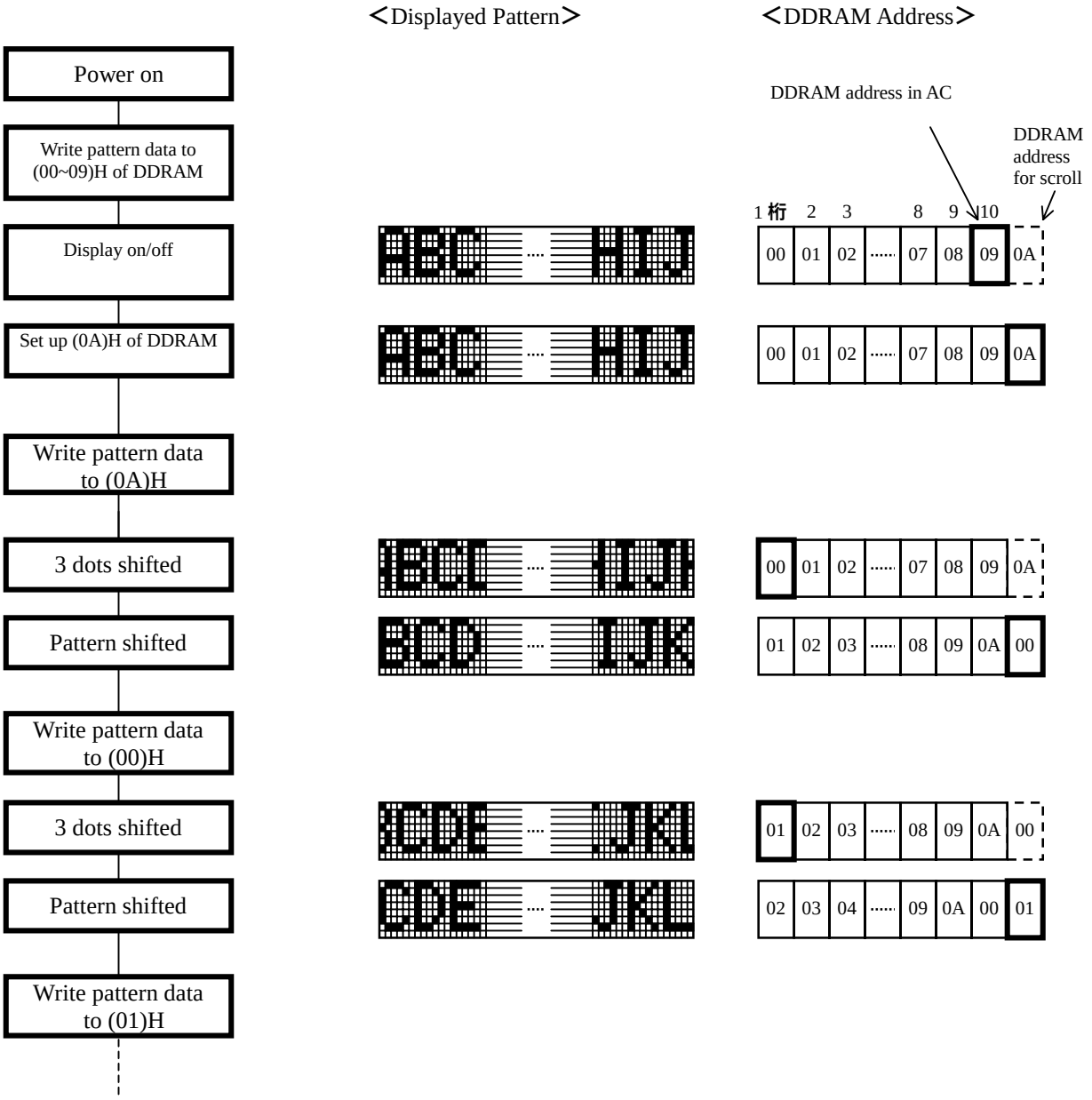
- 2-dot Smooth Scroll

  The displayed pattern and DDRAM address will change like below under 2-dot smooth scroll.



- 3-dot Smooth Scroll

  The displayed pattern and DDRAM address will change like below under 3-dot smooth scroll.



(j) Power Control

	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	1	0	0	0	0	0	1	0	0	1	V	RE2	RE1	RE0

The voltage boost and the regulator are controlled by this instruction. The regulator output can be selected from 8 steps.

V	Function
1	Voltage boost on
0	Voltage boost off

RE2	RE1	RE0	Output of the Regulator (VREG pin)
0	0	0	1.9V (Default)
0	0	1	2.0V
0	1	0	2.1V
0	1	1	2.2V
1	0	0	2.3V
1	0	1	2.4V
1	1	0	2.5V
1	1	1	2.6V

(k) General Ports

	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	1	0	0	0	0	0	1	0	1	0	*	P3	P2	P1

Outputs from the general ports (P3, P2, P1) are controlled by the instruction, the general ports can be used to control LED. The outputs are initialized to “L”.

Px	General Ports
1	"H"
0	"L"

(l) Electronic Volume

	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	1	0	0	0	0	0	1	0	1	1	EV3	EV2	EV1	EV0

The contrast of LCD can be adjusted by setting the value of EV3-0, The LCD driving voltage VLCD can be selected from 16 steps. If not using this function, set (EV3, EV2, EV1, EV0) = (0,0,0,0).

EV3	EV2	EV1	EV0	VLCD
0	0	0	0	Low
0	0	0	1	:
0	0	1	0	:
:	:	:	:	:
:	:	:	:	:
1	1	0	1	:
1	1	1	0	:
1	1	1	1	High

VLCD=VLCD2-VSS

(m) RAM Address

	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	1	0	1	1	0	0	A	A	A	A	A	A	A	A

If DB11~DB8 =(1,1,0,0) to, and DB7~DB0 will be the RAM address, and this address is also informed to AC (Address Count).

DD RAM: (00)H ~ (0A)H
CG RAM: (80)H ~ (D6)H
MK RAM: (E0)H ~ (F3)H

			UPPER 4bit															
			0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
			0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
LOWER 4bit	0	0000		*	*	*	*	*	*	*								
	1	0001		*	*	*	*	*	*	*								COMMK2
	2	0010		*	*	*	*	*	*	*	① (00)H	③ (02)H	⑤ (04)H	⑦ (06)H	⑨ (08)H	⑪ (0A)H		
	3	0011		*	*	*	*	*	*	*								▲
	4	0100		*	*	*	*	*	*	*							COMMK1	*
	5	0101		*	*	*	*	*	*	*								*
	6	0110		*	*	*	*	*	*	*								*
	7	0111		*	*	*	*	*	*	*	*	*	*	*	*	*		*
	8	1000		*	*	*	*	*	*	*						*		*
	9	1001		*	*	*	*	*	*	*						*	▲	*
	A	1010		*	*	*	*	*	*	*						*		*
	B	1011	*	*	*	*	*	*	*	*	② (01)H	④ (03)H	⑥ (05)H	⑧ (07)H	⑩ (09)H	*		*
	C	1100	*	*	*	*	*	*	*	*						*	COMMK2	*
	D	1101	*	*	*	*	*	*	*	*						*		*
	E	1110	*	*	*	*	*	*	*	*						*		*
	F	1111	*	*	*	*	*	*	*	*	*	*	*	*	*	*		*
			DD RAM Address								CG RAM Address						MK RAM Address	

--- DD RAM: 8-bit data for one address

--- CG RAM: 5-bit data for one address

--- MK RAM: 6-bit data for one address

* Invalid area.
LSB is invalid at (E9)H and (F3)H of MKRAM area (▲).

(n) RAM Data Writing

-DD RAM

	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	1	0	0	0	1	1	D	D	D	D	D	D	D	D

-CG RAM

	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	1	0	0	0	1	1	*	*	*	D	D	D	D	D

-MK RAM

	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	1	0	0	0	1	1	*	*	D	D	D	D	D	D

Write (0,0,1,1) to DB11~DB8, and DB7~DB0 will be stored in DDRAM/CGRAM/MKRAM. And it is 8 bits for DDRAM, 5 bits for CGRAM, 6 bits for MKRAM. After data writing, the address will automatically increase/decrease 1.

The invalid address of CGRAM will be automatically over passed during writing data to CGRAM

• Increment

-DDRAM : (00)H → (01)H --- (0A)H → (00)H
-CGRAM : (80)H → (81)H --- (D6)H → (80)H
-MKRAM(1/8Duty) : (E0)H → (E1)H --- (E9)H → (E0)H
-MKRAM(1/9Duty) : (E0)H → (E1)H --- (F3)H → (E0)H

• Decrement

-DDRAM : (0A)H → (09)H --- (00)H → (0A)H
-CGRAM : (D6)H → (D5)H --- (80)H→ (D6)H
-MKRAM(1/8Duty) : (E9)H → (E8)H --- (E0)H → (E9)H
-MKRAM(1/9Duty) : (F3)H → (F2)H --- (E0)H → (F3)H

(3-2) Display

The DDRAM is used to store 11 patterns' code. Using "Pattern shift" instruction, scroll display can be realized. The "Pattern Shift" instruction only changes the patterns' display location. The data stored on DDRAM is not changed. Using "Return Home" instruction, the initial pattern array can be restored.

Note) If using internal reset circuit, the power supply shall meet the condition of the reset circuit. If power supply can not meet the request, please use instruction to reset.

Table 6 Display Example (Using Internal Reset)

No.	Instruction	Display	Function
1	Power on		Initialized, no display
2	Power Control DB11~DB0 (0000 1001 1XXX)		Voltage boost on
3	Display control (0000 0101 0101)		Display on, blink on, space pattern displayed
4	Entry Mode (0000 0011 0010)		Address increment mode during DDRAM / CGRAM access. No pattern shift
5	Write code of N to DDRAM (0011 0100 1110)	N	AC= (01)H
6	Write code of E to DDRAM (0011 0100 0101)	NE	AC= (02)H
7	Write code of W to DDRAM (0011 0101 0111)	NEW	AC= (03)H
8	Entry mode (0000 0011 0011)	NEW	Pattern shift on
9	Write code of space to DDRAM (0011 0010 0000)	EW	AC= (03)H
10	Write code of J to DDRAM (0011 0100 1010)	W J N	AC= (03)H
11	--- --- ---	----- ----- -----	---- --- ---
12	Write code of N to DDRAM (0011 0100 1110)	PON NEW J	AC= (03)H
13	Address Shift (0000 0110 0000)	PO NEW J	AC=(02)H left shift of address
14	Address Shift (0000 0110 0000)	P N NEW J	AC=(01)H left shift of address
15	Write code of A to DDRAM (0011 0100 0001)	A NEW JA	Revise "O" to "A", AC=(01)H Left shift of address。
16	Return Home (0000 0010 0000)	EW JAPAN	AC=(00)H, the patterns relocated according to input sequence

(3-3) Initialization by Instruction

If internal reset circuit cannot operate correctly, initialization can be realized by instruction.

Power On

↓

DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	1	0	0	1	V	RE2	RE1	RE0	Regulator / Voltage boost setting
0	0	0	0	1	0	1	1	EV3	EV2	EV1	EV0	Electronic Volume
0	0	0	0	0	0	0	1	*	*	*	*	Display clear
0	0	0	0	0	0	1	1	*	*	I/D	S	Entry mode
0	0	0	0	0	1	0	0	*	*	*	DT	Duty ratio
0	0	0	0	0	1	0	1	*	D	M	B	Display, mark, blink on/off
0	0	0	0	1	0	1	0	*	P3	P2	P1	General ports
0	0	0	0	1	0	0	0	*	DS2	DS1	DS0	Dot shift

↓

Initialization over

(4) Power Supply for LCD Driving Circuit

(4-1) Regulator/ Voltage boost

The regulator is built in, and input voltage from Vci is regulated and the output voltage from regulator can be selected by setting RE bits of "Power Control" instruction, this output voltage is supplied to the voltage boost.

By setting REGON pin, the voltage regulator can be turned on or off.

REGON = "H": Regulator on.
(The regulator output voltage is supplied to the voltage boost via VREG pin.)
REGON = "L": Regulator off
(The input voltage via Vci pin is directly supplied to the voltage boost.)

Note) Be sure not let the VOUT over 5.5V.

< x2 boost >

If Vci≦2.7V, let the Regulator off, and supply Vci directly to the voltage boost.

If Vci≧3.3V, use the Regulator to step down the Vci and then supply to the voltage boost.

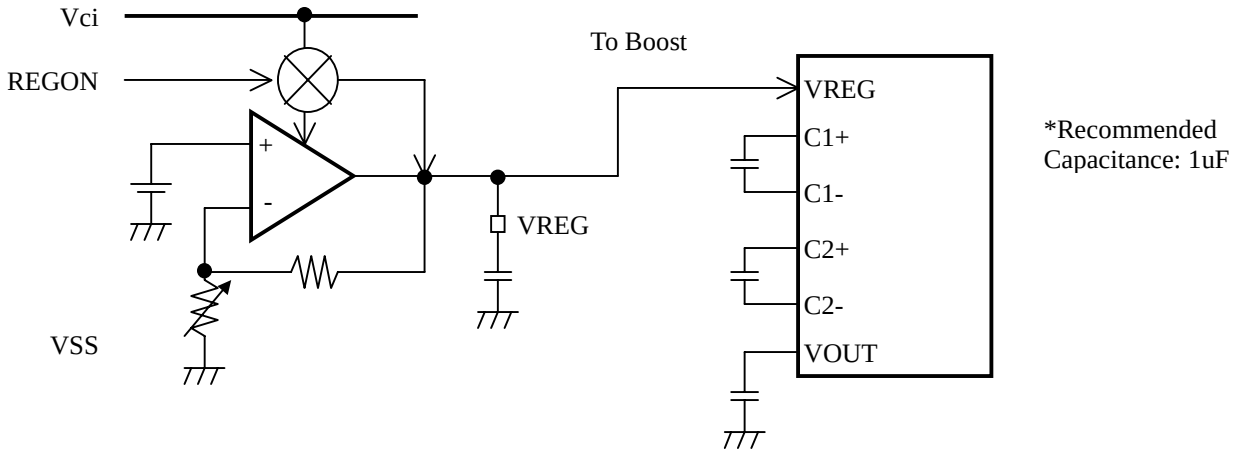
If 2.7V<Vci<3.3V, use the Regulator to step down the Vci and then supply to the voltage boost, but, sometimes because the RE valve, there is limitation of the Regulator output voltage. (The device electronic characteristics will be affected when set a higher output voltage of the Regulator)

RE2, RE1, RE0	Output Voltage from the Regulator (VREG pin)
000	1.9V (default)
001	2.0V
010	2.1V
011	2.2V
100	2.3V
101	2.4V
110	2.5V
111	2.6V

*It is better to connect capacitor with VREG pin to stabilize the output voltage of the Regulator. The capacitance shall be confirmed with the panel.

*The voltage boost will cause ripple voltage and sometimes can affect the display quality. This problem can be avoided by supplying the VLCD1/VLCD2 directly from outside instead of using the Regulator and the voltage boost. But be sure VLCD1≧VLCD2.

*After power on, the LCD driving circuit takes about some ten microseconds to start up. So it needs wait-time for display on.



*Recommended Capacitance: 1uF

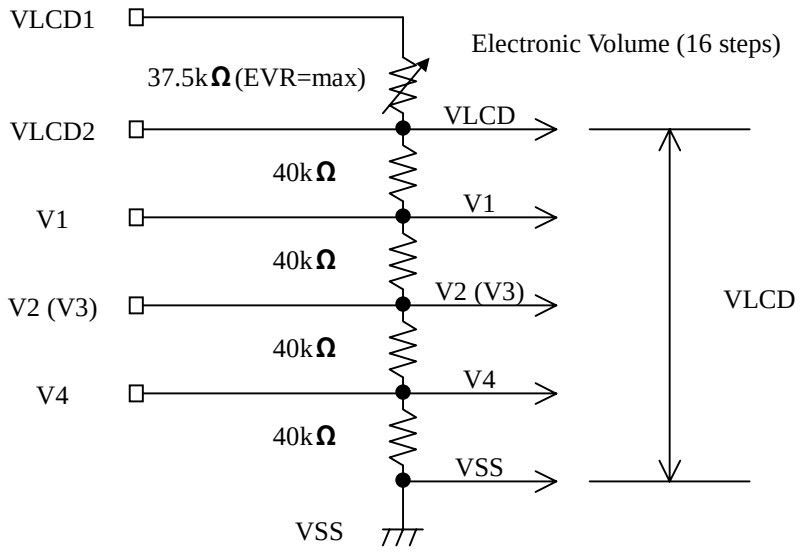
The Regulator and the Voltage Boost

< x3 boost>

The regulator is unavailable.

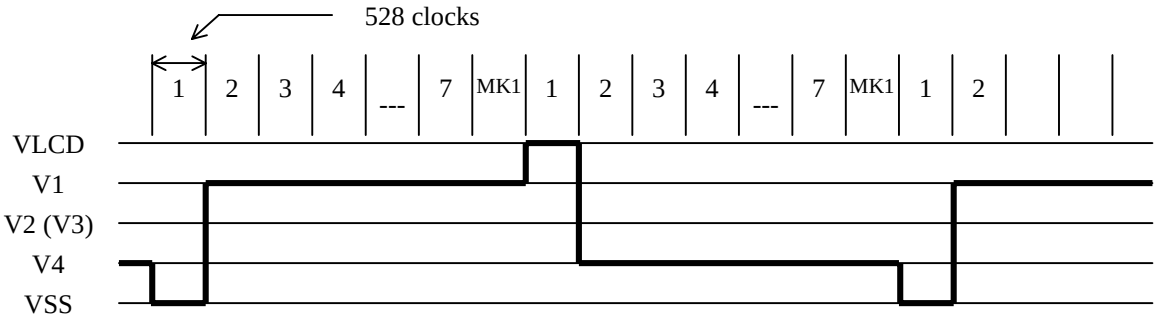
(4-2) Electronic Volume/Internal Bleeder Resistor

The “Electronic Volume” is used to optimize the LCD contrast ratio by adjusting the VLCD. By setting the 4-bit Electronic Volume Register, the VLCD can select from 16 levels.

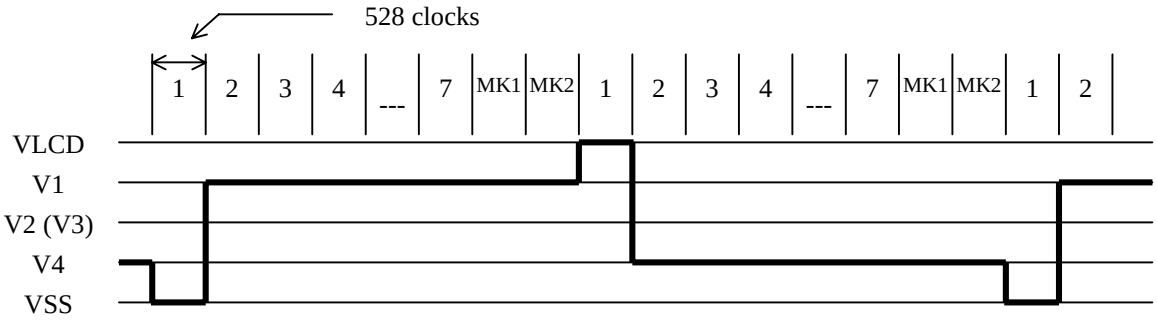


(4-3) Oscillator Frequency and Frame Frequency
When the oscillator frequency is 380KHz, the frame frequency is like below.
(1clock = 1/380000=2.631μs)

<1/8 duty>



<1/9 duty>



<1/9 duty>
1 frame = 2.631(μs) x 528 x 9 = 12.503(ms)
Frame frequency = 1/12.503(ms) = 79.984(Hz)

<1/8 duty>
1 frame = 2.631(μs) x 528 x 8 = 11.113(ms)
Frame frequency = 1/11.113(ms) = 89.982(Hz)

* Power on/off

① Using the regulator/the voltage boost

Power on:
Input Vci after VDD on. Start up the regulator and supply the VREG to the voltage boot until it is stabilized. After the boost stabilized, enable the display on.

Power off:
After display off, stop the operation of the voltage boost, and then let Vci down, finally VDD down.

② Not using the regulator and the voltage boost, input VLCD directly from outside.

Power on:
First VDD on, then input VLCD.

Power off:
First display off, then VLCD down, last VDD down.

(5) Interface with CPU

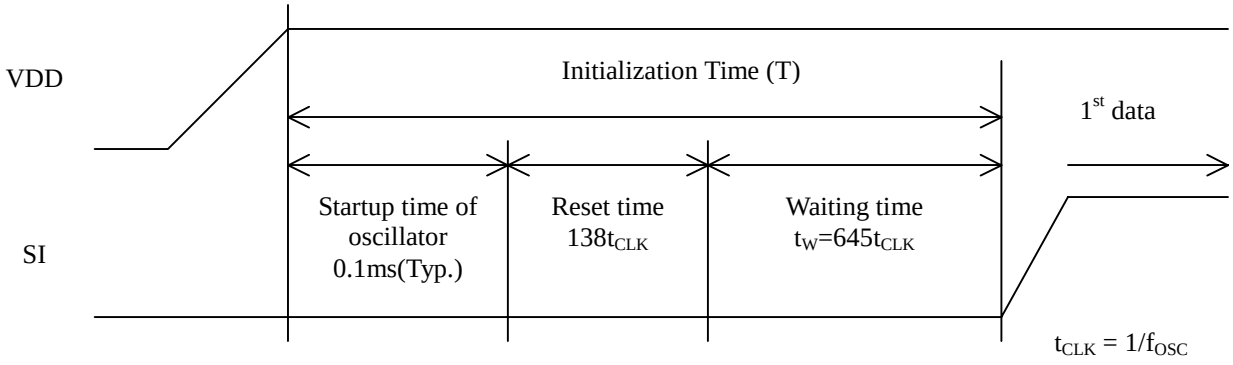
The 16-bit per word serial data is transferred via one line. According to the time length of "H" or "L" level of the signals, the data is interrupted as "1" or "0". After setting a fixed waiting time, if the first 4 MSB is "1010"(a start signal), the rest 12 bit will be read in as the instruction/address/display data. The cycle time of one bit can be selected from 4 levels according to the different combinations of IF1 and IF2 pin (Refer to the "Bus Timing Characteristics").

After the power supply reaching 1.7V, keep SI at "L" level at least T microseconds before the data input.

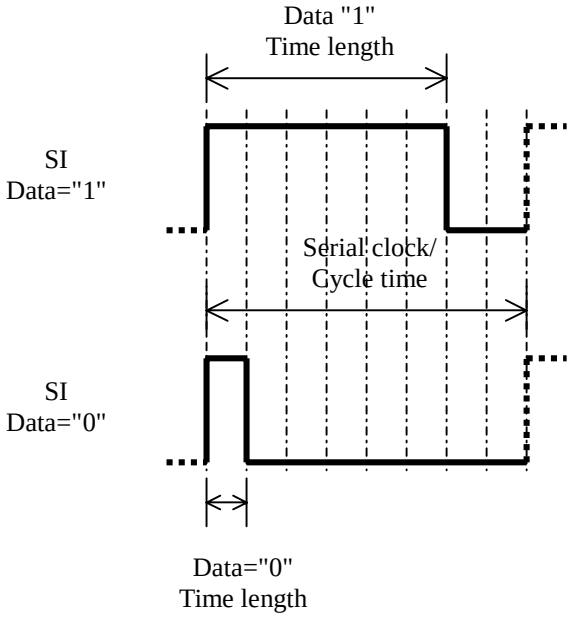
$T=0.1ms(Typ.) + 138t_{CLK} + 645t_{CLK}$

Note) T is valid when the "DC Characteristics" determined resistance and capacitance for oscillator are used. Namely the resistance =51kohm, capacitance=120pF. The t_w is different from t_{W1}, t_{W2} and only used for initialization.

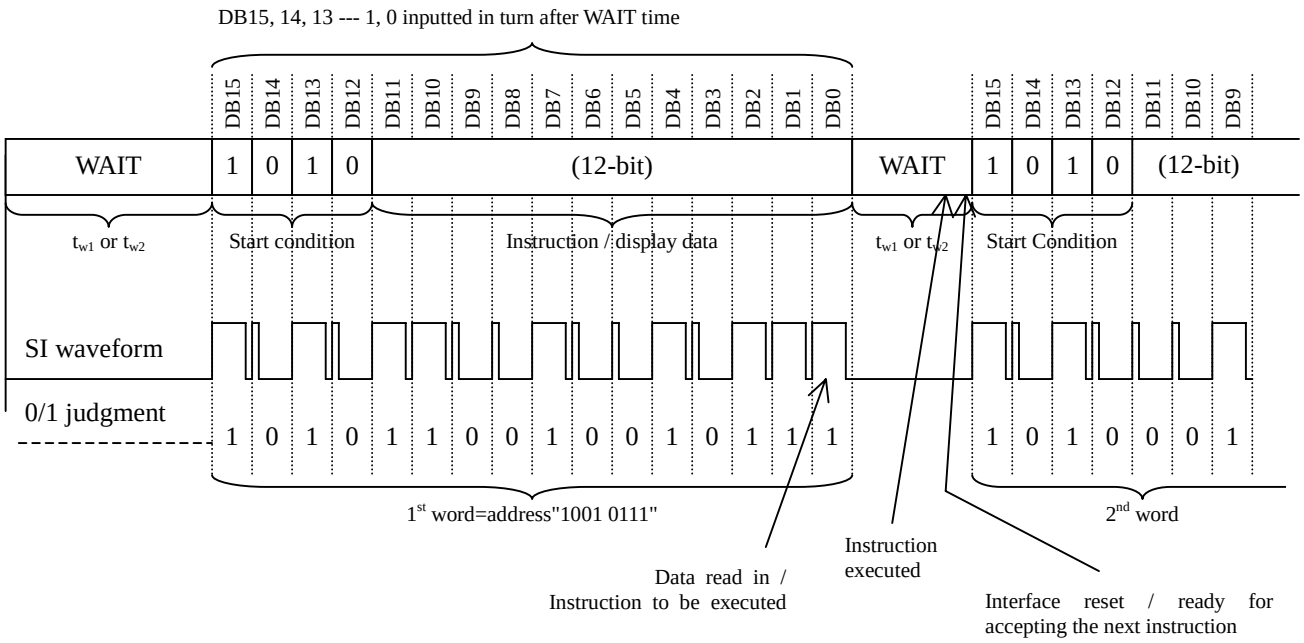
• Data input



• Data interruption ("1" / "0")



• Example of data input



The instruction is executed during the WAIT time, and ready to accept of the next instruction. If more than16 bits data inputted, only the MSB 16 bits are valid. If less than 15 bits data inputted, If less than 15 bits is inputted during WAIT time, the interface is reset and this 15-bit data become invalid. The instruction data is read in during the 16^{th} cycle time and then start to be executed.

■ ABSOLUTE MAXIMUM RATING

(Ta=25°C)

Parameter	Symbol	Condition	Rating	Unit
Power Supply (1)	VDD	VSS (0V)	-0.3 ~ +7.0	V
Power Supply (2)	VLCD1		-0.3 ~ +7.0	V
Power Supply (3)	VLCD2		-0.3 ~ +7.0	V
Power Supply (4)	Vci		-0.3 ~ +7.0	V
Input Voltage	Vt		-0.3 ~ VDD+0.3	V
Operating Temperature	Topr		-40 ~ +85	°C
Storage Temperature	Tstg		-55 ~ +125	°C

Note1) Stress beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device.
Note 2) It is necessary to meet the conditions of VDD>VSS, Vci>VSS and VSS=0V, and VLCD1 shall be applied after VDD on.
Note 3) To stabilize the device operation, it is better to insert decoupling capacitors between VDD-VSS, Vci-VSS, and VLCD1,2-VSS.

■ DC CHARACTERISTICS

(VDD=1.7 ~ 3.6V, Ta=-40 ~ +85°C)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Note
Power Supply	V_{DD}	VDD pin	1.7	-	5.5	V	
Input Voltage	V_{IH}		$0.8V_{DD}$	-	V_{DD}	V	4
	V_{IL}		0	-	$0.2V_{DD}$	V	
Hysteresis Voltage	V_H	SI pin, V_{DD}=2V	-	0.5	-	V	
		SI pin, V_{DD}=3V	-	0.6	-	V	
Driver ON Resistance (COM)	R_{COM}	$\pm I_d$=1μA, V_{LCD1}=V_{LCD2}=3V/5.5V	-	-	20	kΩ	5
Driver ON Resistance (SEG)	R_{SEG}	$\pm I_d$=1μA, V_{LCD1}=V_{LCD2}=3V/5.5V	-	-	30	kΩ	
Input Leak Current	I_{LI}	V_{IN}=0V ~ V_{DD}	-1	-	1	μA	6
Power Supply Current (1)	I_{DD1}	V_{DD}=2V, Vci=3.3V, Display On, x2 boost (DC=V_{SS}), SI=V_{SS}	-	55	100	μA	7
	Ici_1	Regulator On: (RE2, 1, 0)=(000) V_{IN}=0V or 2V, Ta=25℃, f_{OSC} within the range, IF2=IF1=V_{SS}	-	55	100		
Power Supply Current (2)	I_{DD2}	V_{DD}=1.8V, Vci=1.8V, Display On, x3 boost (DC=V_{DD}), SI=V_{SS}	-	50	100	μA	7
	Ici_2	Regulator Off: (RE2, 1, 0)=(000) V_{IN}=0V or 1.8V, Ta=25℃, f_{OSC} within the range, IF2=IF1=V_{SS}	-	110	170		
Power Supply Current (3)	I_{LCD1}	V_{DD}=3V, Vci=3.3V, Display On, SI=V_{SS}, V_{IN}=0V or 3V, Ta=25℃, f_{OSC} within the range.	-	30	60	μA	7
Output Voltage	V_{OH}	V_{DD}=2V, I_O=0.4mA, P3~P1 pins	V_{DD}-0.4	-	-	V	
	V_{OL}	V_{DD}=2V, I_O=0.4mA, P3~P1 pins	-	-	0.4	V	
LCD Operation Voltage	V_{LCD1}	V_{LCD1} pin, V_{DD}=3V, V_{LCD}>V_{DD}	3.0	-	5.5	V	
LCD Bias Voltage	V_1	Ta=25℃	3.45	3.75	4.05	V	
	V_2 (V_3)	V_{DD}=3V, V_{LCD1}= V_{LCD2}=5V, V_{SS}=0V	2.2	2.5	2.8		
	V_4		0.95	1.25	1.55		
Bleeder Resistance	R_B	V_{LCD2}-V_{SS}=5V, Ta=25℃, R_B=(V_{LCD2}-V_{SS})/IB, EVR=(1111), IB: current of bleeder resistor, Ta=25℃	130	160	190	kΩ	
Oscillator Frequency	f_{OSC}	V_{DD}=3V,Ta=25℃, FSEL=V_{SS}, R=51kΩ, C=120pF	342	380	418	kHz	
External Clock	f_{CP}	Input to OSC1 pin, FSEL=V_{DD}	342	380	418	kHz	
Duty of External Clock	Duty	Input to OSC1 pin, FSEL=V_{DD}	45	50	55	%	
Regulator: Output Voltage	V_{REG}	Vci=3.3V Ta=25°C, (RE2, 1, 0)=(000)	1.80	1.90	2.00	V	8
		(RE2, 1, 0)=(001)	1.90	2.00	2.1		
		(RE2, 1, 0)=(010)	1.99	2.10	2.21		
		(RE2, 1, 0)=(011)	2.09	2.20	2.31		
		(RE2, 1, 0)=(100)	2.18	2.30	2.42		
		(RE2, 1, 0)=(101)	2.28	2.40	2.52		
		(RE2, 1, 0)=(110)	2.37	2.50	2.63		
		(RE2, 1, 0)=(111)	2.47	2.60	2.73		
Regulator: Difference between Input and Output Voltage	ΔV_{IO}	I_{OUT}=1mA, Ta=25℃	-	0.2	0.6	V	8
Regulator: Input Voltage	Vci	Vci pin, Regulator ON, Ta=25℃	-	-	5.5	V	8
Regulator: Regulator Current	I_{REG}	Vci=3.3V, Regulator ON: (RE2,1,0)=(000), Ta=25℃, Vci pin. V_{OUT} Open, V_{LCD1}=5V, Boost Off, 1μF capacitor between V_{REG}-V_{SS}.	-	6	20	μA	
Regulator: Load Stability	ΔV_{REG}	Vci=3.3V, I_{OUT}=1~5mA, Ta=25℃	-	-	200	mV	8
Boost Output Voltage	V_{OUT}	Vci=2.7V,REGON=0V,DC=0(x2 boost), Ta=25°C	5.0	5.3	-	V	9
		Vci=1.8V,REGON=0V, DC=1(x3 boost), Ta=25°C	5.0	5.3	-		

Note 4) Apply to OSC1, SEL1, SEL2, REGON, IF2, IF1, DC and SI pins
Note 5) The resistance between each COM/SEG driver and VLCD/VSS/V1/V2/V4 pins when Id current pass through.
Note 6) Apply to SI, SEL1, SEL2, REGON, IF2, IF1, DC and FSEL pins.
Note 7) IDD: VDD pin, VOUT and VLCD1 connected, boost On, EVR=(1111).
Ici: Vci pin, VOUT and VLCD1 connected, boost On, EVR=(1111).
ILCD1: VLCD1 pin, VOUT open, VLCD1=5V, boost off, EVR=(1111).
*Connect 1µF capacitor between VREG-VSS, C1-~C1+, C2-~C2+, VOUT-VSS.
Note 8) Connect 1µF capacitors between Vci-VSS, VREG-VSS. The min. input voltage is limited by the output voltage and ΔV_{IO}.
Note 9) VOUT and VLCD1 connected, Connect 1µF capacitors between VREG-VSS, C1-~C1+, C2-~C2+, VOUT-VSS.
Note 10) If VIN is defined in the Conditions, it applies to the input pins which is not specified in the Conditions.

■ SYSTEM INTERFACE TIMING

• 1-line serial interface

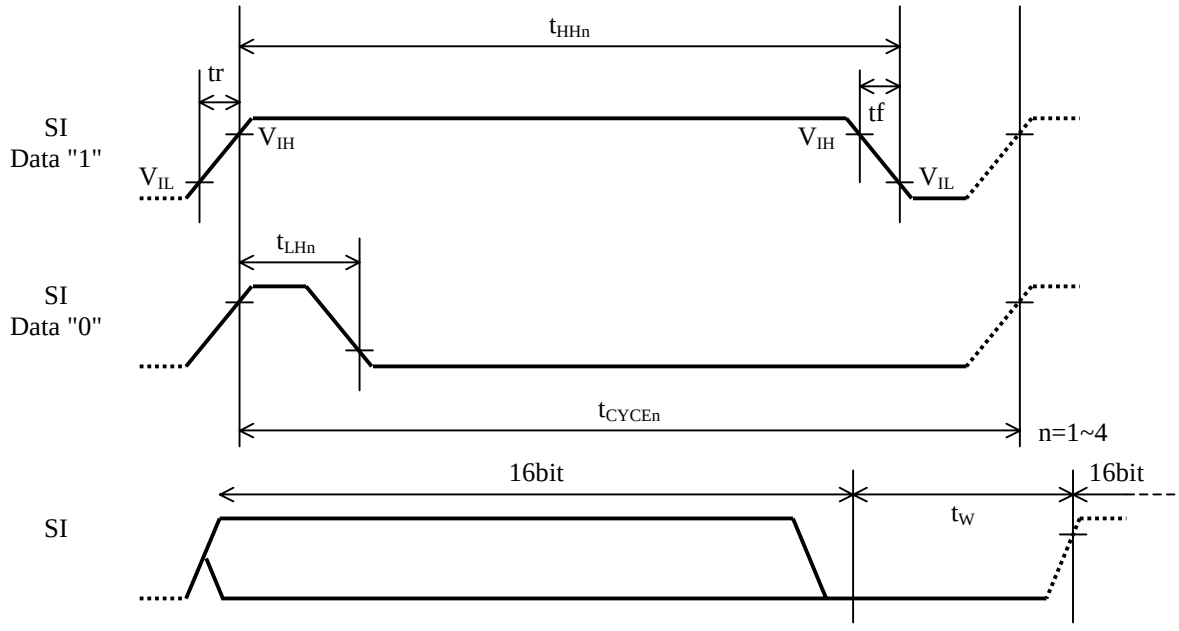
(VDD=1.7 ~ 3.6V, VSS=0V, Ta=-40 ~ +85°C, fosc=380kHz)

Parameter	Symbol	MIN	TYP	MAX	Unit	IF2	IF1
Wait time 1 *1	t_{W1}	$600t_{CLK}$	-	-	µs	-	-
Wait time 2 *2	t_{W2}	$280t_{CLK}$	-	-	µs	-	-
Serial Clock cycle time 1	$t_{CYCE}1$	$30t_{CLK}$	$32t_{CLK}$	$34t_{CLK}$	µs	L	L
Serial Clock cycle time 2	$t_{CYCE}2$	$62t_{CLK}$	$64t_{CLK}$	$66t_{CLK}$	µs	L	H
Serial Clock cycle time 3	$t_{CYCE}3$	$126t_{CLK}$	$128t_{CLK}$	$130t_{CLK}$	µs	H	L
Serial Clock cycle time 4	$t_{CYCE}4$	$254t_{CLK}$	$256t_{CLK}$	$258t_{CLK}$	µs	H	H
Time length for data"1" 1	$t_{HH}1$	$22t_{CLK}$	$24t_{CLK}$	$26t_{CLK}$	µs	L	L
Time length for data “1” 2	$t_{HH}2$	$46t_{CLK}$	$48t_{CLK}$	$50t_{CLK}$	µs	L	H
Time length for data “1” 3	$t_{HH}3$	$94t_{CLK}$	$96t_{CLK}$	$98t_{CLK}$	µs	H	L
Time length for data “1” 4	$t_{HH}4$	$190t_{CLK}$	$192t_{CLK}$	$194t_{CLK}$	µs	H	H
Time length for data “0” 1	$t_{LH}1$	$2t_{CLK}$	$4t_{CLK}$	$6t_{CLK}$	µs	L	L
Time length for data “0” 2	$t_{LH}2$	$6t_{CLK}$	$8t_{CLK}$	$10t_{CLK}$	µs	L	H
Time length for data “0” 3	$t_{LH}3$	$14t_{CLK}$	$16t_{CLK}$	$18t_{CLK}$	µs	H	L
Time length for Data “0” 4	$t_{LH}4$	$30t_{CLK}$	$32t_{CLK}$	$34t_{CLK}$	µs	H	H
Rising time of serial clock	tr	-	-	100	ns	-	-
Falling time of serial clock	tf	-	-	100	ns	-	-

*1: After “Display Clear” instruction

*2: After the instruction other than “Display Clear”.

※ t_{CLK} = 1/fosc

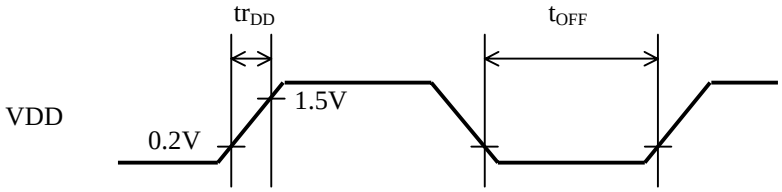


- Power Supply Startup

(Ta=-40 ~ +85°C)

Parameter	Symbol	MIN	TYP	MAX	Unit
Startup time of power supply	tr_{DD}	0.1	-	5	ms
Time for Power supply off	t_{OFF}	1	-	-	ms

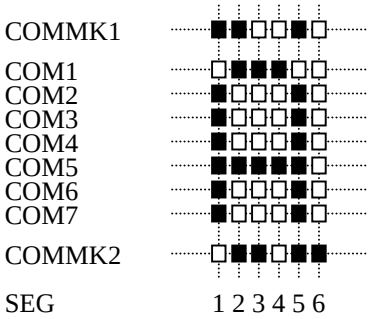
If the above conditions cannot be met, the internal reset circuit will malfunction.

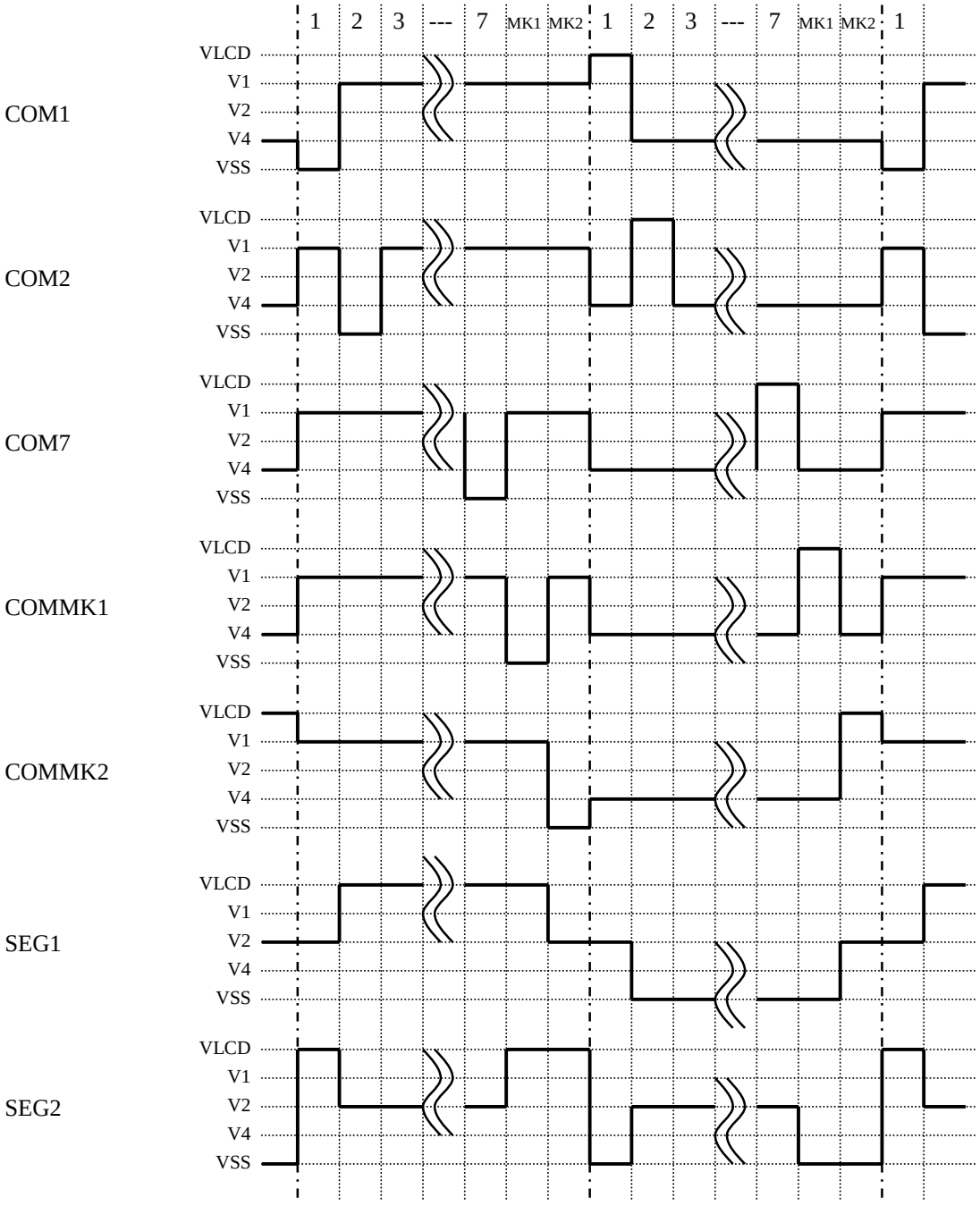


t_{OFF} is the period when VDD is below than 0.2V during power temporarily blackout or power cycle on/off.

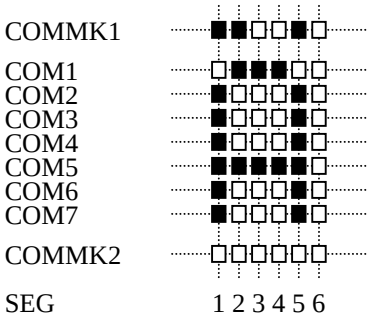
■ LCD DRIVING VOLTAGE WAVEFORM

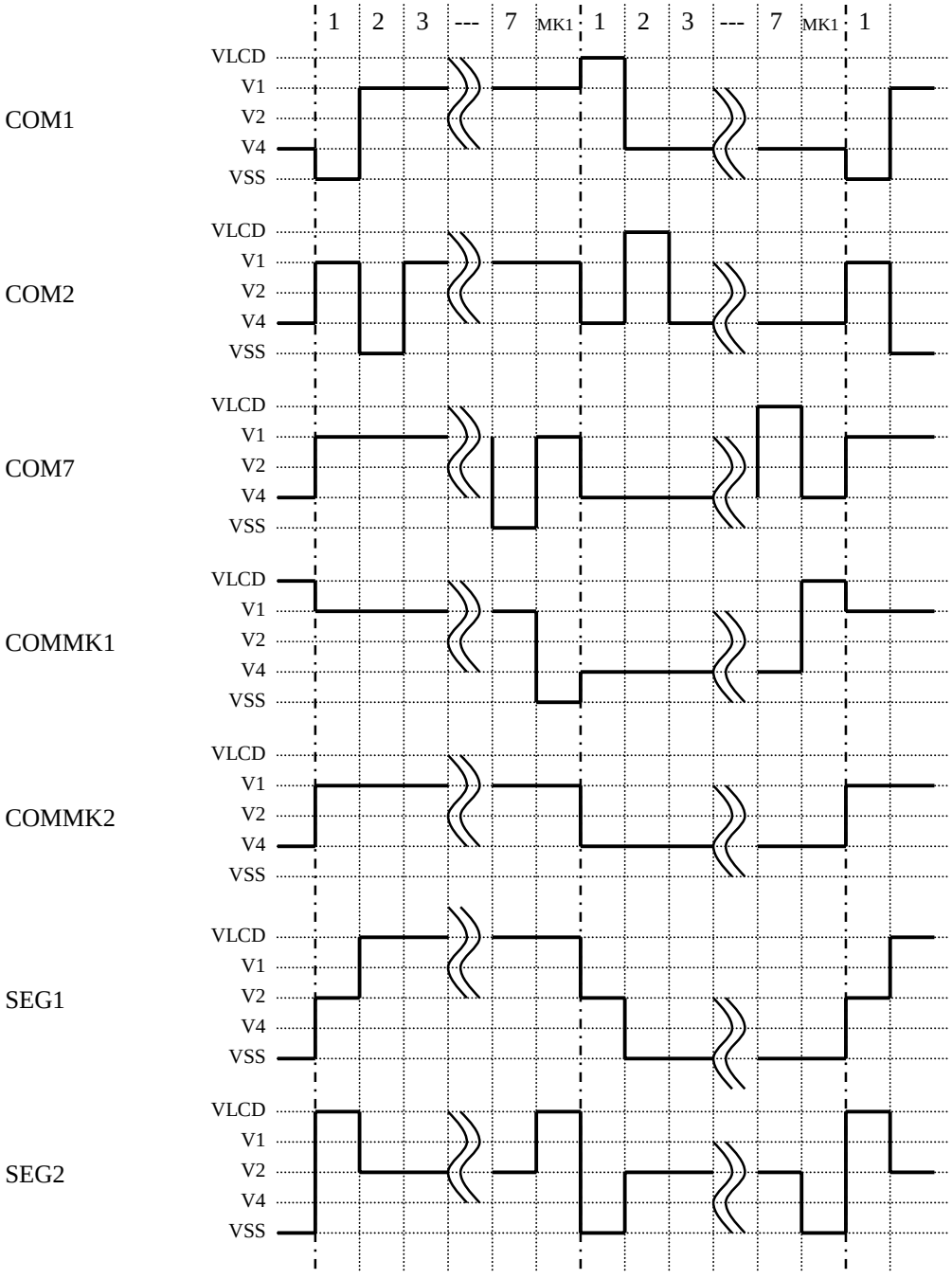
(1) 1/9Duty





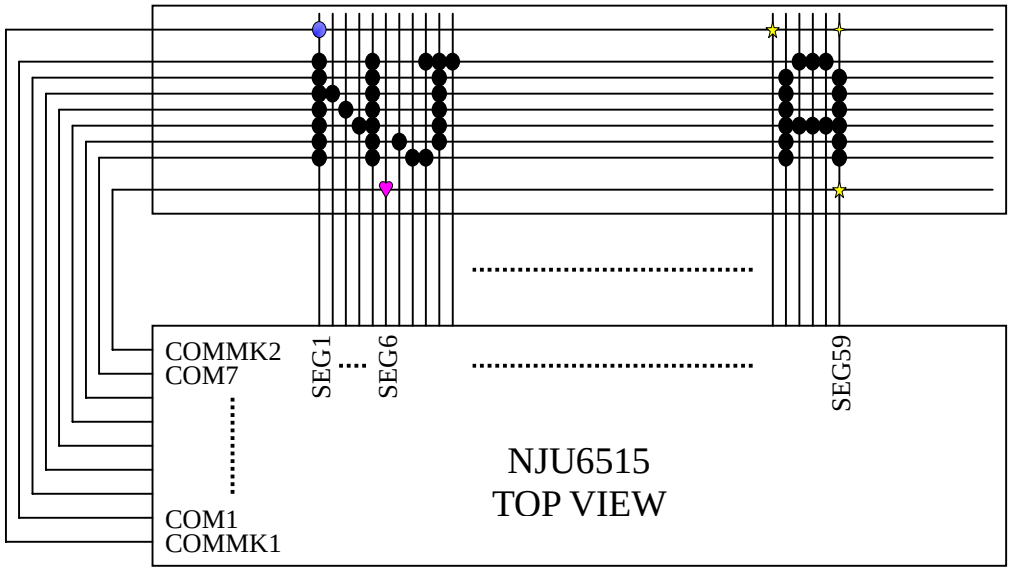
(2) 1/8Duty



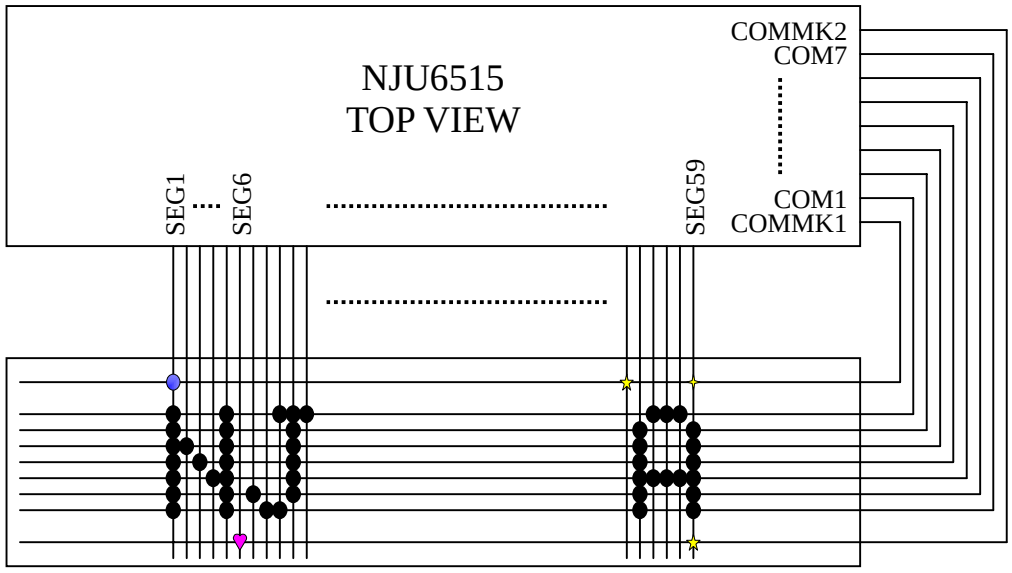


■ APPLICATION INFROMATION

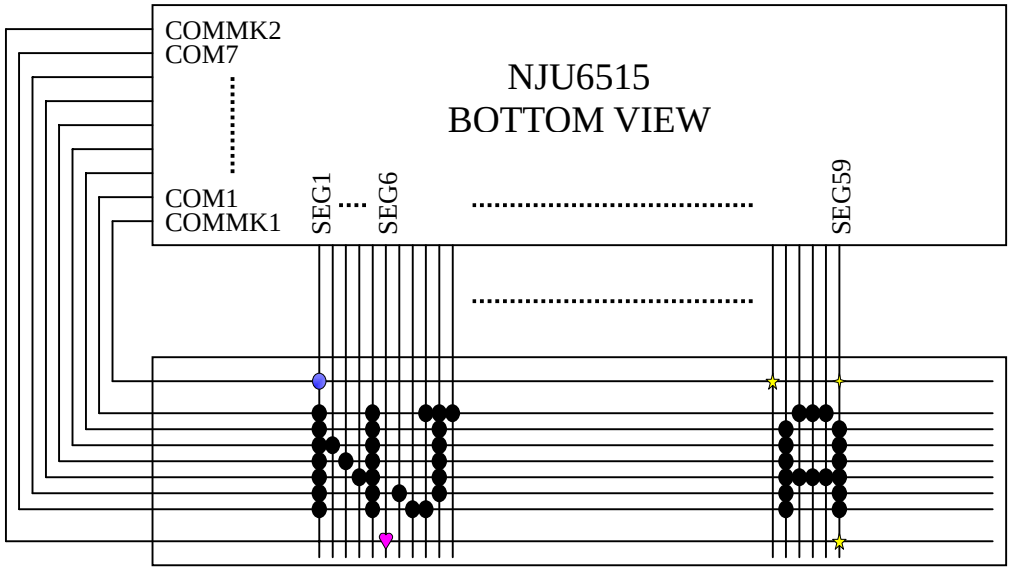
(1-1) Interface with LCD panel, SEL1=0, SEL2=0



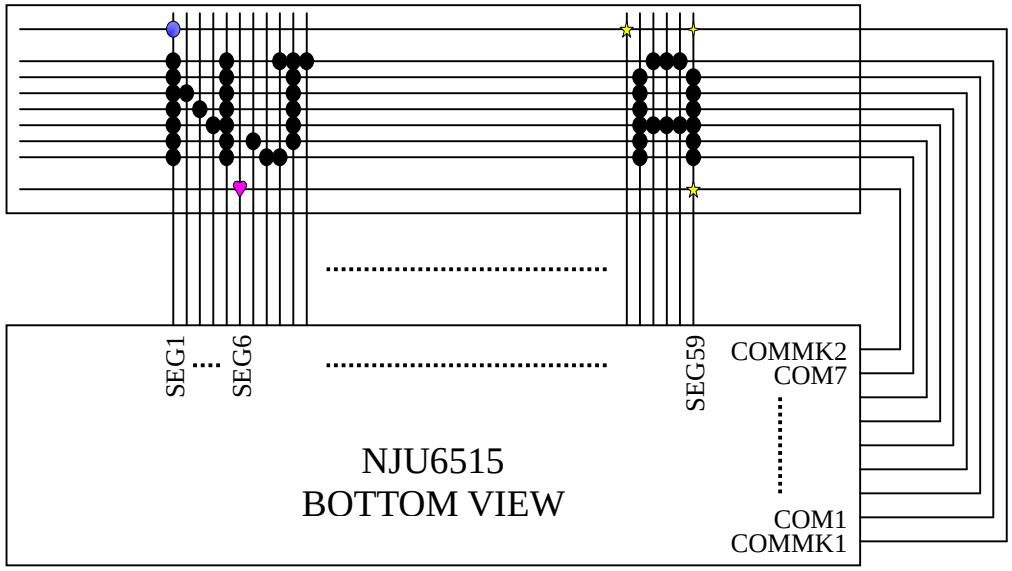
(1-2) Interface with LCD panel, SEL1=1, SEL2=1



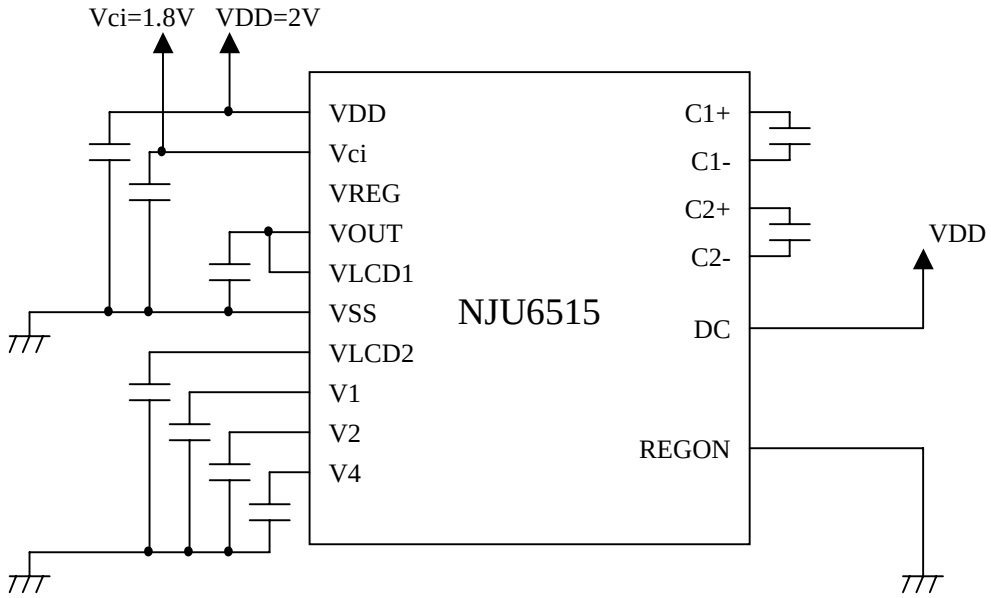
(1-3) Interface with LCD panel, SEL1=1, SEL2=0



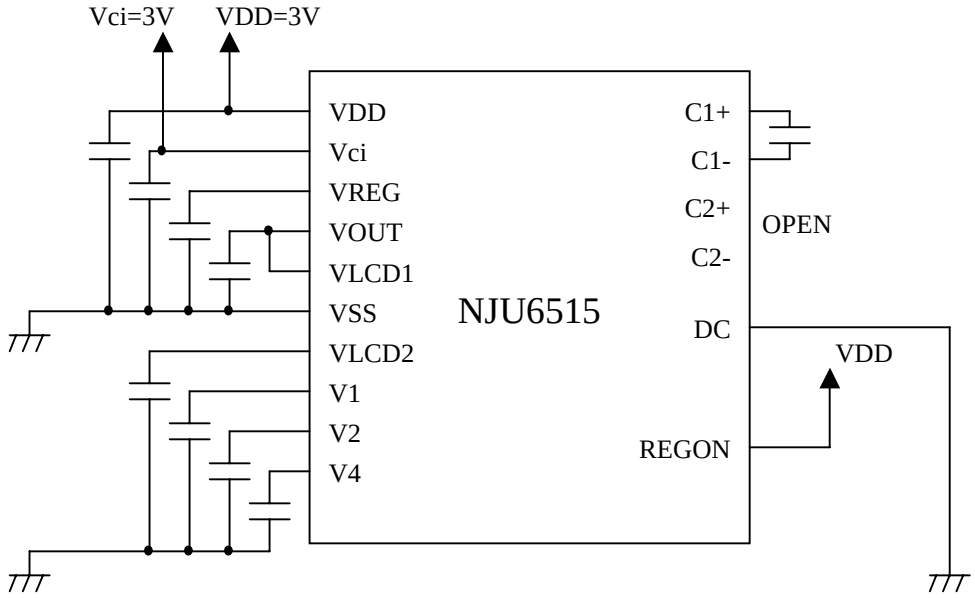
(1-4) Interface with LCD panel, SEL1=0, SEL2=1



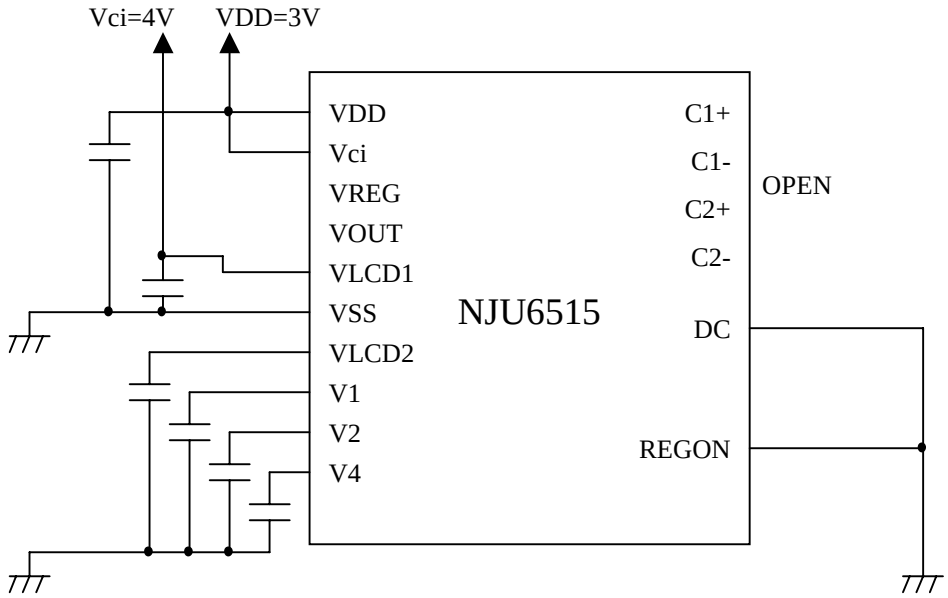
(2-1) Voltage boost ON (x 3), Regulator OFF, Electrical Volume ON.



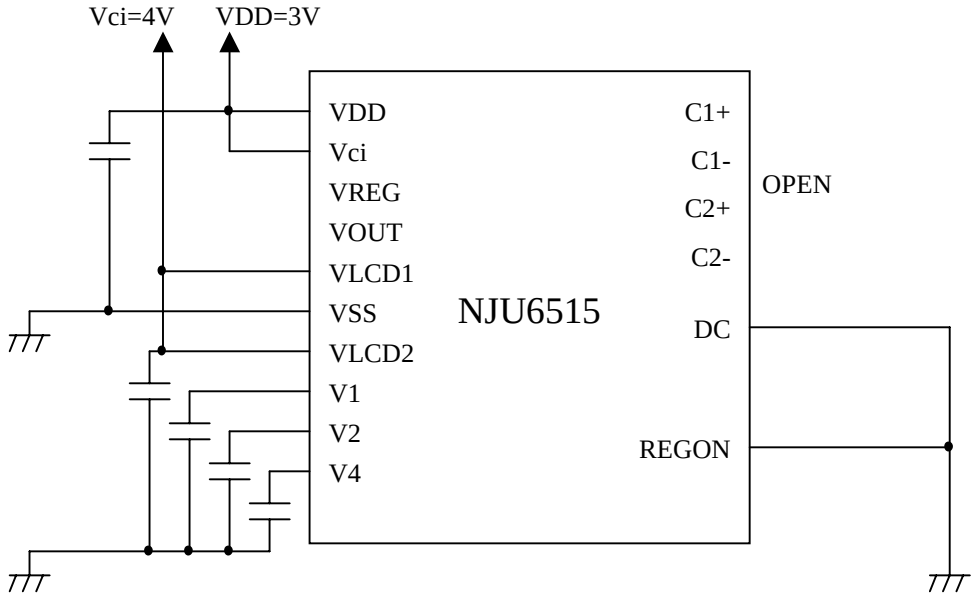
(2-2) Voltage boost ON (x 2), Regulator ON, Electrical Volume ON



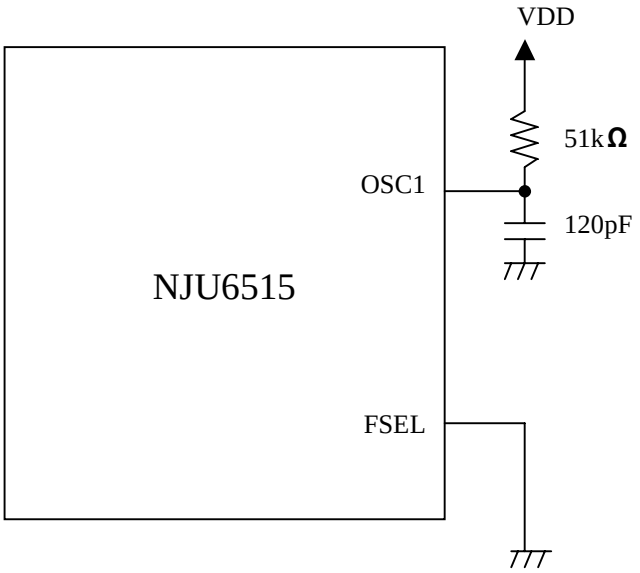
(2-3) Voltage boost OFF, Regulator OFF, Electrical Volume ON



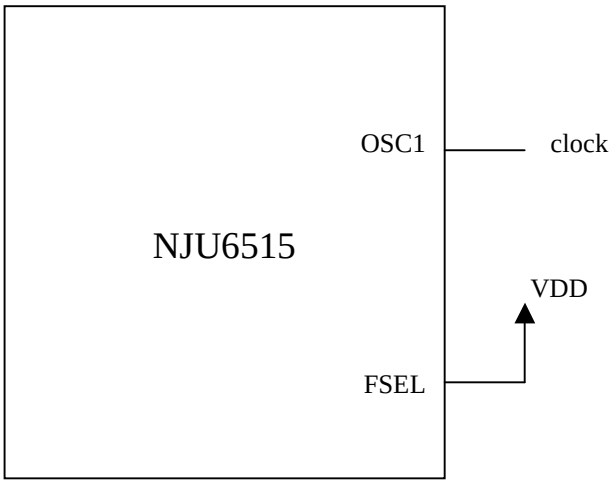
(2-4) Voltage boost OFF, Regulator OFF, Electrical Volume OFF



(3-1) Using external CR for oscillation



(3-2) Using external clock



[CAUTION]
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