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MPC823ELE/D
Revision 1

MOTOROLA

MPC823 AC Electrical Specifications

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC823.

Note: Visit our website at www.motorola.com if you are using a frequency other than 25, 40, or 50MHz. Our website contains a spreadsheet that you can use to calculate the timing for your specific system frequency.

This device contains circuitry protecting against damage from high-static voltage or electrical fields. However, it is advised that precautions be taken to avoid application of any voltages higher than the maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

MAXIMUM RATINGS (GND = 0V)

RATING	SYMBOL	VALUE	UNIT
Supply Voltage	VDDH	-0.3 to 4.0	V
	VDD	-0.3 to 4.0	V
	KAPWR	-0.3 to 4.0	V
	VDDSYN	-0.3 to 4.0	V
Input Voltage (JTAG and GPIO)	VIN	-0.3 to 5.8	V
Input Voltage (All other pins)	VIN	-0.3 to 3.3	V
Operating Temperature	T_A	0 to 70˚ or -40˚ to 85˚	˚C
Storage Temperature Range	T_{STG}	-55 to +150	˚C

NOTES:

1. Functional operating conditions are given in **DC Electrical Characteristics (VCC = 3.0 - 3.6 V)**. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
2. **CAUTION**: The JTAG and GPIO input voltages cannot be more than 2.5 V greater than supply voltage, this restriction applies also on “power-on” as well as on normal operation.
3. 5 Volt friendly inputs are inputs that tolerate 5 volts for JTAG and GPIO pins.
4. If you are using Mask Revision Base #F98S (Revision 0), all pins except EXTAL and CLK4IN are 5V tolerant inputs.

THERMAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Thermal Resistance for BGA	θ_{Jc}	~30	°C/W

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from

$$T_J = T_A + (P_D \bullet q_{JA}) \qquad (1)$$

where

T_A = Ambient Temperature, ∞C
q_{JA} = Package Thermal Resistance, Junction to Ambient, ∞C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = I_{DD} x V_{DD}, Watts—Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins—User Determined

For most applications $P_{I/O} < 0.3 \bullet P_{INT}$ and can be neglected. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is:

$$P_D = K \prod (T_J + 273\infty C) \qquad (2)$$

Solving equations (1) and (2) for K gives

$$K = P_D \bullet (T_A + 273\infty C) + q_{JA} \bullet P_D^{\,2} \qquad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Layout Practices

Each V_{CC} pin on the MPC823 should be provided with a low-impedance path to the board's supply. Each GND pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 μF bypass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and GND should be kept to less than half an inch per capacitor lead. A four-layer board that employs two inner layers as V_{CC} and GND planes should be used.

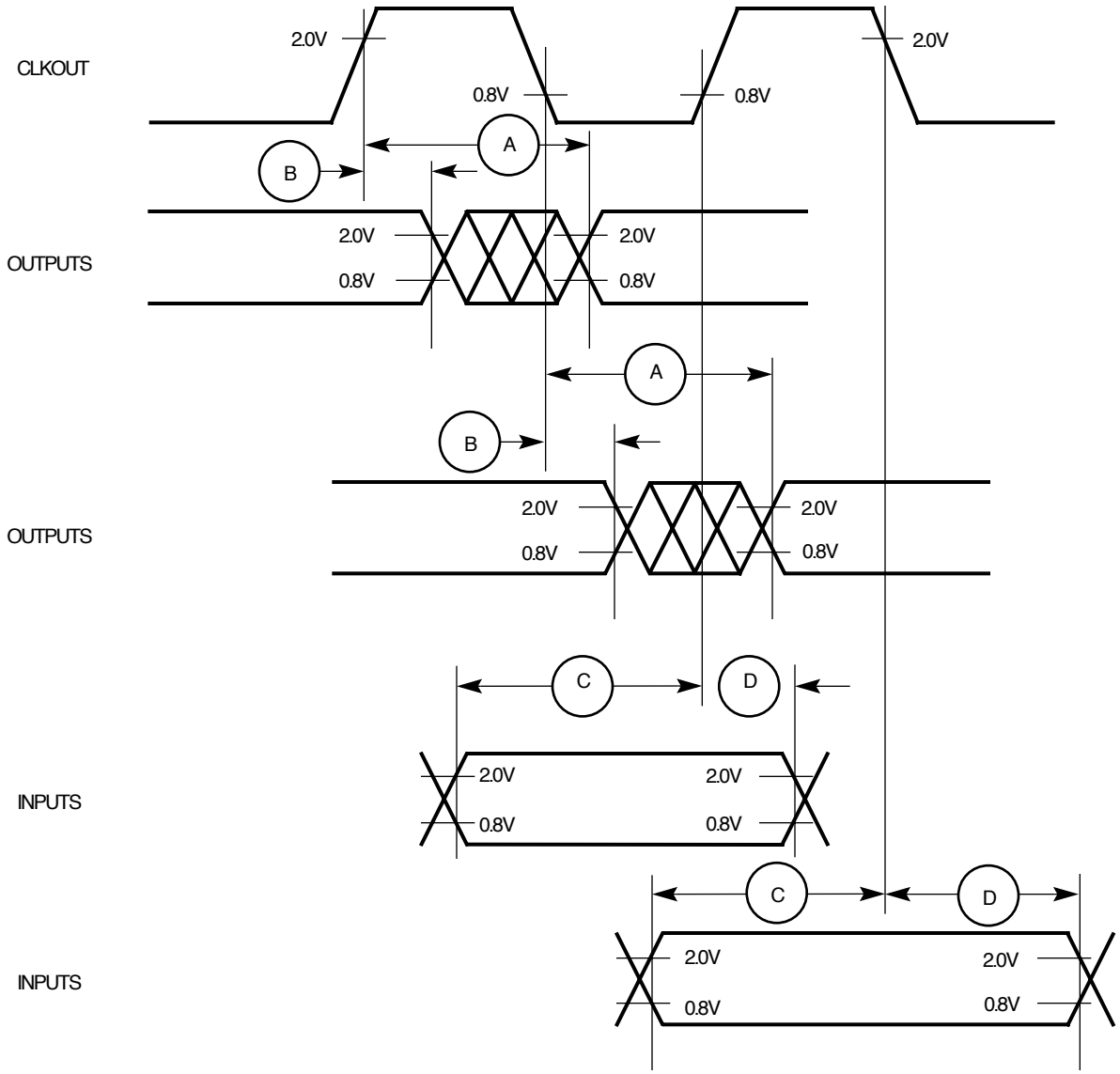
All output pins on the MPC823 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.0 - 3.6 V)

CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT
Input High Voltage (for JTAG and GPIO)	V_{IH}	2.0	5.5	V
Input High Voltage (all other pins)	V_{IH}	2.0	3.6	V
Input Low Voltage	V_{IL}	GND	0.8	V
EXTAL and EXTCLK Input High Voltage	V_{IHC}	0.7*(V_{CC})	V_{CC}+0.3	V
Input Leakage Current, V_{IN} = 5.5 V	I_{IN}	—	±10	μA
Hi-z (Off State) Leakage Current, V_{IN} = 3.5V	I_{OZ}	—	±10	μA
Signal Low Input Current, V_{IL} = 0.8 V	I_L		±10	μA
Signal High Input Current, V_{IH} = 2.0 V	I_H		±10	μA
Output High Voltage, I_{OH} = –2.0 mA, V_{DDH} = 3.0V Except XTAL, XFC, and Open-Drain Pins	V_{OH}	2.4	—	V
Output Low Voltage IOL = 2.0 mA CLKOUT IOL = 3.2 mAA[6:31], TSIZ0/REG, TSIZ1, D(0:31), DP[0:3]/IRQ[3:6], RD/WR, BURST, RSV/IRQ2, IP_B[0:1]/IWP[0:1]/VFLS[0:1], IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, USBRXD/PA15, RXD2/PA13, SMRXD2/L1TXDA/PA9, SMTXD2/L1RXDA/PA8, IRQ4/KR/SPKROUT, TIN1/L1RCLKA/BRGO1/CLK1/PA7, TIN3/TOUT1/CLK2/PA6, TIN2/L1TCLKA/BRGO2/CLK3/PA5, TIN4/TOUT2/CLK4/PA4, LCD_A/SPISEL/PB31, SPICLK/PB30, SPIMOSI/PB29, BRGO3/SPIMISO/PB28, BRGO1/I2CSDA/PB27, BRGO2/I2CSCL/PB26, SMTXD1/PB25, SMRXD1/PB24, SMSYN1/SDACK1/PB23, SMSYN2/SDACK2/PB22, LCD_B/L1ST1/PB19, L1ST2/RTS2/PB18, LCD_C/L1ST3/PB17, L1ST4/L1RQA/PB16, L1ST5/DREQ1/PC15, L1ST6/RTS2/DREQ2/PC14, L1ST7/PC13, L1ST8/L1RQA/PC12, USBRXP/PC11, USBRXN/TGATE1/PC10, CTS2/PC9, TGATE1/CD2/PC8, USBTXP/PC7, USBTXN/PC6, SDACK1/L1TSYNCA/PC5, L1RSYNCA/PC4, LD8/VD7/PD15, LD7/VD6/PD14, LD6/VD5/PD13, LD5/VD4/PD12, LD4/VD3/PD11, LD3/VD2/PD10, LD2/VD1/PD9, LD1/VD0/PD8, FRAME/VSYNC/PD5, LCD_AC/LOE/BLANK/PD6, LD0/FIELD/PD7, LOAD/HSYNC/PD4, SHIFT/CLK/PD3	V_{OL}	—	0.5	V
IOL = 5.3 mABDIP/GPL_B5, BR, BG, FRZ/IRQ6, CS[0:5], CS6/CE1_B, CS7/CE2_B, WE0/BS_AB0/IORD, WE1/BS_AB1/IOWR, WE2/BS_AB2/PCOE, WE3/BS_AB3/PCWE, GPL_A0/GPL_B0, OE/GPL_A1/GPL_B1, GPL_A[2:3]/GPL_B[2:3]/CS[2:3], UPWAITA/GPL_A4/AS, UPWAITB/GPL_B4, GPL_A5, ALE_B/DSCK/AT1, OP2/MODCK1/STS, OP3/MODCK2/DSDO IOL = 7.0 mA USBOE/PA14, TXD2/PA12 IOL = 8.9 mATS, TA, TEA, BI, BB, HRESET, SRESET				

NOTE: Input pin voltage specifications are V_{CC} = +4 V or 5.8 V, whichever is less.
AC timings are based on a 50 pf load.
If you are using Mask Revision Base #F98S, all pins except EXTAL and CLK4IN are 5V tolerant inputs.

AC ELECTRICAL CHARACTERISTICS



A = MAXIMUM OUTPUT DELAY SPECIFICATION
B = MINIMUM OUTPUT HOLD TIME
C = MINIMUM INPUT SETUP TIME SPECIFICATION
D = MINIMUM INPUT HOLD TIME SPECIFICATION

EXTERNAL BUS ELECTRICAL CHARACTERISTICS

Table 1. Bus Operation Timing

NUM	CHARACTERISTIC	25MHz		40MHz		50MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
B1	CLKOUT Period	40	—	25	—	20	—	ns
B1a	EXTCLK to CLKOUT Phase Skew (EXTCLK>15MHz and MF ≤ 2)	-0.9	0.9	-0.9	0.9	-0.9	0.9	ns
B1b	EXTCLK to CLKOUT Phase Skew (EXTCLK>10MHz and MF ≤ 10)	-2.3	2.3	-2.3	2.3	-2.3	2.3	ns
B1c	CLKOUT Phase Jitter (EXTCLK>15MHz and MF≤2)	-0.6	0.6	-0.6	0.6	-0.6	0.6	ns
B1d	CLKOUT Phase Jitter (EXTCLK>10MHz and MF≤10)	-2	2	-2	2	-2	2	ns
B1e	CLKOUT Frequency Jitter (MF<10)	—	0.5	—	0.5	—	0.5	%
B1f	CLKOUT Frequency Jitter (10<MF<500)	—	2	—	2	—	2	%
B1g	CLKOUT Frequency Jitter (MF>500)	—	3	—	3	—	3	%
B1h	Frequency Jitter on EXTCLK	—	0.5	—	0.5	—	0.5	%
B2	Clock Pulse Width Low	16	—	10	—	8	—	ns
B3	Clock Pulse Width High	16	—	10	—	8	—	ns
B4	CLKOUT Rise Time	—	4	—	4	—	4	ns
B5	CLKOUT Fall Time	—	4	—	4	—	4	ns
B6	N/A (Used on Interactive Spreadsheet)							
B7	CLKOUT to A(6:31), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) Invalid	10	—	5	—	5	—	ns
B7a	CLKOUT to TSIZ(0:1),$\overline{REG}$, $\overline{RSV}$, AT(0:3),$\overline{BDIP}$, $\overline{PTR}$ Invalid	10	—	5	—	5	—	ns
B7b	CLKOUT to $\overline{BR}$, $\overline{BG}$, FRZ, VFLS(0:1), VF(0:2), IWP(0:2), LWP(0:1), $\overline{STS}$ Invalid	10	—	5	—	5	—	ns
B8	CLKOUT to A(6:31), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) Valid	10	19	5	13	5	12	ns
B8a	CLKOUT to TSIZ(0:1),$\overline{REG}$, $\overline{RSV}$, AT(0:3), $\overline{BDIP}$, $\overline{PTR}$ Valid	10	19	5	13	5	12	ns
B8b	CLKOUT to $\overline{BR}$, $\overline{BG}$, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), $\overline{STS}$ Valid	10	19	5	13	5	12	ns
B9	CLKOUT to A(6:31), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3), TSIZ(0:1),$\overline{REG}$, $\overline{RSV}$, AT(0:3), $\overline{PTR}$ Hi Z	10	19	5	13	5	12	ns
B10	N/A							
B11	CLKOUT to $\overline{TS}$, $\overline{BB}$ Assertion	10	19	5	12.25	5	12.25	ns
B11a	CLKOUT to $\overline{TA}$, $\overline{BI}$ Assertion (when driven by the Memory Controller or PCMCIA Interface)	2.5	11	2.5	9.25	2.5	9.25	ns
B12	CLKOUT to $\overline{TS}$, $\overline{BB}$ Negation	10	19	5	13	5	12	ns
B12a	CLKOUT to $\overline{TA}$, $\overline{BI}$ Negation (when driven by the Memory Controller or PCMCIA Interface)	2.5	11	2.5	11	2.5	11	ns
B13	CLKOUT to $\overline{TS}$, $\overline{BB}$ Hi Z	10	24	5	21	5	19	ns

Table 1. Bus Operation Timing (Continued)

NUM	CHARACTERISTIC	25MHz		40MHz		50MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
B13a	CLKOUT to $\overline{TA}$, $\overline{BI}$ Hi Z (When Driven by the Memory Controller or PCMCIA Interface)	2.5	15	2.5	15	2.5	16	ns
B14	CLKOUT to $\overline{TEA}$ Assertion	2.5	11	2.5	11	2.5	10	ns
B15	CLKOUT to $\overline{TEA}$ Hi Z	2.5	15	2.5	15	2.5	15	ns
B16	$\overline{TA}$, $\overline{BI}$ Valid to CLKOUT (Setup Time)	9.75	—	9.75	—	9.75	—	ns
B16a	$\overline{TEA}$, $\overline{KR}$, $\overline{RETRY}$ Valid to CLKOUT (Setup Time)	11	—	10	—	10	—	ns
B16b	$\overline{BB}$, $\overline{BG}$, $\overline{BR}$ Valid to CLKOUT (Setup Time)	8.5	—	8.5	—	8.5	—	ns
B17	CLKOUT to $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{BG}$, $\overline{BR}$ Valid (Hold Time)	1	—	1	—	1	—	ns
B17a	CLKOUT to $\overline{KR}$, $\overline{RETRY}$ Valid (Hold Time)	2	—	2	—	2	—	ns
B18	D(0:31), DP(0:3) Valid to CLKOUT Rising Edge (Setup Time)	6	—	6	—	6	—	ns
B19	CLKOUT Rising Edge to D(0:31), DP(0:3) Valid (Hold Time)	2	—	2	—	2	—	ns
B20	D(0:31), DP(0:3) Valid to CLKOUT Falling Edge (Setup Time)	4	—	4	—	4	—	ns
B21	CLKOUT Falling Edge to D(0:31), DP(0:3) Valid (Hold Time)	2	—	2	—	2	—	ns
B22	CLKOUT Rising Edge to $\overline{CS}$ Asserted -GPCM- ACS = 00	10	20	5	13	5	13	ns
B22a	CLKOUT Falling Edge to $\overline{CS}$ Asserted -GPCM- ACS = 10, TRLX = 0	—	10	—	8	—	8	ns
B22b	CLKOUT Falling Edge to $\overline{CS}$ Asserted -GPCM- ACS = 11, TRLX = 0, EBDF = 0	10	20	5	13	5	13	ns
B22c	CLKOUT Falling Edge to $\overline{CS}$ Asserted -GPCM- ACS = 11, TRLX = 0, EBDF = 1	14	25	7	16	7	16	ns
B23	CLKOUT Rising Edge to $\overline{CS}$ Negated -GPCM-Read Access - GPCM-Write Access, ACS=00, TRLX=0, CSNT=0	3	10	2	8	2	8	ns
B24	A(6:31) to $\overline{CS}$ Asserted -GPCM- ACS = 10, TRLX = 0	8	—	3	—	3	—	ns
B24a	A(6:31) to $\overline{CS}$ Asserted -GPCM- ACS = 11, TRLX = 0	18	—	8	—	8	—	ns
B25	CLKOUT Rising Edge to $\overline{OE}$, $\overline{WE}$(0:3) Asserted	—	11	—	9	—	9	ns
B26	CLKOUT Rising Edge to $\overline{OE}$ Negated	3	11	2	9	2	9	ns
B27	A(6:31) to $\overline{CS}$ Asserted -GPCM- ACS = 10, TRLX = 1	48	—	23	—	23	—	ns
B27a	A(6:31) to $\overline{CS}$ Asserted -GPCM- ACS = 11, TRLX = 1	58	—	28	—	28	—	ns
B28	CLKOUT Rising Edge to $\overline{WE}$(0:3) Negated -GPCM-Write Access CSNT = '0'	—	11	—	9	—	9	ns
B28a	CLKOUT Falling Edge to $\overline{WE}$(0:3) Negated -GPCM-Write Access TRLX = '0', CSNT = '1', EBDF=0	10	20	5	13	5	13	ns
B28b	CLKOUT Falling Edge to $\overline{CS}$ Negated -GPCM-Write Access TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', EBDF = 0	—	20	—	13	—	13	ns

Table 1. Bus Operation Timing (Continued)

NUM	CHARACTERISTIC	25MHz		40MHz		50MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
B28c	CLKOUT Falling Edge to $\overline{WE}$(0:3) Negated -GPCM-Write Access TRLX = '0', CSNT = '1', EBDF=1	14	25	7	16	7	16	ns
B28d	CLKOUT Falling Edge to $\overline{CS}$ Negated -GPCM-Write Access TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', EBDF = 1	—	25	—	16	—	16	ns
B29	$\overline{WE}$(0:3) Negated to D(0:31), DP(0:3) Hi Z -GPCM- Write Access, CSNT = '0'	8	—	3	—	3	—	ns
B29a	$\overline{WE}$(0:3) Negated to D(0:31), DP(0:3) Hi Z -GPCM- Write Access, TRLX = '0', CSNT = '1', EBDF = 0	18	—	8	—	8	—	ns
B29b	$\overline{CS}$ Negated to D(0:31), DP(0:3) Hi Z -GPCM- Write Access, ACS = '00', TRLX = '0' & CSNT = '0'	8	—	3	—	3	—	ns
B29c	$\overline{CS}$ Negated to D(0:31), DP(0:3) Hi Z -GPCM- Write Access, TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', EBDF = 0	18	—	8	—	8	—	ns
B29d	$\overline{WE}$(0:3) Negated to D(0:31), DP(0:3) Hi Z -GPCM- Write Access, TRLX = '1', CSNT = '1', EBDF = 0	58	—	28	—	28	—	ns
B29e	$\overline{CS}$ Negated to D(0:31), DP(0:3) Hi Z -GPCM- Write Access, TRLX = '1', CSNT = '1', ACS = '10' or ACS='11', EBDF = 0	58	—	28	—	28	—	ns
B29f	$\overline{WE}$(0:3) Negated to D(0:31), DP(0:3) Hi Z -GPCM- Write Access, TRLX = '0', CSNT = '1', EBDF = 1	12	—	5	—	5	—	ns
B29g	$\overline{CS}$ Negated to D(0:31), DP(0:3) Hi Z -GPCM- Write Access, TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', EBDF = 1	12	—	5	—	5	—	ns
B29h	$\overline{WE}$(0:3) Negated to D(0:31), DP(0:3) Hi Z -GPCM- Write Access, TRLX = '1', CSNT = '1', EBDF = 1	52	—	24	—	24	—	ns
B29i	$\overline{CS}$ Negated to D(0:31), DP(0:3) Hi Z -GPCM- Write Access, TRLX = '1', CSNT = '1', ACS = '10' or ACS='11', EBDF =1	52	—	24	—	24	—	ns
B30	$\overline{CS}$, $\overline{WE}$(0:3) Negated to A(6:31) invalid -GPCM- Write Access.	8	—	3	—	3	—	
B30a	$\overline{WE}$(0:3) Negated to A(6:31) Invalid -GPCM- Write Access, TRLX='0', CSNT = '1'. CS Negated to A(6:31) Invalid -GPCM-Write Access, TRLX='0', CSNT = '1', ACS = 10,ACS = ='11', EBDF = 0	18	—	8	—	8	—	ns
B30b	$\overline{WE}$(0:3) Negated to A(6:31)Invalid -GPCM- Write Access, TRLX='1', CSNT = '1'. CS Negated to A(6:31)Invalid -GPCM-Write Access, TRLX='1', CSNT = '1', ACS = 10,ACS = ='11', EBDF = 0	58	—	28	—	28	—	ns
B30c	$\overline{WE}$(0:3) Negated to A(6:31) Invalid -GPCM- Write Access, TRLX='0', CSNT = '1'. CS Negated to A(6:31) Invalid -GPCM-Write Access, TRLX='0', CSNT = '1', ACS = 10 ,ACS = ='11', EBDF = 1	12	—	4	—	4	—	ns
B30d	$\overline{WE}$(0:3) Negated to A(6:31) Invalid -GPCM- Write Access, TRLX='1', CSNT = '1'. CS Negated to A(6:31) Invalid -GPCM-Write Access, TRLX='1', CSNT = '1', ACS = 10,ACS = ='11', EBDF = 1	52	—	24	—	24	—	ns
B31	CLKOUT Falling Edge to $\overline{CS}$ valid as requested by CST4 in the corresponding word of the UPM	1.5	10	1.5	8	1.5	8	ns

Table 1. Bus Operation Timing (Continued)

NUM	CHARACTERISTIC	25MHz		40MHz		50MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
B31a	CLKOUT Falling Edge to $\overline{CS}$ valid as requested by CST1 in the corresponding word of the UPM, EBDF = 0	10	20	5	13	5	13	ns
B31b	CLKOUT Rising Edge to $\overline{CS}$ valid as requested by CST2 in the corresponding word of the UPM	1.5	10	1.5	8	1.5	8	ns
B31c	CLKOUT Rising Edge to $\overline{CS}$ valid as requested by CST3 in the corresponding word of the UPM	10	20	5	13	5	13	ns
B31d	CLKOUT Falling Edge to $\overline{CS}$ valid as requested by CST1 in the corresponding word of the UPM, EBDF = 1	10	25	5	16	5	16	ns
B32	CLKOUT Falling Edge to $\overline{BS}$ valid as requested by BST4 in the corresponding word of the UPM	1.5	10	1.5	8	1.5	8	ns
B32a	CLKOUT Falling Edge to $\overline{BS}$ valid as requested by BST1 in the corresponding word of the UPM, EBDF = 0	10	20	5	13	5	13	ns
B32b	CLKOUT Rising Edge to $\overline{BS}$ valid as requested by BST2 in the corresponding word of the UPM	1.5	10	1.5	8	1.5	8	ns
B32c	CLKOUT Rising Edge to $\overline{BS}$ valid as requested by BST3 in the corresponding word of the UPM	10	20	5	13	5	13	ns
B32d	CLKOUT Falling Edge to $\overline{BS}$ valid as requested by BST1 in the corresponding word of the UPM, EBDF = 1	10	25	5	16	5	16	ns
B33	CLKOUT Falling Edge to $\overline{GPL}$ valid as requested by GxT4 in the corresponding word of the UPM	1.5	10	1.5	8	1.5	8	ns
B33a	CLKOUT Rising Edge to $\overline{GPL}$ valid as requested by GxT3 in the corresponding word of the UPM	10	20	5	13	5	13	ns
B34	A(6:31) and D(0:31) to $\overline{CS}$ valid as requested by CST4 in the corresponding word of the UPM	8	—	3	—	3	—	ns
B34a	A(6:31) and D(0:31) to $\overline{CS}$ valid as requested by CST1 in the corresponding word of the UPM	18	—	8	—	8	—	ns
B34b	A(6:31) and D(0:31) to $\overline{CS}$ valid as requested by CST2 in the corresponding word of the UPM	28	—	13	—	13	—	ns
B35	A(6:31) and D(0:31) to $\overline{BS}$ valid as requested by BST4 in the corresponding word of the UPM	8	—	3	—	3	—	ns
B35a	A(6:31) and D(0:31) to $\overline{BS}$ valid as requested by BST1 in the corresponding word of the UPM	18	—	8	—	8	—	ns
B35b	A(6:31) and D(0:31) to $\overline{BS}$ valid as requested by BST2 in the corresponding word of the UPM	28	—	13	—	13	—	ns
B36	A(6:31) and D(0:31) to $\overline{GPL}$ valid as requested by GxT4 in the corresponding word of the UPM	8	—	3	—	3	—	ns
B37	UPWAIT Valid to CLKOUT Falling Edge	6	—	6	—	6	—	ns
B38	CLKOUT Falling Edge to UPWAIT Valid	1	—	1	—	1	—	ns
B39	$\overline{AS}$ Valid to CLKOUT Rising Edge	9	—	7	—	7	—	ns

Table 1. Bus Operation Timing (Continued)

NUM	CHARACTERISTIC	25MHz		40MHz		50MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
B40	A(6:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, Valid to CLKOUT Rising Edge	9	—	7	—	7	—	ns
B41	$\overline{TS}$ Valid to CLKOUT Rising Edge (Setup Time)	9	—	7	—	7	—	ns
B42	CLKOUT Rising Edge to $\overline{TS}$ Valid (Hold Time)	2	—	2	—	2	—	ns
B43	$\overline{AS}$ Negation to Memory Controller Signals Negation	—	13	—	13	—	13	ns

NOTES:

1. The timing for $\overline{BR}$ output is relevant when the MPC823 is selected to work with the external bus arbiter. The timing for $\overline{BG}$ output is relevant when the MPC823 is selected to work with the internal bus arbiter.
2. The setup times required for $\overline{TA}$, $\overline{TEA}$ and $\overline{BI}$ are relevant only when they are supplied by an external device (and not when the memory controller or the PCMCIA interface drive them).
3. The timing required for $\overline{BR}$ input is relevant when the MPC823 is selected to work with the internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC823 is selected to work with the external bus arbiter.
4. The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.
5. The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only under control of the UPM in the memory controller.
6. The timing B30 refers to $\overline{CS}$ when ACS = '00' and to $\overline{WE}$(0:3) when CSNT = '0'.
7. The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals.
8. The $\overline{AS}$ signal is considered asynchronous to the CLKOUT signal.

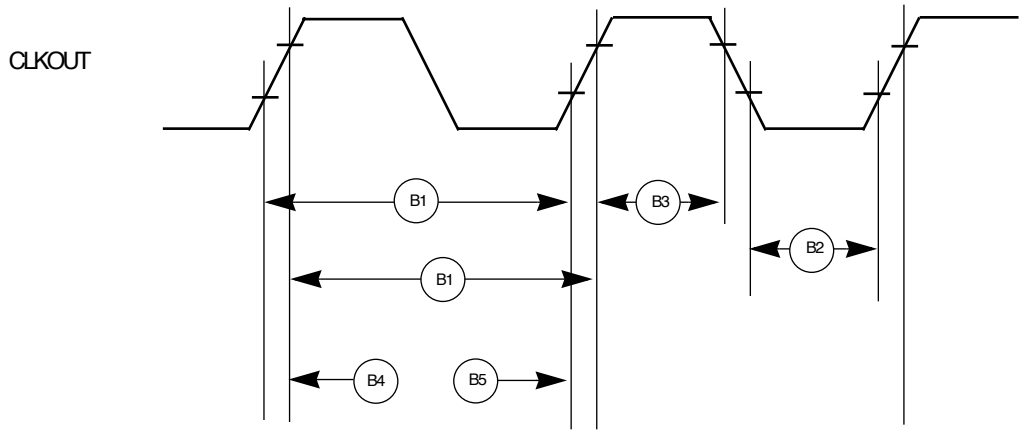


Figure 1. External Clock Timing Diagram

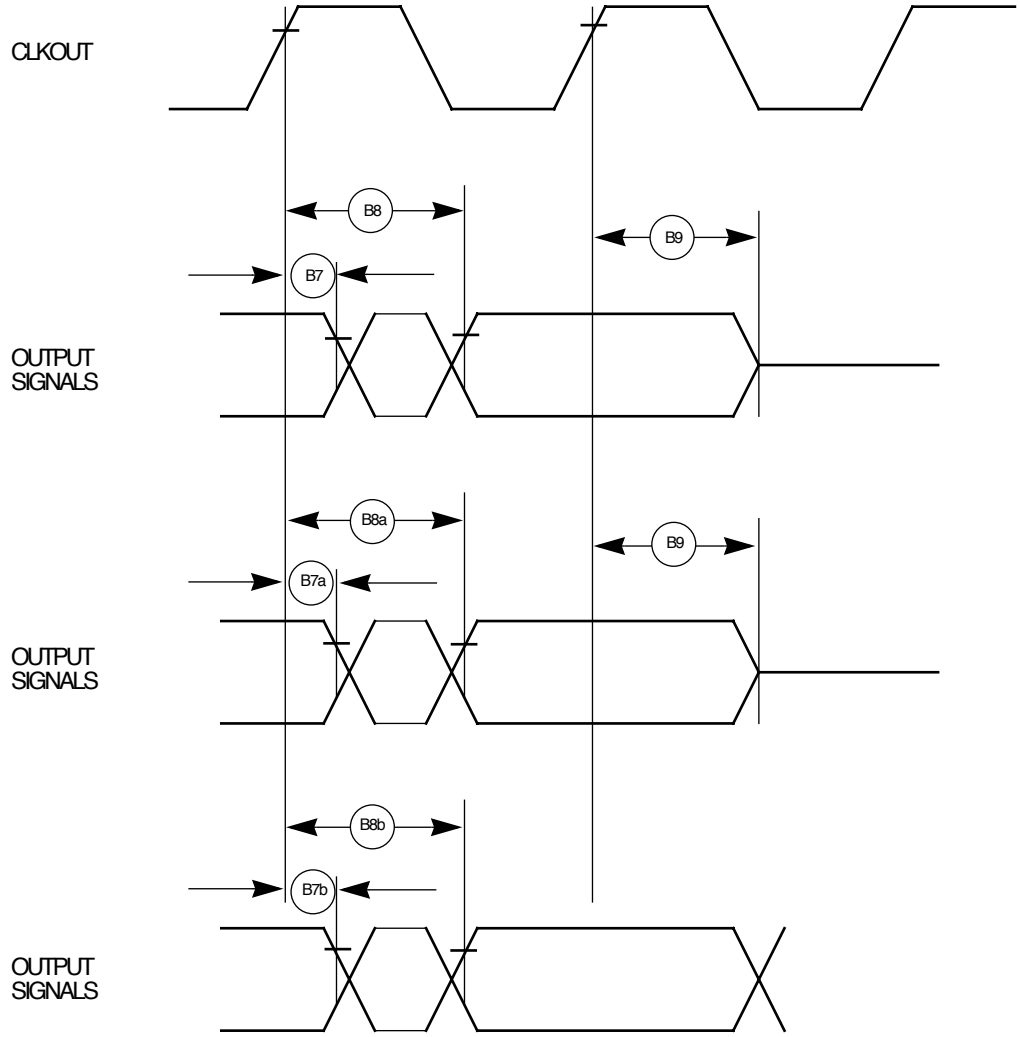


Figure 2. Synchronous Output Signals Timing Diagram

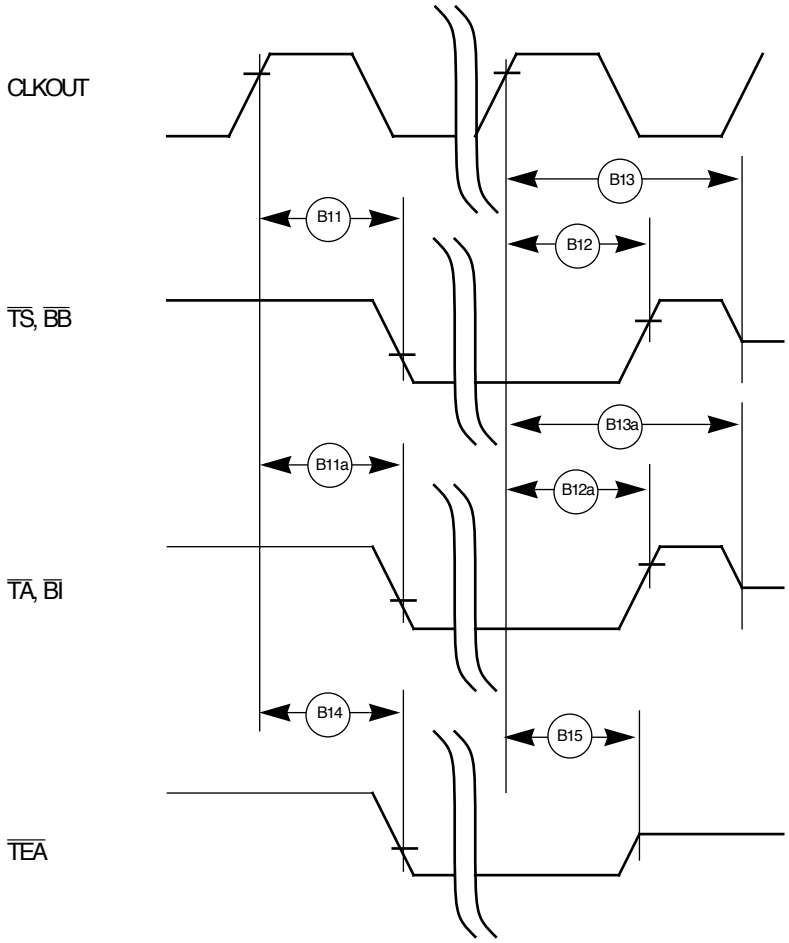


Figure 3. Synchronous Active Pull-Up and Open-Drain Outputs Signals Timing Diagram

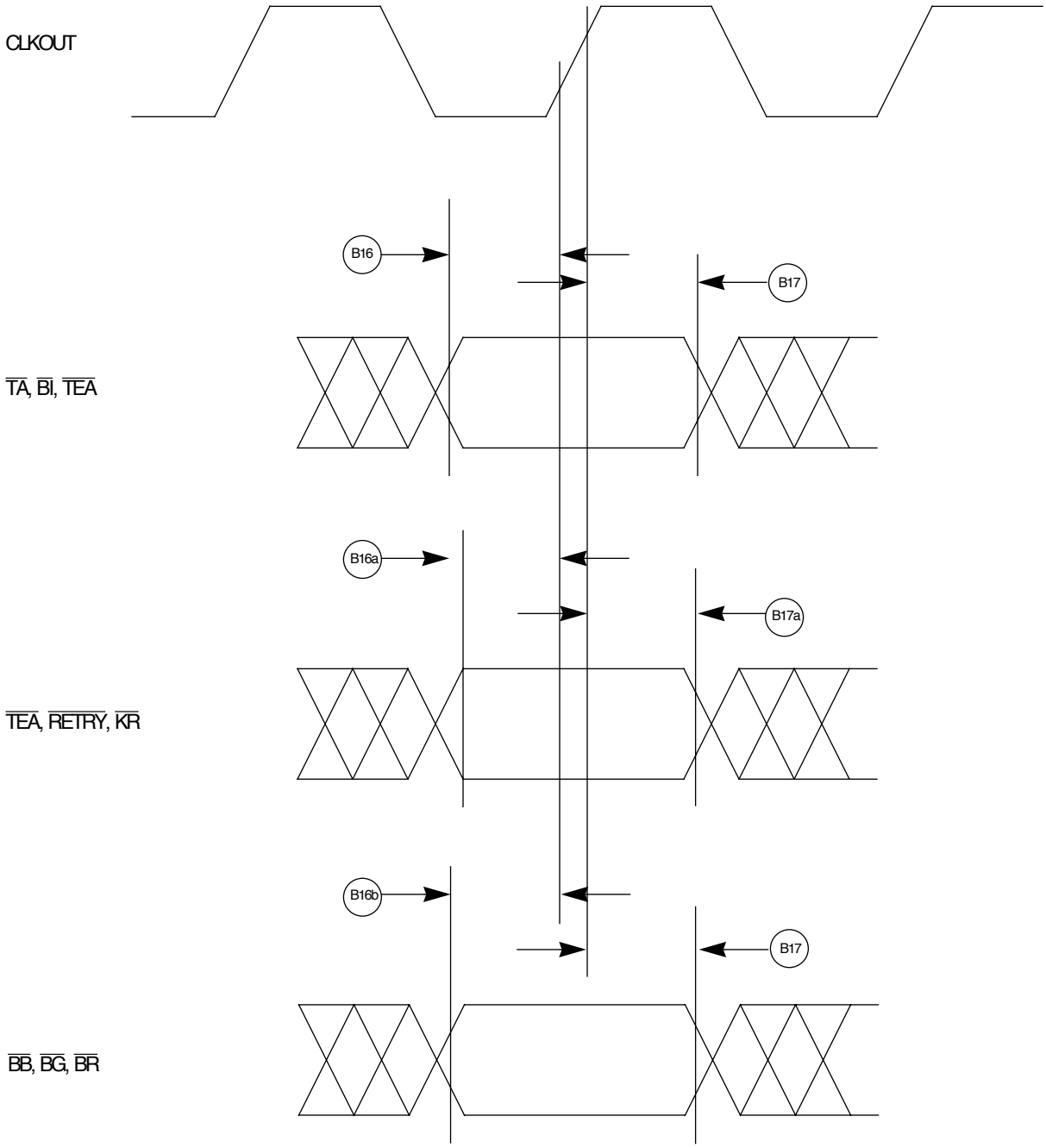


Figure 4. Synchronous Input Signals Timing Diagram

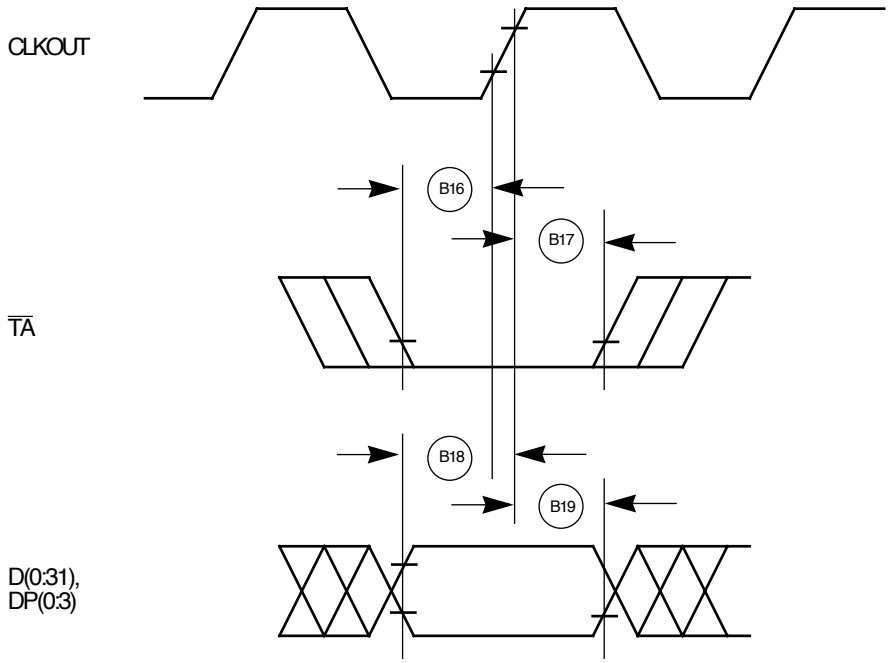


Figure 5. Input Data In Normal Case Timing Diagram

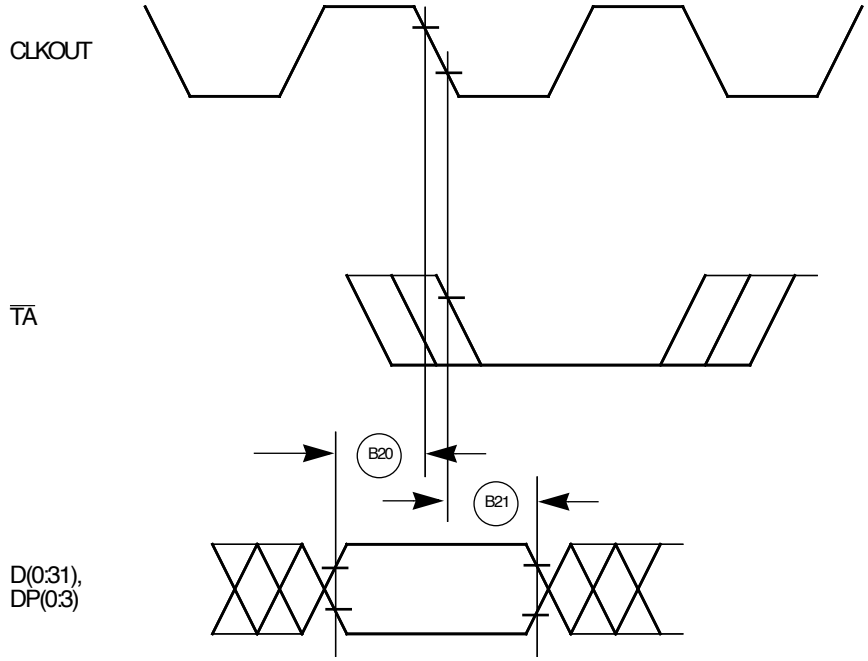


Figure 6. Input Data When Controlled by the UPM Timing Diagram

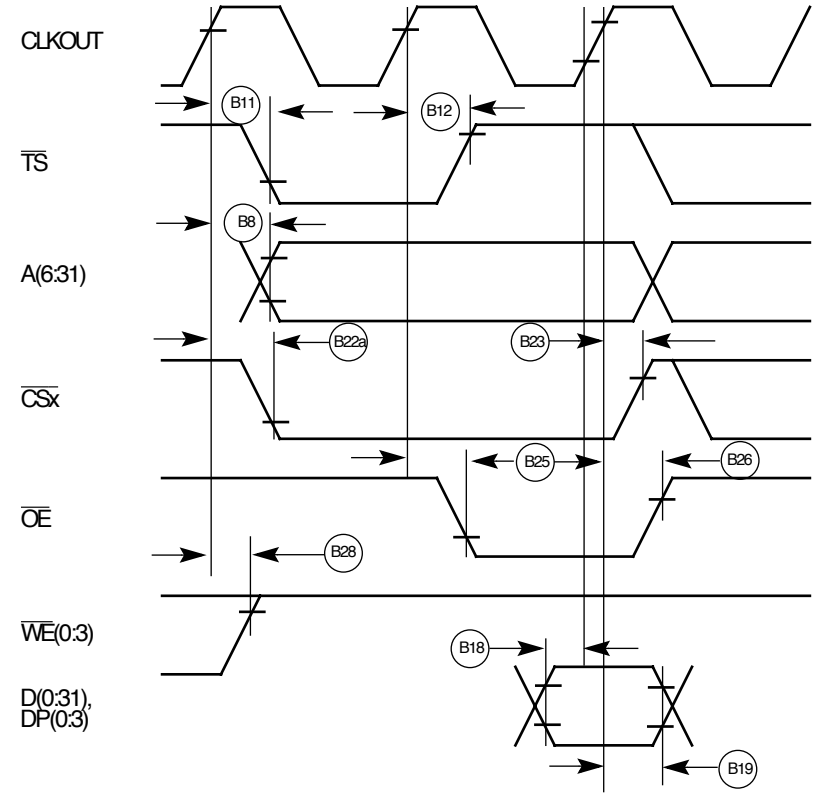


Figure 7. External Bus Read Timing Diagram (GPCM Controlled–ACS = ‘00’)

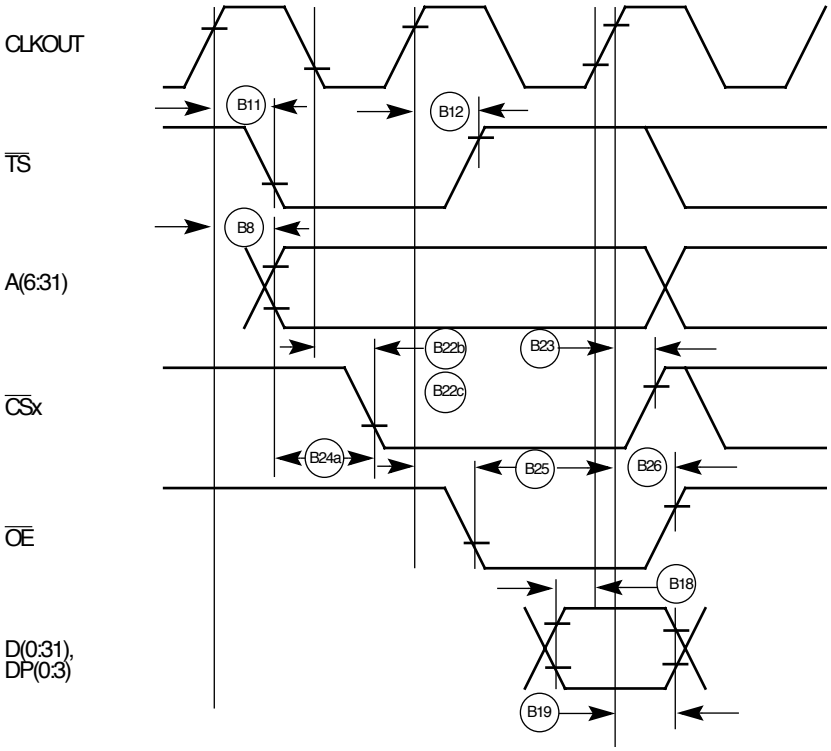


Figure 8. External Bus Read Timing Diagram (GPCM Controlled–TRLX = ‘0’, ACS = ‘10’)

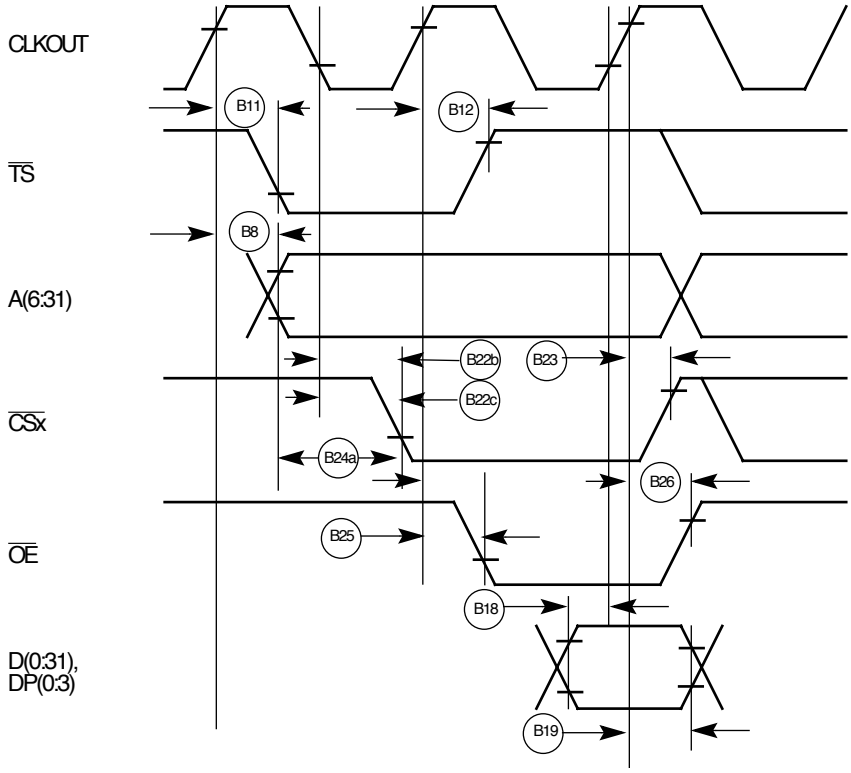


Figure 9. External Bus Read Timing Diagram (GPCM Controlled–TRLX = '0', ACS = '11')

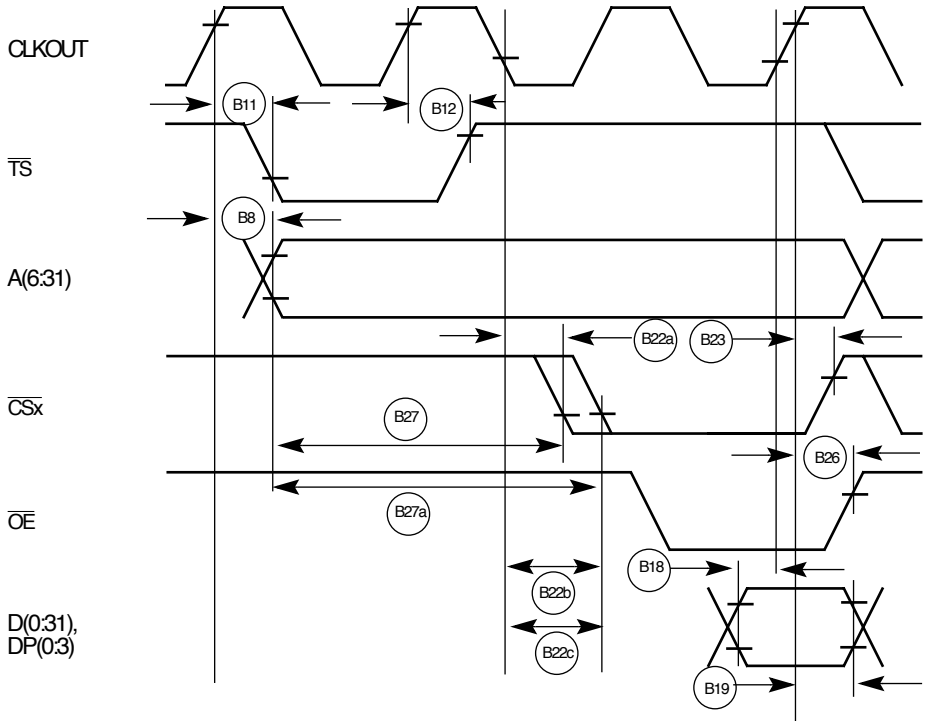


Figure 10. External Bus Read Timing Diagram (GPCM Controlled–TRLX = ‘1’, ACS = ‘10’, ACS = ‘11’)

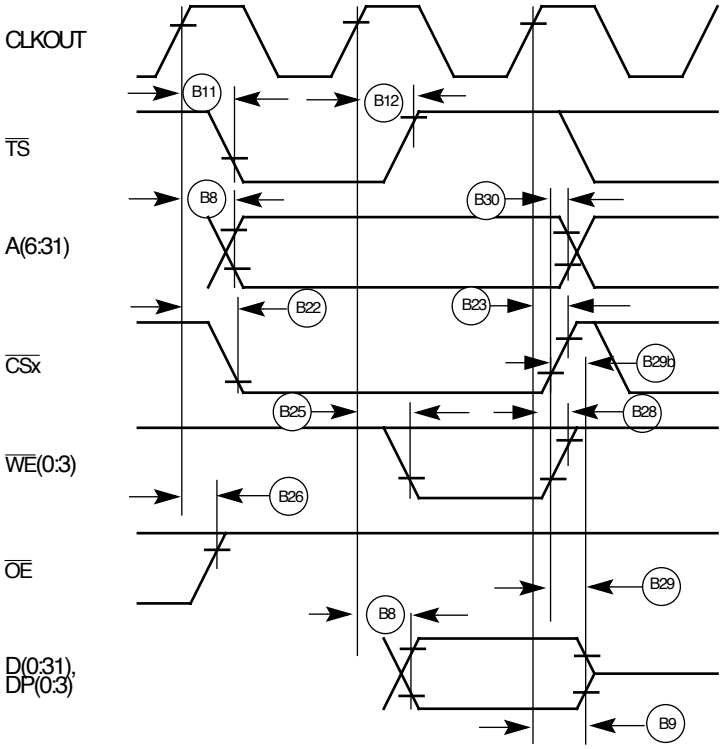


Figure 11. External Bus Write Timing Diagram (GPCM Controlled–TRLX = ‘0’, CSNT = ‘0’)

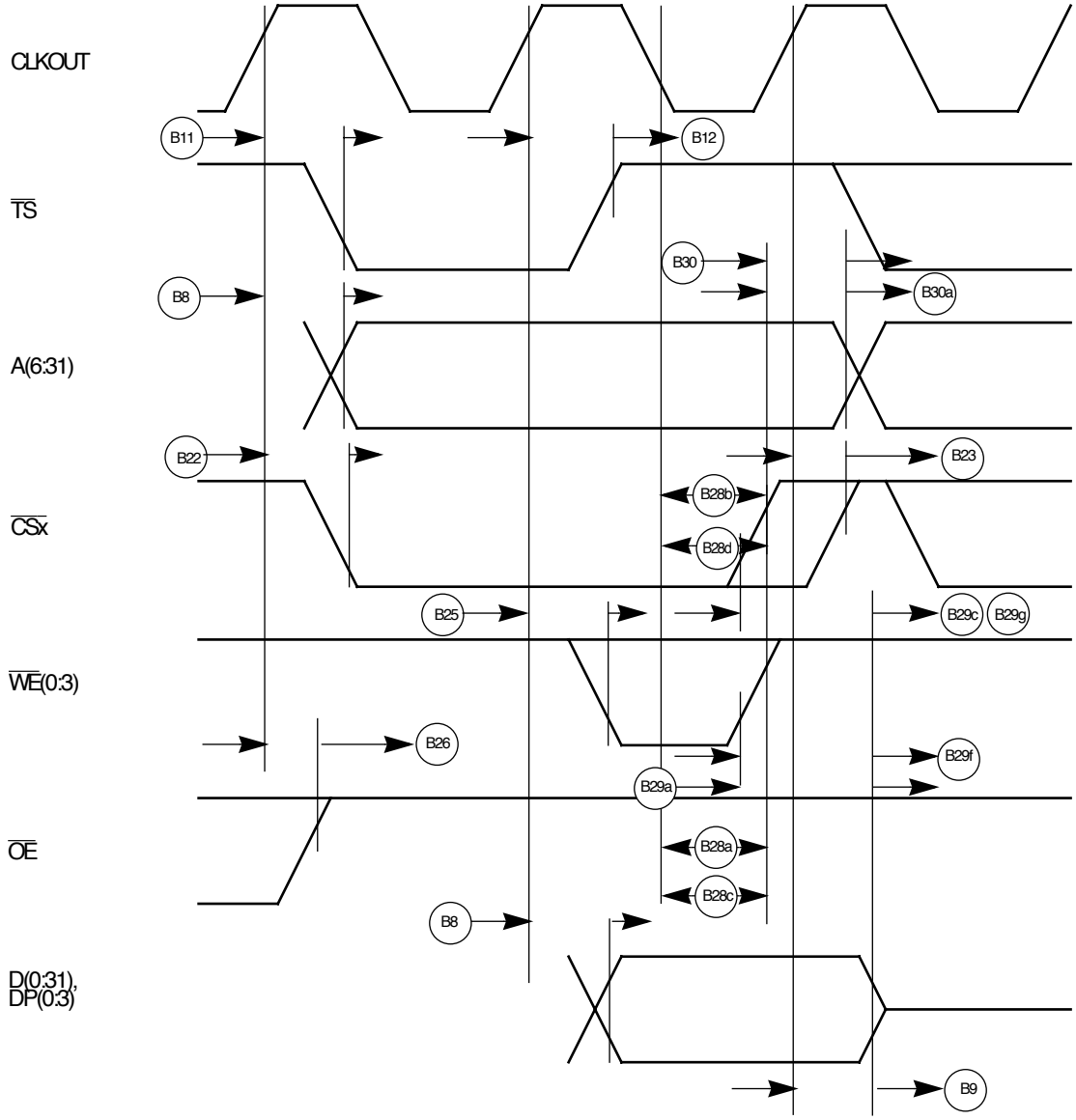


Figure 12. External Bus Write Timing Diagram (GPCM Controlled–TRLX = '0', CSNT = '1')

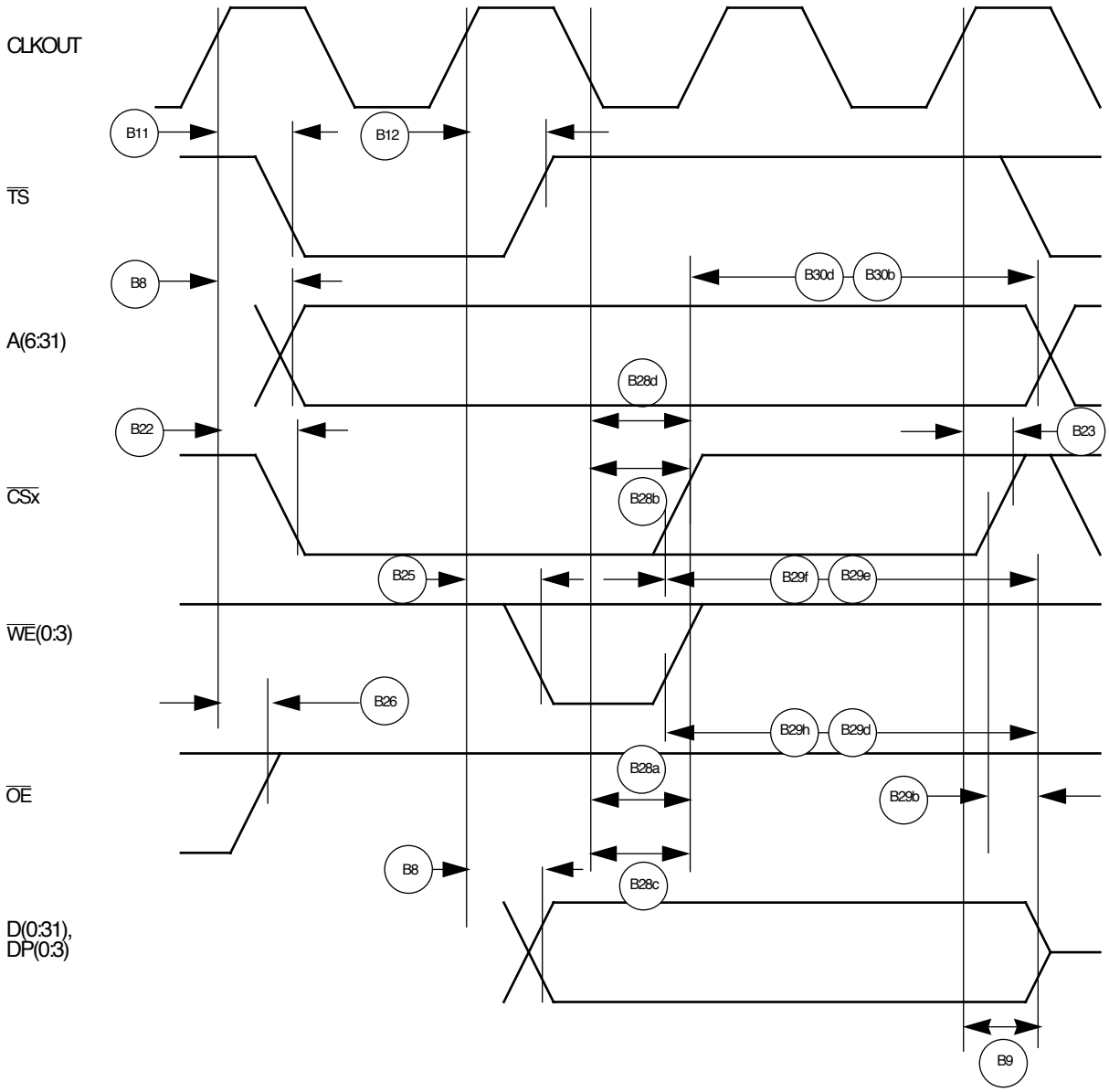


Figure 13. External Bus Write Timing Diagram (GPCM Controlled–TRLX = '1', CSNT = '1')

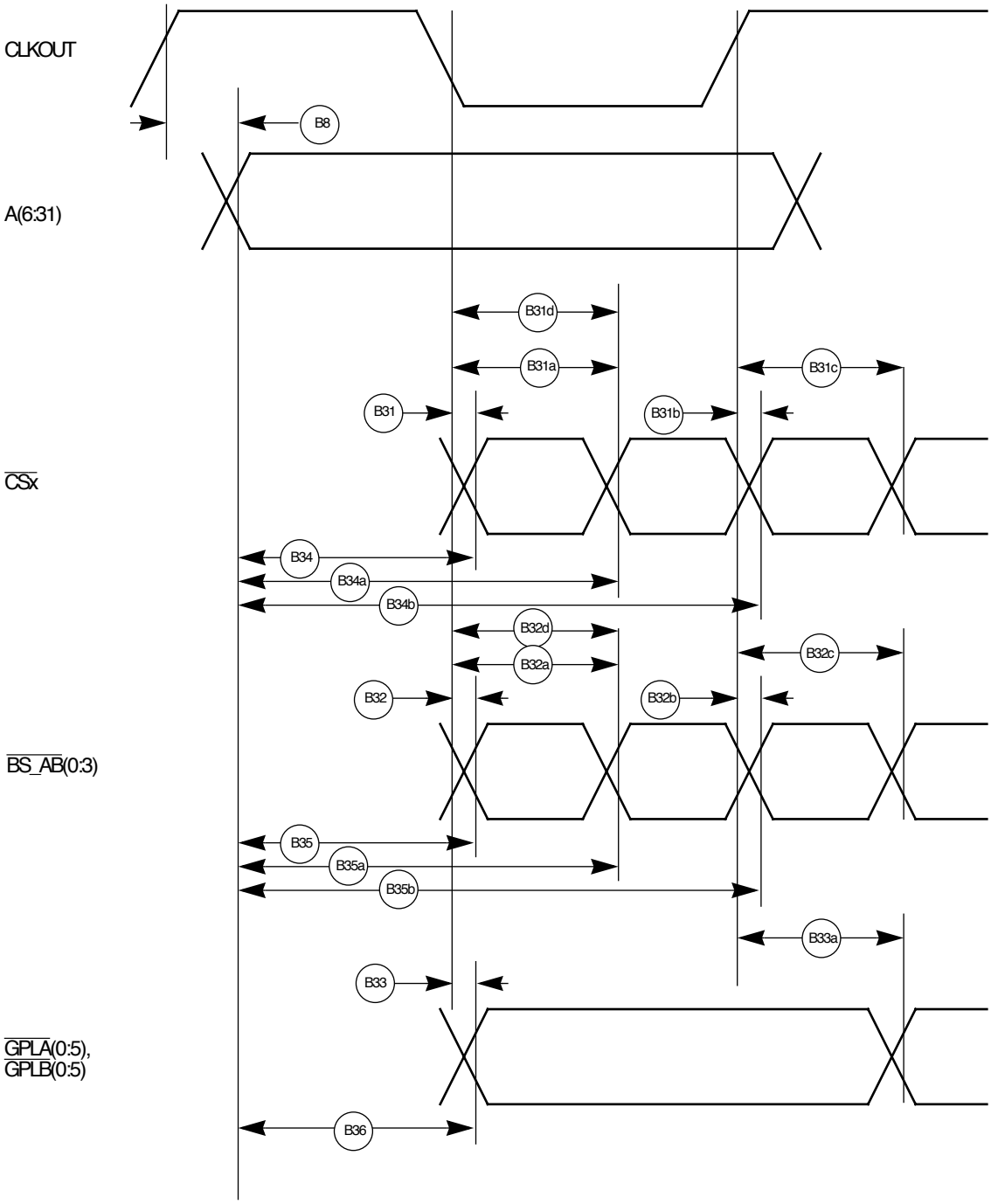


Figure 14. External Bus Timing Diagram (UPM-Controlled Signals)

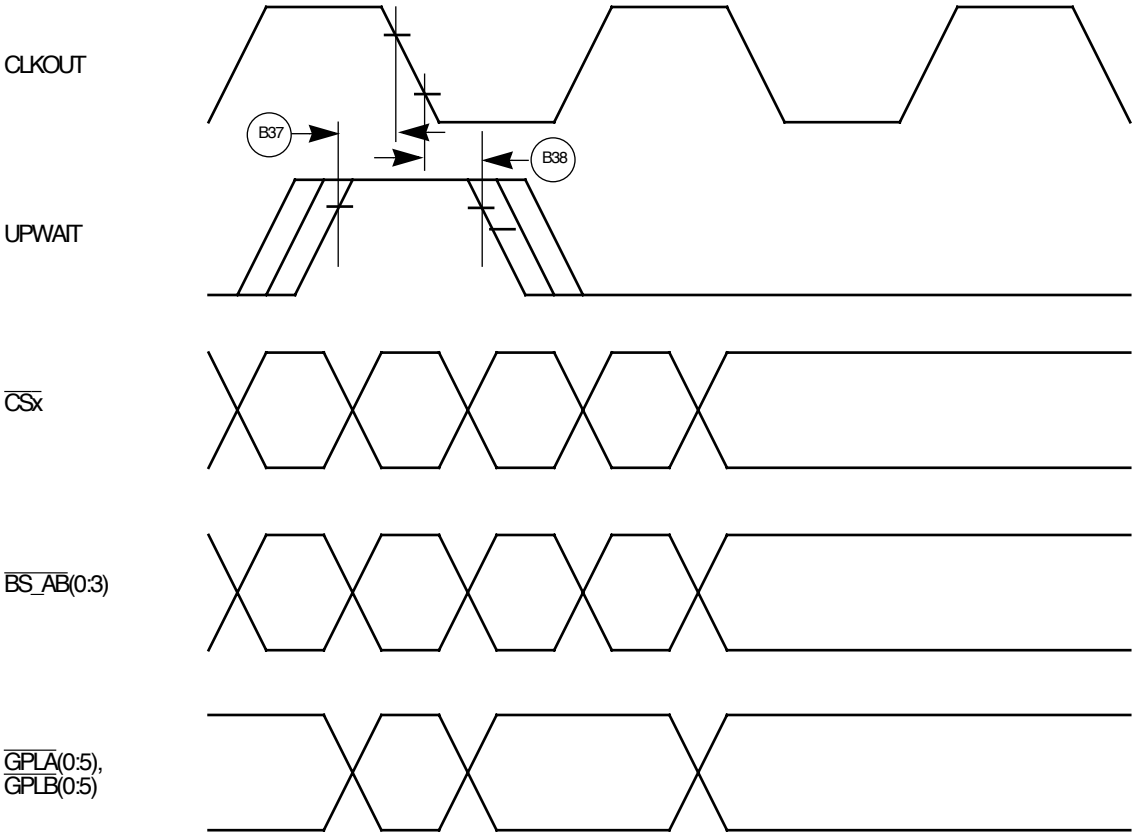


Figure 15. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing Diagram

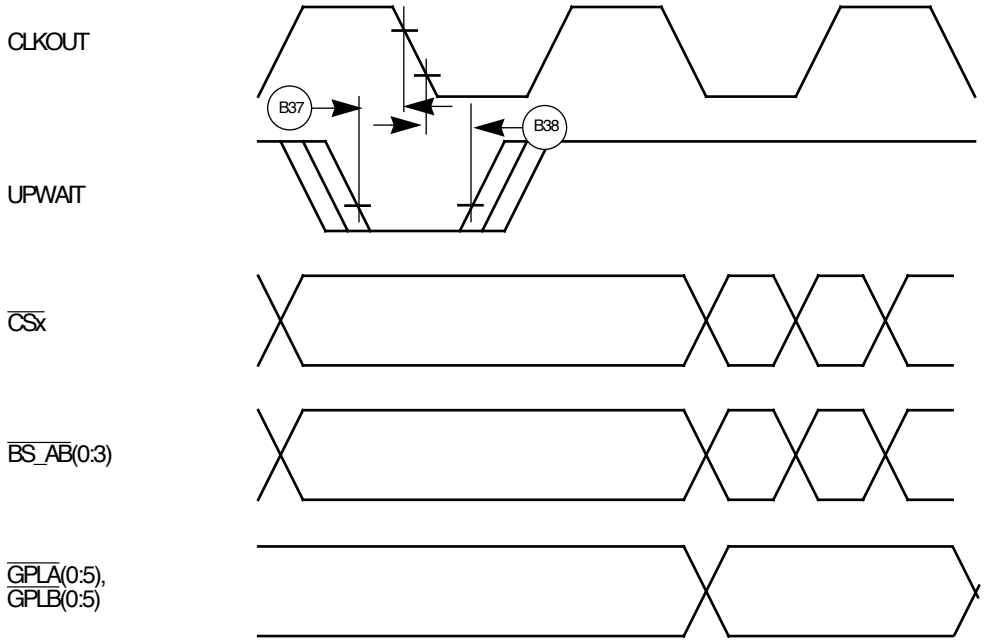


Figure 16. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing Diagram

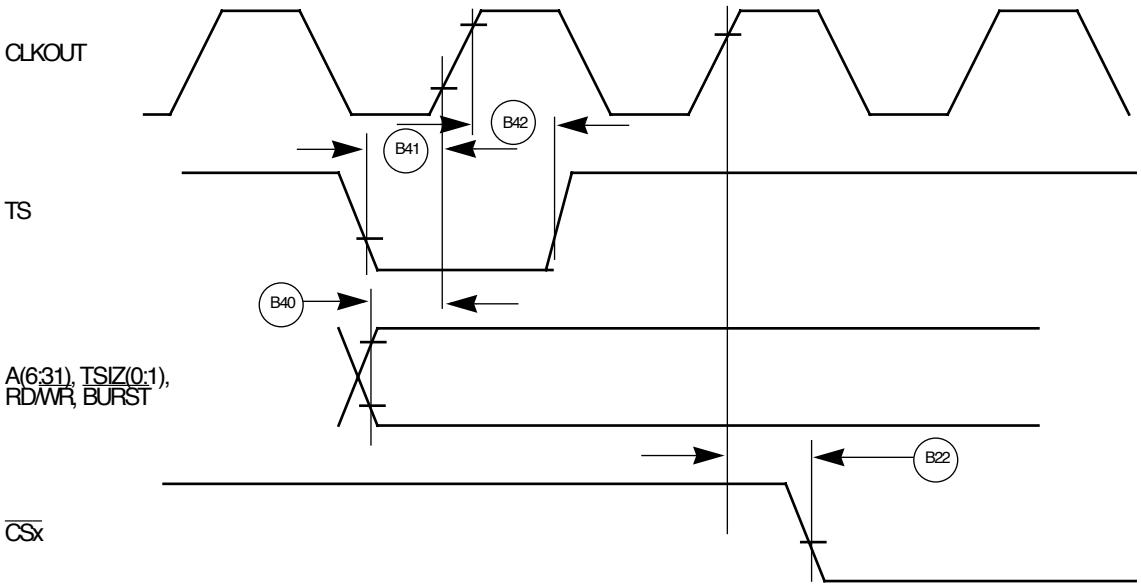


Figure 17. Synchronous External Master Access Timing Diagram (GPCM Handled–ACS = '00')

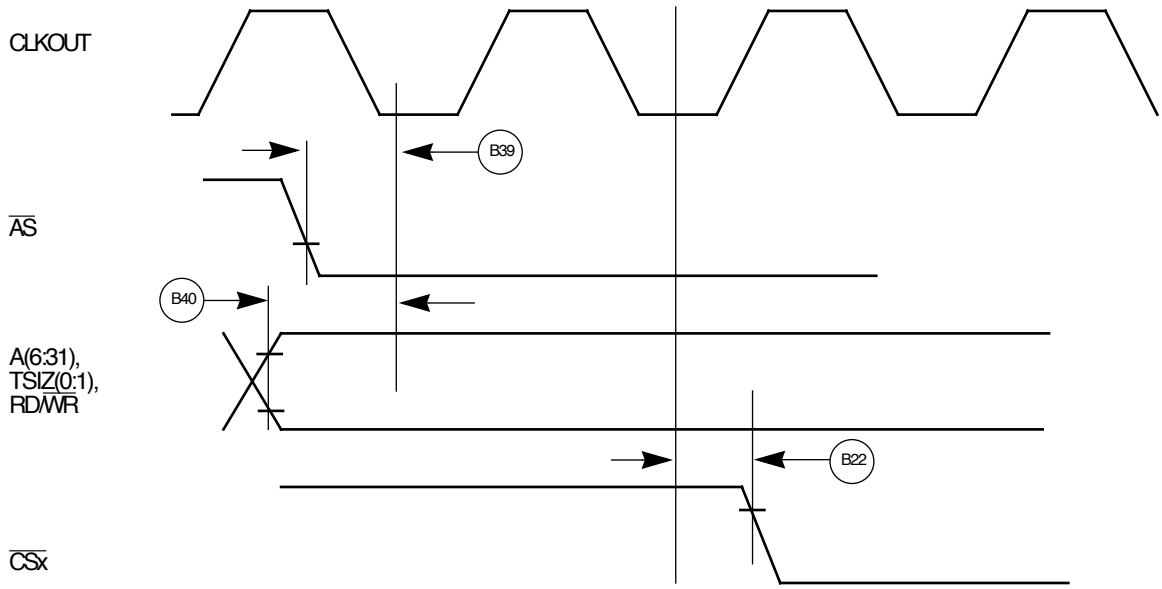


Figure 18. Asynchronous External Master Memory Access Timing Diagram (GPCM Controlled–ACS = ’00’)

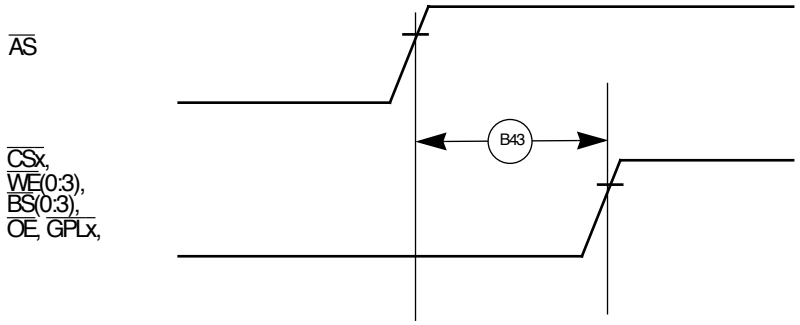


Figure 19. Asynchronous External Master Timing Diagram (Control Signals Negation Time)

Table 2. Interrupt Timing

NUM	CHARACTERISTIC	25MHZ		40MHZ		50MHZ		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
I39	$\overline{\text{IRQ}}$x valid to CLKOUT rising edge (setup time)	6	—	6/6	—	6/6	—	ns
I40	$\overline{\text{IRQ}}$x hold time after CLKOUT	2	—	2/2	—	2/2	—	ns
I41	$\overline{\text{IRQ}}$x pulse width low	3	—	3/3	—	3/3	—	ns
I42	$\overline{\text{IRQ}}$x pulse width high	3	—	3/3	—	3/3	—	ns
I43	$\overline{\text{IRQ}}$x edge to edge time	160	—	80/80	—	80/80	—	ns

NOTES:

1. The timings I39 and I40 describe the testing conditions under which the $\overline{\text{IRQ}}$ lines are tested when defined as level sensitive. The $\overline{\text{IRQ}}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.
2. The timings I41 and I42 are specified to allow the correct function of the $\overline{\text{IRQ}}$ lines detection circuitry, and has no direct relation with the total system interrupt latency that the MPC823 can support.

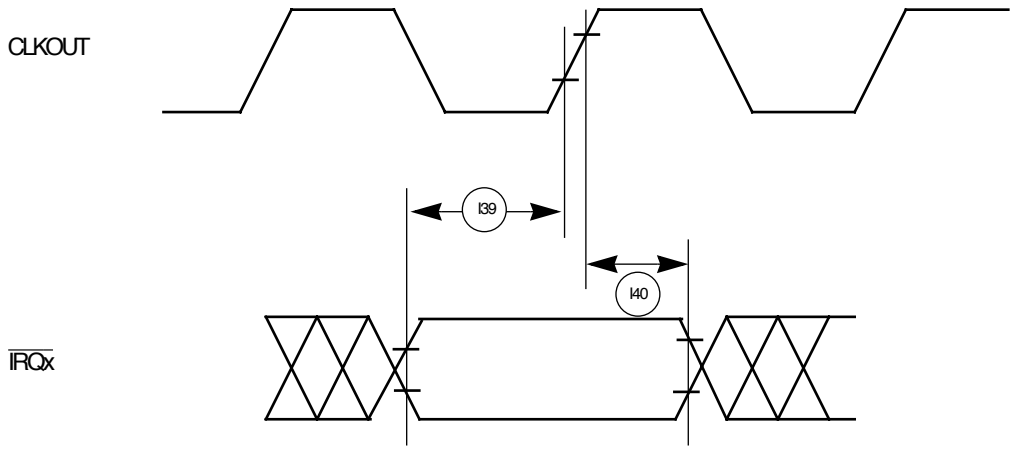


Figure 20. Interrupt Detection Timing Diagram for External Level-Sensitive Lines

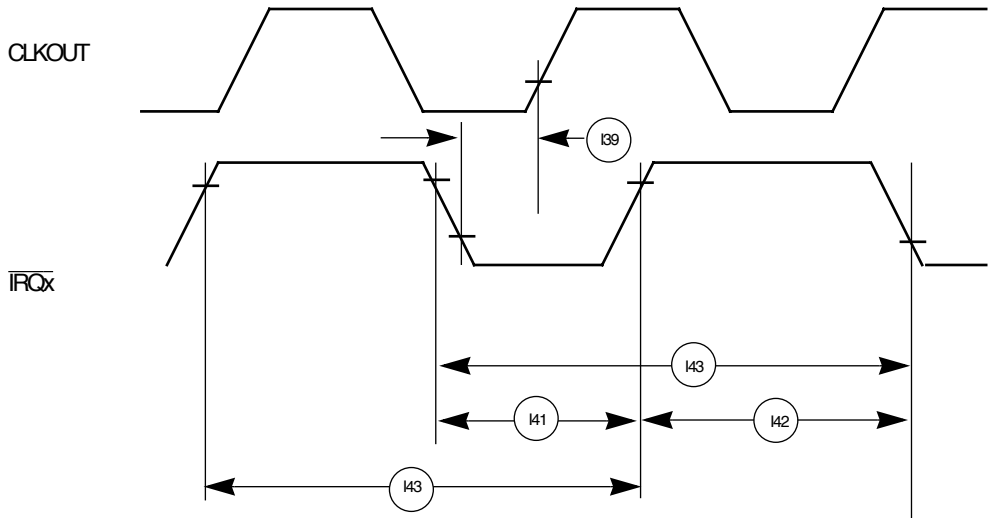


Figure 21. Interrupt Detection Timing Diagram for External Edge-Sensitive Lines

Table 3. PCMCIA Timing

NUM	CHARACTERISTIC	25MHZ		40MHZ		50MHZ		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
P44	A(6:31), $\overline{\text{REG}}$ valid to PCMCIA strobe asserted	28	—	13	—	13	—	ns
P45	A(6:31), $\overline{\text{REG}}$ valid to ALE negation	38	—	18	—	18	—	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid	10	19	5	13	5	13	ns
P47	CLKOUT to $\overline{\text{REG}}$ invalid	11	—	6	—	6	—	ns
P48	CLKOUT to $\overline{\text{CE}}$1, $\overline{\text{CE}}$2 asserted	10	19	5	13	5	13	ns
P49	CLKOUT to $\overline{\text{CE}}$1, $\overline{\text{CE}}$2 negated	10	19	5	13	5	13	ns
P50	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time	—	12	—	11	—	11	ns
P51	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time	3	12	2	11	2	11	ns
P52	CLKOUT to ALE assert time	10	19	5	13	5	13	ns
P53	CLKOUT to ALE negate time	—	19	—	13	—	13	ns
P54	$\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D(0:31) invalid	8	—	3	—	3	—	ns
P55	$\overline{\text{WAIT\_B}}$ valid to CLKOUT rising edge	8	—	8	—	8	—	ns
P56	CLKOUT rising edge to $\overline{\text{WAIT\_B}}$ invalid	2	—	2	—	2	—	ns

NOTES:

1. PSST = 1. Otherwise, add PSST times cycle time.
2. PSHT = 0. Otherwise, add PSHT times cycle time.
3. These synchronous timings define when the $\overline{\text{WAIT\_B}}$ signal is detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAIT\_B}}$ assertion will be effective only if it is detected two cycles before the PSL timer expiration.

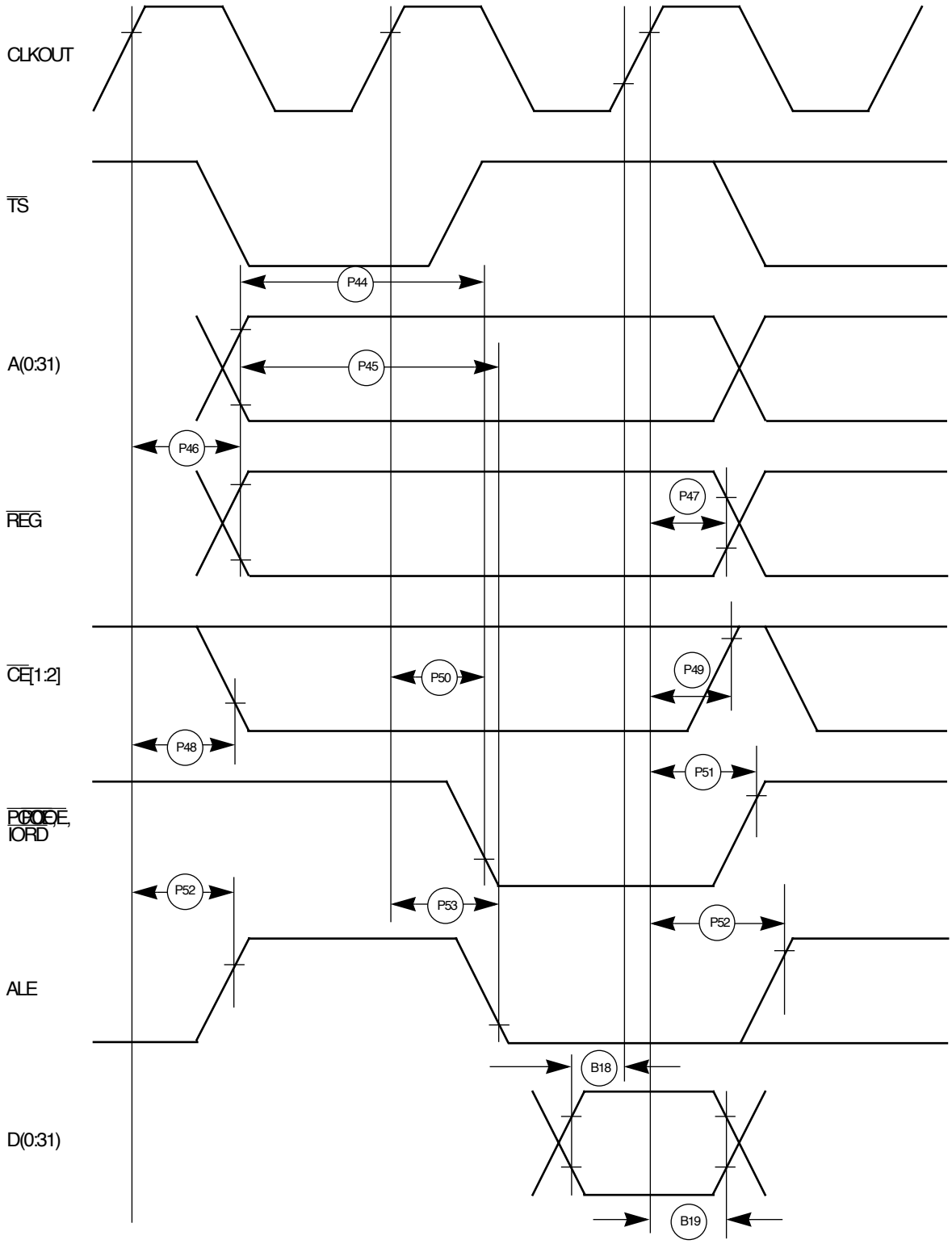


Figure 22. PCMCIA Access Cycles Timing Diagram (External Bus Read)

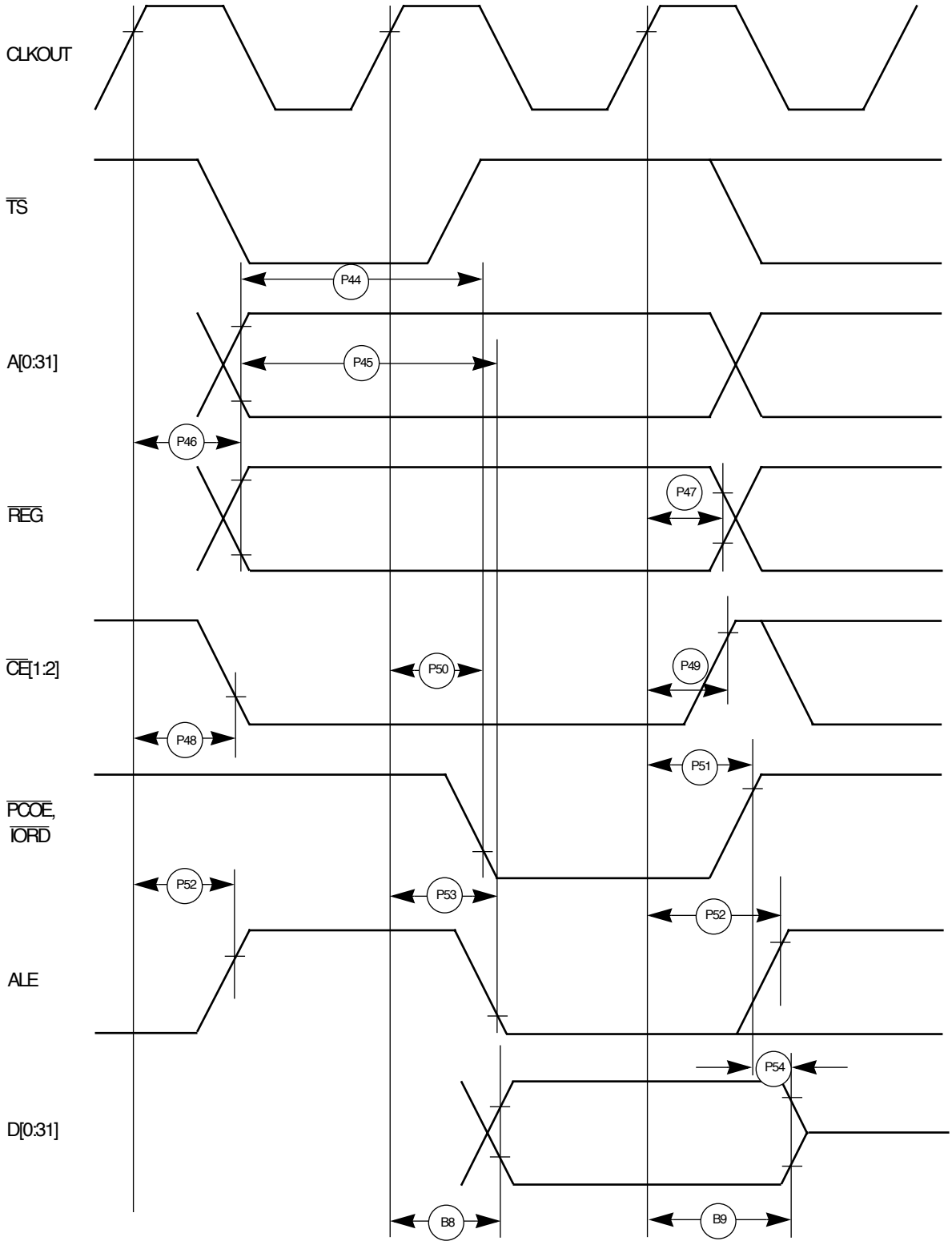


Figure 23. PCMCIA Access Cycles Timing Diagram (External Bus Write)

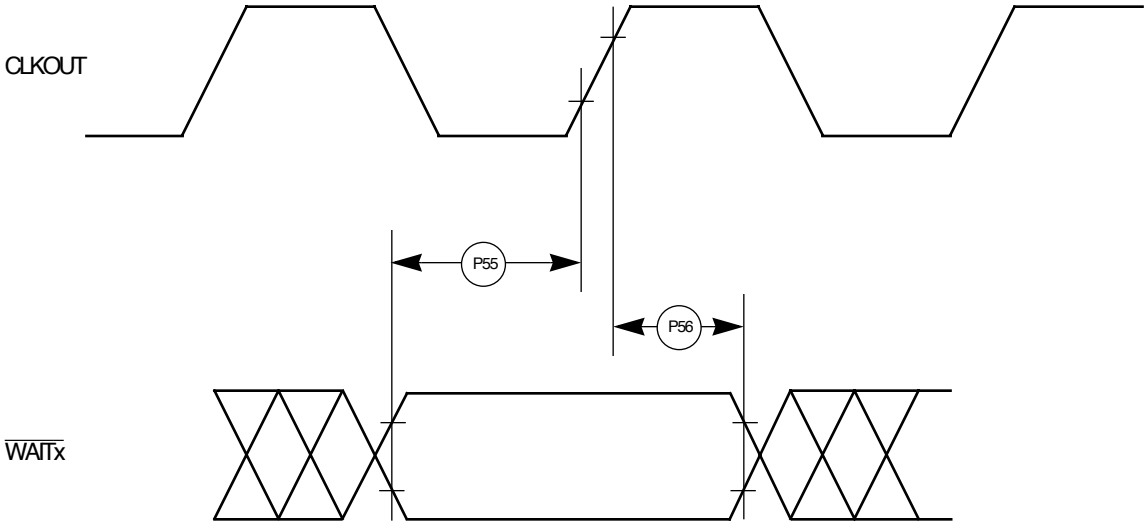


Figure 24. PCMCIA Wait Signals Detection Timing Diagram

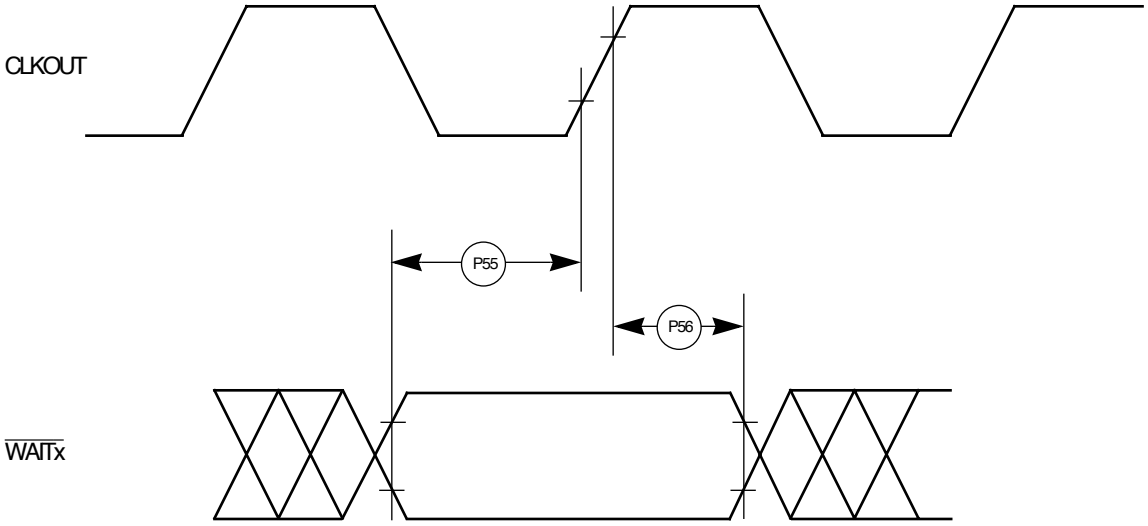


Figure 25. PCMCIA Wait Signals Detection Timing Diagram

Table 4. PCMCIA Port Timing

NUM	CHARACTERISTIC	25MHZ		40MHZ		50MHZ		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
P57	CLKOUT to OPx Valid	—	25	—	19	—	19	ns
P58	HRESET negated to OPx drive	30	—	18	—	18	—	ns
P59	IP_Bx valid to CLKOUT Rising Edge	6	—	5	—	5	—	ns
P60	CLKOUT Rising Edge to IP_Bx invalid	2	—	1	—	1	—	ns

NOTE: *OP2 and OP3 only.

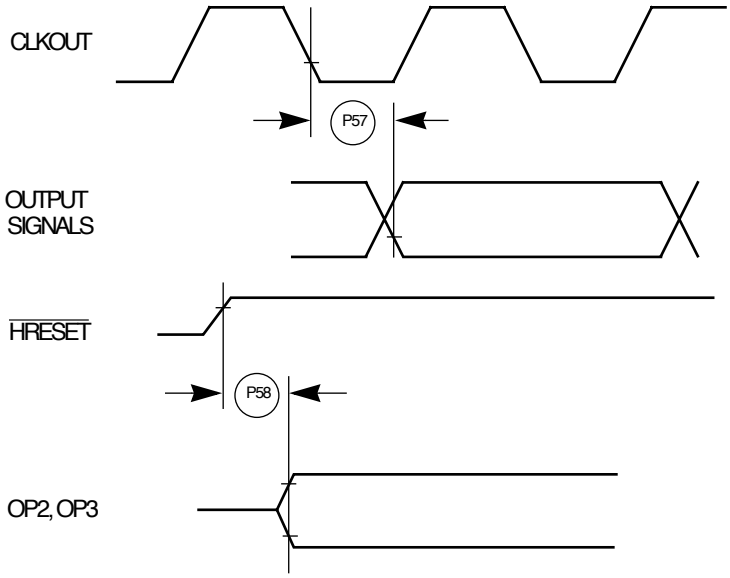


Figure 26. PCMCIA Output Port Timing Diagram

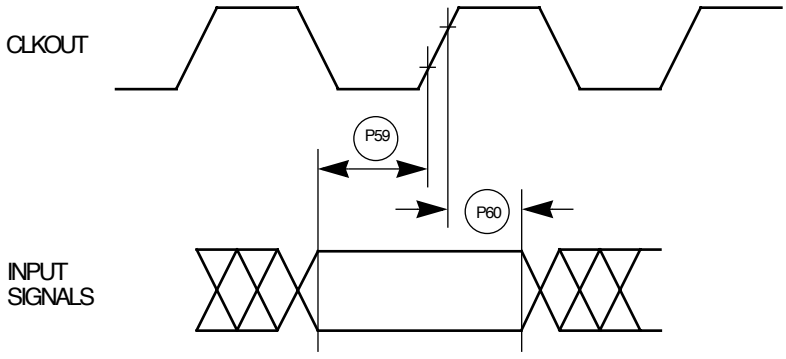


Figure 27. PCMCIA Input Port Timing Diagram

Table 5. Debug Port Timing

NUM	CHARACTERISTIC	25MHZ		40MHZ		50MHZ		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
D61	DSCK cycle time	120	—	60	—	60	—	ns
D62	DSCK clock pulse width	50	—	25	—	25	—	ns
D63	DSCK rise and fall times	0	3	0	3	0	3	ns
D64	DSDI input data setup time	8	—	8	—	8	—	ns
D65	DSDI data hold time	5	—	5	—	5	—	ns
D66	DSCK low to DSDO data valid	0	15	0	15	0	15	ns
D67	DSCK low to DSDO invalid	0	2	0	2	0	2	ns

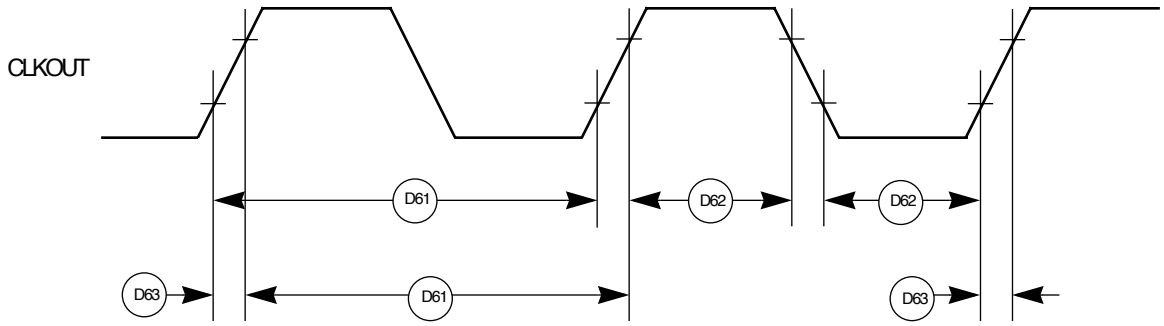


Figure 28. Debug Port Clock Input Timing Diagram

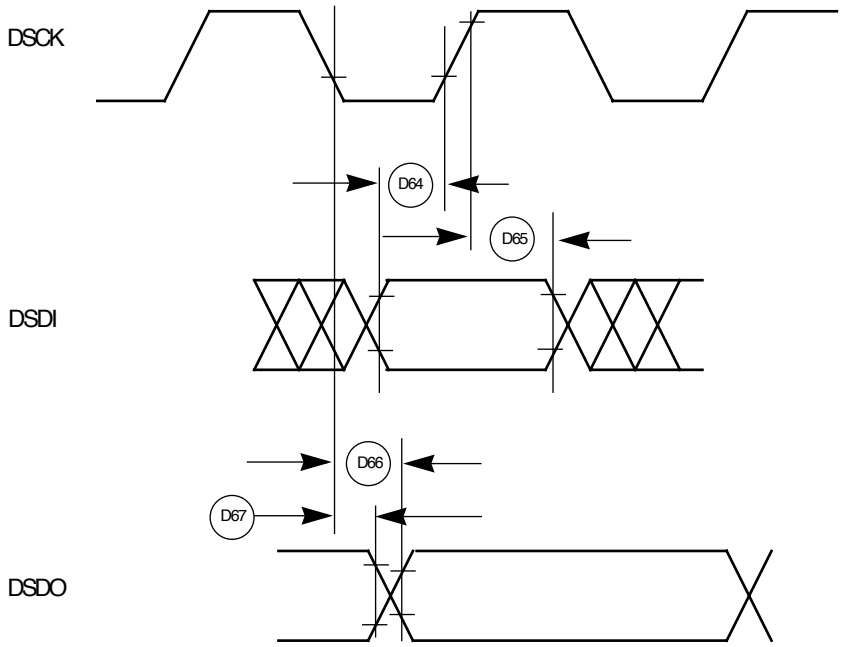


Figure 29. Debug Port Timing Diagram

Table 6. Reset Timing

NUM	CHARACTERISTIC	25MHZ		40MHZ		50MHZ		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
R68	CLKOUT to $\overline{\text{HRESET}}$ high impedance	—	20	—	20	—	20	ns
R69	CLKOUT to $\overline{\text{SRESET}}$ high impedance	—	20	—	20	—	20	ns
R70	$\overline{\text{RSTCONF}}$ pulse width	680	—	425	—	340	—	ns
R71	N/A							
R72	Configuration data to $\overline{\text{HRESET}}$ rising edge setup time	650	—	425	—	350	—	ns
R73	Configuration data to $\overline{\text{RSTCONF}}$ rising edge setup time	650	—	425	—	350	—	ns
R74	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation	0	—	0	—	0	—	ns
R75	Configuration data hold time after $\overline{\text{HRESET}}$ negation	0	—	0	—	0	—	ns
R76	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive	—	25	—	25	—	25	ns
R77	$\overline{\text{RSTCONF}}$ negated to data out high impedance	—	25	—	25	—	25	ns
R78	CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance	—	25	—	25	—	25	ns
R79	DSDI and DSCK setup	120	—	75	—	60	—	ns
R80	DSDI and DSCK hold time	0	—	0	—	0	—	ns
R81	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample	320	—	200	—	160	—	ns

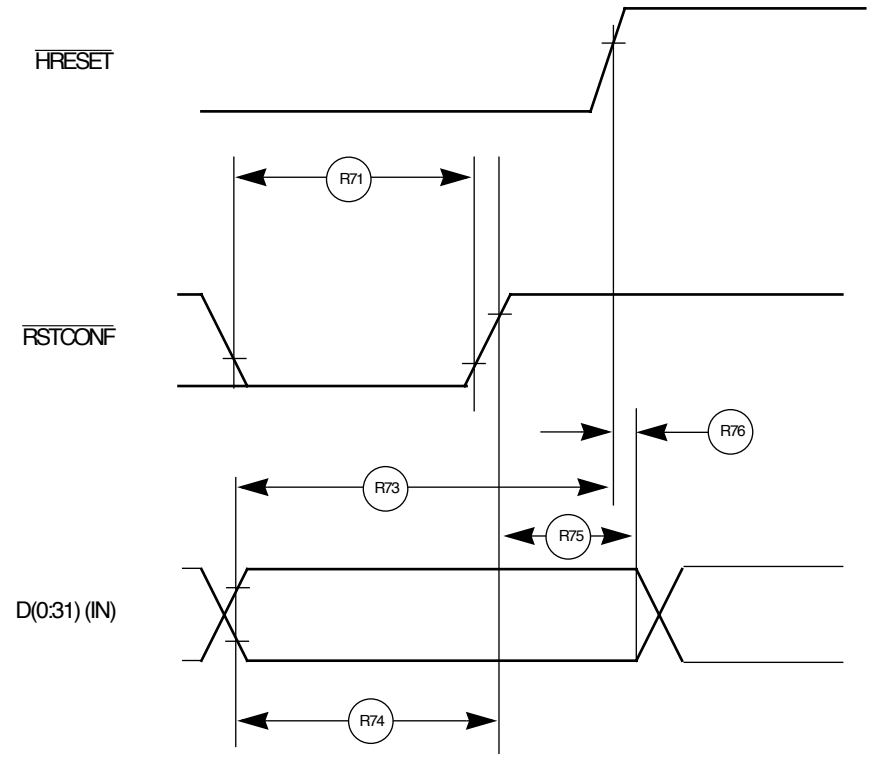


Figure 30. Reset Timing Diagram (Configuration from Data Bus)

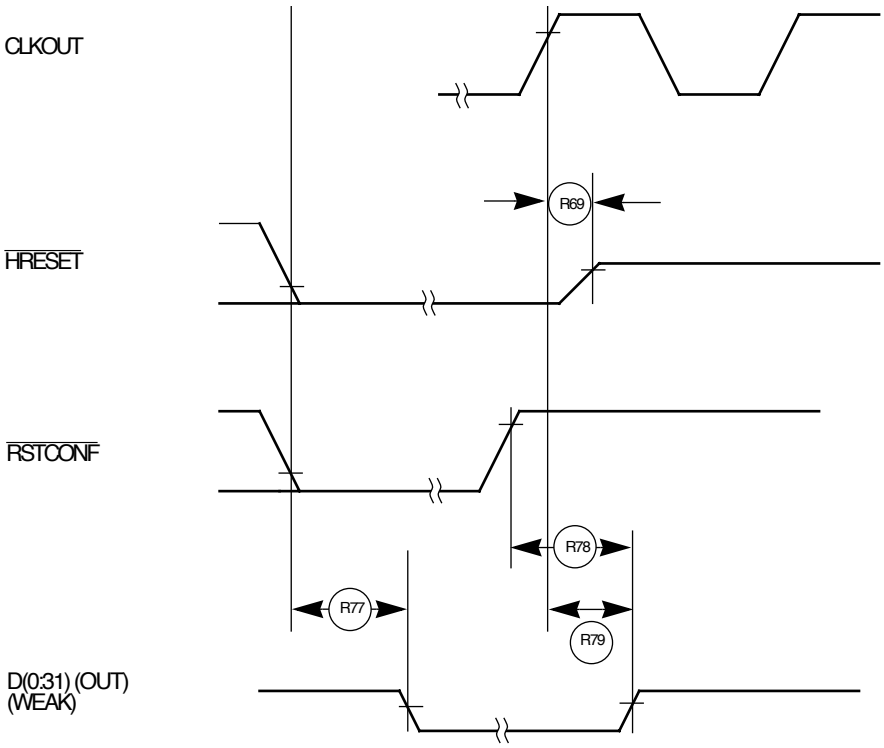


Figure 31. Reset Timing Diagram–MPC823 Data Bus Weak Drive During Configuration

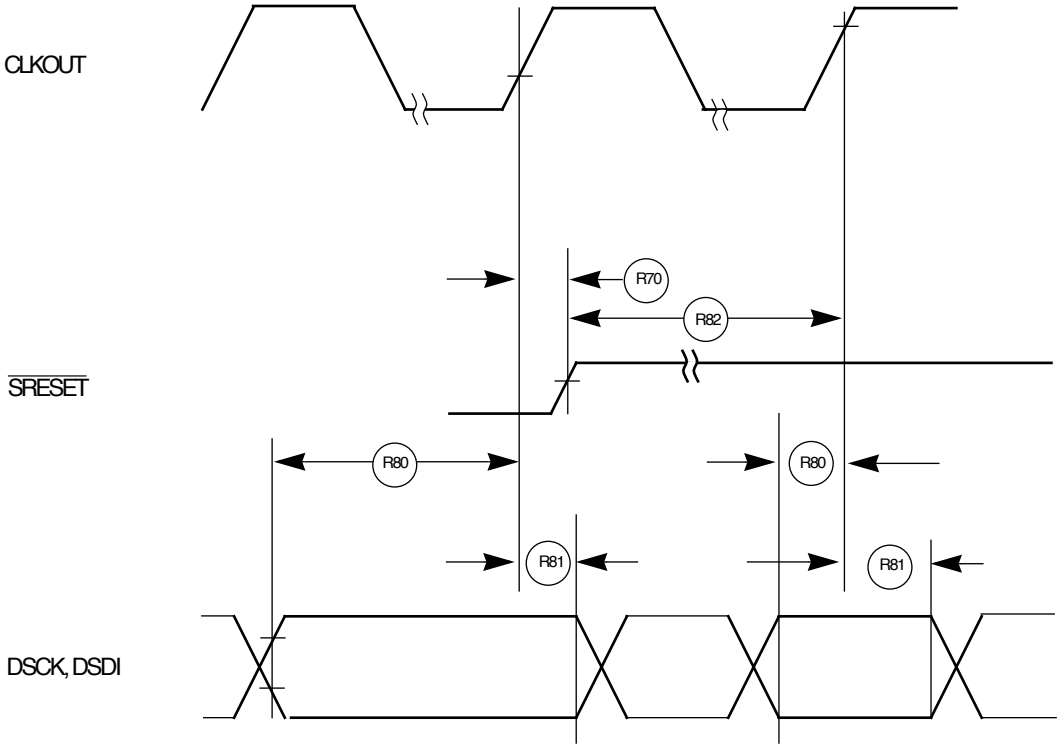


Figure 32. Reset Timing Diagram–Debug Port Configuration

Table 7. JTAG Timing

NUM	CHARACTERISTIC	25MHZ		40MHZ		50MHZ		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
J82	TCK cycle time	100	—	100	—	100	—	ns
J83	TCK clock pulse width measured at 1.5V	40	—	40	—	40	—	ns
J84	TCK rise and fall times	0	10	0	10	0	10	ns
J85	TMS, TDI data setup time	5	—	5	—	5	—	ns
J86	TMS, TDI data hold time	25	—	25	—	25	—	ns
J87	TCK low to TDO data valid	—	27	—	27	—	27	ns
J88	TCK low to TDO data invalid	0	—	0	—	0	—	ns
J89	TCK low to TDO high impedance	—	20	—	20	—	20	ns
J90	$\overline{\text{TRST}}$ assert time	100	—	100	—	100	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40	—	40	—	40	—	ns
J92	TCK falling edge to output valid	—	50	—	50	—	50	ns
J93	TCK falling edge to ouput valid out of high impedance	—	50	—	50	—	50	ns
J94	TCK falling edge to output high impedance	—	50	—	50	—	50	ns
J95	Boundary scan input valid to TCK rising edge	50	—	50	—	50	—	ns
J96	TCK rising edge to boundary scan input invalid	50	—	50	—	50	—	ns

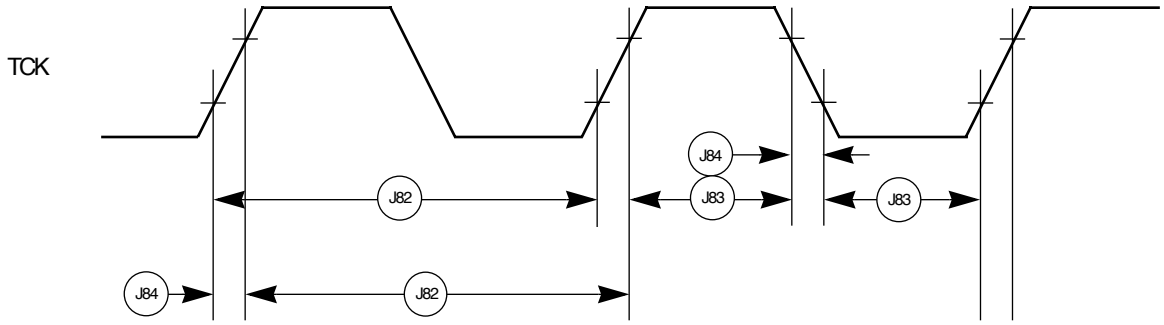


Figure 33. JTAG Test Clock Input Timing Diagram

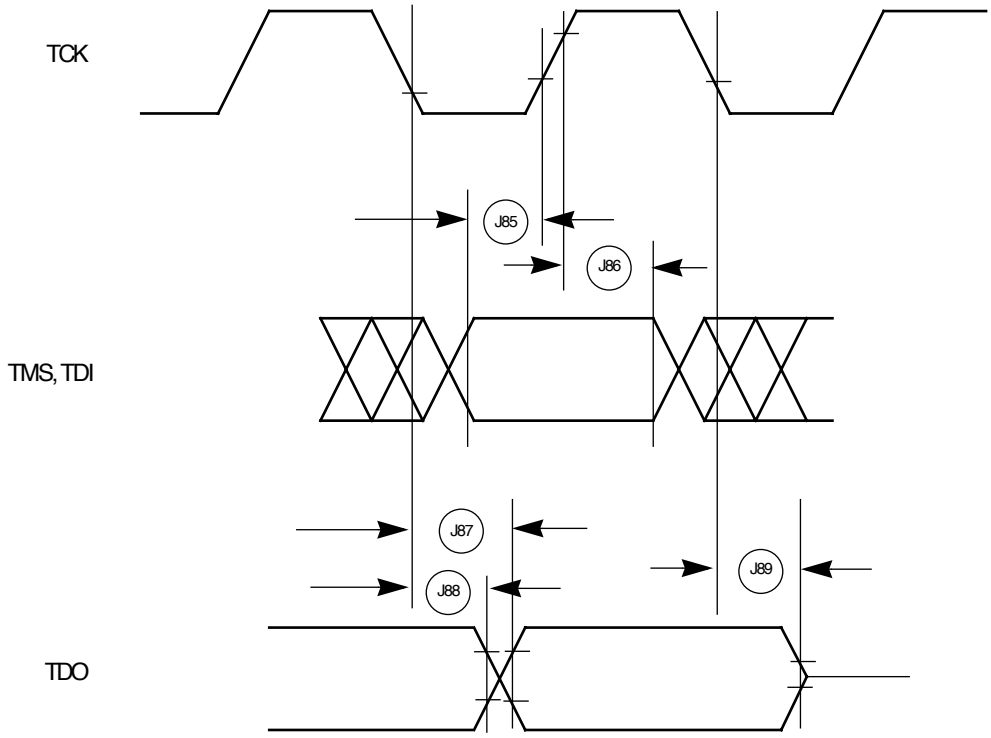


Figure 34. JTAG–Test Access Port Timing Diagram

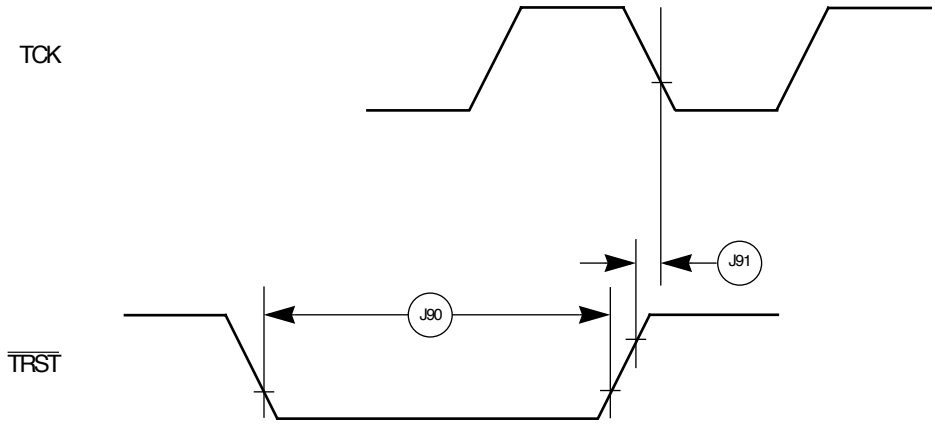


Figure 35. JTAG–$\overline{\text{TRST}}$ Timing Diagram

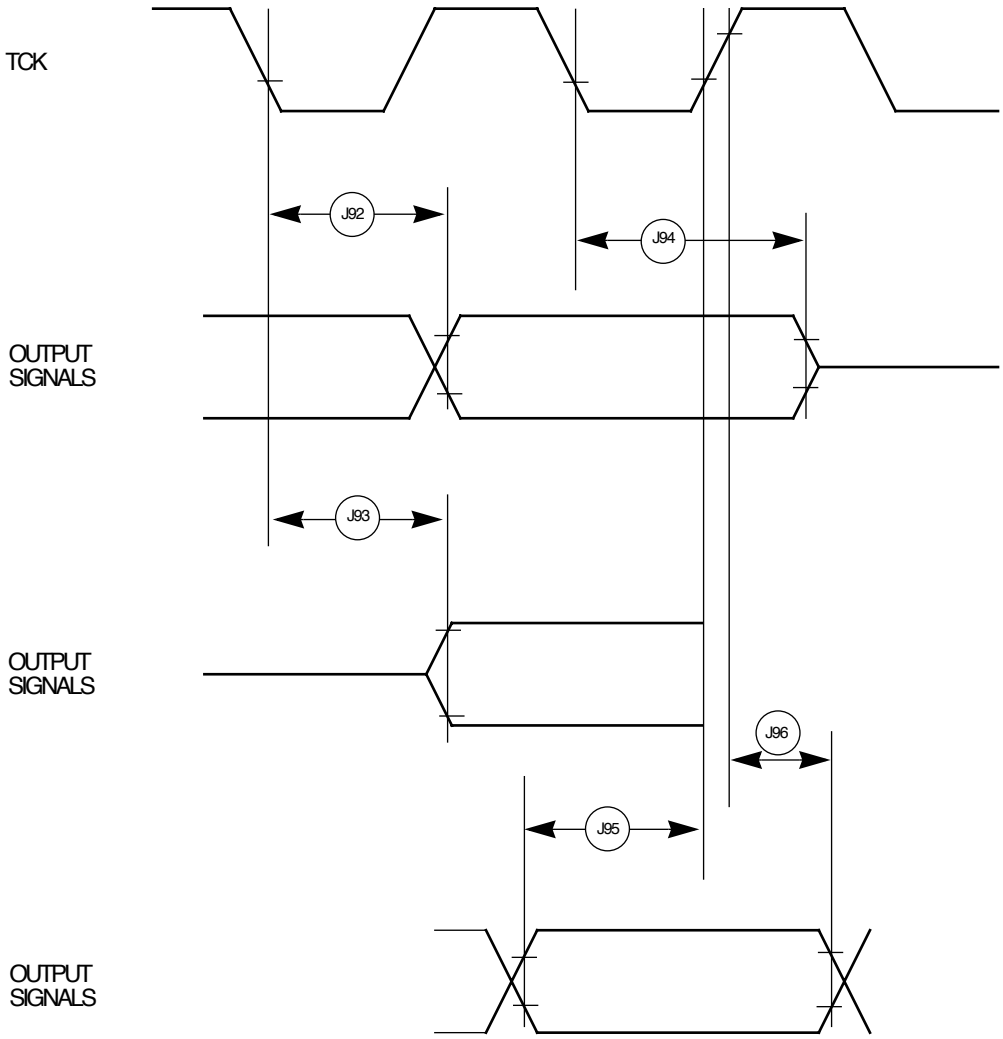


Figure 36. Boundary Scan (JTAG) Timing Diagram

COMMUNICATION ELECTRICAL CHARACTERISTICS

Table 8. Parallel Input/Output Port Timing

NUM	CHARACTERISTIC	25MHZ		40MHZ		50MHZ		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
29	Data-in setup time to clock high	20	—	15	—	15	—	ns
30	Data-in hold time from clock high	10	—	7.5	—	7.5	—	ns
31	Clock high to data-out valid (CPU writes data, control, or direction)	—	25	—	25	—	25	ns

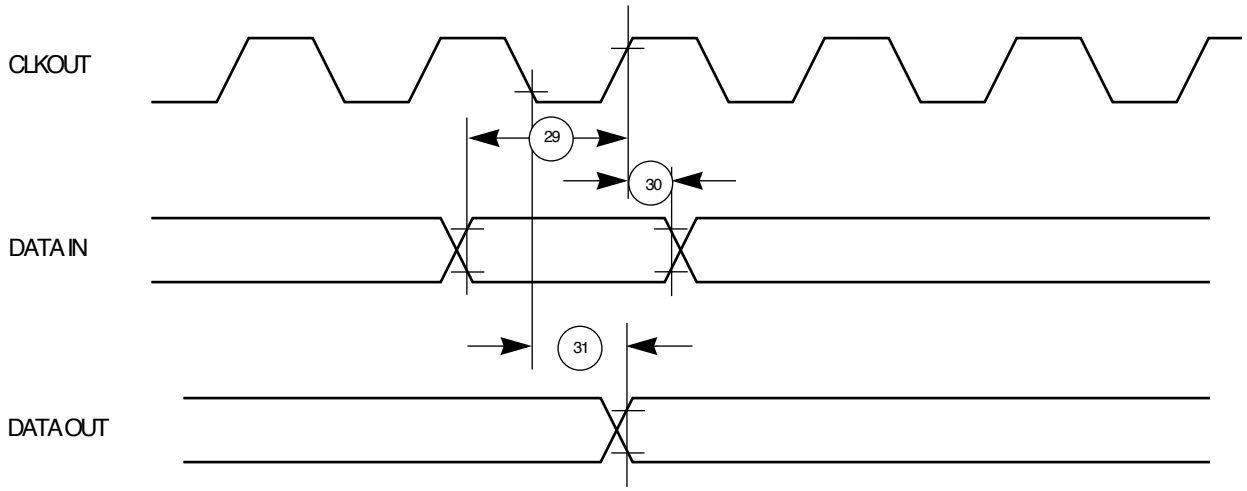


Figure 37. Parallel Input/Output Data-In/Data-Out Timing Diagram

Table 9. IDMA Timing

NUM	CHARACTERISTIC	25MHZ		40MHZ		50MHZ		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
40	$\overline{\text{DREQ}}$ setup time to clock high	12	—	7	—	7	—	nsec
41	$\overline{\text{DREQ}}$ hold time from clock high	5	—	3	—	3	—	nsec
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	20	—	12	—	12	nsec
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	20	—	12	—	12	nsec
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	25	—	20	—	20	nsec
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	20	—	15	—	15	nsec
46	$\overline{\text{TA}}$ assertion to falling edge of the clock setup time	12	—	7	—	7	—	nsec

NOTE: Applies to external $\overline{\text{TA}}$.

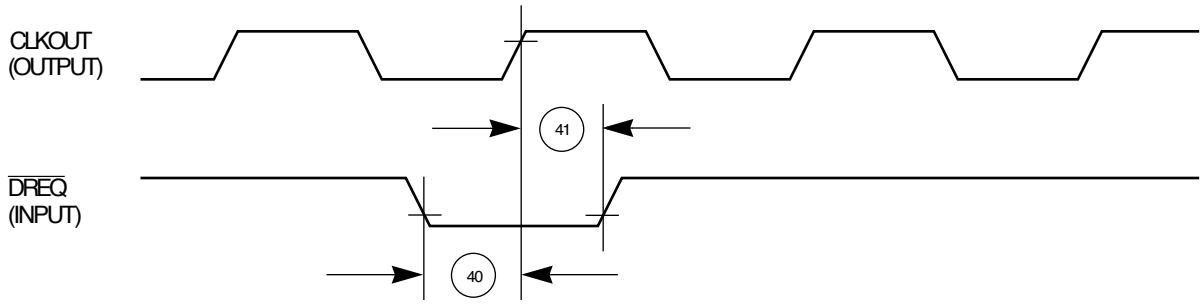


Figure 38. IDMA External Requests Timing Diagram

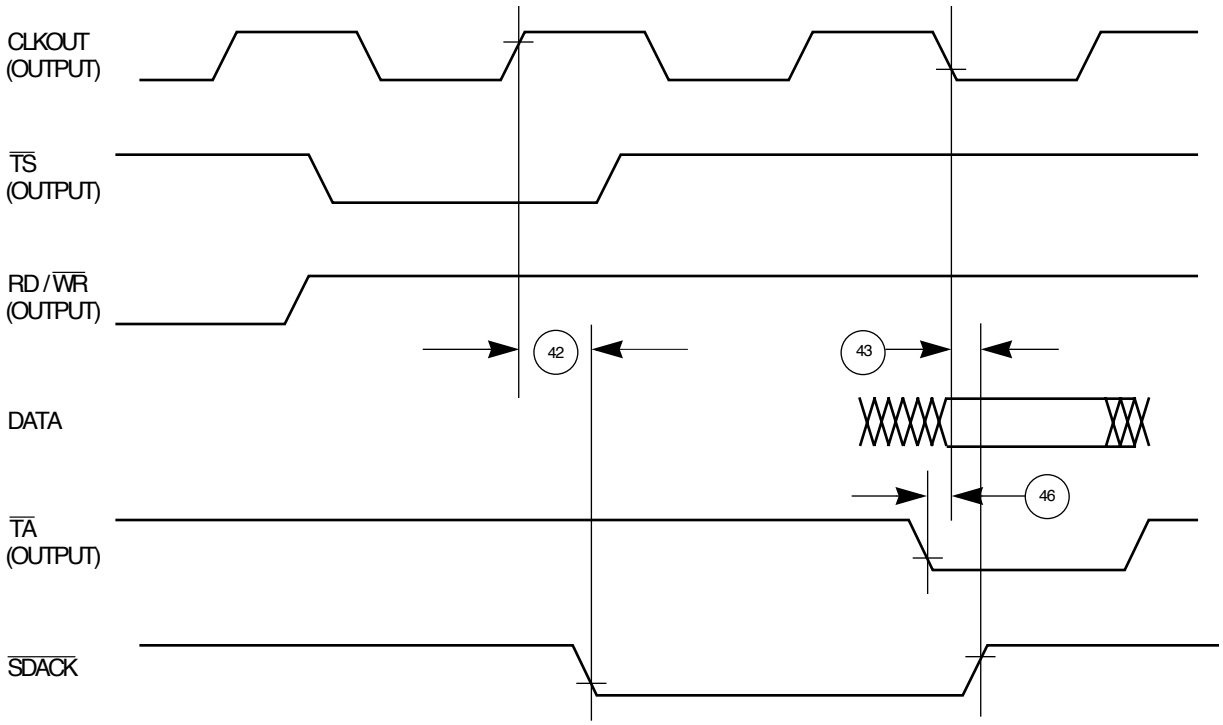


Figure 39. SDACK Timing Diagram–Peripheral Write, TA Sampled Low at the Falling Edge of the Clock

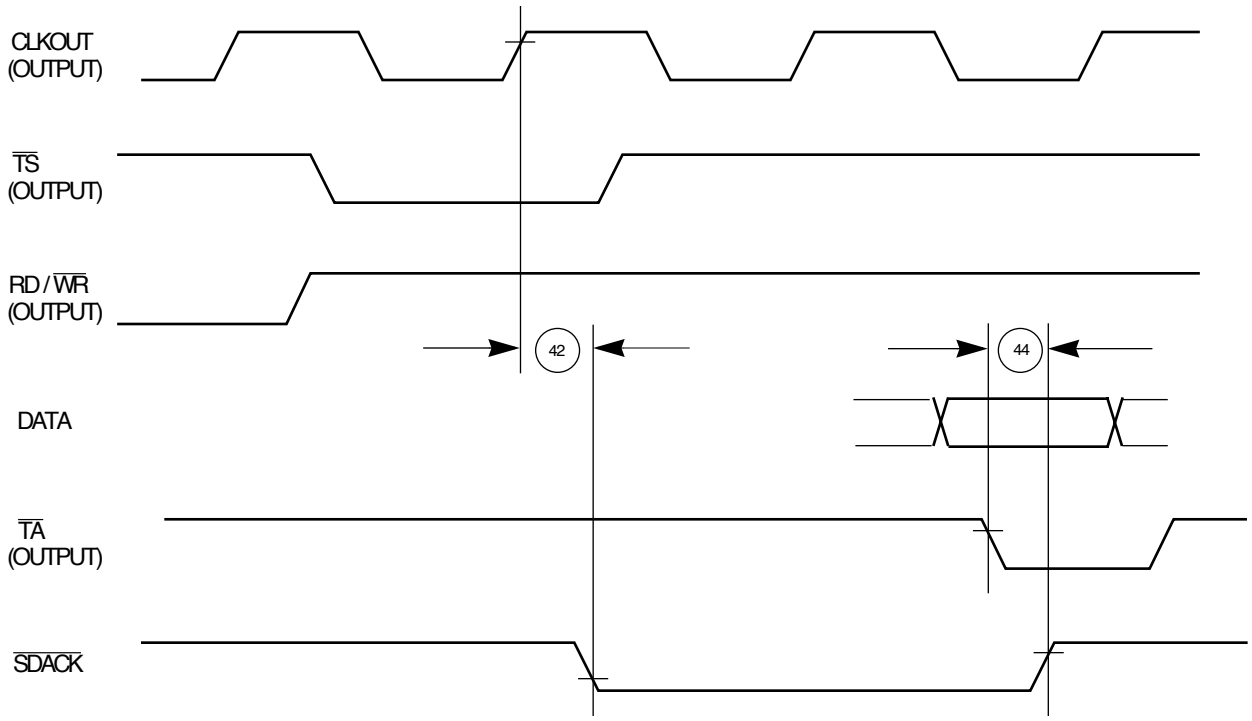


Figure 40. SDACK Timing Diagram–Peripheral Write, TA Sampled High at the Falling Edge of the Clock

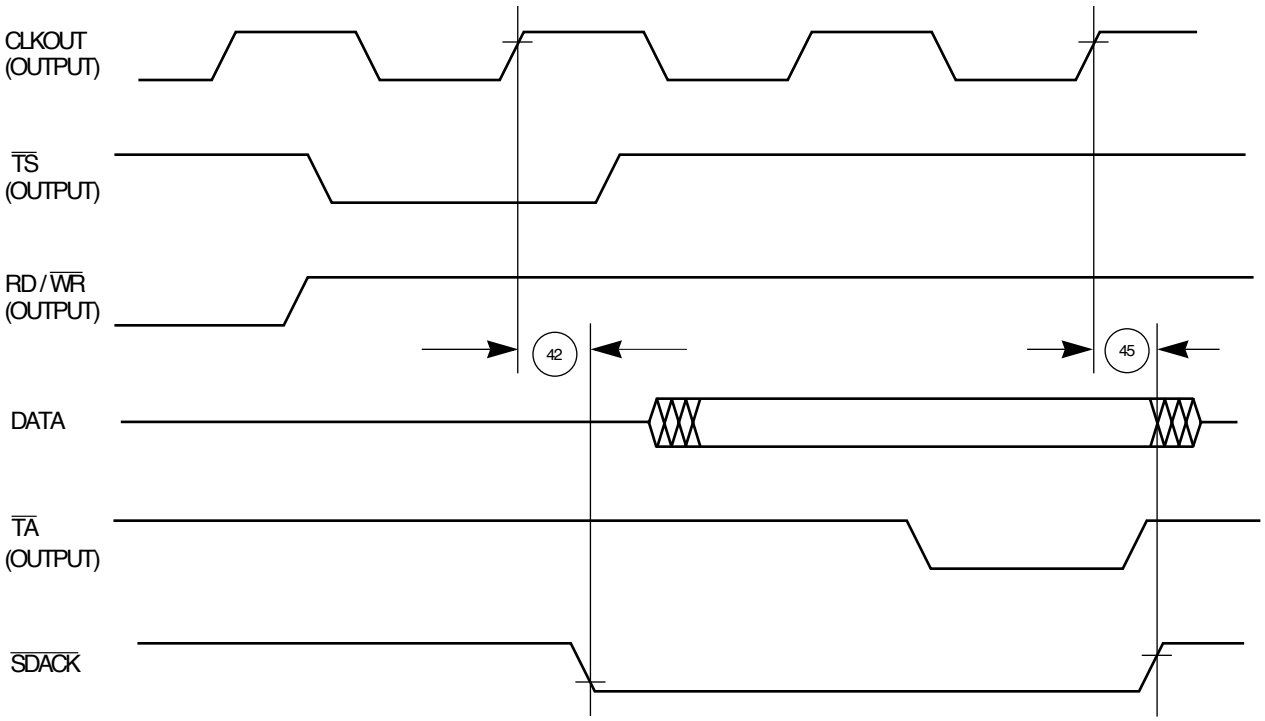


Figure 41. SDACK Timing Diagram–Peripheral Read

Table 10. Baud Rate Generator Timing

NUM	CHARACTERISTIC	25MHZ		40MHZ		50MHZ		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
50	BRGO rise and fall times	—	10	—	10	—	10	ns
51	BRGO duty cycle	40	60	40	60	40	60	%
52	BRGO cycle	40	—	40	—	40	—	ns

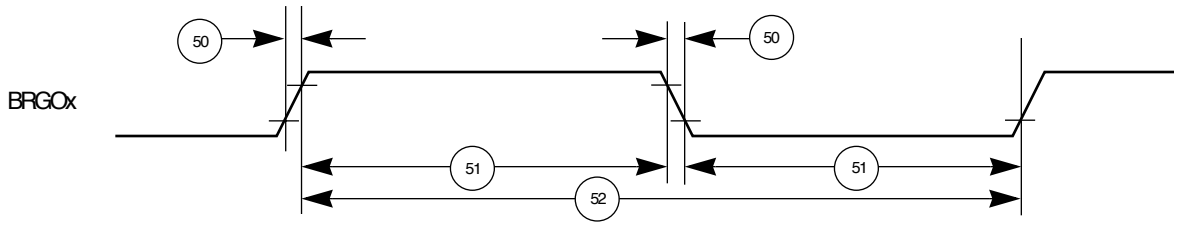


Figure 42. Baud Rate Generator Timing Diagram

Table 11. General-Purpose Timers Timing

NUM	CHARACTERISTIC	25MHZ		40MHZ		50MHZ		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
61	TIN/$\overline{\text{TGATE}}$ rise and fall times	12	10	7	10	7	10	ns
62	TIN/$\overline{\text{TGATE}}$ low time	5	1	3	1	3	1	clk
63	TIN/$\overline{\text{TGATE}}$ high time	—	20	—	12	—	12	clk
64	TIN/$\overline{\text{TGATE}}$ cycle time	—	20	—	12	—	12	clk
65	CLKO low to $\overline{\text{TOUT}}$ valid	—	25	—	20	—	20	ns

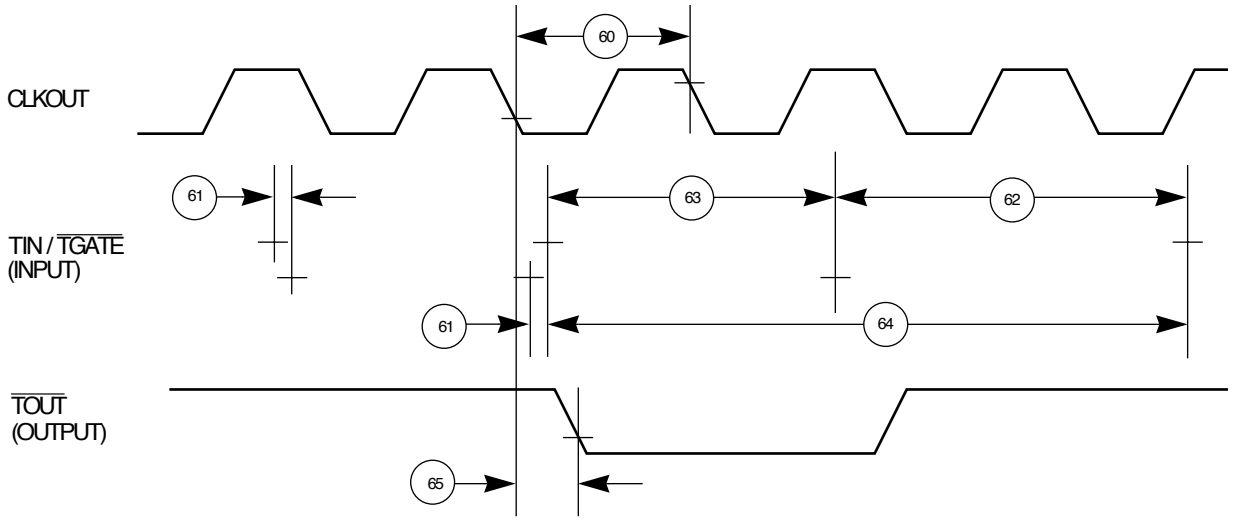


Figure 43. General-Purpose Timers Timing Diagram

Table 12. Serial Interface Timing

NUM	CHARACTERISTIC	25MHZ		40MHZ		50MHZ		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
70	L1RCLK and L1TCLK frequency (DSC=0)[1,3]	—	10	—	10	—	10	MHz
71	L1RCLK and L1TCLK width low (DSC=0)[3]	P+10	—	P+10	—	P+10	—	ns
71a	L1RCLK and L1TCLK width high (DSC=0)[2]	P+10	—	P+10	—	P+10	—	ns
72	L1TXD, L1ST(1–8), L1RQ, L1CLKO rise and fall times	—	15	—	15	—	15	ns
73	L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time)	20	—	20	—	20	—	ns
74	L1CLK edge to L1RSYNC and L1TSYNC invalid (SYNC hold time)	35	—	35	—	35	—	ns
75	L1RSYNC and L1TSYNC rise and fall times	—	15	—	15	—	15	ns
76	L1RXD valid to L1CLK edge (L1RXD setup time)	42	—	42	—	42	—	ns
77	L1CLK edge to L1RXD invalid (L1RXD hold time)	35	—	35	—	35	—	ns
78	L1CLK edge to L1ST(1–8) valid	10	45	10	45	10	45	ns
78a	L1SYNC valid to L1ST(1–8) valid[4]	10	45	10	45	10	45	ns
79	L1CLK edge to L1ST(1–8) invalid	10	45	10	45	10	45	ns
80	L1CLK edge to L1TXD valid	10	65	10	65	10	65	ns
80a	L1TSYNC valid to L1TXD valid[4]	10	65	10	65	10	65	ns
81	L1CLK edge to L1TXD high impedance	0	42	0	42	0	42	ns
82	L1RCLK and L1TCLK frequency (DSC=1)	—	12.5	—	16	—	16	MHz
83	L1RCLK and L1TCLK width low (DSC=1)	P+10	—	P+10	—	P+10	—	ns
83a	L1RCLK and L1TCLK width high (DSC=1)[2]	P+10	—	P+10	—	P+10	—	ns
84	L1CLK edge to L1CLKO valid (DSC=1)	—	30	—	30	—	30	ns
85	L1RQ valid before falling edge of L1TSYNC[3]	1	—	1	—	1	—	L1TCLK
86	L1GR setup time[3]	42	—	42	—	42	—	ns
87	L1GR hold time[3]	42	—	42	—	42	—	ns
88	L1CLK edge to L1SYNC valid (FSD = 00, CNT = 0000, BYT = 0, DSC=0)	—	0	—	0	—	0	ns

NOTES:

1. The ratio SyncCLK/L1RCLK must be greater than 2.5/1.
2. Where P=1/CLKO1. For a 25MHz CLKO1 rate, P=40ns.
3. These electrical specifications are only valid for IDL mode.
4. The strobes and TXD2 on the first bit of the frame becomes valid after L1CLK edge or L1SYNC, whichever is later.

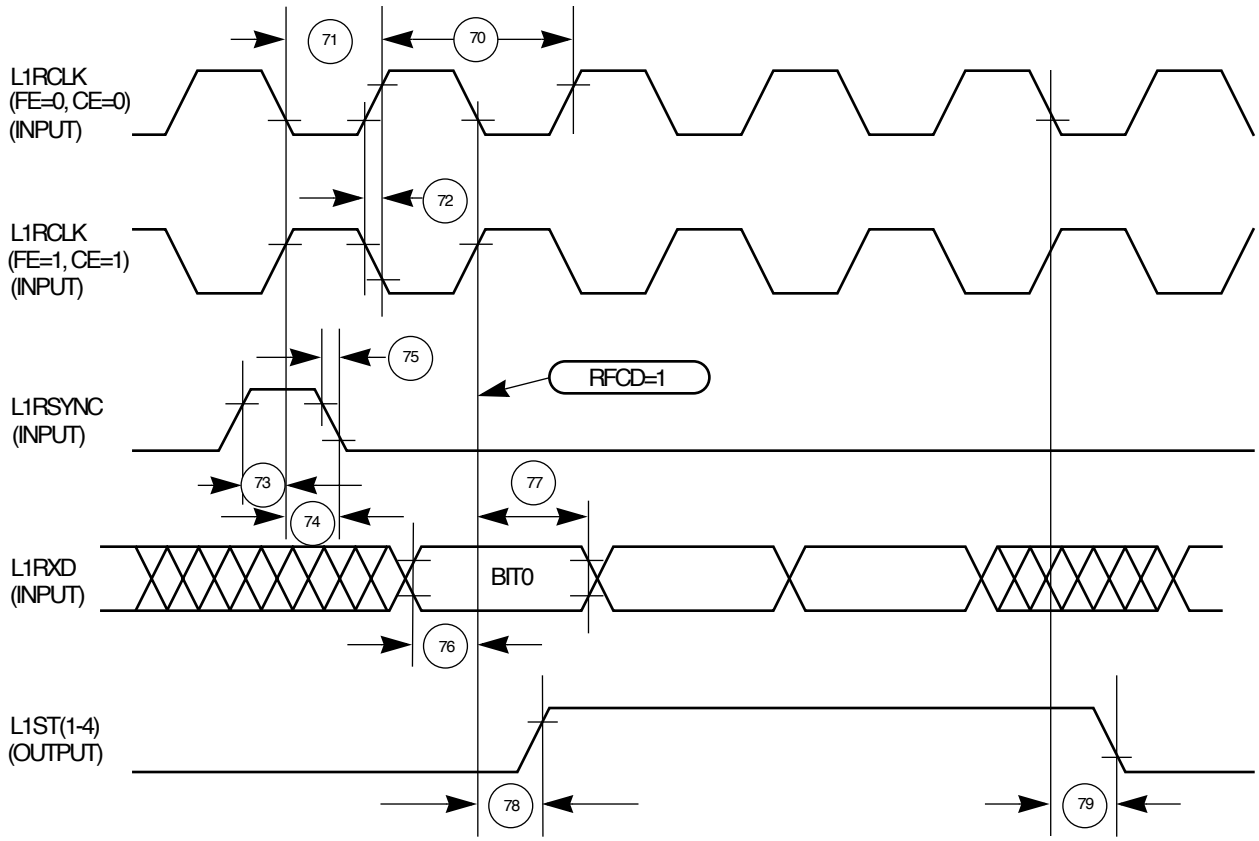


Figure 44. Serial Interface Receive Timing Diagram With Normal Clocking (DSC =0)

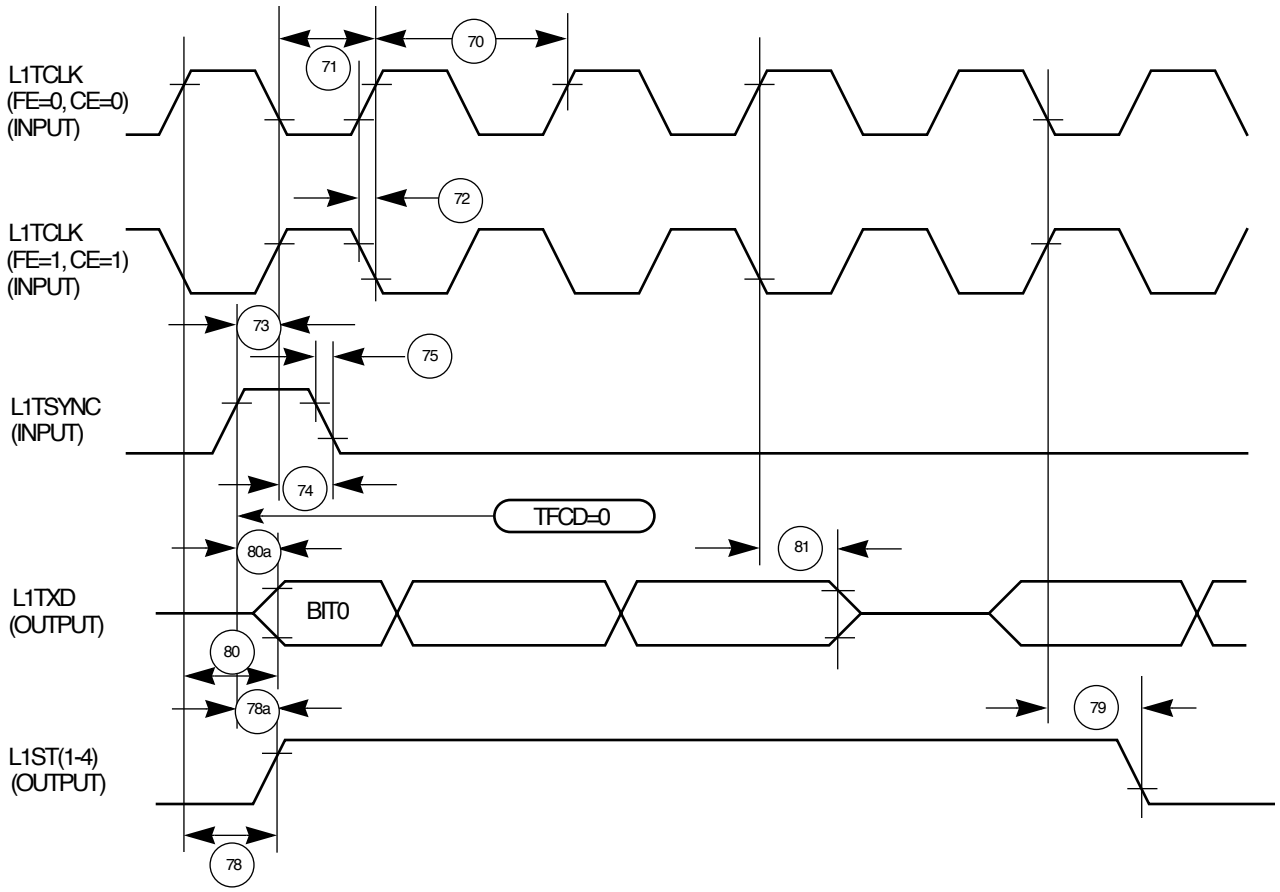


Figure 45. Serial Interface Transmit Timing Diagram

Table 13. Serial Communication Controller in NMSI External Timing

NUM	CHARACTERISTIC	25MHZ		40MHZ		50MHZ		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
100	RCLK1 and TCLK1 width high[1]	CLKOUT F	—	CLKOUT F	—	CLKOUT F	—	MHz
101	RCLK1 and TCLK1 width low	CLKOUT +5ns	—	CLKOUT +5ns	—	CLKOUT +5ns	—	ns
102	RCLK1 and TCLK1 rise and fall times	—	15	—	15	—	15	ns
103	TXD2 active delay (from TCLK1 falling edge)	0	50	0	50	0	50	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0	50	0	50	0	50	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	5	—	5	—	5	—	ns
106	RXD2 setup time to RCLK1 rising edge	5	—	5	—	5	—	ns
107	RXD2 hold time from RCLK1 rising edge2	5	—	5	—	5	—	ns
108	$\overline{\text{CD1}}$ setup time to RCLK1 rising edge	5	—	5	—	5	—	ns

NOTES:

1. The ratio SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2.25/1.
2. Applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

Table 14. Serial Communication Controller in NMSI Internal Timing

NUM	CHARACTERISTIC	25MHZ		40MHZ		50MHZ		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
100	RCLK1 and TCLK1 frequency[1]	0	8.3	0	13	0	16	MHz
102	RCLK1 and TCLK1 rise and all times	—	—	—	—	—	—	ns
103	TXD2 active delay (from TCLK1 falling edge)	0	30	0	30	0	30	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0	30	0	30	0	30	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	40	—	40	—	40	—	ns
106	RXD2 setup time to RCLK1 rising edge	40	—	40	—	40	—	ns
107	RXD2 hold time from RCLK1 rising edge[2]	0	—	0	—	0	—	ns
108	$\overline{\text{CD1}}$ setup time to RCLK1 rising edge	40	—	40	—	40	—	ns

NOTES:

1. The ratio SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 3/1.
2. Applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

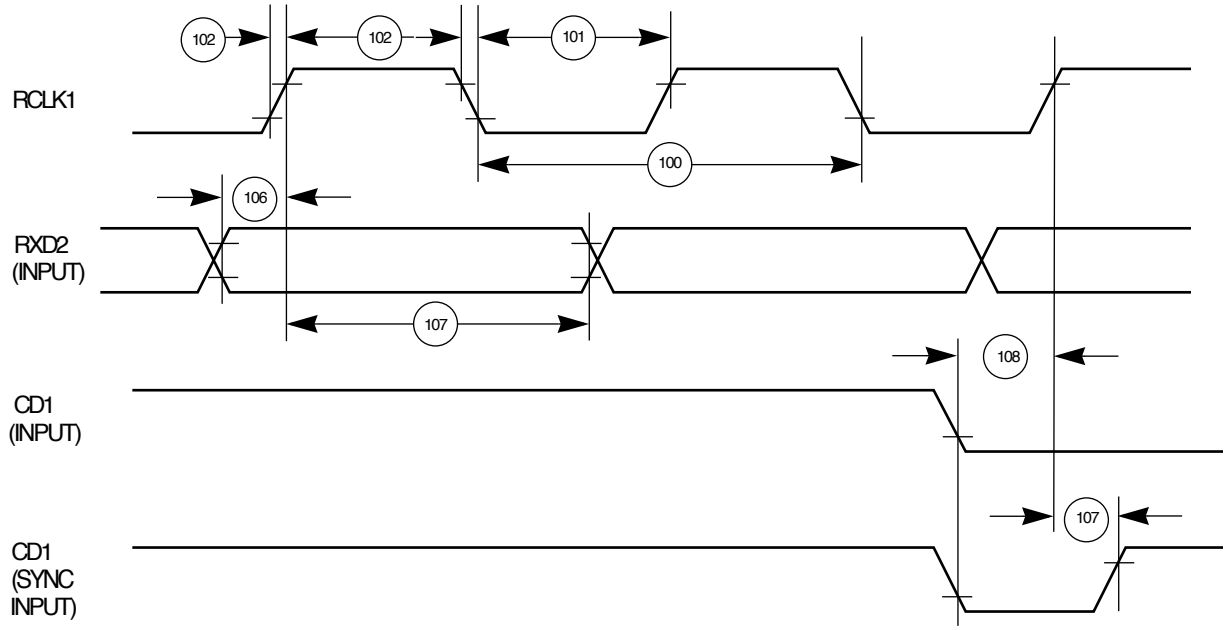


Figure 46. SCC NMSI Receive Timing Diagram

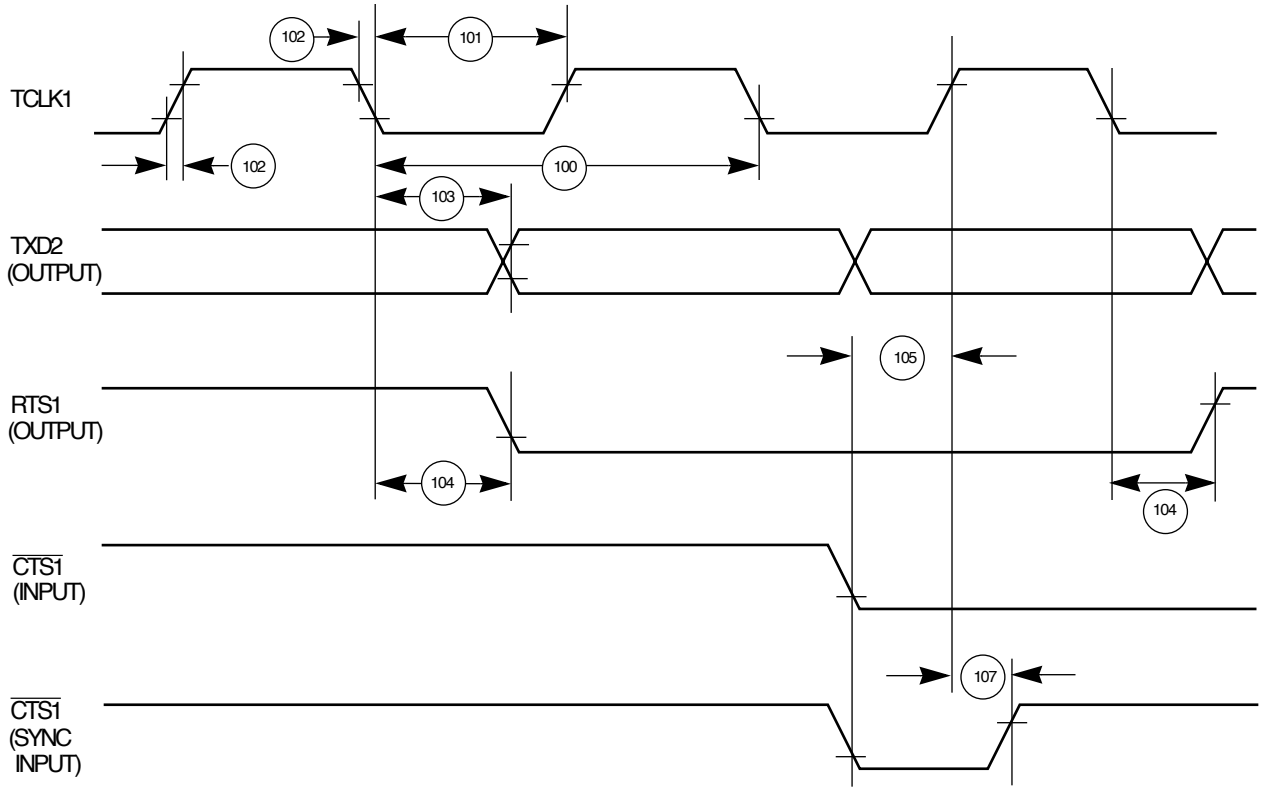


Figure 47. SCC NMSI Transmit Timing Diagram

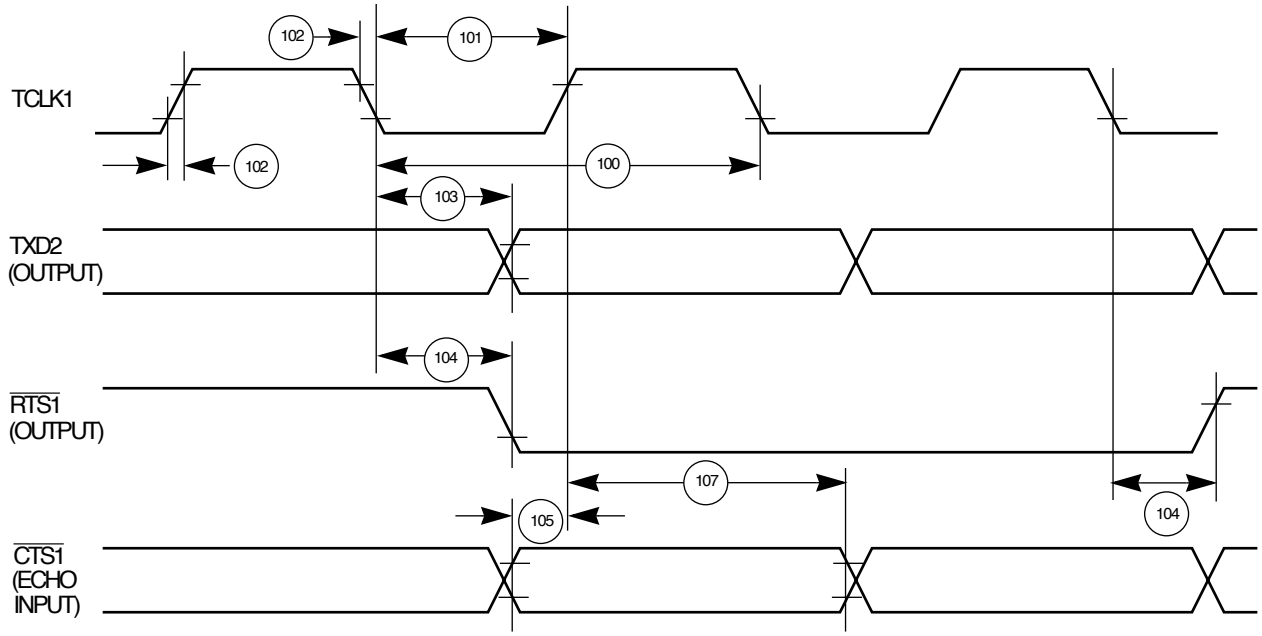


Figure 48. HDLC Bus Timing Diagram

Table 15. Ethernet Timing

NUM	CHARACTERISTIC	25MHZ		40MHZ		50MHZ		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
120	CLSN (CTS2) width high	40	—	40	—	40	—	ns
121	RCLK1 rise and fall times	—	15	—	15	—	15	ns
122	RCLK1 width low	40	—	40	—	40	—	ns
123	RCLK1 clock period[1]	80	120	80	120	80	120	ns
124	RXD2 setup time	20	—	20	—	20	—	ns
125	RXD2 hold time	5	—	5	—	5	—	ns
126	RENA (CD2) active delay (from RCLK1 rising edge of the last data bit)	10	—	10	—	10	—	ns
127	RENA (CD2) width low	100	—	100	—	100	—	ns
128	TCLK1 rise and fall times	—	15	—	15	—	15	ns
129	TCLK1 width low	40	—	40	—	40	—	ns
130	TCLK1 clock period[1]	99	101	99	101	99	101	ns
131	TXD2 active delay (from TCLK1 rising edge)	10	50	10	50	10	50	ns
132	TXD2 inactive delay (from TCLK1 rising edge)	10	50	10	50	10	50	ns
133	TENA (RTS2) active delay (from TCLK1 rising edge)	10	50	10	50	10	50	ns
134	TENA (RTS2) inactive delay (from TCLK1 rising edge)	10	50	10	50	10	50	ns
135	N/A							
136	N/A							
137	N/A							
138	CLKx low to $\overline{\text{SDACK}}$ asserted[2]	—	20	—	20	—	20	ns
139	CLKx low to $\overline{\text{SDACK}}$ negated[3]	—	20	—	20	—	20	ns

NOTES:

1. The ratio SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2/1.
2. $\overline{\text{SDACK}}$ is asserted when the SDMA writes the incoming frame DA into memory.

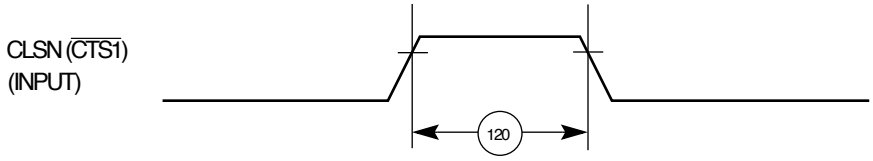


Figure 49. Ethernet Collision Timing Diagram

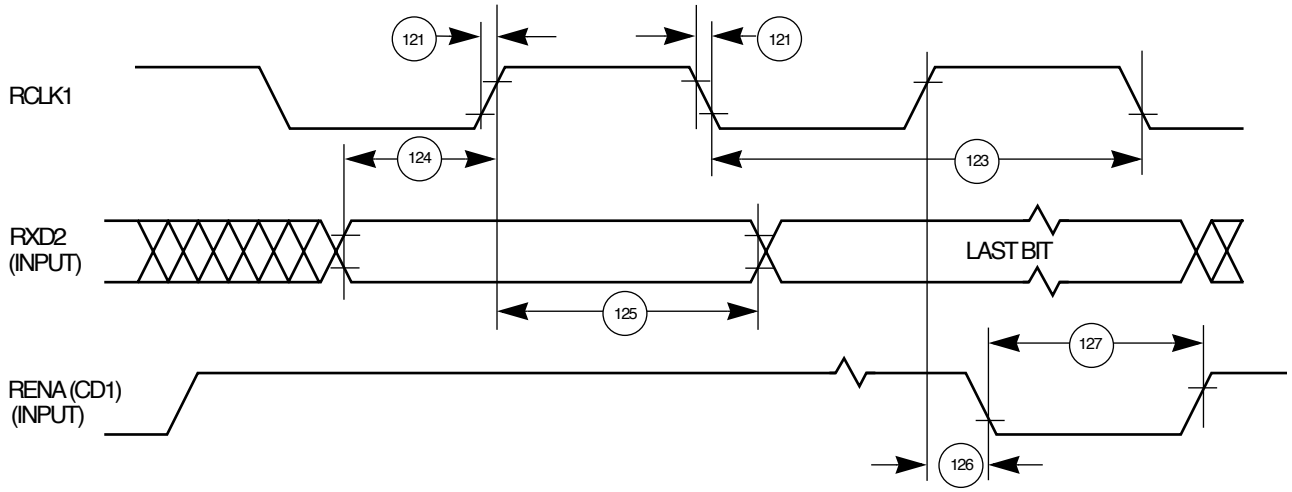
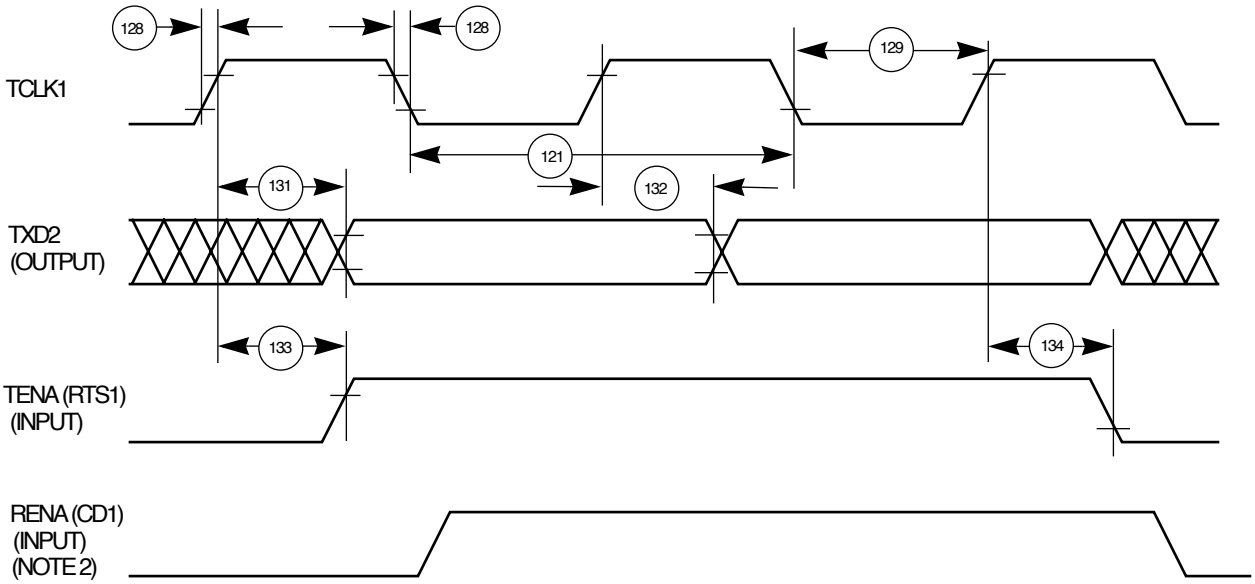


Figure 50. Ethernet Receive Timing Diagram



NOTES: 1. TRANSMIT CLOCK INVERT (TCI) BIT IN THE GSMR IS SET.
2. IF RENA IS DEASSERTED BEFORE TENA, OR RENA IS NOT ASSERTED AT ALL DURING TRANSMIT, THEN THE CSL BIT IS SET IN THE BUFFER DESCRIPTOR AT THE END OF FRAME TRANSMISSION.

Figure 51. Ethernet Transmit Timing Diagram

Table 16. Serial Peripheral Interface Master Timing

NUM	CHARACTERISTIC	25MHZ		40MHZ		50MHZ		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
160	Master cycle time	4	1,024	4	1,024	4	1,024	tcyc
161	Master clock (SCK) high or low time	2	512	2	512	2	512	tcyc
162	Master data setup time (inputs)	50	—	50	—	50	—	ns
163	Master data hold time (inputs)	0	—	0	—	0	—	ns
164	Master data valid (after SCK edge)	—	20	—	20	—	20	ns
165	Master data hold time (outputs)	0	—	0	—	0	—	ns
166	Rise time output	—	15	—	15	—	15	ns
167	Fall time output	—	15	—	15	—	15	ns

NOTE: The ratio SyncCLK/SMCLK must be greater than or equal to 2/1.

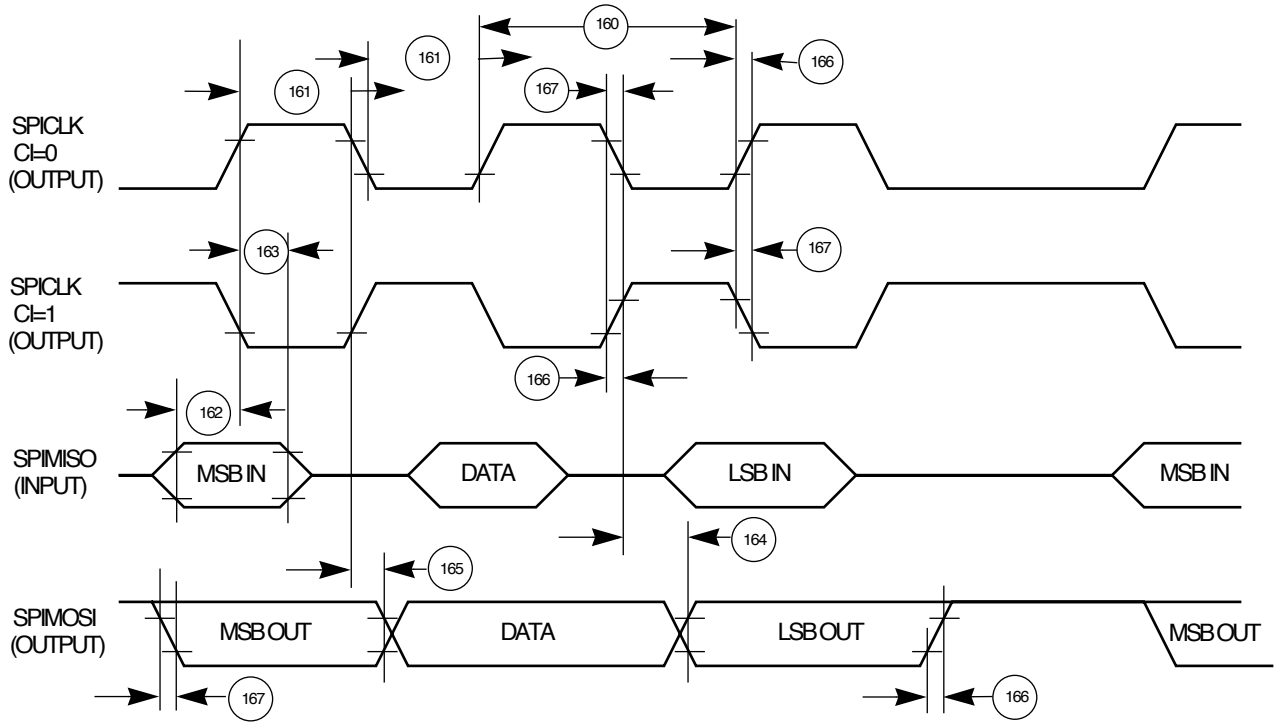


Figure 52. SPI Master (CP=0) Timing Diagram

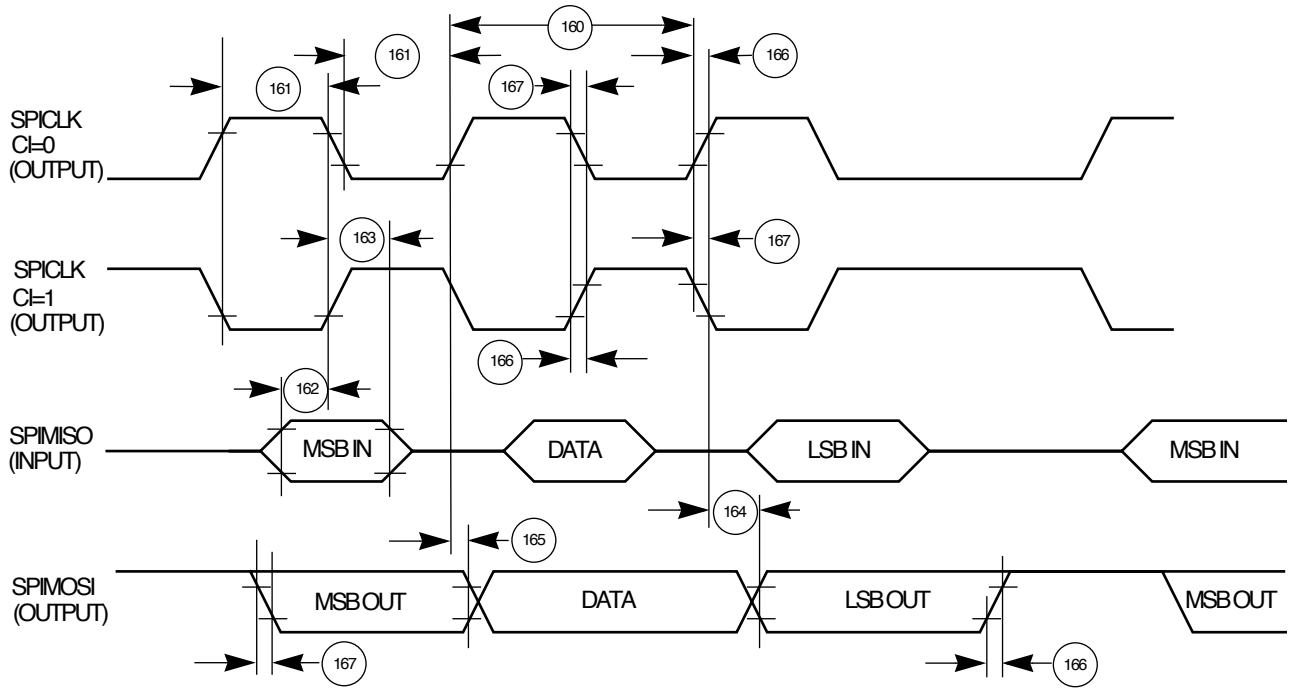


Figure 53. SPI Master (CP=1) Timing Diagram

Table 17. Serial Peripheral Interface Slave Timing

NUM	CHARACTERISTIC	25MHZ		40MHZ		50MHZ		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
170	Slave cycle time	2	—	2	—	2	—	tcyc
171	Slave enable lead time	15	—	15	—	15	—	ns
172	Slave enable lag time	15	—	15	—	15	—	ns
173	Slave clock (SPICLK) high or low time	1	—	1	—	1	—	tcyc
174	Slave sequential transfer delay (does not require deselect)	1	—	1	—	1	—	tcyc
175	Slave data setup time (inputs)	20	—	20	—	20	—	ns
176	Slave data hold time (inputs)	20	—	20	—	20	—	ns
177	Slave access time	—	50	—	50	—	50	ns
178	Slave SPI MISO disable time	—	50	—	50	—	50	ns
179	Slave data valid (after SPICLK edge)	—	50	—	50	—	50	ns
180	Slave data hold time (outputs)	0	—	0	—	0	—	ns
181	Rise time (input)	—	15	—	15	—	15	ns
182	Fall time (input)	—	15	—	15	—	15	ns

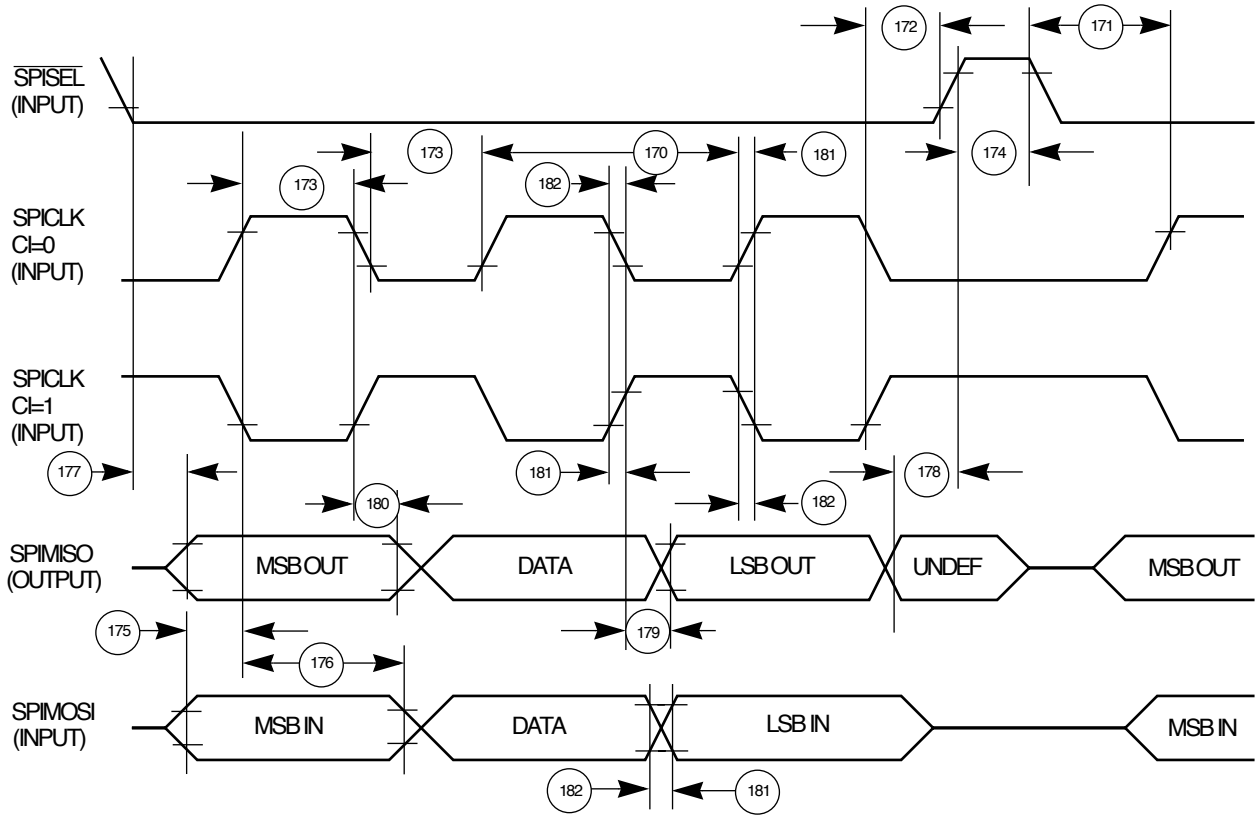


Figure 54. SPI Slave (CP=0) Timing Diagram

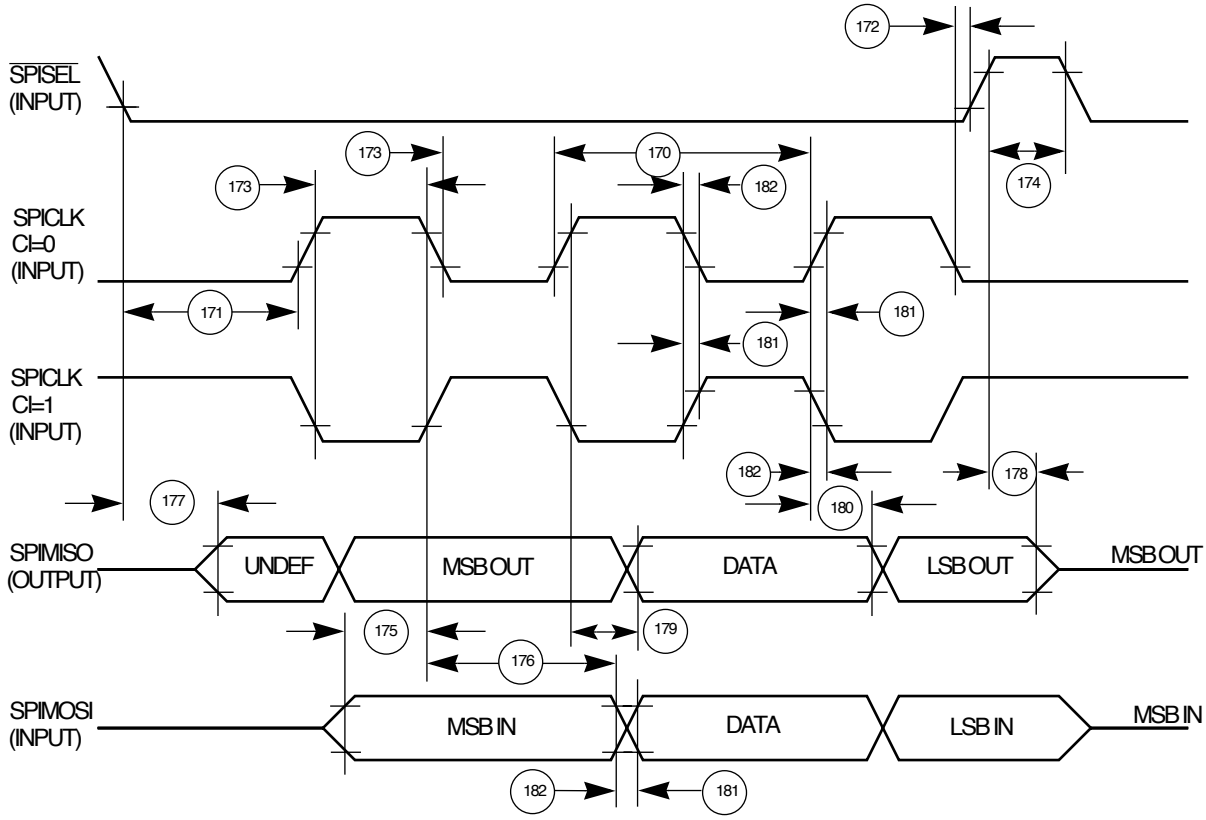


Figure 55. SPI Slave (CP=1) Timing Diagram

Table 18. I²C Timing—SCL < 100 kHz

NUM	CHARACTERISTIC	25MHZ		40MHZ		50MHZ		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
200	SCL clock frequency (slave)	0	100	0	100	0	100	kHz
200	SCL clock frequency (master)	1.5	100	1.5	100	1.5	100	kHz
202	Bus free time between transmissions	4.7	—	4.7	—	4.7	—	μs
203	Low period of SCL	4.7	—	4.7	—	4.7	—	μs
204	High period of SCL	4.0	—	4.0	—	4.0	—	μs
205	Start condition setup time	4.7	—	4.7	—	4.7	—	μs
206	Start condition hold time	4.0	—	4.0	—	4.0	—	μs
207	Data hold time	0	—	0	—	0	—	μs
208	Data setup time	250	—	250	—	250	—	ns
209	SDL/SCL rise time	—	1	—	1	—	1	μs
210	SDL/SCL fall time	—	300	—	300	—	300	ns
211	STOP condition setup time	4.7	—	4.7	—	4.7	—	μs

NOTE: SCL frequency is given by SCL = BRGCLK_frequency/((BRG register + 3) * pre_scaler * 2).
The ratio SyncClk/(BRGCLK/pre_scaler) must be greater than or equal to 4/1.

Table 19. I²C Timing—SCL > 100 kHz

NUM	CHARACTERISTIC	MINIMUM	MAXIMUM	UNIT
200	SCL clock frequency (slave)	0	BRGCLK/48	Hz
200	SCL clock frequency (master)	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions	1/(2.2 * fSCL)	—	sec
203	Low period of SCL	1/(2.2 * fSCL)	—	sec
204	High period of SCL	1/(2.2 * fSCL)	—	sec
205	Start condition setup time	1/(2.2 * fSCL)	—	sec
206	Start condition hold time	1/(2.2 * fSCL)	—	sec
207	Data hold time	0	—	sec
208	Data setup time	1/(40 * fSCL)	—	sec
209	SDL/SCL rise time	—	1/(10 * fSCL)	sec
210	SDL/SCL fall time	—	1/(33 * fSCL)	sec
211	Stop condition setup time	1/(2.2 * fSCL)	—	sec

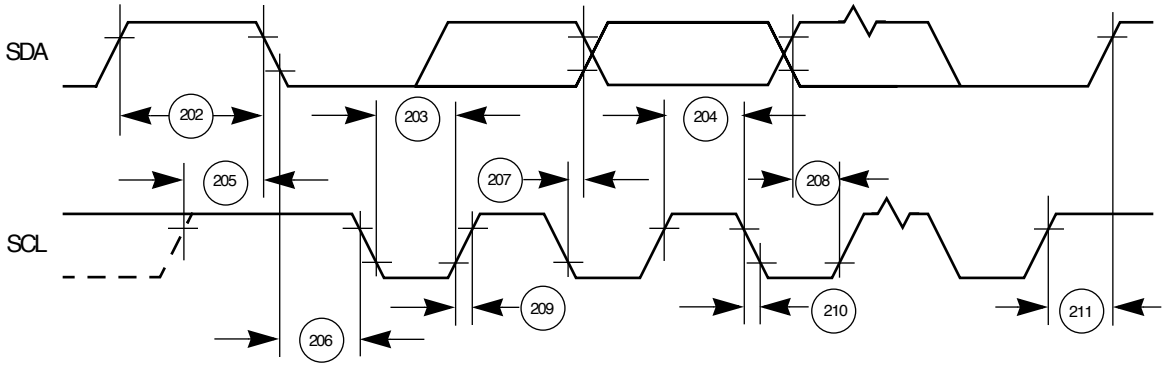
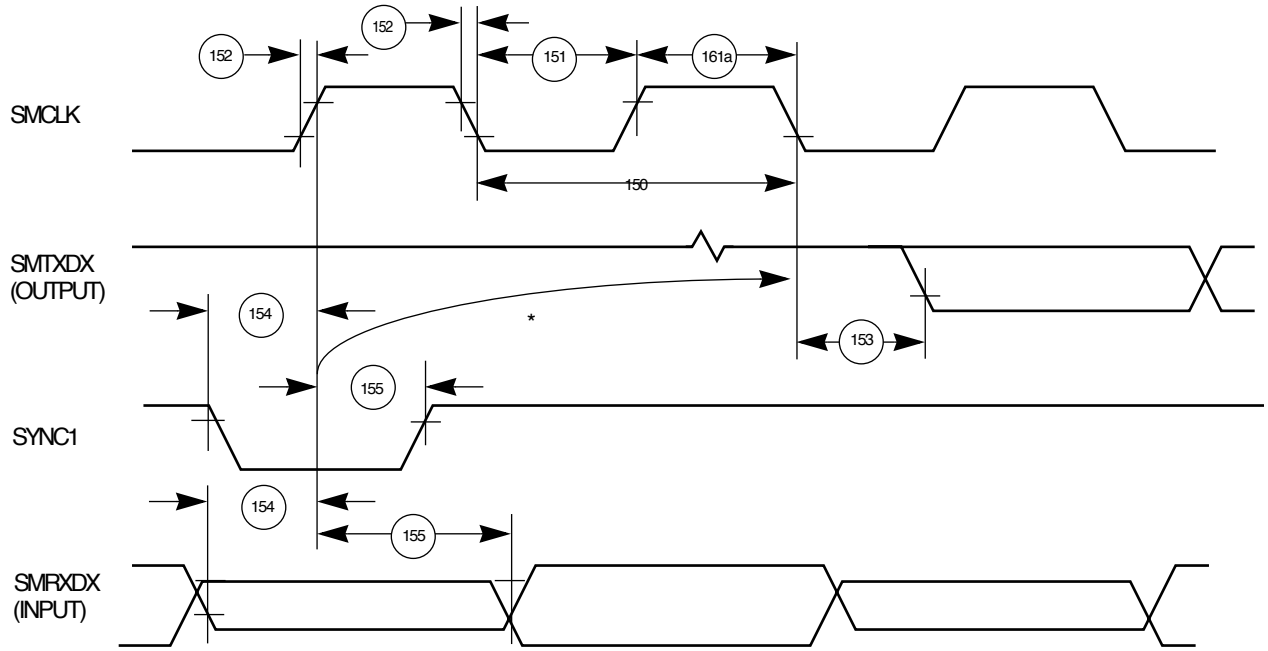


Figure 56. I²C Bus Timing Diagram

Table 20. Serial Management Controller Timing

NUM	CHARACTERISTIC	25MHZ		40MHZ		50MHZ		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
150	CLK1 clock period	100	—	100	—	100	—	ns
151	CLK1 width low	50	—	50	—	50	—	ns
151A	CLK1 width high	50	—	50	—	50	—	ns
152	CLK1 rise and fall times	—	15	—	15	—	15	ns
153	SMTXDx active delay (from CLK1 falling edge)	10	50	10	50	10	50	ns
154	SMRXDx/SYNC1 setup time	20	—	20	—	20	—	ns
155	SMRXDx/SYNC1 hold time	5	—	5	—	5	—	ns

NOTE: The ratio SyncCLK/SMCLK must be greater than or equal to 2/1.



NOTE: * THIS DELAY IS EQUAL TO AN INTEGER NUMBER OF "CHARACTER LENGTH" CLOCKS.

Figure 57. SMC Transparent Timing Diagram

Table 21. LCD Controller Timing

NUM	CHARACTERISTIC	25MHZ		40MHZ		50MHZ		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
220	Shift clock cycle time	40	—	40	—	40	—	nsec
221	Shift clock high time	20	—	20	—	20	—	nsec
223	CLOCK/HSYNC/VSYNC/$\overline{OE}$ rise and fall times	—	10	—	10	—	10	nsec
224	Data valid delay from shift clock high	—	15	—	15	—	15	nsec
225	VSYNC to HSYNC setup time[1]	5	—	5	—	5	—	T
226	VSYNC hold time	1	—	1	—	1	—	T
227	HSYNC pulse width	4	—	4	—	4	—	T
228	Time from clock falling edge to HSYNC rising edge	4.5	—	4.5	—	4.5	—	T
229	Time from HSYNC falling edge to clock rising edge[2]	4	—	4	—	4	—	T
230	AC active delay	—	25	—	25	—	25	nsec
231	VSYNC pulse width (TFT)	1	16	1	16	1	16	Line
232	HSYNC to $\overline{OE}$ delay[3]	4	—	4	—	4	—	T
233	$\overline{OE}$ to HSYNC delay	4	—	4	—	4	—	T
234	VSYNC to $\overline{OE}$ delay (TFT)	0	1,023	0	1,023	0	1,023	T
235	VSYNC/HSYNC/$\overline{OE}$ active delay (TFT)	—	15	—	15	—	15	nsec
236	Wait between frames[4]	WBF	—	WBF	—	WBF	—	Line

NOTES:

1. T = shift clock cycle (220).
2. This number is given for wbl(wait between lines) ≤ 2. For wbl=n {n>2} the timing will be (n+2)T.
3. This number is given for wbl(wait between lines) ≤ 2. For wbl=n {n>2} the timing will be (n+2)T.
4. Wait Between Frames (WBF) is a programmable parameter.

Tcyc is the cycle time of the LCD clock (shift clock). Tdelay is a circuit delay that is specified in the AC electrical specifications. 1–16 lines is a time period that can vary between one scan line and 16, depending on how the LCD controller is programmed in the VPW field of the LCVCR. 0–1,023 lines is a time period that can vary between 0 and 1,023 scan lines in the WBF field of the LCVCR.

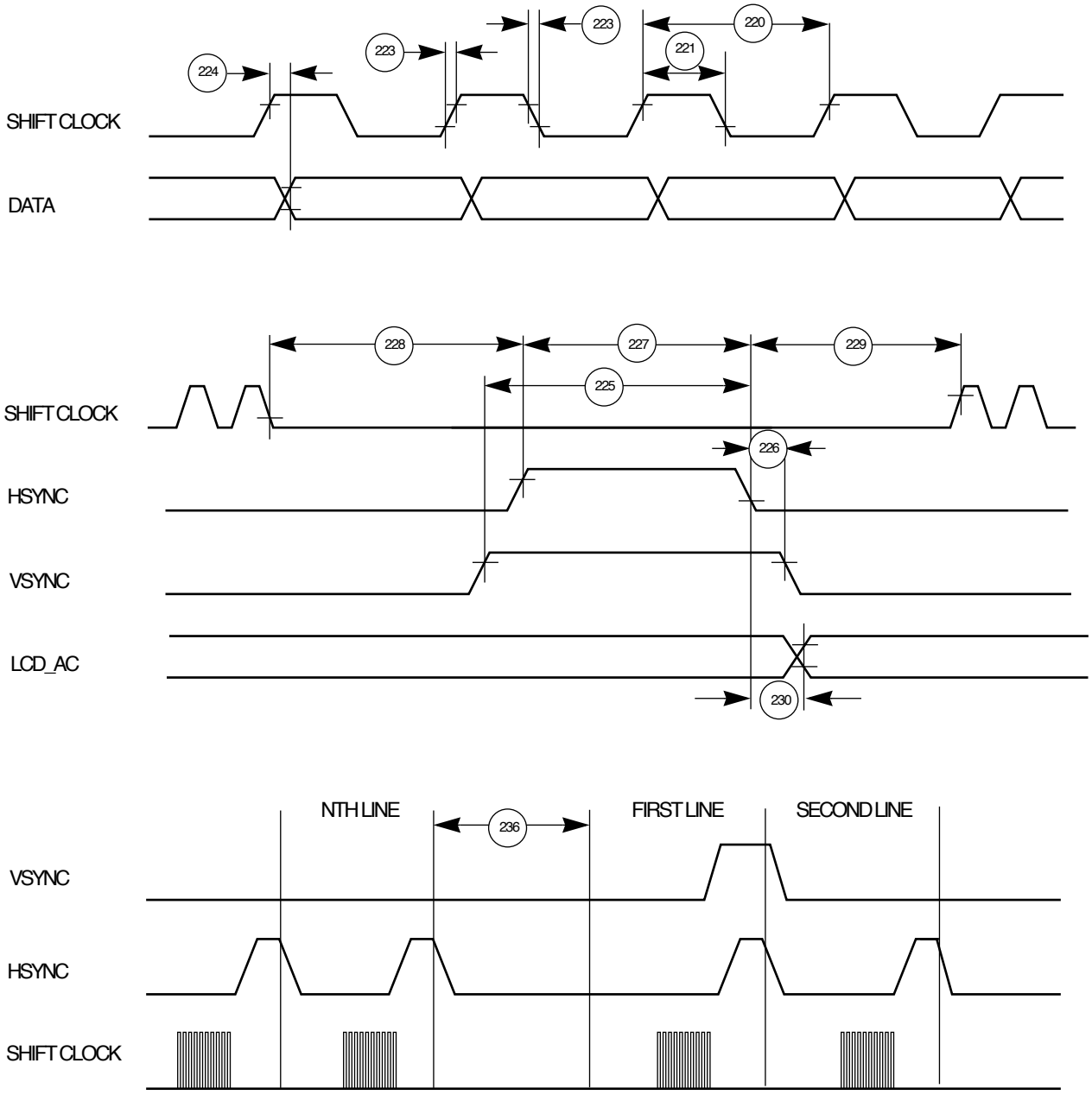


Figure 58. Passive Panel Timing Diagram

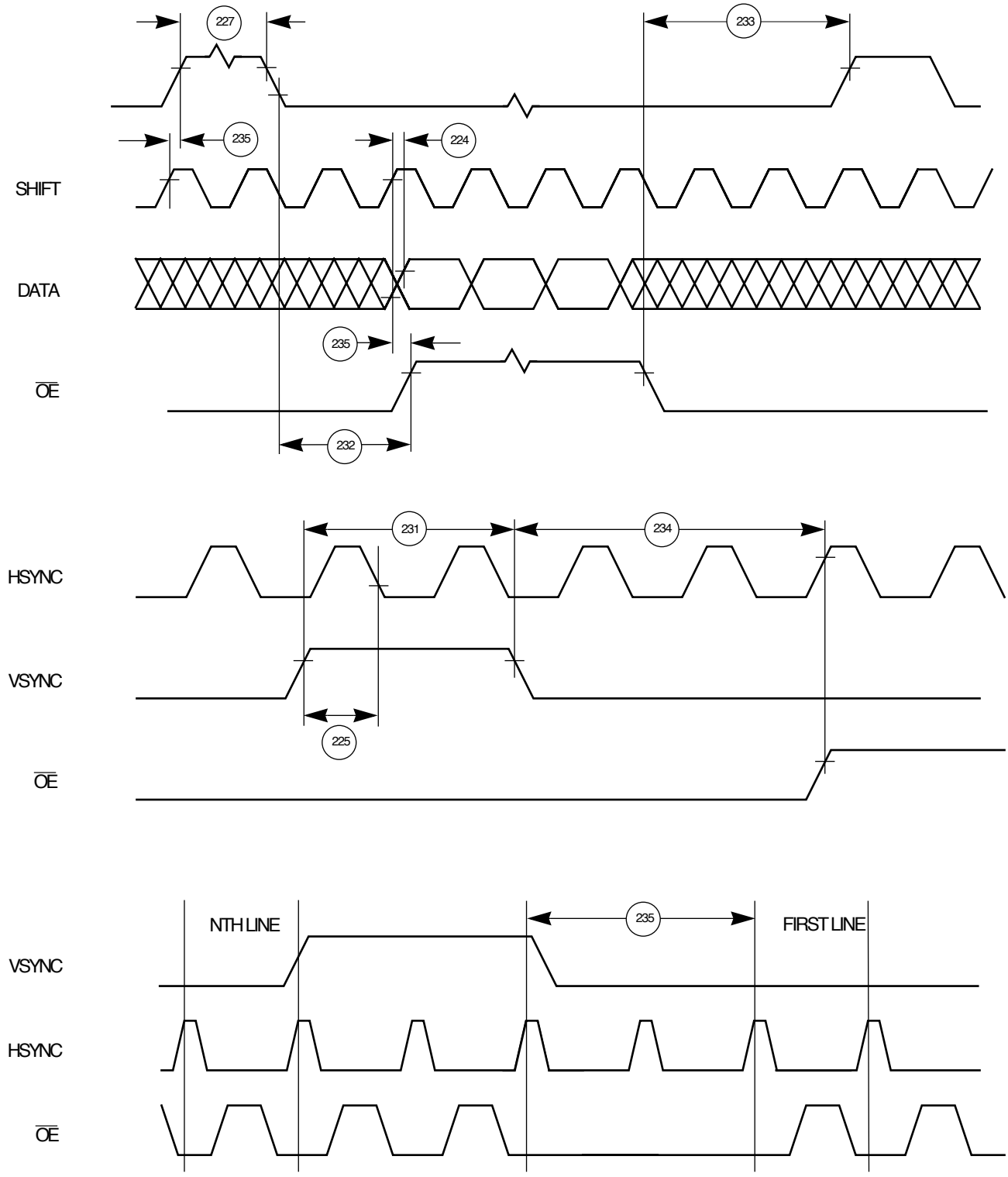


Figure 59. TFT Panel Timing Diagram

Table 22. Video Controller Timing

NUM	CHARACTERISTIC	25MHZ		40MHZ		50MHZ		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
240	Clock cycle time	32	—	32	—	32	—	nsec
241	Clock high time	13	—	13	—	13	—	nsec
242	CLK/$\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$/$\overline{\text{BLANK}}$/FIELD rise and fall times	—	10	—	10	—	10	nsec
243	Clock high to data valid	10	25	10	25	10	25	nsec

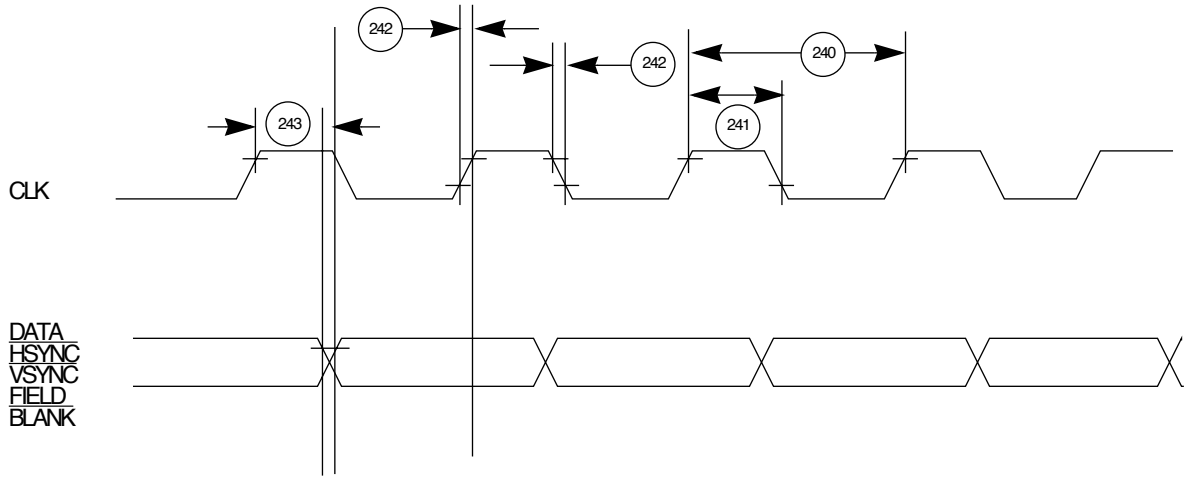


Figure 60. Video Controller Timing

Literature Distribution Centers:

USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912, Arizona 85036.

JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.

ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

Search

MPC823 : PowerQUICC" Integrated Communications Processor for Portable Systems

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The MPC823 microprocessor is a versatile, one-chip integrated microprocessor and peripheral combination that can be used in a variety of electronic products. It particularly excels in low-power, portable, image capture and personal communication products. It has a universal serial bus (USB) interface and video display controller, as well as the existing LCD controller of the MPC821 device.

The MPC823 microprocessor integrates a high-performance embedded MPC8xx core with a communication processor module that uses a specialized RISC processor for imaging and communication. The communication processor module can perform embedded signal processing functions for image compression and decompression. It also supports seven serial channels--two serial communication controllers, two serial management controllers, one I^2C port, one USB channel, and one serial peripheral interface.

This two-processor architecture consumes power more efficiently than traditional architectures because the communication processor module frees the core from peripheral tasks like imaging and communication.

Link Product Picture

Link Block Diagram

MPC823 Features

(Rev B and later)

- Embedded MPC8xx Core Provides 99MIPS (Using Dhrystone 2.1) or 172K Dhrystones 2.1 at 75MHz
- Advanced On-Chip Emulation Debug Mode
- Data Bus Dynamic Bus Sizing for 8-,16-, and 32-Bit Buses
- Completely Static Design (0-75MHz Operation)
- Communication Processor Module
- Four Baud Rate Generators
- Two Serial Communication Controllers (SCCs)
- One Dedicated High-Speed Serial Channel for the Universal Serial Bus (USB)
- Two Serial Management Controllers (SMCs) with Externally Accessible Pins
- One Serial Peripheral Interface
- One I^2C Port
- Serial Interface with the Two Time-Slot Assigners
- General-Purpose Timers
- Interrupts
- Memory Controller (Eight Banks)
- System Integration Unit
- Video Controller
- LCD Controller

- Single-Socket PCMCIA-ATA Interface
- Low-Power Support Modes
- Development Capabilities and Interface
- 3.3V Operation with 5V TTL Compatibility for the General-Purpose I/O Port Pins and 3.3V for All Others
- 256-Pin Plastic Ball Grid Array (BGA) Packaging

MPC823 Versions and Masks

Rev	Mask	IMMR[16:31] (PARTNUM, MASKNUM)	Process	Qual	Part Numbers	Errata[2]	Date
B.2	1K29A 1K24A 3H97G	2101	.32µ TLM	XC	XPC823ZTxxB2, XPC823ZCxxB2, KXPC823ZT81B2, KXPC823ZC81B2, XPC823ZTxxB2T	MASK3H97G	03-30-2000
B.1	1H97G	2101	.32µ TLM	XC	XPC823ZTxxB, XPC823ZCxxB	MASK1H97G	03-30-2000
B.0	0H97G	2101	.32µ TLM	XC	XPC823ZTxxB, XPC823ZCxxB	MASK0H97G	03-30-2000
A	0H89G, 1H89G	2100	.32µ TLM	XC	XPC823ZCxxA	MASK0H89G	03-30-2000
A	0H89G, 1H89G	2100	.32µ TLM	XC	XPC823ZTxxA	MASK0H89G	03-30-2000
0.3 (Z3)	5F98S, 3F98S	2002	.42µ TLM	XC	XPC823ZTxxZ3	MASK5F98S	03-17-1998
0.2 (Z2)	2F98S	2002	.42µ TLM	PC	PPC823ZTxxZ2	MASK2F98S	12-31-1997
0.1	1F98S	2001	.42µ TLM	PC	PPC823ZTxx	MASK1F98S	12-31-1997
0	0F98S	2000	.42µ TLM	PC	PPC823ZTxx	MASK0F98S	12-31-1997

NOTES:

1. Please contact your local Motorola Sales Office or Distributor for exact speeds available.
2. See Documentation section for errata documents listed (collateral ID given).

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MPC823 Parametrics

Description	Speed (Max) (MHz)	Dhrystone Performance (MIPS)	Cache-L1 Data (KBytes)	Cache-L1 Instructional (KBytes)	Translation Lookaside Buffers	Floating Point Unit	Parallel (Bits)	Power Dissipation (Typ) (Watts)	Microprogrammable Module	Miscellaneous Peripherals
PowerQUICC" Integrated Communications Processor for Portable Systems	81	107 @ 80MHz	1	2	8-entry	No	53	170m @25MHz	CPM	2 UARTs, 1IC, 1 SPI, USB

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MPC823 Documentation

Application Note

ID	Name	Format	Size K	Rev #	Date Last Modified	Order Availability
AN2065/D	MP8XX True Little-Endian Mode	pdf	75	0	2/02/1998	
AN2066/D	MP8xx SDRAM Interface	pdf	108	1.5	11/29/2001	
PPCEABI/D	Embedded Application Binary Interface (EABI): 32-Bit Implementations of the PowerPC Architecture	pdf	74	0	1/10/1995	

Data Sheets

ID	Name	Format	Size K	Rev #	Date Last Modified	Order Availability
MPC823ELE/D	MPC823 AC Electrical Specifications	pdf	487	1	10/25/2000	
MPC823PWR	MPC823 Power Consumption	pdf	52	-	1/01/1999	-

Engineering Bulletin

ID	Name	Format	Size K	Rev #	Date Last Modified	Order Availability
EB374/D	EB374 Differences Between the MPC82X Series Microprocessors	pdf	17	0.0	2/07/2001	

Errata

ID	Name	Format	Size K	Rev #	Date Last Modified	Order Availability
MPC823DIFF	Feature Differences Between Each Revision of the MPC823 Silicon	html	2	-	1/30/2002	-
MPC823_0F98S_CE/D	MPC823 Device Errata for Silicon Revision 0 - Mask Set 0F98S	pdf	24	3	12/31/1997	-
MPC823_0H89G_CE/D	MPC823 Device Errata for Silicon Revision A - Mask Set 0H89G, 1H89G	pdf	103	5	3/30/2000	-
MPC823_0H97G_CE/D	MPC823 Device Errata for Silicon Revision B.0 - Mask Set 0H97G	pdf	69	5	3/30/2000	-
MPC823_1F98S_CE/D	MPC823 Device Errata for Silicon Revision 0.1 - Mask Set 1F98S	pdf	24	3	12/31/1997	-
MPC823_1H97G_CE/D	MPC823 Device Errata for Silicon Revision B.1 - Mask Set1H97G	pdf	69	2	3/30/2000	-
MPC823_2F98S_CE/D	MPC823 Device Errata for Silicon Revision 0.2 - Mask Set 2F98S	pdf	23	0	12/31/1997	-
MPC823_3H97G_CE/D	MPC823 Device Errata for Silicon Revision B.2 - Mask Set 3H97G	pdf	68	2	3/30/2000	-
MPC823_5F98S_CE/D	MPC823 Device Errata for Silicon Revision 0.3 - Mask Set 5F98S, 3F98S	pdf	26	1	3/17/1998	-

Fact Sheets

ID	Name	Format	Size K	Rev #	Date Last Modified	Order Availability

MPC823FACT/D	MPC823 and MPC823e Integrated Communication Processors Fact Sheet	pdf	39	0	1/01/2000	
PPCCPUINTFACT/D	Fact Sheet - Motorola CPUs and Integrated Processors That Implement the PowerPC Architecture	pdf	476	3	5/01/2000	
PPCMKTFACT/D	Fact Sheet - Motorola Market Focus for Integrated and Host Processors	pdf	26	1	10/01/1999	

Miscellaneous

ID	Name	Format	Size K	Rev #	Date Last Modified	Order Availability
MPC823TS	MPC823 Mobile Computing Microprocessor Technical Summary	pdf	116	1	6/30/1999	-

Packages & Pinouts

ID	Name	Format	Size K	Rev #	Date Last Modified	Order Availability
MPC823PIN2	MPC823 Pin Functions Implemented From MPC821	pdf	19	1	11/14/1997	-
MPC823PIN3	MPC823 256-Pin PBGA Dimensional Drawing	pdf	61	0	1/01/1999	-
PBGAPRES	PBGA Customer Tutorial	pdf	2947	0	8/17/2000	-

Pocket Guide

ID	Name	Format	Size K	Rev #	Date Last Modified	Order Availability
MPC823RG/D	MPC823 Pocket Guide	pdf	211	1	4/01/1996	

Product Change Notices

ID	Name	Format	Size K	Rev #	Date Last Modified	Order Availability
PCN5911/D	MPC823 XC Qualification in TSMC/WaferTech-PCN5911	pdf	23	-	8/03/2001	-

Reference Manual

ID	Name	Format	Size K	Rev #	Date Last Modified	Order Availability
MPC823UM/D	MPC823 Reference Manual	pdf	4493	1	10/26/2000	
MPC823UMAD/D	Addendum to MPC823 and MPC823e Reference Manuals	pdf	9	0	11/01/2000	
MPC82XINSET	MPC823/MPC21 PowerPC Instruction Set	pdf	748	1	1/31/1997	-
MPCFPE32B/AD	Programming Environments Manual for 32-Bit Implementations of the PowerPC Architecture	pdf	6909	2	12/21/2001	
MPCFPE32BAD/AD	Errata to MPCFPE32B, Programming Environments Manual for 32-Bit Implementations of the Power PC Architecture, Rev. 2	pdf	40	0	10/11/2002	-
MPCFPE32B_CH	Individual chapter downloads from the Programming Environments Manual	html	6	2	12/21/2001	-
MPCPRG/D	Programmers Reference Guide for 32-Bit Implementations of the PowerPC Architecture	pdf	238	1	10/31/1995	

MPCPRGREF/D	PowerPC Microprocessor Family: The Programmer's Pocket Reference Guide	pdf	375	0	1/01/1996	

Reports or Presentations

ID	Name	Format	Size K	Rev #	Date Last Modified	Order Availability
ORDPARTS	Codec, Communication Processor, and ISDN Orderable Parts	pdf	61	-	7/30/2002	-

Selector Guide

ID	Name	Format	Size K	Rev #	Date Last Modified	Order Availability
SG1007/D	Network and Communications Processors Sales Guide	pdf	161	0	9/26/2002	

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MPC823 Development Tools/Boards

ID	Name	Vendor ID	Order Availability
MPC823FADS	MPC823 Family Application Development System	MOTOROLA	
CWEPPC	CodeWarrior Development Studio for PowerPC ISA	METROWERKS	
CWLINPPC	CodeWarrior Development Studio. Linux Application Edition for PowerPC	METROWERKS	

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Design Tools

BSDL Files

ID	Name	Vendor ID	Format	Size K	Rev #
MPC823JTAG	JTAG Boundary Scan File for MPC823 (12/02/97)	MOTOROLA	bdl	35	1.0

Debuggers

ID	Name	Vendor ID	Format	Size K	Rev #
MPC8BUGPKG	MPC8bug Monitor Debugger MPC8bug is a monitor debugger for the MPC8XX devices that runs on both SUN SPARCstations and PCs. Includes DOS compatibility. Requires 600K of memory. Via an ADI connection, it communicates with the MPC8xxFADS systems through the onboard ADS debug port. Open README file first. (03/20/1998)	MOTOROLA	zip	5399	1.3

Drivers

ID	Name	Vendor ID	Format	Size K	Rev #

MPC821IDMA	MPC821/MPC823 IDMA Driver The IDMA driver provides an initialization example and starts an IDMA transfer on the MPC821FADS system in the following modes: memory-to-memory, memory-to-peripheral, single address fly-by, and burst address fly-by. Special downloadable microcode routines are also included. Note: Use "pkzip -d" to unbundle. (02/19/97)	MOTOROLA	zip	63	-
MPC821MMU	MPC821/MPC823 MMU & Cache Driver The MMU and cache driver initializes the cache and MMU registers. It then dynamically maps regions for DRAM, FLASH, and internal I/O registers using the standard two-level segment and page descriptor tables. The virtual address of each region is mapped one-to-one to a physical address with page attributes that allow memory areas to be cacheable, cache-inhibited, or write-protected. Now includes fix for CPU2 errata. (09/15/98)	MOTOROLA	zip	79	-
MPC821MMUL	MPC821/MPC823 MMU Lite Driver Initializes the cache and MMU registers. Statically maps entire regions of DRAM, FLASH, and internal I/O registers by preloading the translation lookaside buffers with large page-size entries. This prevents TLB-miss exceptions that could degrade the performance of your system. The virtual address of each region is mapped one-to-one to a physical address with large page attributes that allow memory areas to be cacheable, cache-inhibited, or write-protected. This driver is perfect for benchmarking, but it can also be used in small systems that do not have a demand page memory allocation scheme. Requires very little memory. The MMU Lite executable, a README file, and source code is in a pkzip archive. The MPC8Bug monitor debugger is used to download the MMU Lite executable. (02/26/96)	MOTOROLA	zip	43	-
MPC821RTC	MPC821/MPC823 Real-Time Clock (RTC) Driver Operates the real-time clock (RTC). Can be configured to register an RTC interrupt once per second (per-second mode). Alternatively, can configure the interrupt period of the driver to be a 32-bit programmable value in units of seconds (alarm mode). Will light the ETH ON LED on the MPC821FADS system to indicate an RTC interrupt. (09/02/1997)	MOTOROLA	zip	54	-
MPC821SCCX	MPC821/MPC823 UART Driver (SCCx Interrupt) The SCCx UART driver supports internal loopback and two external loopback operating modes that you configure. This driver allows you to select the SCC that you want to use for UART. It also processes the SCC2 UART receive interrupt. (09/16/97)	MOTOROLA	zip	67	-
MPC821SMC2	MPC821/MPC823 UART Driver (SMC2 Polling) The SMC2 UART driver sets up SMC2 for UART communication. It then verifies the setup by performing a put, a get, and a poll for a single character. To use this code with the MPC821FADS, you must physically connect the SMC2 transmission and reception pins. The PKZIP archive contains the driver's source code and object files. (09/02/97)	MOTOROLA	zip	49	-
MPC821SPI	MPC821/MPC823 SPI Internal Loopback Driver The SPI Loopback Driver transmits and receives a single character that is 4 to 16 bits long and then it verifies the transmission. The driver operates in internal loopback mode. The character length (4..16 bits) and interrupt level (0..7) are both programmable. The SPI Loopback Driver processes the SPI receive interrupt. (09/02/97)	MOTOROLA	zip	62	-
MPC821TPD	MPC821/MPC823 SPI TouchPanel Driver Uses the on-chip SPI controller to communicate with the DynaPro DTFP95617 touch panel through a MAXIM MAX192 Analog/Digital converter. The touch event is processed as an IRQ1 interrupt. A pair of XY coordinates are received as 10-bit values from the A/D converter. The two sub-LSBs provided by the A/D converter are discarded and no scaling or calibration of the coordinates is performed. The SPI controller operates in master mode with 8-bit character length. A schematic of the touch panel interface to the MPC821 is included in the PKZIP archive. (09/02/97)	MOTOROLA	zip	105	-

MPC823I2C	MPC821/MPC823 I2C Driver This driver uses the on-chip I2C controller to transmit and receive 4 characters from a 128x8 Serial EEPROM. It is designed to work with either an MPC821 ADS board or an MPC823 FADS board. I2C interrupts are processed. Required: MPC821FADS (09/29/98)	MOTOROLA	zip	75	-
MPC823IRQ	MPC821/MPC823 IRQ Interrupt Driver (06/05/98) This sample driver services an externally generated IRQ* interrupt. The following interrupt parameters are programmable: 1. IRQ* Level: 1, 2, 7; 2. IRQ* Trigger Detection: Edge (Falling) or Level (Low) 3. IRQ* Handling Mechanism: Via Interrupt Service Routine or Polling	MOTOROLA	zip	61	-
MPC823MPANEL	MPC821/MPC823 LCD Driver - Multipanel This LCD driver initializes the MPC821 or MPC823 LCD controller for several LCD panels. Required: MPC821FADS (01/26/98)	MOTOROLA	zip	57	-
MPC823MPATT	MPC821/MPC823 LCD Driver - Multipattern This LCD driver initializes the MPC821/MPC823 LCD controller for the Hitachi LMG5320XUFC LCD panel (B/W operation only). After initialization is completed, the driver prompts the user via SMC1 to display one of several patterns. Note: Use "pkunzip -d" to unzip the archive. (01/26/98)	MOTOROLA	zip	827	-
MPC823PCMCIA	MPC823 PCMCIA Driver The PCMCIA driver performs a write and read access of a single half-word value on the FLASH memory card. This driver supports the following memory cards: SanDisk FlashDisk SDP3B 2M FLASH Memory Card, and Motorola MCM390180ATA 1.8M FlashDisk Memory Card. (09/04/97)	MOTOROLA	zip	62	-
MPC823SCC2E	MPC823 Ethernet Driver (External Receive) The Ethernet External Receive Driver processes external ethernet receive interrupts. Contains source and binary code for the Ethernet External Receive driver that runs specifically on the MPC823FADS. (08/17/99)	MOTOROLA	zip	36	-
MPC823USB	MPC823 USB Local Loopback Drivers Package This package contains a set of 4 sample programs that use the MPC823 USB controller in local loopback mode, running on the MPC823FADS board. Each sample program demonstrates one of the following transactions: IN, OUT, SETUP, and SOF. All possible USB interrupts are processed, and the expected results of each transaction are verified. (10/22/98)	MOTOROLA	zip	271	-
MPC823VCD	MPC823 Video Controller Driver (05/19/98)	MOTOROLA	exe	853	-

Libraries

ID	Name	Vendor ID	Format	Size K	Rev #
MPC823ORCAD	MPC823 (1.27mm and 1.00mm) and MPC821 OrCAD Library (11/30/98)	MOTOROLA	zip	13	-

Microcode

ID	Name	Vendor ID	Format	Size K	Rev #
MPC823I2CMICRO	I2C/SPI Microcode Package for MPC823 and MPC821 (02/06/97)	MOTOROLA	html	1	-
MPC823INTER	MPC823 Interlaced DMA Microcode Package This package is the one described on pg. 16-112 of the MPC823 User's Manual to add interlaced DMA functionality to older version MPC823s. For MPC823 silicon versions 0.3 (Z3) and later, you do not need to download this microcode. (5/20/98)	MOTOROLA	zip	1	-

MPC823IRDA	MPC823 Rev 0.3 Microcode Patch For IrDA This microcode patch is for MPC823 Rev 0.3 (Mask Numbers: 3F98S, 5F98S). This error was fixed in the Rev. A silicon; i.e., this patch is only to be used by Rev 0.3 silicon. (11/20/98)	MOTOROLA	zip	23	-
MPC823SOFGEN	MPC823 USB Host Start-of-Frame Package This microcode patch provides automatic start-of-frame (SOF) token generation functionality. ZIP file includes: USB S-Record Microcode Patch - S-RECORD, C version, Microcode Patch Implementation Notes. (4/10/00)	MOTOROLA	zip	7	-

Models

ID	Name	Vendor ID	Format	Size K	Rev #
MPC823IBIS1	MPC823 IBIS Model - JEDEC Please download the README file (MPC8XXIBIS). (01/24/2002)	MOTOROLA	zip	26	-
MPC823IBIS2	MPC823 IBIS Model - Motorola Please download the README file (MPC8XXIBIS). (01/24/2002)	MOTOROLA	zip	26	-
MPC8XXIBIS	README File for MPC8XX IBIS Models Please read before using the IBIS models for the MPC8xx products. (10/25/2001)	MOTOROLA	zip	0	-

Software

ID	Name	Vendor ID	Format	Size K	Rev #
MPC823CRC5	CRC5 Generator Package for USB The CRC5 Generator Package is built under Metrowerks CodeWarrior for the PC, and contains the C source code to compute the 5-bit CRC5. The CRC5, which is used in USB host mode token packets, is computed on the concatenation of the 7-bit address and 4-bit endpoint fields. The CRC5 must be computed in software because the MPC823 does not provide CRC5 hardware support. (04/19/99)	MOTOROLA	zip	52	-
MPC823HEADER	MPC823 Header File The MPC823 C header file contains a data structure which provides access to the complete set of internal memory mapped registers for the MPC823, as described in the MPC823 User's Manual. (10/16/98)	MOTOROLA	h	33	-
MPC823JPEG	MPC8xx JPEG Encoder/Decoder Package Unzip the file and see READ ME files. (06/11/98)	MOTOROLA	zip	1330	-
MPC823SDSMON	MPC823 SDS Monitor Package Using an RS-232 connection, the MPC823 SDS Monitor software provides communication between the MPC82xFADS board and the Single Step Debugger software. Required: MPC823 Family Application Development System (MPC823FADS) Note: Use "pkunzip -d" when unbundling. (08/31/98)	MOTOROLA	zip	435	-
MPC823SLAPIINS	Scalable Language API (SLAPI") Scalable Language API (SLAPI) is a specification that allows application developers to combine powerful speech recognition and language processing engines with their application software to create a product. SLAPI specifically addresses the need for low memory and limited computation. It is particularly suited for smart cellular phones, handheld PCs, set-top devices, and other personal systems. (01/05/00)	MOTOROLA	html	1	-
MPC823USBTEST	MPC823 USB API and Test Package This package, which only runs on both PCs and SUN Workstations, contains several USB tests that can be downloaded and run on a 823 FADS board. Open README file first. (08/15/97)	MOTOROLA	zip	1152	-

MPC860COD18	Example HDLC Bus Software (06/20/2002)	MOTOROLA	zip	45	0
UPM860	UPM860 Memory Controller Tool and Examples for MPC823 The UPM860 Memory Controller Tool is a freeware tool that can be used to program the memory controller of the MPC860, MPC821, and MPC823. (07/09/98)	MOTOROLA	zip	4196	-

Supporting Information

ID	Name	Vendor ID	Format	Size K	Rev #
823ERRATA	MPC823 Device Errata Table showing device errata, mask sets, revision numbers for MPC823. (01/31/2002)	MOTOROLA	html	8	-
DWARF	DWARF Debugging Information Format, Rev 1.1.0, UNIX International ©1992 (10/06/92)	MOTOROLA	pdf	163	1.1.0
MPC823BAUD	MPC821/MPC823 Asynchronous Baud Rate Tables The asynchronous baud rate tables contain additional information to Table 16-22 "Typical Baud Rates of Asynchronous Communication" in the MPC821 User's Manual. There is a separate table for system clock frequencies between 20 and 50MHz. In addition, each table contains the corresponding settings for the BRGC register. The files are in spreadsheet and C header file formats. (03/31/97)	MOTOROLA	zip	8	-
MPC823CHECK	MPC823 Design Checklist v1.3+	MOTOROLA	html	25	1.3+
MPC823CPM	MPC821/MPC823 CPM/CPU Interaction Writeup This application note provides information on interaction between the CPM and CPU. In particular: 1. Host Commands from the CPU that control CPM state. 2. Buffer Descriptors used by the CPM to transmit and receive data. 3. Event Registers in the CPM for use with microcode or interrupt processing. 4. Configuration Registers in the CPM that control its operation. (12/30/97)	MOTOROLA	pdf	25	-
MPC823CRYS	MPC821/MPC823 Crystal Oscillator Characteristics and Design Notes (02/18/98)	MOTOROLA	pdf	29	-
MPC823HINTS	MPC821/MPC823 Performance Optimizing Hints Download this file for tips on how to get the best performance out of your MPC821 and MPC823. (01/15/97)	MOTOROLA	pdf	3	-
MPC823ICAN	MPC821/MPC823 CPM Interrupt Controller Programming Model This application note provides introductory information on the CPM Interrupt Controller programming model for MPC8XX Family processors. Also included is a sample C program listing that processes an interrupt generated by the CPM. (12/30/97)	MOTOROLA	pdf	46	-
MPC823LCD	MPC821/MPC823 LCD Controller Bus Utilization Spreadsheet This is a spreadsheet that helps you compute the percentage of System Bus utilization consumed by the LCD controller on MPC8XX Family Embedded Microprocessors. The input parameters are: System Frequency, LCD Refresh Frequency, LCD Panel Row and Column Resolution, and Memory Burst Characteristics. (12/23/97)	MOTOROLA	xls	16	-
MPC823LEM	MPC8xx True Little-Endian Mode Application Note (03/05/98)	MOTOROLA	pdf	55	-

MPC823OVER	Video Controller Application Note: Overlaying MPC823 Graphics on a Remote Video Source This application note demonstrates the considerable power and flexibility of the MPC823 and its integrated video controller. (11/27/98)	MOTOROLA	pdf	228	0.6
MPC823PERF	MPC821/MPC823 CPM Utilization Note and Spreadsheet (01/09/98)	MOTOROLA	zip	24	-
MPC823TIME	MPC823 Electrical Timing Specifications Spreadsheet (10/28/98)	MOTOROLA	xls	319	-
MPC823USB10	USB 1.0 Compliance Checklist (Peripheral Silicon) (07/19/99)	MOTOROLA	pdf	69	-
MPC823USB11	USB 1.1 Compliance Checklist (Peripheral Silicon) (07/27/99)	MOTOROLA	pdf	61	-
MPC82XBAR	MPC82X Bar Code Reader Microcode Package Manual (07/02/98)	MOTOROLA	pdf	61	-
MPC8XXSDRAM	MPC8XX SDRAM Interface Application Note This application note provides a brief introduction to SDRAMs (Synchronous DRAMs) and how to interface an MPC8XX microprocessor to them, using the MPC8XX on-chip memory controller. A sample SDRAM init file for MPC8bug is included. (bugsdram.txt) (12/30/97)	MOTOROLA	zip	65	-
MPC8XXSIU	MPC8xx SIU Interrupt Controller Programming Model This application note provides introductory information on the SIU (System Interface Unit) Interrupt Controller programming model for MPC8XX Family processors. Also included is a sample C program listing that processes an SIU interrupt. (12/30/97)	MOTOROLA	pdf	60	-
MPC8XX_MMUCACHE	MPC8XX Performance Driven Optimization of Caches and MMUs (01/31/2002)	MOTOROLA	zip	66	-
PPCABI	ABI: System V Application Binary Interface: Processor Supplement, 1995 (Note: Pages are in reverse order) (09/01/95)	MOTOROLA	pdf	327	-
PPCEXCP	MPC8xx Core Exception Processing Programming Model This application note provides introductory information on the embedded CPU exception processing programming model. The application note also provides a sample C program that processes a system call exception. (12/30/97)	MOTOROLA	pdf	47	-

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Orderable Parts Information

PartNumber	Package Info	Life Cycle Description (code)	Remarks	Budgetary Price QTY 1000+ ($US)	Order Availability
KXPC823ZT81B2T	PBGA 256 23*23*1.5P1.27	PRODUCT STABLE GROWTH/MATURITY(3)	part number for ordering samples only	-	
XPC823CVF66B2	MAPBGA 256 17*17*1.6P1.0	PROD PHASE OUT/SEE LAST ORD DT(6) 08 Apr 2003	66MHz, extended temp	-	-
XPC823CZT66B2	PBGA 256 23*23*1.5P1.27	PRODUCT STABLE GROWTH/MATURITY(3)	66MHz, extended temp	-	-

XPC823CZT66B2T	PBGA 256 23*23*1.5P1.27	PRODUCT STABLE GROWTH/MATURITY(3)	66MHz, extended temp	-	
XPC823VF66B2	MAPBGA 256 17*17*1.6P1.0	PROD PHASE OUT/SEE LAST ORD DT(6) 08 Apr 2003	66MHz	-	-
XPC823VF75B2	MAPBGA 256 17*17*1.6P1.0	PROD PHASE OUT/SEE LAST ORD DT(6) 08 Apr 2003	75MHz	-	-
XPC823VF81B2	MAPBGA 256 17*17*1.6P1.0	PROD PHASE OUT/SEE LAST ORD DT(6) 08 Apr 2003	81MHz	-	-
XPC823ZT66B2T	PBGA 256 23*23*1.5P1.27	PRODUCT STABLE GROWTH/MATURITY(3)	66MHz	-	
XPC823ZT75B2T	PBGA 256 23*23*1.5P1.27	PRODUCT STABLE GROWTH/MATURITY(3)	75MHz	-	
XPC823ZT81B2T	PBGA 256 23*23*1.5P1.27	PRODUCT STABLE GROWTH/MATURITY(3)	81MHz	-	

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