UT54ACS191/UT54ACTS191

Radiation-Hardened
Synchronous 4-Bit Up-Down Binary Counters

FEATURES

- Single down/up count control line
-
  counters
- Fully synchronous in count modes
- Asynchronously presetable with load control
- 1.2µ radiation-hardened CMOS

- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
  - 16-pin DIP
  - 16-lead flatpack

DESCRIPTION

The UT54ACS191 and the UT54ACTS191 are synchronous 4-bit reversible up-down binary counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed. Synchronous operation eliminates the output counting spikes associated with asynchronous counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ($\overline{CTEN}$) is low. A logic one applied to $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up and when D/$\overline{U}$ is high, it counts down.

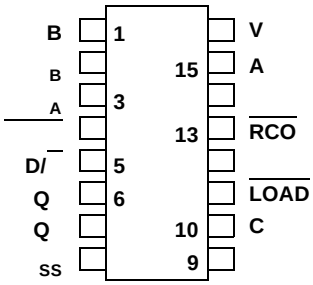
The counters feature a fully independent clock circuit. Changes at control inputs ($\overline{CTEN}$ and D/$\overline{U}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs.

The counters are fully programmable. The outputs may be preset to either logic level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. The asynchronous load allows counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

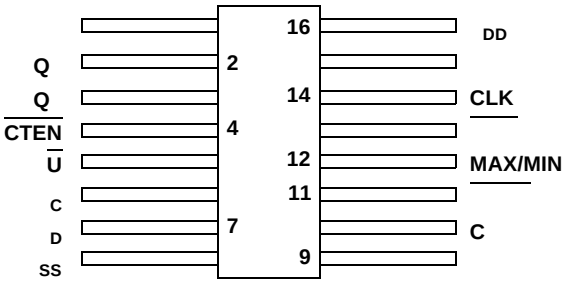
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum (MAX/MIN) count. The MAX/MIN output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (15) counting up.

PINOUTS

16-Pin DIP
Top View



16-Lead Flatpack
Top View



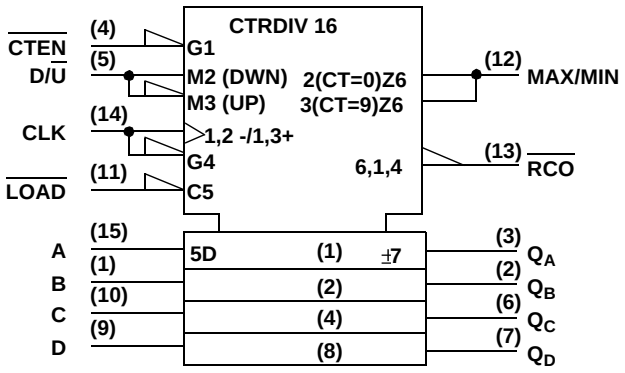
The ripple clock output ($\overline{RCO}$) produces a low-level output pulse under those same conditions but only while the clock input is low. The counters easily cascade by feeding the $\overline{RCO}$ to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. Use the MAX/MIN count output to accomplish look-ahead for high-speed operation.

The devices are characterized over full military temperature range of -55°C to +125°

FUNCTION TABLE

FUNCTION	$\overline{LOAD}$	$\overline{CTEN}$	D/$\overline{U}$	CLK
Count Up	H	L	L	↑
Count Down	H	L	H	↑
Asynchronous Reset	L	X	X	X
No Change	H	H	X	X

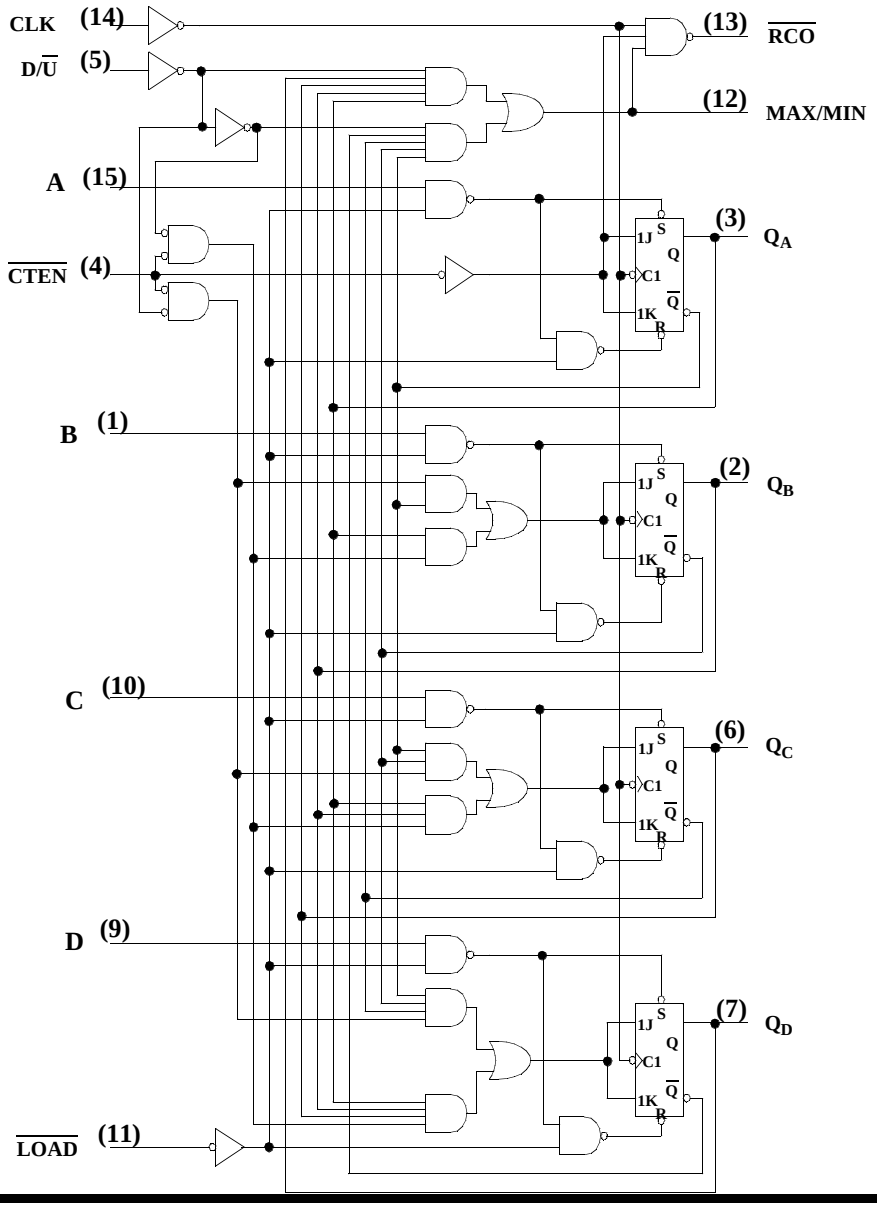
LOGIC SYMBOL



Note:

1. Logic symbol in accordance with ANSI/IEEE standard 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM



RADIATION HARDNESS SPECIFICATIONS [1]

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU Threshold [2]	80	MeV-cm^2/mg
SEL Threshold	120	MeV-cm^2/mg
Neutron Fluence	1.0E14	n/cm^2

Notes:
1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage any pin	-.3 to V_{DD} +.3	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
T_{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ_{JC}	Thermal resistance junction to case	20	°C/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation	1	W

Note:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	4.5 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to + 125	°C

DC ELECTRICAL CHARACTERISTICS [7]

(V_{DD} = 5.0V ±10%; V_{SS} = 0V [6], -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IL}	Low-level input voltage [1] ACTS ACS			0.8 .3V_{DD}	V
V_{IH}	High-level input voltage [1] ACTS ACS		.5V_{DD} .7V_{DD}		V
I_{IN}	Input leakage current ACTS/ACS	V_{IN} = V_{DD} or V_{SS}	-1	1	µA
V_{OL}	Low-level output voltage [3] ACTS ACS	I_{OL} = 8.0mA I_{OL} = 100µA		0.40 0.25	V
V_{OH}	High-level output voltage [3] ACTS ACS	I_{OH} = -8.0mA I_{OH} = -100µA	.7V_{DD} V_{DD} - 0.25		V
I_{OS}	Short-circuit output current [2,4] ACTS/ACS	V_O = V_{DD} and V_{SS}	-200	200	mA
I_{OL}	Output current[10] (Sink)	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V	8		mA
I_{OH}	Output current[10] (Source)	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD} - 0.4V	-8		mA
P_{total}	Power dissipation [2, 8, 9]	C_L = 50pF		2.1	mW/ MHz
I_{DDQ}	Quiescent Supply Current	V_{DD} = 5.5V		10	µA
ΔI_{DDQ}	Quiescent Supply Current Delta ACTS	For input under test V_{IN} = V_{DD} - 2.1V For all other inputs V_{IN} = V_{DD} or V_{SS} V_{DD} = 5.5V		1.6	mA
C_{IN}	Input capacitance [5]	f = 1MHz @ 0V		15	pF
C_{OUT}	Output capacitance [5]	f = 1MHz @ 0V		15	pF

Notes:

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(min) + 20\%, - 0\%$; $V_{IL} = V_{IL}(max) + 0\%, - 50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density $\leq 5.0E5$ amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6. Maximum allowable relative shift equals 50mV.
7. All specifications valid for radiation dose $\leq$ 1E6 rads(Si).
8. Power does not include power contribution of any TTL output sink current.
9. Power dissipation specified per switching output.
10. This value is guaranteed based on characterization data, but not tested.

AC ELECTRICAL CHARACTERISTICS [2]

(V_{DD} = 5.0V ±10%; V_{SS} = 0V [1], -55°C < T_C < +125°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{PLH}	$\overline{LOAD}$ to Q_n	2	20	ns
t_{PHL}	$\overline{LOAD}$ to Q_n	2	22	ns
t_{PLH}	Data In to Q_n	2	23	ns
t_{PHL}	Data In to Q_n	2	19	ns
t_{PLH}	CLK to Q_n	2	17	ns
t_{PHL}	CLK to Q_n	2	22	ns
t_{PLH}	CLK to $\overline{RCO}$	2	12	ns
t_{PHL}	CLK to $\overline{RCO}$	2	15	ns
t_{PLH}	CLK to MAX/MIN	2	22	ns
t_{PHL}	CLK to MAX/MIN	2	23	ns
t_{PLH}	D/$\overline{U}$ to $\overline{RCO}$	2	16	ns
t_{PHL}	D/$\overline{U}$ to $\overline{RCO}$	2	18	ns
t_{PLH}	D/$\overline{U}$ to MAX/MIN	2	15	ns
t_{PHL}	D/$\overline{U}$ to MAX/MIN	2	17	ns
t_{PLH}	$\overline{CTEN}$ to $\overline{RCO}$	2	12	ns
t_{PHL}	$\overline{CTEN}$ to $\overline{RCO}$	2	16	ns
f_{MAX}	Maximum clock frequency		63	MHz
t_{SU1}	$\overline{LOAD}$, $\overline{CTEN}$, D/$\overline{U}$ Setup time before CLK ↑	12		ns
t_{SU2}	A, B, C, D setup time before $\overline{LOAD}$ ↑	5		ns
t_{H1}	$\overline{CTEN}$ and D/$\overline{U}$ hold time after CLK ↑	2		ns
t_{H2} [3]	A, B, C, D hold time after $\overline{LOAD}$ ↑	2		ns
t_W	Minimum pulse width CLK high CLK low $\overline{LOAD}$ low	8		ns

Notes:
1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose ≤ 1E6 rads(Si).
3. Based on characterization, hold time (t_{H2}) of 0ns can be assumed if data setup time (t_{SU2}) is ≥10ns. This is guaranteed, but not tested.