QL2020
20,000 Gate pASIC® 2 FPGA
Combining Speed, Density, Low Cost and Flexibility

ADVANCED DATA

pASIC 2 HIGHLIGHTS

Ultimate Verilog/VHDL Silicon Solution
-Abundant, high-speed interconnect eliminates manual routing
-Flexible logic cell provides high efficiency *and* performance
-Design tools produce fast, efficient Verilog/VHDL synthesis

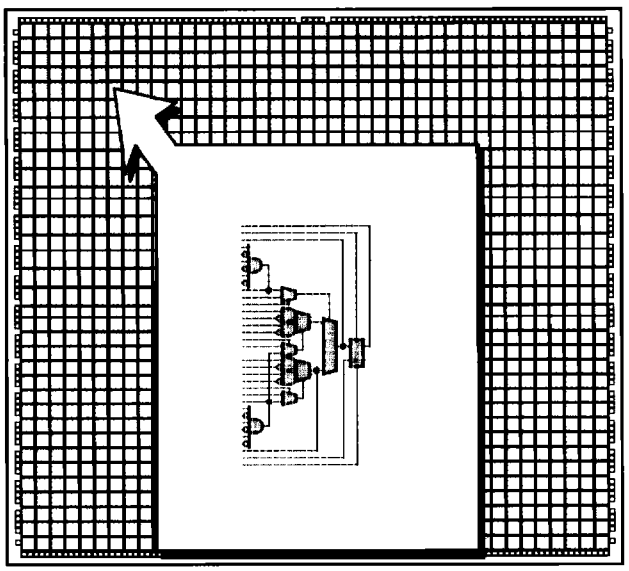
Speed, Density, Low Cost and Flexibility in One Device
... 20,000 usable gates, 336 I/O pins

-Datapath speeds exceeding 200 MHz
-20,000 to 25,500 usable gates, 336 I/Os
-3-layer metal ViaLink® process for smallest die sizes
-100% routable and pin-out maintainable

Advanced Logic Cell and I/O Capabilities
-Complex functions (up to 16 inputs) in a single logic cell
-High synthesis gate utilization from logic cell fragments
-Full IEEE Standard 1149.1a JTAG boundary scan capability
-Individually-controlled input/feedback registers and OEs on all I/O pins

Other Important Family Features
-Low standby power
-I/O pin-compatibility between different devices in the same packages
-PCI compliant, full speed 33 MHz master and target implementations
-High design security provided by security fuses

QL2020 Block Diagram



1440 Logic Cells

QUICKLOGIC

PRODUCT SUMMARY

The QL2020 is a 20,000 usable gate member of the pASIC 2 family of FPGAs. pASIC 2 FPGAs employ a unique combination of architecture, technology, and software tools to provide high speed, high usable density, low price, and flexibility in the same devices. The flexibility and speed make pASIC 2 devices an efficient and high performance silicon solution for designs described using HDLs such as Verilog and VHDL, as well as schematics.

The QL2020 contains 1440 logic cells, each with the logic capacity of 40 gate array gates, giving the device a total capacity of over 57,000 gates. As a typical application will use 13 to 15 gates per logic cell, the QL2020 is described as a 20,000 usable gate device. However, comparative analysis shows that the QL2020 will implement designs requiring up to 25,500 gates from competitive FPGA devices. With 336 maximum I/Os, the QL2020 is available in 208-PQFP, 352-PBGA, and over 500-pin PBGA packages.

Software support for the complete pASIC 1 and 2 families, including the QL2020, is available through two basic packages. The turnkey Quick*Works*™ package provides the most complete FPGA software solution from design entry to logic synthesis (by Synplicity, Inc.), to place and route, to simulation. The Quick*Tools*™ package provides a solution for designers who use Cadence, Mentor, Synopsys, Viewlogic, Intergraph, or other third-party tools for design entry, synthesis, or simulation.

FEATURES

Total of 336 I/O Pins

- 328 bidirectional input/output pins, PCI-compliant in -1/-2 speed grades
- 4 high-drive input-only pins
- 4 high-drive input/distributed network pins

Four Low-Skew (less than 0.5ns) Distributed Networks

- Two array networks available to logic cell flip-flop clock, set, and reset - each driven by an input-only pin
- Two global clock/control networks available to F1 logic input, and logic cell flip-flop clock, set, reset; input and I/O register clock, reset, enable; and output enable controls - each driven by an input-only pin, or any input or I/O pin, or any logic cell output or I/O cell feedback

High Performance

- Input + logic cell + output delays under 6 ns
- Datapath speeds exceeding 200 MHz
- Counter speeds over 175 MHz