

ADM8515/X

USB2.0 to 10/100 Mbit/s Ethernet LAN Controller
ADM8515/X

Communications



N e v e r s t o p t h i n k i n g .

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USB2.0 to 10/100 Mbit/s Ethernet LAN Controller

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1 Product Overview

The ADM8515/X, USB based chip set, provides desktop, notebook and computer peripheral with greater connectivity and data-transmission to Ethernet and home network. The ADM8515X is the environmentally friendly "green" package version.

The ADM8515/X device combines USB2.0 transceiver with UTMI interface, an EP decoder used for USB interface through Parallel Interface Engine (PIE), FIFO controller with 24K SRAM, 64 byte and 2K byte buffers, 10/100 Mbit/s Ethernet physical layer (PHY) and MII interface.

It is capable of providing an easy, universal connectivity to computer peripherals with USB. The transfer rate of USB interface is 480 Mbit/s belonging to a high speed USB device. The ADM8515/X supports all USB commands, 4 endpoints and suspend/resume function.

The ADM8515/X's LAN PHY supports 100 Base TX (100 Mbit/s mode) and 10 Base T (10 Mbit/s mode) full-duplex operations. It uses the auto-negotiation function to optimize the network traffic and the built-in 24K bytes SRAM for receiving buffer, especially for 100 Mbit/s. Through FIFO controller, data can communicate in fluently between buffers and external device. To obtain the better signal quality, the PHY provides wave-shaper, filter and adaptive equalizer to reach. By using diagnostic mechanism (loop-back mode), the data correctness will be increased. The LAN PHY supports external transmit/receive transformer turn ratio 1:1. The ADM8515/X chip set can be programmed for MAC analysis and provides MII interface for external PHY, such as MII interface for HomePNA and Homeplug. In system application, EEPROM is essential in that it needs to load device ID, vendor ID automatically. So for ADM8515/X, serial interface is applied for EEPROM communication including read/write function. Furthermore, some LED pins report system statuses. Infineon-ADMtek provides an EEPROM Access Program utility for programming vendor ID, Product ID Etc.

ADM8515/X is ideally suited for USB adapter and intelligent networked peripheral design. It can also be used in Wide Area Network (WAN), such as xDSL, Cable Modem, router, and Information Appliance (IA) application etc.

1.1 Package Information

Table 1 Package Information

Product Name	Product Type	Package	Ordering Number
ADM8515/X	ADM8515/X-AC-T-1	P-LQFP-100-1	Q67801H 24A101

1.2 Features

Main features:

- **Industrial Standard**
 - IEEE 802.3u 100BASE-TX and IEEE 802.3 10BASE-T compliant
 - Supports IEEE 802.3x flow control
 - Supports IEEE 802.3u Auto-Negotiation for 10BASE-T and 100BASE-TX
 - USB specification 2.0 compliant
- **USB Interface**
 - High speed USB Device
 - Supports 1 USB configuration and 1 interface
 - Supports all USB standard commands
 - Supports two vendor specific commands
 - Supports USB Suspend/Resume detection logic
 - Supports 4 endpoints: 1 control endpoint with maximum 64-byte packet, 1 bulk IN endpoint with maximum 512-byte packet, 1 bulk OUT endpoint with maximum 512-byte packet and 1 interrupt IN endpoint with maximum 8-byte packet
- **MAC/PHY**

- Integrates the whole physical layer functions of 100BASE-TX and 10BASE-T by using PHY address 1
- Can be programmed to isolate the internal PHY, supports MII interface to external 10/100 PHY
- Supports configurable threshold for PAUSE frame
- Supports wakeup frame, link status change and magic packet wake-up
- Supports full-duplex operation on both 100 Mbit/s and 10Mbit/s speed modes
- Supports Auto-Negotiation (N-Way) function of full/half duplex operation for both 10/100 Mbit/s
- Provides transmit wave-shaper, receives filter, and adapter equalizer
- Provides MLT-3 transceiver with DC restoration for Base-Line Wander compensation
- Supports MAC and Transceiver loop back diagnostic modes
- Supports external transmit/receive transformer with turn ratio 1:1
- **EEPROM Interface**
 - Provides serial interface to access 93C46 EEPROM
 - Automatically load device ID, vendor ID from EEPROM after power-on reset
- **FIFO**
 - Supports internal 2K bytes SRAM for transmission
 - Supports internal 24K bytes synchronous SRAM for receiving
- **LED Interface**
 - Provides 4 LED display modes
 - Provides USB full speed/high speed display modes
- **Support Power Save Function @ USB suspend mode**
 - Mode 0: Resume by remote wakeup or host when OS goes into standby
 - Mode 1: Resume by host when OS goes into standby.
 - Power consumption < 2.5 mA @ mode 1
- **Support Software**
 - Windows 98/ME/2000/XP driver
 - Linux driver
 - WinCE 3.0 & 4.0 drivers
 - EEPROM burn-in program
 - MFG testing program
- **Miscellaneous**
 - Supports 6 GPIO pins
 - Provides 100-pin LQFP package
 - 3.3 V power supply with 5 V/3.3 V I/O tolerance

1.3 Block Diagram

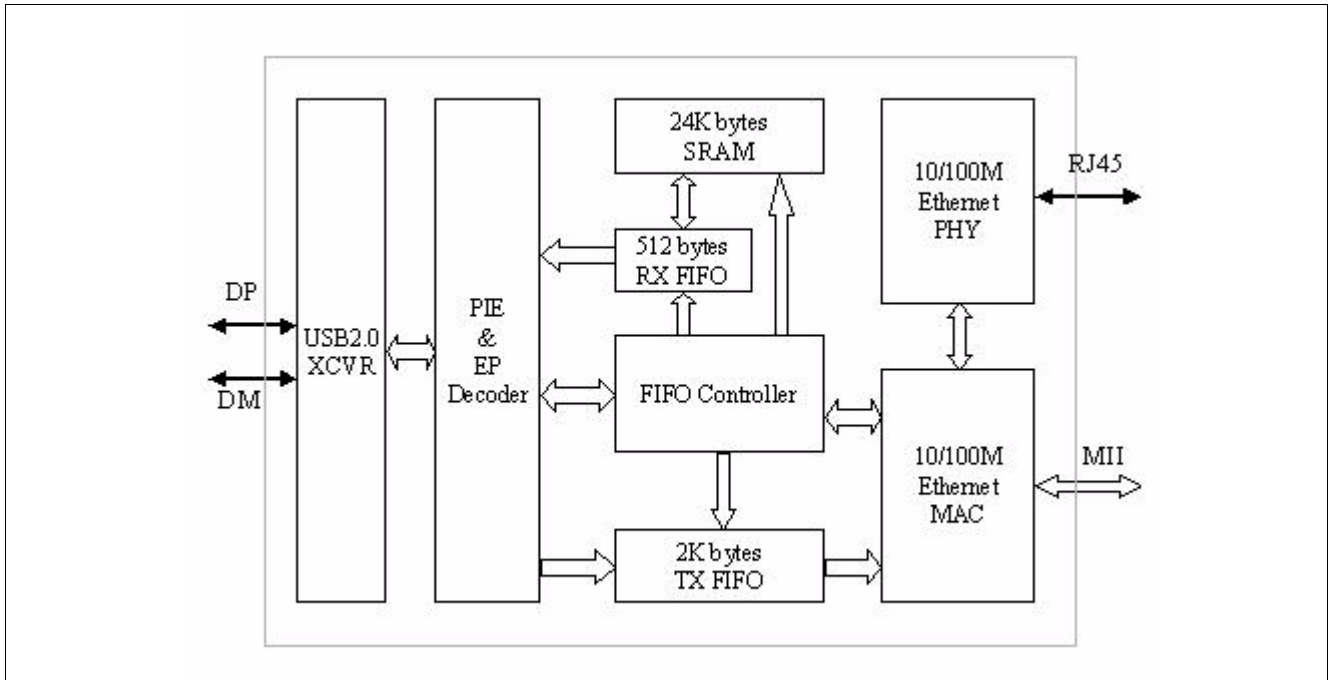


Figure 1 Block Diagram

1.4 Conventions

1.4.1 Data Lengths

qword 64 bits

dword 32 bits

word 16 bits

byte 8 bits

nibble 4 bits

2 Interface Description

2.1 Pin Diagram

Pin Diagram of ADM8515/X.

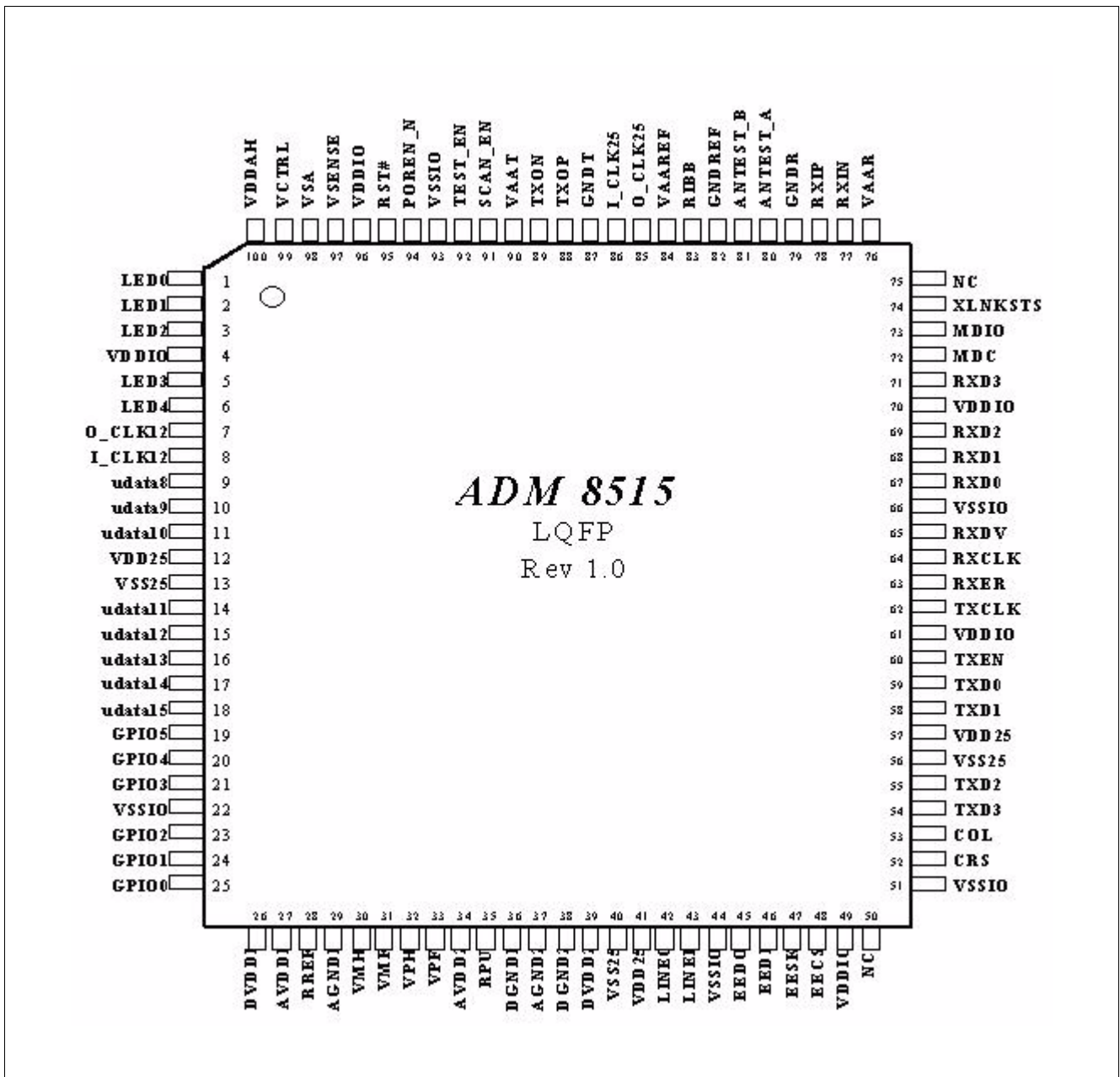


Figure 2 Pin Diagram

2.2 Pin Description by Function

ADM8515/X pins are categorized into one of the following groups:

- Host Interface
- MII Interface
- Physical Layer Interface
- LED Display Mode
- EEPROM Interface
- Regulator Pins
- Power Pins
- Miscellaneous

Table 2 Abbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or Output. Analog levels.
PWR	Power
GND	Ground
MCL	Must be connected to Low (JEDEC Standard)
MCH	Must be connected to High (JEDEC Standard)
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 3 Abbreviations for Buffer Type

Abbreviations	Description
Z	High impedance
PU1	Pull up, 10 k Ω
PD1	Pull down, 10 k Ω
PD2	Pull down, 20 k Ω
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OC	Open Collector
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).
OD/PP	Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.
ST	Schmitt-Trigger characteristics
TTL	TTL characteristics

2.2.1 Host Interface

Table 4 Host Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
8	I_CLK12	I		Input Clock 12 MHz clock input from crystal or oscillator.
7	O_CLK12	O		Output for Crystal
95	RST#	I		External Hardware Reset Input Schmitt trigger, internal pull high.
94	POREN_N	I		Internal Power on Reset Logic Enable Default is enable and internal pull-low. When external hardware reset is used, this pin should be connected to Vcc via 4.7 kΩ resistor.
32	VPH	I/O		USB D + Port for High Speed
30	VMH	I/O		USB D - Port for High Speed
33	VPF	I/O		USB D + Port for Full Speed
31	VMF	I/O		USB D - Port for Full Speed
28	RREF			Pull Down with 510 Ohm Precise Resistor (± 1%)
35	RPU			Pull up with a 1.5 k Ohm Resistor
42	LINE0	O		USB Line State They directly reflect the current state of the DP (LINE1) and DM (LINE0) signals, see Table 5
43	LINE1			

Table 5 DM and DP Signals

DM	DP	Description
0	0	0: SE0
0	1	1: "J" State
1	0	2: "K" State
1	1	3: SE1

2.2.2 MII Interface

Note: Program ADM8515/X as MAC-only mode, set register 81_H[4:2] = 001_B and register 01_H bit 2 = 0

Table 6 MII Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
53	COL	I		Collision Detected This signal is asserted high asynchronously by the external physical unit upon detection of a collision on the medium. It will remain asserted as long as the collision condition persists.
52	CRS	I		Carrier Sense This signal is asserted high asynchronously by the external physical unit upon detection of a non-idle medium.
72	MDC	O		Management Data Clock Clock signal with a maximum rate of 2.5 MHz used to transfer management data for the external PMD on the MDIO pin.
73	MDIO	I/O		Management Data I/O Bi-directional signal used to transfer management information for the external PMD. Requires a 1.5 kΩ pull-up resistor if external PHY is used.
64	RXCLK	I		Receive Clock A continuous clock that is recovered from the incoming data. During 100 Mbit/s operation, RXCLK is 25 MHz. During 10 Mbit/s, this is 2.5 MHz.
71	RXD3	I		Receive Data This is a group of 4 data signals aligned on nibble boundary which are driven synchronous to the RXCLK by the external physical unit. RXD[3] is the most significant bit and RXD[0] is the least significant bit.
69	RXD2			
68	RXD1			
67	RXD0			
65	RXDV	I		Receive Data Valid This indicates that the external physical unit is presenting recovered and decoded nibbles on the RXD[3:0] and that RXCLK is synchronous to the recovered data
63	RXER	I		Receive Error This signal is asserted high synchronously by the external physical unit whenever it detects a media error and RXDV is asserted. If not used, it should be grounded, e.g. isolate internal PHY and use external PHY.
62	TXCLK	I		Transmit Clock A continuous clock that gets its source by the physical layer. During 100 Mbit/s operation, this clock is 25 MHz. During 10 Mbit/s operation, this clock is 2.5 MHz.

Interface Description

Table 6 MII Interface (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
54	TXD3	O		Transmit Data This is a group of 4 data signals which are driven synchronously to the TXCLK for transmission to the external physical unit. TXD[3] is the most significant bit and TXD[0] is the least significant bit.
55	TXD2			
58	TXD1			
59	TXD0			
60	TXEN	O		Transmit Enable This signal is synchronous to TXCLK and provides precise framing for data carried on TXD[3:0]. It is asserted when TX[3:0] contains valid data to be transmitted. Requires external pull-down resistor 4.7 k Ω if external PHY is used.
74	XLNKSTS	I		Link Status Indication External PHY reports link status information to system and level change trigger. Connect to external PHY's link status report pin or pull-down to low if not used.

2.2.3 Physical Layer Interface

Table 7 Physical Layer Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
85	O_CLK25	O		Crystal Out 25 MHz
86	I_CLK25	I		Crystal In 25 MHz
78	RXIP	I		Receives Inputs The differential receives inputs of 100BASE-TX or 10BASE-T, these pins directly input from Magnetic.
77	RXIN			
88	TXOP	O		Transmits Outputs The differential transmits outputs of 100BASE-TX or 10BASE-T, these pins directly output to Magnetic.
89	TXON			
83	RIBB	I		Reference Bias Resistor To be tied to an external 10.0 k Ω (1%) resistor which should be connected to the analog ground at the other end.
80	ANTEST_A	O		PHY Test Pins
81	ANTEST_B			

2.2.4 LED Display Mode

Table 8 LED Display Mode

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
1	LED0	O		Function of LED0 Function of LED0 is described below.
2	LED1	O		Function of LED1 Function of LED1 is described below.
3	LED2	O		Function of LED2 Function of LED2 is described below.
5	LED3	O		LED Display for USB Full LED display for USB full speed rate link, active high.
6	LED4	O		LED Display for USB High LED display for USB high speed rate link, active high.

The LED interface is EEPROM programmable, 2 EEPROM control bits, Address OB [7:6] in EEPROM are used to select the LED display mode.

Notes

- EEPROM 0B[7:6] = 00_B**
LED0: 100 Mbit/s (on, drive '0') or 10 Mbit/s (off, drive '1')
LED1: Link (keeps on when link on) or Activity (Flash with 10 Hz when ADM8515/X is receiving or transmitting without collision)
LED2: Full duplex (keeps on when in full duplex mode) or Collision (flash with 20 Hz when collision occurred in half duplex mode)
- EEPROM 0B[7:6] = 01_B**
LED0: Activity (Flash with 10 Hz when ADM8515/X is receiving or transmitting without collision)
LED1: Link 10 (keeps on when link on 10 Mbit/s)
LED2: Link 100 (keeps on when link on 100 Mbit/s)
- EEPROM 0B[7:6] = 10_B**
LED0: 100 Mbit/s (on, drive '0') or 10 Mbit/s (off, drive '1')
LED1: Activity (Flash with 10 Hz when ADM8515/X is receiving or transmitting without collision)
LED2: Link (keeps on when link on)
- EEPROM 0B[7:6] = 11_B**
LED0: Link 10 (LED on when link on 10Mbit/s) and Activity (Flash with 10Hz when ADM8515/X is receiving or transmitting without collision)
LED1: Link 100 (LED on when link on 100Mbit/s) and Activity (Flash with 10Hz when ADM8515/X is receiving or transmitting without collision)
LED2: Full duplex (keeps on when in full duplex mode)

2.2.5 EEPROM Interface

Table 9 EEPROM Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
48	EECS	O		EEPROM Chip Select This pin enables the EEPROM during loading of the Ethernet configuration data.
46	EEDI	O		EEPROM Data In ADM8515/X will use this pin to serially write opcodes, addresses and data into the serial EEPROM.
45	EEDO	I		EEPROM Data Out ADM8515/X will read the contents of the EEPROM serially through this pin.
47	EESK	O		EEPROM Clock After reset, ADM8515/X will auto-load the contents of the EEPROM by using EESK, EEDO, and EEDI. This pin provides the clock for the EEPROM device.

2.2.6 Regulator Pins

Table 10 Regulator Pins

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
100	VDDAH	P		Chip Regulator 3.3 V power supply for on chip regulator.
98	VSA	P		Ground for Regulator
99	VCTRL	I/O		Regulator Control Pin
97	VSENSE	I		2.5 V Voltage Sense Input

Note: ADM8515/X is a dual power device, it needs both 3.3 V and 2.5 V power supply. Inside the chip, there is an embedded 3.3 V to 2.5 V power regulator that can generate the needed 2.5 V power to supply the chip. The reference schematics design is shown in [Figure 3](#)

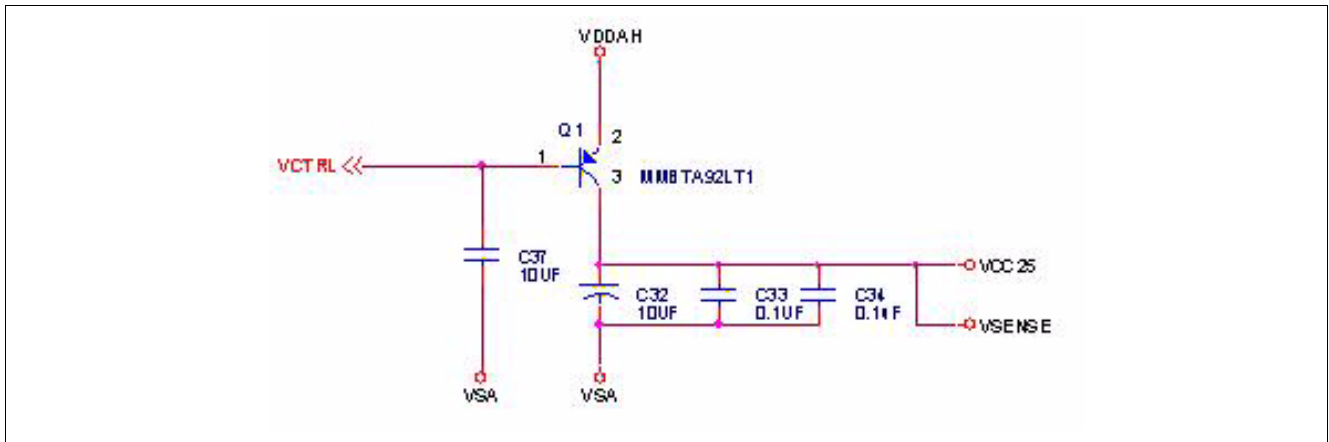


Figure 3 Reference Design

2.2.7 Power Pins

Table 11 Power Pins

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
12, 41, 57	VDD25	P		2.5 V Power Supply for Core
13, 40, 56	VSS25	P		Ground for VDD25
4, 49, 61, 70, 96	VDDIO	P		3.3 V Power Supply for I/O
22, 44, 51, 66, 93	VSSIO	P		Ground for VDDIO
26	DVDD1	P		2.5 V Digital Power Supply
39	DVDD2			
36	DGND1	P		Digital Ground
38	DGND2			
27	AVDD1	P		3.3 V Analog Power Supply
34	AVDD2			
29	AGND1	P		Analog Ground
37	AGND2			
90	VAAT	P		3.3 V Power Supply for Transmitter
87	GNDT	P		Ground for VAAT
76	VAAR	P		3.3 V Power Supply for Receiver
79	GNDR	P		Ground for VAAR
84	VAAREF	P		3.3 V Power Supply for PHY
82	GNDREF	P		Ground for VAAREF

2.2.8 Miscellaneous

Table 12 Miscellaneous

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
19	GPIO5	I/O		General Purpose Input/Output Pins These pins are used as general purpose Input/Output pins. These pins are internal pull-low.
20	GPIO4			
21	GPIO3			
23	GPIO2			
24	GPIO1			
25	GPIO0			
92, 91	TEST 1	I		Test Pins
9, 10, 11, 14, 15, 16, 17, 18	TEST2	I/O		Test Pins

3 Function Description

3.1 USB Interface

USB is a straightforward solution when you want to use a computer for communication with devices outside the computer. The interface is suitable for one-of-a-kind and small-scale designs as well as mass-produced, standard peripheral. The benefits of USB are easy to use and easy to apply, fast and reliable data transfers, flexibility, cost, and power conservation.

3.1.1 PIE

PIE (Parallel Interface Engine) is to control USB communications and check USB protocol, then transfer protocol to EP decoder. The PIE and USB transceivers, which provide the hardware interface to the USB cable, together comprise the USB engine.

3.1.2 EP Decoder

The detail description is in Section 4.5 USB Command.

3.2 MAC Controller

3.2.1 MII

The Media Independent Interface (MII) is an 18 wire MAC/PHY interface described in 802.3u. The purpose of the interface is to allow MAC layer devices to attach to a variety of Physical Layer devices through a common interface. MII operates at 100 Mbit/s or 10 Mbit/s, dependant on the speed of the Physical Layer. With clocks running at either 25 MHz or 2.5 MHz, 4 bit data is clocked between the MAC and PHY, synchronous with Enable and Error signals.

On receipt of valid data from the wire interface, RX_DV will go active signaling to the MAC that the valid data will be presented on the RXD[3:0] pins at the speed of the RX_CLK.

On transmission of data from the MAC, TX_EN is presented to the PHY indicating the presence of valid data on TXD[3:0]. TXD[3:0] are sampled by the PHY synchronous to TX_CLK during the time that TX_EN is valid.

3.2.2 Adaptive Equalizer

The amplitude and phase distortion from a cable causes inter-symbol interference (ISI) which makes clock and data recovery difficult. The adaptive equalizer is designed to closely match the inverse transfer function of the twisted-pairs cable. The equalizer has the ability to change its equalizer frequency response according to the cable length. The equalizer will tune itself automatically for any cable, compensating for the amplitude and phase distortion introduced by the cable.

3.2.3 Jabber and SQE

After the MAC transmitter exceeds the jabber timer, the transmit and loop back functions will be disabled and COL signal gets asserted. After TX_EN goes low for more than 500 ms, the TP transmitter will reactivate and COL gets de-asserted. Setting Jabber Disable will disable the jabber function.

When the SQE test is enabled, a COL pulse is asserted after each transmitted packet. SQE is enabled in 10Base-T by default.

3.2.4 Auto Polarity

Certain cable plants have crossed wiring on the twisted pairs; the reversal of TXIN and TXIP. Under normal circumstances this would cause the receive circuitry to reject all data. When the Auto Polarity Disable bit is cleared, the PHY has the ability to detect the fact that either 8 Normal Link Pulses (NLP) or a burst of FLPs are inverted and automatically reverse the receiver's polarity. The polarity state is stored in the Reverse Polarity bit.

3.2.5 Auto-Negotiation

It provides a linked device with the capability to detect the abilities (modes of operations) supported by the device at the other end of the link, determine common abilities, and configure for joint operation. Auto-Negotiation is performed out-of-band using a pulse code sequence that is compatible with the 10BASE-T link integrity test sequence.

3.2.6 Baseline Wander Compensation

The 100BASE-TX data stream is not always DC balanced. The transformer blocks the DC components of the incoming signal, thus the DC offset of the differential receive inputs can drift. The shifting of the signal level, coupled with non-zero rise and fall times of the serial stream can cause pulse-width distortion. This creates jitter and possible increase in the bit error rates. Therefore, a DC restoration circuit is needed to compensate for the attenuation of the DC component. Unlike the traditional implementation, the circuit does not need the feedback information from the slicer or the clock recovery circuit. The design simplifies the circuit design. In 10BASE-T, the baseline wander correction circuit is not required.

3.3 FIFO Controller

3.3.1 FIFO Controller in Receive Path

- Store received Ethernet packets to SRAM (internal 24 Kbyte) and total 16 packets can be stored to SRAM. If more than 16 packets are received or total packet size is more than 24 Kbytes, the subsequent coming Ethernet packet will be discarded.
- FIFO controller will load data from SRAM to internal RX FIFO then inform EP Decoder that 512-byte data or a packet is ready in RX FIFO. Before FIFO controller informs about this, any USB access to bulk IN endpoint will return NAK. This is to maintain the data transfer on USB bus via bulk IN transfer is continuous, thus a 512-byte internal RX FIFO is needed.
- If an Ethernet packet is being received and loading into SRAM while FIFO Controller is moving data from SRAM to internal RX FIFO, writing the Ethernet packet to SRAM will get the higher priority.

3.3.2 FIFO Controller in Transmit Path

- Store each individual USB packet to internal TX FIFO. When EP decoder informs end of packet, a complete Ethernet packet is stored in TX FIFO. FIFO Controller then informs MAC to transmit this packet.
- Total 4 Ethernet packets can be stored in TX FIFO. If all 4 Ethernet packets are stored in TX FIFO or total packet size is more than 2 Kbytes, FIFO Controller will inform EP Decoder that TX FIFO is full and EP Decoder will return NAK if accessing to bulk OUT endpoint is invoked. Thus additional USB packet won't be written into TX FIFO until TX FIFO has free space.

3.4 TX FIFO and RX FIFO

RX FIFO is a one-port 512 byte FIFO and TX FIFO is a two-port 2 Kbyte FIFO

3.5 10/100M Ethernet PHY

The Ethernet PHY is compliant to IEEE 802.3u 100BASE-TX and IEEE802.3 10BASE-T. It provides the whole physical layer functions for both 10M and 100M Ethernet speed.

3.6 USB Device Endpoint Operation

3.6.1 Endpoint 0

Endpoint 0 is in charge of response to standard USB commands and vendor specific commands. Internal register settings are also via this Endpoint 0. The response to each command is described in “USB Commands”.

3.6.2 Endpoint 1 Bulk IN

Endpoint 1 is in charge of sending the received Ethernet packet to USB host. An Ethernet packet will be split to multiple 512 bytes USB packets on USB. The end of the Ethernet packet is indicated by less than 512 byte or 0 length data transfer in this pipe. The Ethernet received status is optionally reported at the end of the packet.

While accessing to this endpoint, if RXFIFO is either full or any packet is inside, the data in RXFIFO is returned in USB data stage. If ACK is received from USB host, data in RXFIFO is flushed. If no response or NAK is received from USB host, the content in RXFIFO will be re-transmitted. If RXFIFO isn't ready for transmission, NAK is returned to USB host.

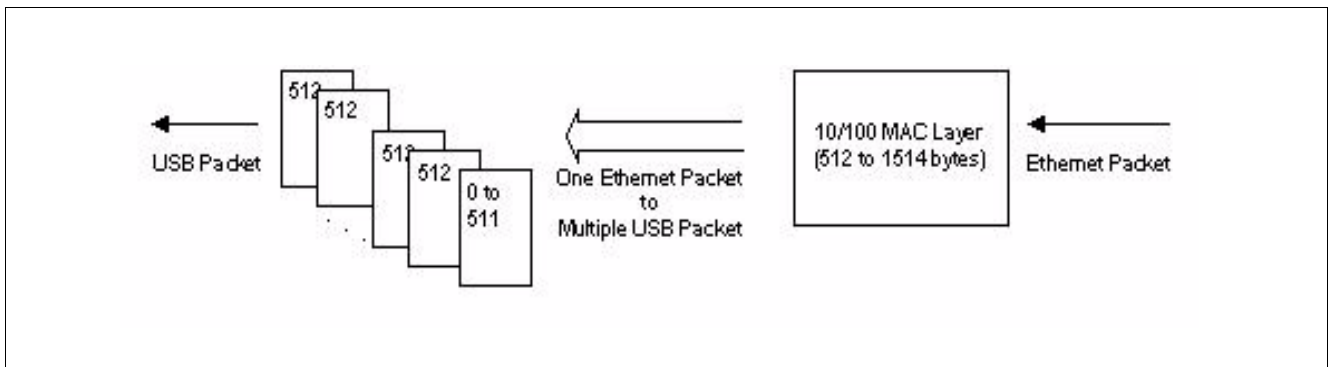


Figure 4 Packet Form when Receive

The Received Status is Reported as Follows:

Table 13 USB Received Status

Offset	Bit	Field	Description
Offset0	7-0	rx_bytectl_lo	The received byte count[7:0].
Offset1	3-0	rx_bytectl_hi	The received byte count[11:8].
	7-4	reserved	
Offset2	0	multicast_frame	Indicates received multicast frame.
	1	long_pkt	Indicates received packet length > 1518 bytes.
	2	runt_pkt	Indicates received packet length < 64 bytes.
	3	crc_err	Indicates CRC check error.
	4	dribble_bit	Indicates packet length is not integer multiple of 8-bit.
	7-5	reserved	
Offset3	7-0	reserved	

3.6.3 Endpoint 2 Bulk OUT

Endpoint 2 is in charge of sending the USB packet to Ethernet. An Ethernet packet is concatenated by multiple 512 bytes USB packets on USB. The first two bytes in every first concatenated USB packet indicate the length of the Ethernet packet. The end of the Ethernet packet is indicated by less than 512-byte or 0 length data transfer in this pipe. The Ethernet transmit status is reported in transmit status register.

When access to this endpoint, data in USB data stage are transferred to TXFIFO, if TXFIFO is free and ACK is returned. If TXFIFO isn't free, NAK is returned.

Table 14 USB Packet Format

Field	1st Byte in 1st USB Packet	2nd Byte in 1st USB Packet	The Following Packets
Content	len[7:0]: Low byte Ethernet packet length	{reserved[4:0], len[10:8]}	Ethernet packet

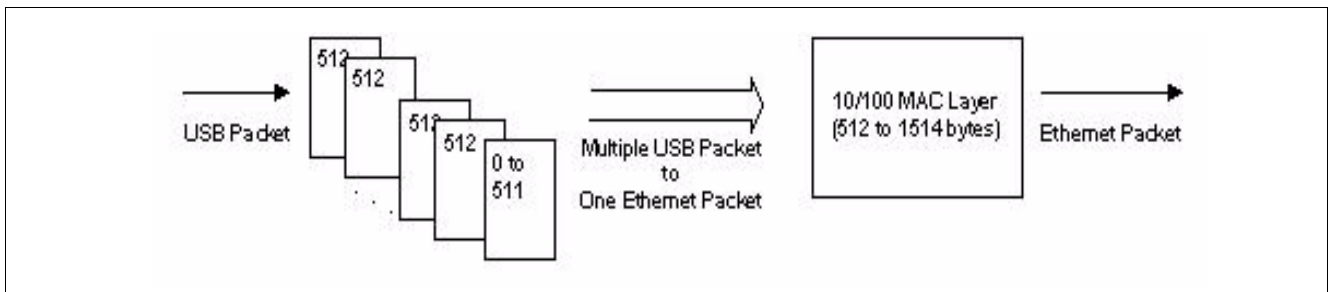


Figure 5 Packet Form when Transmit

3.6.4 Endpoint 3 Interrupt IN

Endpoint 3 is in charge of returning the current Ethernet transfer status every polling interval. When access to this endpoint, 8 bytes data is returned to USB host. The 8-byte packet contains the following in the tables below:

Table 15 Interrupt Packet Form

Offset0	Offset1	Offset2	Offset3	Offset4
tx_status(Reg2B _H)	tx_status(Reg2C _H)	rx_status(Reg2D _H)	rx_lostpkt(Reg2E _H)	rx_lostpkt(Reg2F _H)

Table 16 Interrupt Packet Form

Offset5	Offset6(1B)	Offset7(1B)
wakeup_status(Reg7A _H)	Packet number in RX FIFO (Reg82 _H)	7'b00, length error

4 Registers Description

4.1 System Registers

Table 17 Registers Address Space

Module	Base Address	End Address	Note
	0000 0000 _H	0000 0082 _H	

Table 18 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
EC0	Ethernet Control 0	00 _H	28
EC1	Ethernet Control 1	01 _H	29
EC2	Ethernet Control 2	02 _H	30
Res0	Reserved 0	03 _H	31
Res1	Reserved 1	04 _H	31
Res2	Reserved 2	05 _H	31
Res3	Reserved 3	06 _H	31
Res4	Reserved 4	07 _H	31
MA0	Multicast Address 0	08 _H	32
MA1	Multicast Address 1	09 _H	32
MA2	Multicast Address 2	0A _H	33
MA3	Multicast Address 3	0B _H	33
MA4	Multicast Address 4	0C _H	34
MA5	Multicast Address 5	0D _H	34
MA6	Multicast Address 6	0E _H	35
MA7	Multicast Address 7	0F _H	35
EID0	Ethernet ID 0	10 _H	36
EID1	Ethernet ID 1	11 _H	36
EID2	Ethernet ID 2	12 _H	37
EID3	Ethernet ID 3	13 _H	37
EID4	Ethernet ID 4	14 _H	38
EID5	Ethernet ID 5	15 _H	38
Res5	Reserved 5	16 _H	31
Res6	Reserved 6	17 _H	31
PT	Pause Timer	18 _H	39
Res7	Reserved 7	19 _H	31
RPNBFC	Receive Packet Number Based Flow Control	1A _H	39
ORFBFC	Occupied Receive FIFO Based Flow Control	1B _H	40
EP1C	EP1 Control	1C _H	40
Res8	Reserved 8	1D _H	31

Registers Description System Registers
Table 18 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
BIST	BIST	1E _H	40
Res9	Reserved 9	1F _H	31
EEPROMO	EEPROM Offset	20 _H	41
EEPROMDL	EEPROM Data Low	21 _H	41
EEPROMDH	EEPROM Data High	22 _H	42
EEPROMAC	EEPROM Access Control	23 _H	43
Res10	Reserved 10	24 _H	31
PHYA	PHY Address	25 _H	43
PHYDL	PHY Data Low	26 _H	44
PHYDH	PHY Data High	27 _H	44
PHYAC	PHY Access Control	28 _H	45
Res11	Reserved 11	29 _H	31
USBBS	USB Bus Status	2A _H	45
TS1	Transmit Status 1	2B _H	45
TS2	Transmit Status 2	2C _H	47
RS	Receive Status	2D _H	47
RLPCH	Receive Lost Packet Count High	2E _H	48
RLPCL	Receive Lost Packet Count Low	2F _H	48
WUF0M_0	Wakeup Frame 0 Mask	30 _H	48
WUF0M_1	Wakeup Frame 0 Mask 1	31 _H	49
... _H	49
WUF0M_xx	Wakeup Frame 0 Mask xx	3F _H	49
WUF0O_0	Wakeup Frame 0 Offset	40 _H	49
WUF0CRCL	Wakeup Frame 0 CRC Low	41 _H	50
WUF0CRCH	Wakeup Frame 0 CRC High	42 _H	50
Res12	Reserved 12	43 _H	31
Res13	Reserved 13	44 _H	31
Res14	Reserved 14	45 _H	31
Res15	Reserved 15	46 _H	31
Res16	Reserved 16	47 _H	31
WUF1M_0	Wakeup Frame 1 Mask	48 _H	51
WUF1M_1	Wakeup Frame 1 Mask 1	49 _H	51
... _H	51
WUF1M_xx	Wakeup Frame 1 Mask xx	57 _H	51
WUF1O	Wakeup Frame 1 Offset	58 _H	51
WUF1CRCL	Wakeup Frame 1 CRC Low	59 _H	52
WUF1CRCH	Wakeup Frame 1 CRC High	5A _H	52
Res17	Reserved 17	5B _H	31
Res18	Reserved 18	5C _H	31
Res19	Reserved 19	5D _H	31
Res 20	Reserved 20	5E _H	31

Registers Description System Registers
Table 18 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
Res 21	Reserved 21	5F _H	31
WUF2M	Wakeup Frame 2 Mask	60 _H	53
WUF2M_1	Wakeup Frame 2 Mask 1	61 _H	53
... _H	53
WUF2M_xx	Wakeup Frame 2 Mask xx	6F _H	53
WUF2O	Wakeup Frame 2 Offset	70 _H	53
WUF2CRCL	Wakeup Frame 2 CRC Low	71 _H	54
WUF2CRCH	Wakeup Frame 2 CRC High	72 _H	54
Res 22	Reserved 22	73 _H	31
Res 23	Reserved 23	74 _H	31
Res 24	Reserved 24	75 _H	31
Res 25	Reserved 25	76 _H	31
Res 26	Reserved 26	77 _H	32
WUC	Wakeup Control	78 _H	55
Res 27	Reserved 27	79 _H	32
WUS	Wakeup Status	7A _H	56
IPHYC	Internal PHY Control	7B _H	56
GPIO54C	GPIO[5:4] Control	7C _H	57
Res 28	Reserved 28	7D _H	32
GPIO10C	GPIO[1:0] Control	7E _H	58
GPIO32C	GPIO[3:2] Control	7F _H	59
Test	TEST	80 _H	60
TM	Test Mode	81 _H	60
RPN	Receive Packet Number	82 _H	61
Res 29	Reserved 29	83 _H	32
... _H	32
Res xx	Reserved xx	FF _H	32

The register is addressed wordwise.

Table 19 Register Access Types

Mode	Symbol	Description HW	Description SW
read/write	nw	Register is used as input for the HW	Register is readable and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register

Registers Description System Registers
Table 19 Register Access Types (cont'd)

Mode	Symbol	Description HW	Description SW
Latch high, self clearing	lhsc	Latch high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latch high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latch high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latch high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiate the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiate the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiate the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiate the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is readable and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is readable and writable by SW.

Table 20 Registers Clock Domains

Clock Short Name	Description

4.1.1 Registers

Ethernet Control 0

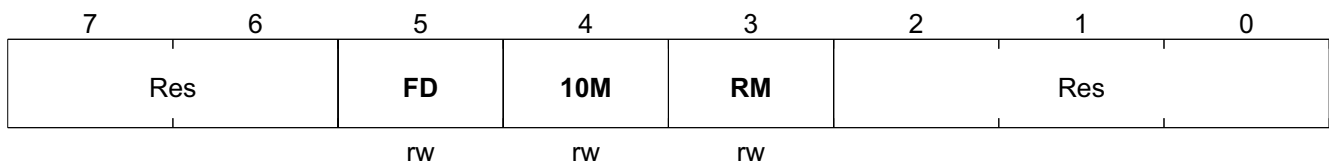
EC0	Offset	Reset Value					
Ethernet Control 0	00 _H	09 _H					
7	6	5	4	3	2	1	0
TXE	RXE	RXFCE	WOE	RXSA	SBO	RXMA	RXCS
rw	rw	rw	rw	rw	rw	rw	rw

Registers Description System Registers

Field	Bits	Type	Description
TXE	7	rw	Ethernet Transmission Enable 1 _B tx_en, Enable
RXE	6	rw	Ethernet Receive Enable 1 _B rx_en, Enable
RXFCE	5	rw	Receive Pause Frame Enable 1 _B rx_flowctl_en, Enable
WOE	4	rw	Wake-on-LAN Mode Enable 1 _B wakeon_en, Enable
RXSA	3	rw	Status Append at the End of Received Packet 1 _B rxstatus_append, Enable
SBO	2	rw	Stop Back Off 0 _B CNOT, Back-off counter isn't affected by carrier 1 _B CST, Back-off counter stop when carrier is active and resume when carrier drop
RXMA	1	rw	Receive All Multicast Packets 1 _B RALL, Receives all multicast packets
RXCS	0	rw	Include CRC in Receive Packet 1 _B ICRC, Includes CRC in receive packet

Ethernet Control 1

EC1 **Offset** **Reset Value**
Ethernet Control 1 **01_H** **00_H**



Field	Bits	Type	Description
FD	5	rw	Full Duplex 0 _B HDM, Half-duplex mode 1 _B FDM, Full-duplex mode
10M	4	rw	10mode 0 _B 10Base, 10Base-T mode 1 _B 100Base, 100Base-T mode
RM	3	rw	Reset MAC After write 1, HW will clear this bit after MAC reset.

Registers DescriptionSystem Registers

Ethernet Control 2

EC2 Offset
Ethernet Control 2 **02_H** Reset Value
40_H

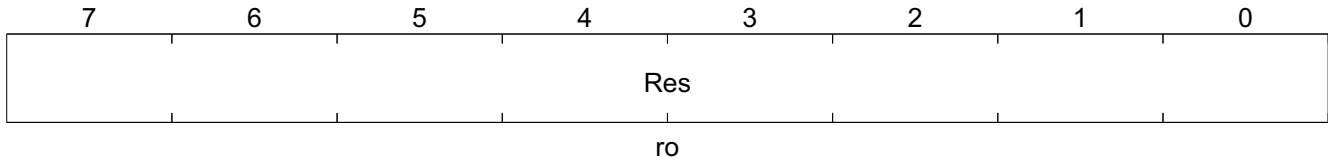
7	6	5	4	3	2	1	0
MEPL	RPNC	LEEPSRS	EEP RW	LB	PROM	RXBP	EP3RC
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
MEPL	7	rw	Max Ethernet Packet Length 0 _B 1528B , 1528 bytes 1 _B 1638B , 1638 bytes, Default is 0
RPNC	6	rw	Receive Packet Number Control This bit controls the clear operation of Register 82 _H (Receive packet number register) 0 _B NRC , No read clear 1 _B RC , Read clear
LEEPSRS	5	rw	Load EEPROM Start When this bit is written with 1, HW will start to load EEPROM.
EEP RW	4	rw	EEPROM Write Enable/disable 0 _B WEDC , EEPROM write enable/disable command 1 _B WC , EEPROM write command
LB	3	rw	Loop Back Enable MAC loop back mode.
PROM	2	rw	Promiscuous 0 _B RPP , Receives packets which pass the address filter 1 _B RAP , Receives any packets
RXBP	1	rw	Receive Bad Packets 0 _B FABP , Filter all bad packet 1 _B RBPP , Receives bad packets which pass the address filter
EP3RC	0	rw	EP3 Read Cleared 0 _B AEP3 , Access EP3, no effect to those registers. 1 _B OEP3 , Once EP3 is accessed, those registers (2B-2F, 7A) will be cleared.

Registers Description System Registers

Reserved 0

Res0 Offset Reset Value
 Reserved 0 03_H 00_H



Field	Bits	Type	Description
Res	7:0	ro	Reserved

Similar Registers

Table 21 Reserved Registers

Register Short Name	Register Long Name	Offset Address	Page Number
Res1	Reserved 1	04 _H	
Res2	Reserved 2	05 _H	
Res3	Reserved 3	06 _H	
Res4	Reserved 4	07 _H	
Res5	Reserved 5	16 _H	
Res6	Reserved 6	17 _H	
Res7	Reserved 7	19 _H	
Res8	Reserved 8	1D _H	
Res9	Reserved 9	1F _H	
Res10	Reserved 10	24 _H	
Res11	Reserved 11	29 _H	
Res12	Reserved 12	43 _H	
Res13	Reserved 13	44 _H	
Res14	Reserved 14	45 _H	
Res15	Reserved 15	46 _H	
Res16	Reserved 16	47 _H	
Res17	Reserved 17	5B _H	
Res18	Reserved 18	5C _H	
Res19	Reserved 19	5D _H	
Res 20	Reserved 20	5E _H	
Res 21	Reserved 21	5F _H	
Res 22	Reserved 22	73 _H	
Res 23	Reserved 23	74 _H	
Res 24	Reserved 24	75 _H	
Res 25	Reserved 25	76 _H	

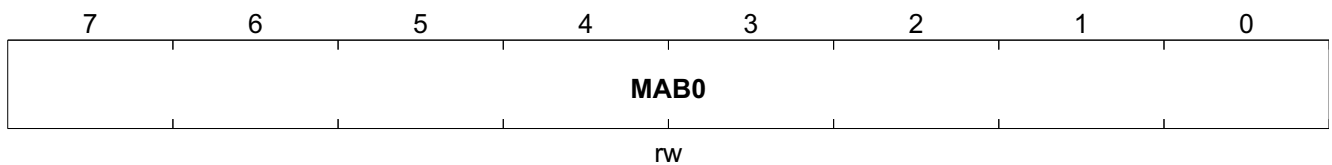
Registers Description System Registers

Table 21 Reserved Registers

Register Short Name	Register Long Name	Offset Address	Page Number
Res 26	Reserved 26	77 _H	
Res 27	Reserved 27	79 _H	
Res 28	Reserved 28	7D _H	
Res 29	Reserved 29	83 _H	
... _H	
Res xx	Reserved xx	FF _H	

Multicast Address 0

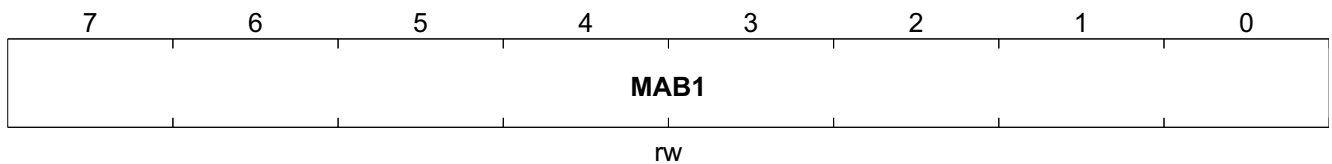
MA0 **Offset**
Multicast Address 0 **08_H** **Reset Value**
00_H



Field	Bits	Type	Description
MAB0	7:0	rw	Multicast 0 Multicast address byte [7:0]

Multicast Address 1

MA1 **Offset**
Multicast Address 1 **09_H** **Reset Value**
00_H

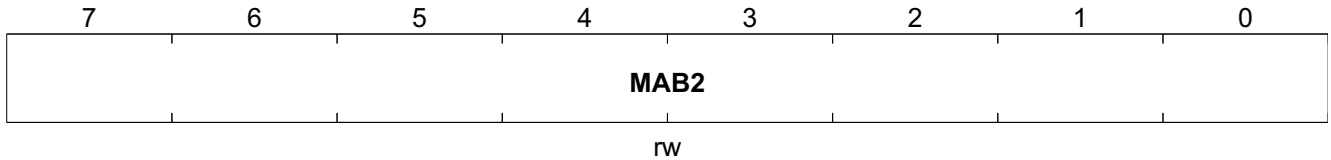


Field	Bits	Type	Description
MAB1	7:0	rw	Multicast 1 Multicast address byte [15:8]

Registers Description System Registers

Multicast Address 2

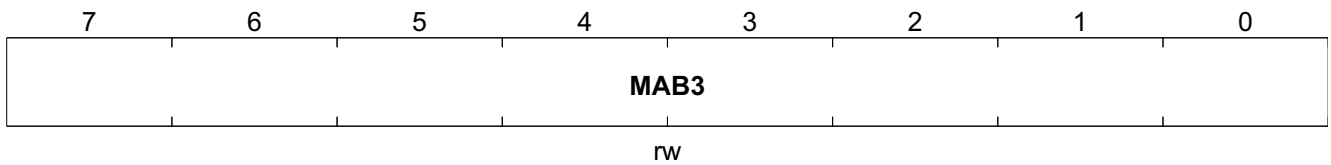
MA2 **Offset**
Multicast Address 2 **0A_H** **Reset Value**
00_H



Field	Bits	Type	Description
MAB2	7:0	rw	Multicast 2 Multicast address byte [23:16]

Multicast Address 3

MA3 **Offset**
Multicast Address 3 **0B_H** **Reset Value**
00_H

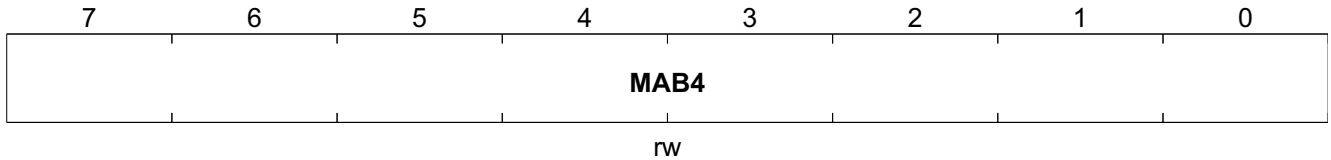


Field	Bits	Type	Description
MAB3	7:0	rw	Multicast 3 Multicast address byte [31:24]

Registers Description System Registers

Multicast Address 4

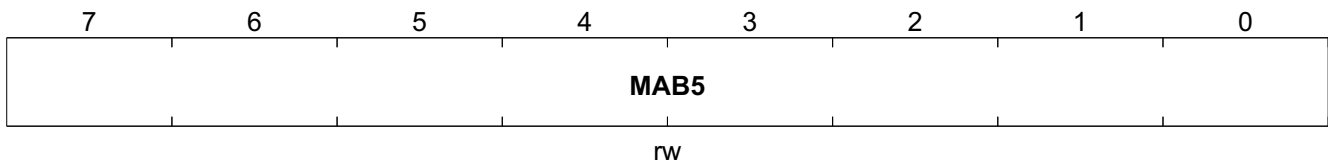
MA4 **Offset** **Reset Value**
Multicast Address 4 **0C_H** **00_H**



Field	Bits	Type	Description
MAB4	7:0	rw	Multicast 4 Multicast address byte [39:32]

Multicast Address 5

MA5 **Offset** **Reset Value**
Multicast Address 5 **0D_H** **00_H**

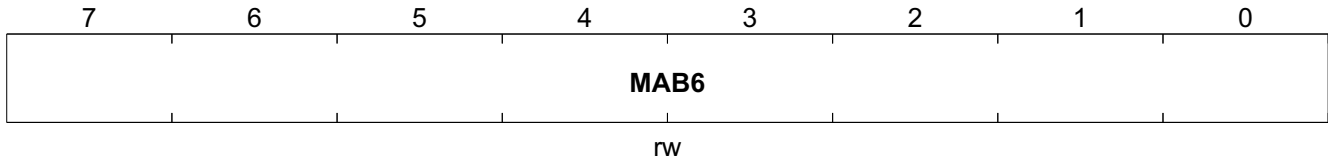


Field	Bits	Type	Description
MAB5	7:0	rw	Multicast 5 Multicast address byte [47:40]

Registers Description System Registers

Multicast Address 6

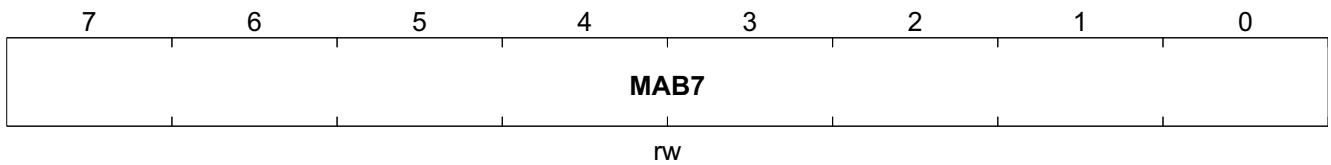
MA6 **Offset** **Reset Value**
Multicast Address 6 **0E_H** **00_H**



Field	Bits	Type	Description
MAB6	7:0	rw	Multicast 6 Multicast address byte [55:48]

Multicast Address 7

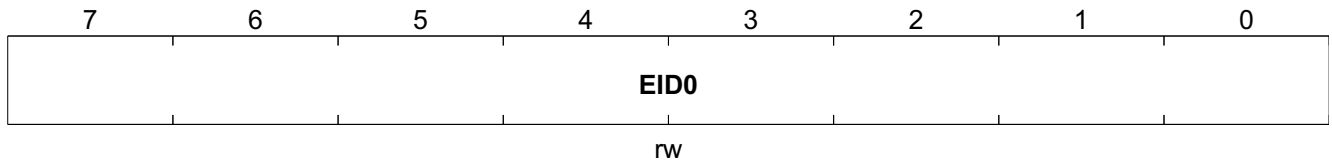
MA7 **Offset** **Reset Value**
Multicast Address 7 **0F_H** **00_H**



Field	Bits	Type	Description
MAB7	7:0	rw	Multicast 7 Multicast address byte [63:56]

Registers Description System Registers
Ethernet ID 0

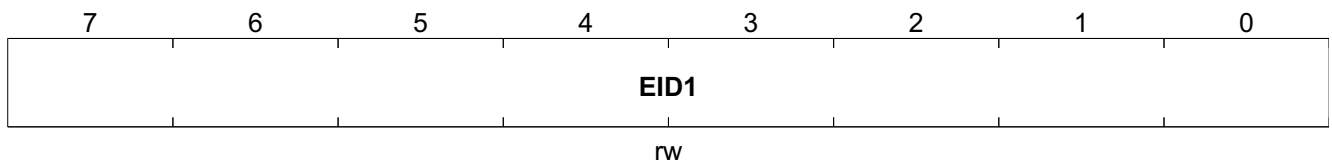
EID0	Offset	Reset Value
Ethernet ID 0	10 _H	00 _H



Field	Bits	Type	Description
EID0	7:0	rw	Ethernet ID 0 The 1st byte of Ethernet ID is automatically loaded from EEPROM after HW reset.

Ethernet ID 1

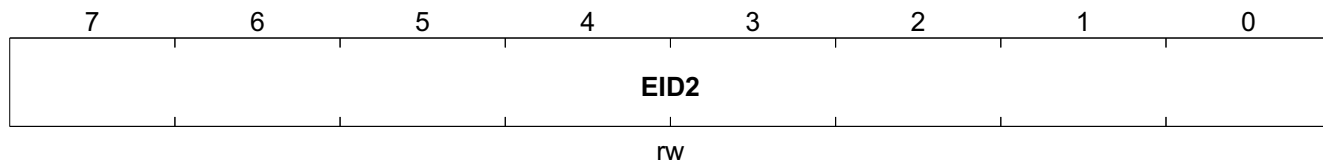
EID1	Offset	Reset Value
Ethernet ID 1	11 _H	00 _H



Field	Bits	Type	Description
EID1	7:0	rw	Ethernet ID 1 The 2nd byte of Ethernet ID.

Registers Description System Registers
Ethernet ID 2

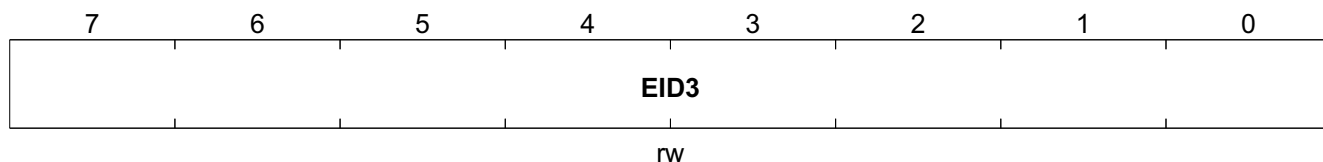
EID2	Offset	Reset Value
Ethernet ID 2	12_H	00_H



Field	Bits	Type	Description
EID2	7:0	rw	Ethernet ID 2 The 3rd byte of Ethernet ID.

Ethernet ID 3

EID3	Offset	Reset Value
Ethernet ID 3	13_H	00_H

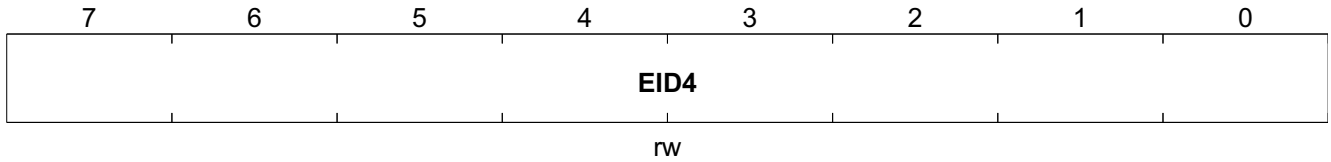


Field	Bits	Type	Description
EID3	7:0	rw	Ethernet ID 3 The 4th byte of Ethernet ID.

Registers Description System Registers

Ethernet ID 4

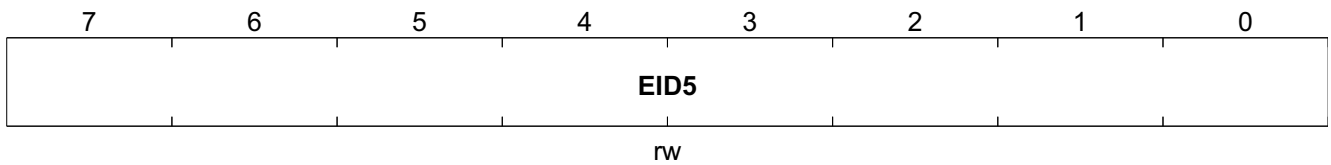
EID4	Offset	Reset Value
Ethernet ID 4	14 _H	00 _H



Field	Bits	Type	Description
EID4	7:0	rw	Ethernet ID 4 The 5th byte of Ethernet ID.

Ethernet ID 5

EID5	Offset	Reset Value
Ethernet ID 5	15 _H	00 _H

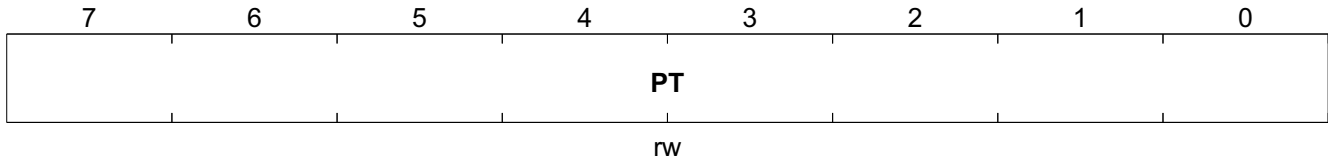


Field	Bits	Type	Description
EID5	7:0	rw	Ethernet ID 5 The 6th byte of Ethernet ID.

Registers Description System Registers

Pause Timer

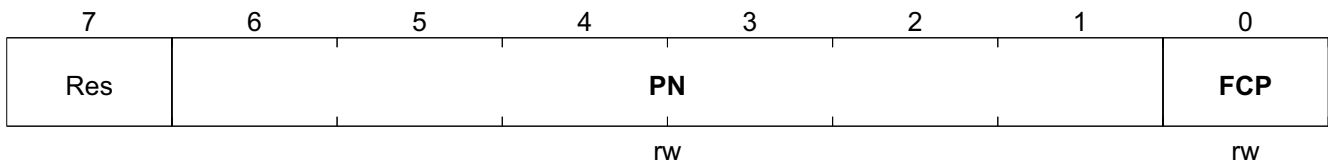
PT **Offset**
Pause Timer **18_H** **Reset Value**
00_H



Field	Bits	Type	Description
PT	7:0	rw	Pause Timer The [11:4] of pause time in the PAUSE frame.

Receive Packet Number Based Flow Control

RPNBFC **Offset**
Receive Packet Number Based Flow Control **1A_H** **Reset Value**
00_H

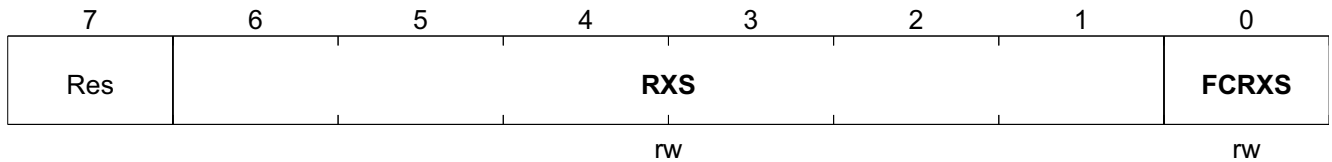


Field	Bits	Type	Description
PN	6:1	rw	Packet Number This field specifies the threshold for transmitting the PAUSE frame. As the received packet number is more than or equal to this field, the PAUSE frame is sent automatically by HW.
FCP	0	rw	Flow Control Packet 1 _B RPN , Enable pause frame transmission bases on receive packet number

Registers Description System Registers

Occupied Receive FIFO Based Flow Control

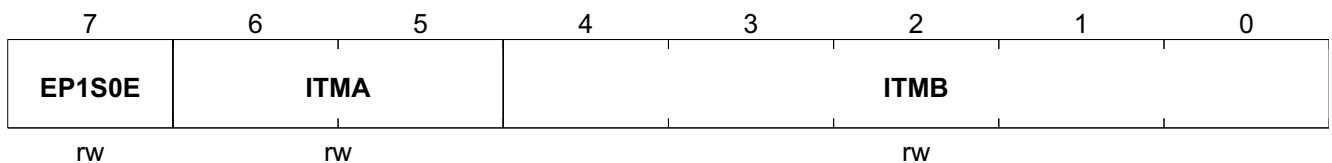
ORFBFC Offset **Reset Value**
Occupied Receive FIFO Based Flow Control **1B_H** **00_H**



Field	Bits	Type	Description
RXS	6:1	rw	RX Size This field specifies the Kbyte threshold for transmitting the PAUSE frame. As the received FIFO is occupied than or equal to this field, the PAUSE frame is sent automatically by HW. If this field = 2, as receive FIFO is occupied more than or equal to 2 Kbyte, the PAUSE frame is transmitted.
FCRXS	0	rw	Flow Control RX Size 1 _B RFS , Enable pause frame transmission bases on occupied receive FIFO size

EP1 Control

EP1C Offset **Reset Value**
EP1 Control **1C_H** **04_H**



Field	Bits	Type	Description
EP1S0E	7	rw	EP1 Send Enable 0 _B DEP1 , Disable EP1 send 1-byte 00 function 1 _B EEP1 , Enable EP1 send 1-byte 00 when more than frame_ interval's NAK is received
ITMA	6:5	rw	Internal Test Mode A This value is used for internal test mode.
ITMB	4:0	rw	Internal Test Mode B This value is used for internal test mode.

BIST

Registers Description System Registers

BIST **Offset**
BIST **1E_H** **Reset Value**
05_H

7	6	5	4	3	2	1	0
Res			BR			BTD	BEN
					r	r	rw

Field	Bits	Type	Description
BR	2	r	Bist Result This bit indicates the bist result and is valid when "bist_test_done" is '1'. This bit also reflects the value of "pass_or_fail" signal in BIST module. 0 _B FA , Fail 1 _B PA , Pass
BTD	1	r	BIST Test Done This bit indicates the completion of bist. The bist completes if this bit is '1'. This bit also reflects the value of "test_done" signal in BIST module.
BEN	0	rw	BIST Enable This bit enable the BIST function and also drives the "reset" signal in BIST module. 0 _B EBI , Enable BIST function 1 _B DBI , Disable BIST function

EEPROM Offset

EEPROM0 **Offset**
EEPROM Offset **20_H** **Reset Value**
00_H

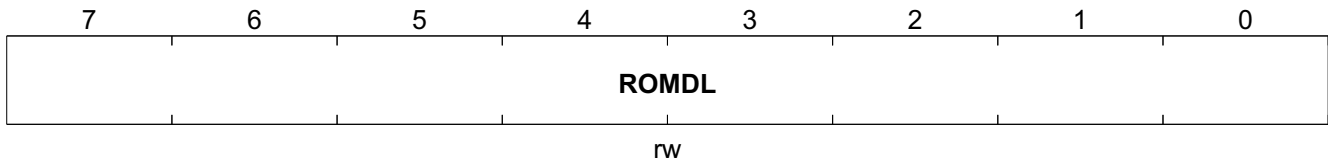
7	6	5	4	3	2	1	0	
Res		ROMO						
					rw			

Field	Bits	Type	Description
ROMO	5:0	rw	ROM Offset SW sets this register when access to EEPROM.

EEPROM Data Low

EEPROMDL **Offset**
EEPROM Data Low **21_H** **Reset Value**
00_H

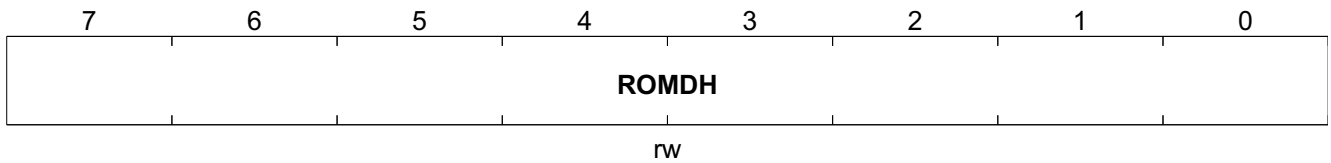
Registers Description System Registers



Field	Bits	Type	Description
ROMDL	7:0	rw	ROM Data Low EEPROM Write: The data set in this register will be written to EEPROM EEPROM Read: The data red from EEPROM will be stored in this register

EEPROM Data High

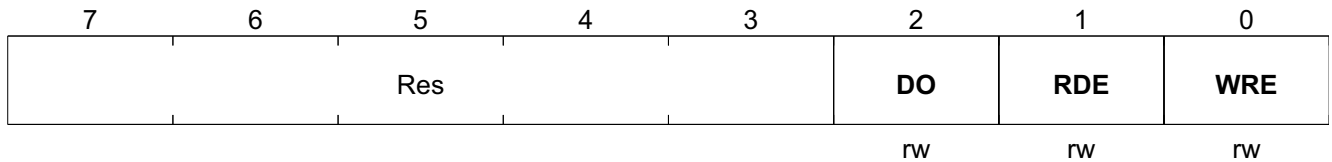
EEPROMDH	Offset	Reset Value
EEPROM Data High	22 _H	00 _H



Field	Bits	Type	Description
ROMDH	7:0	rw	ROM Data High EEPROM Write: The data set in this register will be written to EEPROM EEPROM Read: The data red from EEPROM will be stored in this register

EEPROM Access Control

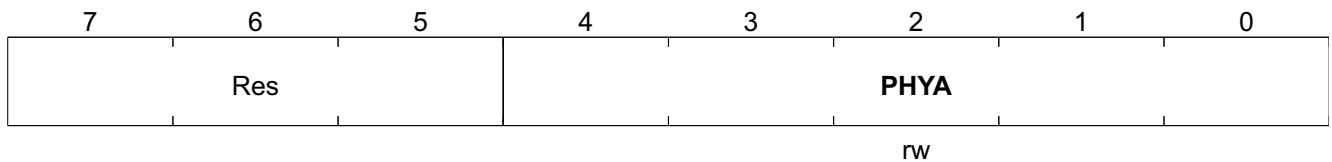
EEPROMAC **Offset**
EEPROM Access Control **23_H** **Reset Value**
00_H



Field	Bits	Type	Description
DO	2	rw	Done Set by HW to indicate successful completion of EEPROM access. Clear by SW when initiate a new access to EEPROM
RDE	1	rw	Read Access to EEPROM rd_eeeprom Set by SW to initiate a read access to EEPROM. SW sets this bit after it well setting the rom_offset.
WRE	0	rw	Write Access to EEPROM wr_eeeprom Set by SW to initiate a write access to EEPROM. SW set this bit after it well setting the rom_offset, romdata_lo and romdata_hi.

PHY Address

PHYA **Offset**
PHY Address **25_H** **Reset Value**
00_H

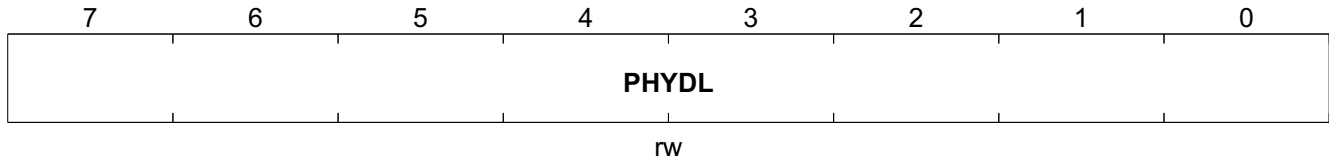


Field	Bits	Type	Description
PHYA	4:0	rw	MII PHY Address

Registers Description System Registers

PHY Data Low

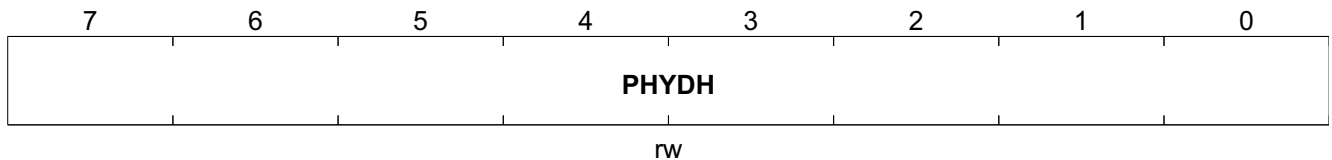
PHYDL	Offset	Reset Value
PHY Data Low	26 _H	00 _H



Field	Bits	Type	Description
PHYDL	7:0	rw	PHY Data Low SW set this register when write to PHY register. HW set this register when read data from PHY register.

PHY Data High

PHYDH	Offset	Reset Value
PHY Data High	27 _H	00 _H



Field	Bits	Type	Description
PHYDH	7:0	rw	PHY Data High SW set this register when write to PHY register. HW set this register when read data from PHY register.

Registers Description System Registers

PHY Access Control

PHYAC **Offset**
PHY Access Control **28_H** **Reset Value**
00_H

7	6	5	4	3	2	1	0
DO	RDPHY	WRPHY	PHYRA				
rw	rw	rw	rw				

Field	Bits	Type	Description
DO	7	rw	Done Set by HW to indicate successful completion of PHY access. Clear by SW when initiate a new access to PHY.
RDPHY	6	rw	Read Access to PHY Register Set by SW to initiate a read access to PHY register. SW set this bit after it well setting the phy_addr and phyreg_addr.
WRPHY	5	rw	Write Access to PHY Register Set by SW to initiate a write access to PHY register. SW set this bit after it well setting the phy_addr, phyreg_addr and phyreg_data.
PHYRA	4:0	rw	PHY Register Address

USB Bus Status

USBBS **Offset**
USB Bus Status **2A_H** **Reset Value**
00_H

7	6	5	4	3	2	1	0
Res						USBR	USBS
						rw	rw

Field	Bits	Type	Description
USBR	1	rw	USB Bus in Resume State It is cleared by reading this register. 1 _B RS , Means USB bus in resume state
USBS	0	rw	USB Bus in Suspend State It is cleared by reading this register. 1 _B SS , Means USB bus in suspend state

Transmit Status 1

Registers Description System Registers

TS1 **Offset** **Reset Value**
Transmit Status 1 **2B_H** **00_H**

	7	6	5	4	3	2	1	0
	TXUE	EC	LC	NC	CL	JTO	Res	
	r	r	r	r	r	r		

Field	Bits	Type	Description
TXUE	7	r	TX Underrun Error It is cleared by reading this register or after EP3 is accessed 1 _B TXUE , Means tx underrun error
EC	6	r	Excessive Collision It is cleared by reading this register or after EP3 is accessed 1 _B EC , Means excessive collision
LC	5	r	Late Collision Error It is cleared by reading this register or after EP3 is accessed 1 _B CE , Means late collision error
NC	4	r	No Carrier It is cleared by reading this register or after EP3 is accessed 1 _B NC , Means no carrier
CL	3	r	Carrier Loss It is cleared by reading this register or after EP3 is accessed 1 _B CL , Means carrier loss
JTO	2	r	Jabber Time Out It is cleared by reading this register or after EP3 is accessed 1 _B JTO , Means jabber time out

Registers Description System Registers

Transmit Status 2

TS2 **Offset**
2C_H **Reset Value**
00_H
Transmit Status 2

	7	6	5	4	3	2	1	0
	TXFF	TXFE	Res		TXPC			
	r	r			r			

Field	Bits	Type	Description
TXFF	7	r	TX Fifo Full It is cleared by reading this register or after EP3 is accessed 1 _B FF , Means tx fifo full
TXFE	6	r	TX Fifo Empty It is cleared by reading this register or after EP3 is accessed 1 _B FE , Means tx fifo empty
TXPC	3:0	r	TX Packet Count It is cleared by reading this register or after EP3 is accessed. 1 _B TPC , Means Ethernet transmit packet count every interrupt EP polling. If more than 15 packets have been transmitted this value will keep as 15.

Receive Status

RS **Offset**
2D_H **Reset Value**
00_H
Receive Status

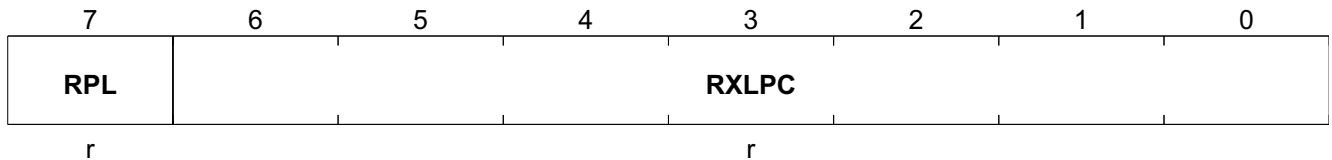
	7	6	5	4	3	2	1	0
	Res						RXP	RXO
							r	r

Field	Bits	Type	Description
RXP	1	r	RX Pause It is cleared by reading this register or after EP3 is accessed 1 _B PF , Means a PAUSE frame is received
RXO	0	r	RX Overflow It is cleared by reading this register or after EP3 is accessed 1 _B RO , Means received SRAM overflow

Registers Description System Registers

Receive Lost Packet Count High

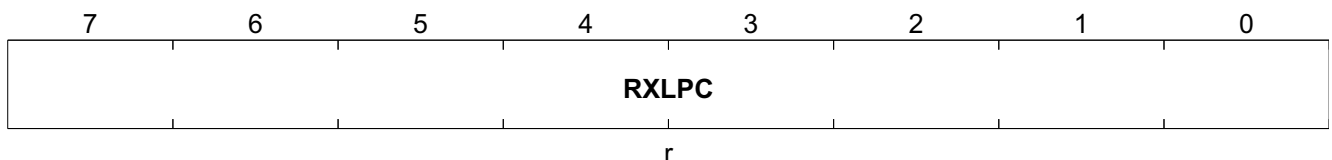
RLPCH **Offset**
Receive Lost Packet Count High **2E_H** **Reset Value**
00_H



Field	Bits	Type	Description
RPL	7	r	Received Packet Lost It is cleared by reading this register or after EP3 is accessed. 1 _B RPL , Means received packet lost
RXLPC	6:0	r	RX Lost Packet Counts The [14:8] of lost packet counts due to receive FIFO overflow. It is cleared by reading this register or after EP3 is accessed.

Receive Lost Packet Count Low

RLPCL **Offset**
Receive Lost Packet Count Low **2F_H** **Reset Value**
00_H

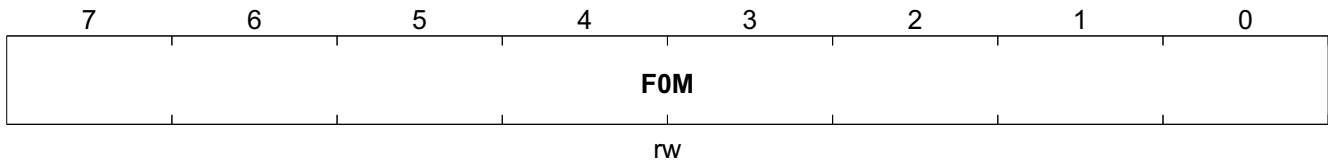


Field	Bits	Type	Description
RXLPC	7:0	r	RX Lost Packet Counts The [7:0] of lost packet counts due to receive FIFO overflow. It is cleared by reading this register or after EP3 is accessed

Wakeup Frame 0 Mask

WUF0M_0 **Offset**
Wakeup Frame 0 Mask **30_H** **Reset Value**
00_H

Registers Description System Registers



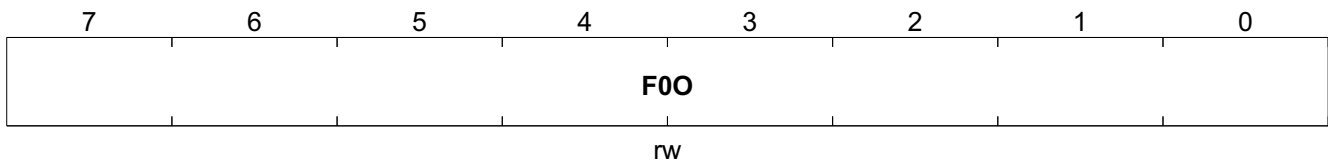
Field	Bits	Type	Description
F0M	7:0	rw	The 128 Mask Bits for Frame 0

Similar Registers
Table 22 Wakeup Frame 0 Mask Registers

Register Short Name	Register Long Name	Offset Address	Page Number
WUF0M_1	Wakeup Frame 0 Mask 1	31 _H	
... _H	
WUF0M_xx	Wakeup Frame 0 Mask xx	3F _H	

Wakeup Frame 0 Offset

WUF00_0	Offset	Reset Value
Wakeup Frame 0 Offset	40 _H	00 _H

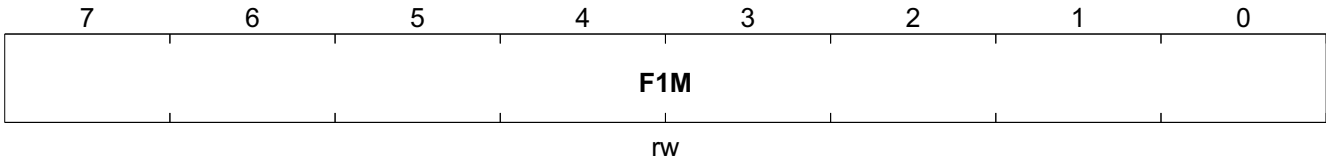


Field	Bits	Type	Description
F0O	7:0	rw	Offset for Wakeup Frame 0

Registers Description System Registers

Wakeup Frame 1 Mask

WUF1M_0 **Offset**
Wakeup Frame 1 Mask **48_H** **Reset Value**
00_H



Field	Bits	Type	Description
F1M	7:0	rw	The 128 Mask Bits for Frame 1

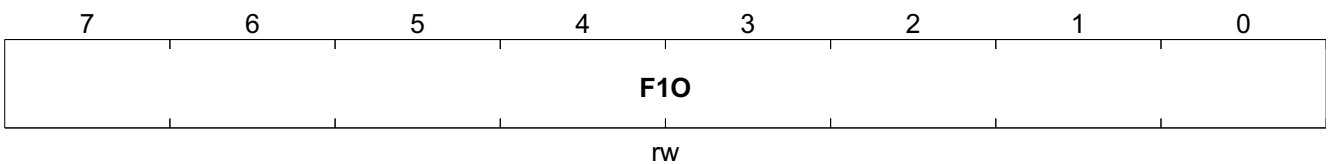
Similar Registers

Table 23 Wakeup Frame 1 Mask Registers

Register Short Name	Register Long Name	Offset Address	Page Number
WUF1M_1	Wakeup Frame 1 Mask 1	49 _H	
... _H	
WUF1M_xx	Wakeup Frame 1 Mask xx	57 _H	

Wakeup Frame 1 Offset

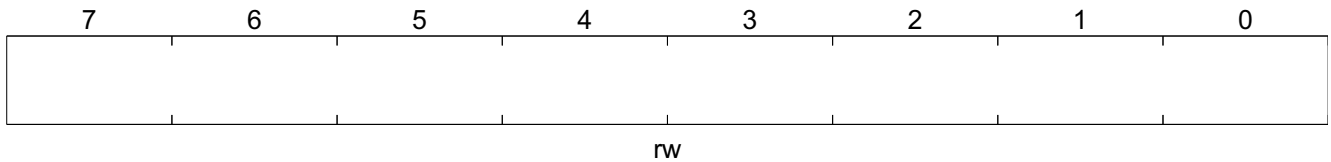
WUF1O **Offset**
Wakeup Frame 1 Offset **58_H** **Reset Value**
00_H



Field	Bits	Type	Description
F1O	7:0	rw	Offset for Wakeup Frame 1

Wakeup Frame 1 CRC Low

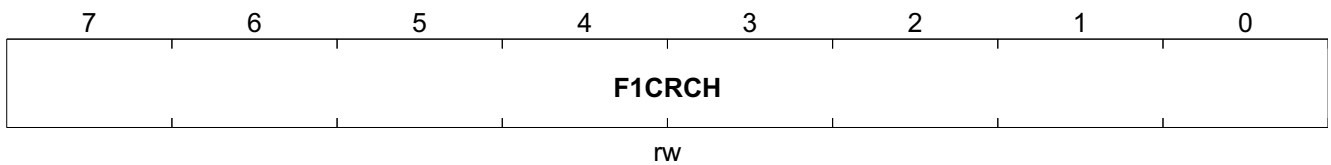
WUF1CRCL Offset **59_H** Reset Value **00_H**
Wakeup Frame 1 CRC Low



Field	Bits	Type	Description
	7:0	rw	The Low Byte of CRC16 Match for Frame 1

Wakeup Frame 1 CRC High

WUF1CRCH Offset **5A_H** Reset Value **00_H**
Wakeup Frame 1 CRC High

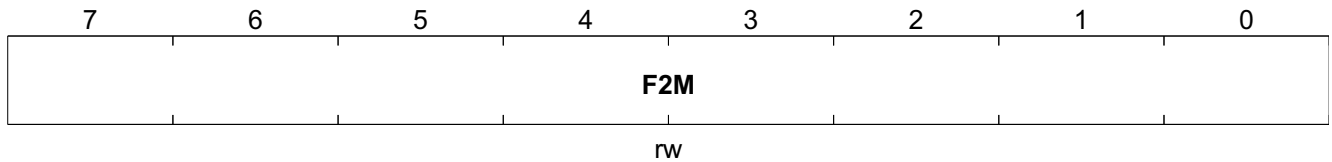


Field	Bits	Type	Description
F1CRCH	7:0	rw	The High Byte of CRC16 Match for Frame 1

Registers Description System Registers

Wakeup Frame 2 Mask

WUF2M **Offset**
Wakeup Frame 2 Mask **60_H** **Reset Value**
00_H



Field	Bits	Type	Description
F2M	7:0	rw	The 128 Mask Bits for Frame 2

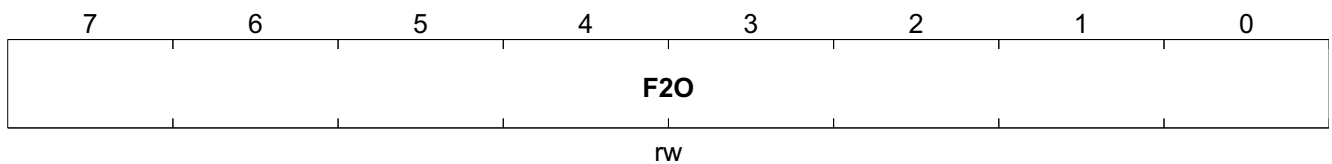
Similar Registers

Table 24 Wakeup Frame 2 Mask Registers

Register Short Name	Register Long Name	Offset Address	Page Number
WUF2M_1	Wakeup Frame 2 Mask 1	61 _H	
... _H	
WUF2M_xx	Wakeup Frame 2 Mask xx	6F _H	

Wakeup Frame 2 Offset

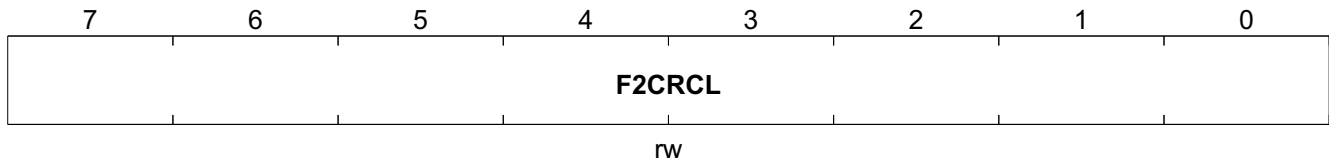
WUF2O **Offset**
Wakeup Frame 2 Offset **70_H** **Reset Value**
00_H



Field	Bits	Type	Description
F2O	7:0	rw	Offset for Wakeup Frame 2

Wakeup Frame 2 CRC Low

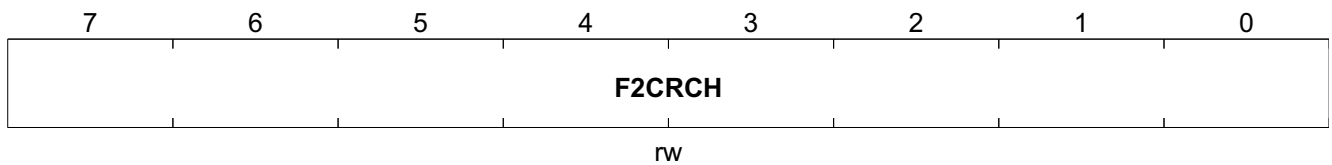
WUF2CRCL Offset **71_H** Reset Value **00_H**
Wakeup Frame 2 CRC Low



Field	Bits	Type	Description
F2CRCL	7:0	rw	The Low Byte of CRC16 Match for Frame 2

Wakeup Frame 2 CRC High

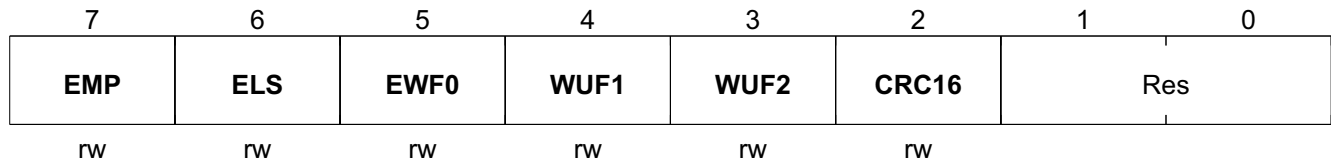
WUF2CRCH Offset **72_H** Reset Value **00_H**
Wakeup Frame 2 CRC High



Field	Bits	Type	Description
F2CRCH	7:0	rw	The High Byte of CRC16 Match for Frame 2

Wakeup Control

WUC	Offset	Reset Value
Wakeup Control	78_H	04_H

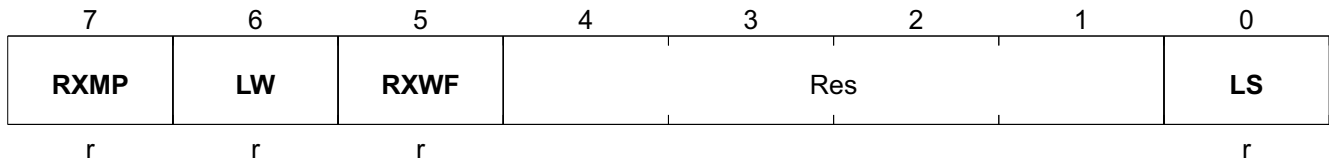


Field	Bits	Type	Description
EMP	7	rw	Enable Magic Packet 1 _B EMP , Enables magic packet wakeup function
ELS	6	rw	Enable Link Status 1 _B ELS , Enables link status wakeup function
EWFO	5	rw	Enable Wakeup Frame 0 1 _B EWFO , Enables wakeup frame0 wakeup function
WUF1	4	rw	Enable Wakeup Frame 1 1 _B WUF1 , Enables wakeup frame1 wakeup function
WUF2	3	rw	Enable Wakeup Frame 2 1 _B WUF2 , Enables wakeup frame2 wakeup function
CRC16	2	rw	CRC-16 Initial Type 0 _B CRC16 , CRC-16 initial contents = 0000 _H 1 _B CRC16 , CRC-16 initial contents = ffff _H

Registers Description System Registers

Wakeup Status

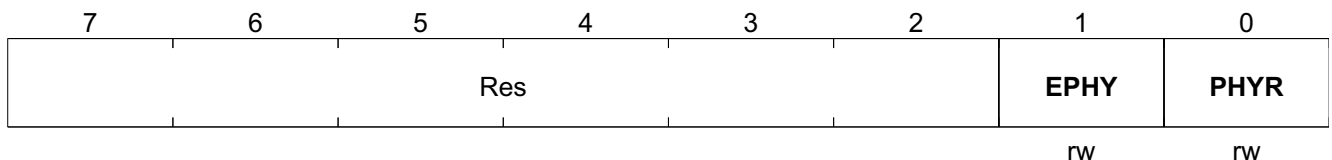
WUS Offset **Reset Value**
Wakeup Status **7A_H** **00_H**



Field	Bits	Type	Description
RXMP	7	r	Receives a Magic Packet It is cleared by reading this register. 1 _B RMP , means ADM8515/X receives a magic packet
LW	6	r	Receives a Link Status Change It is cleared by reading this register. 1 _B RLS , means ADM8515/X receives a link status change
RXWF	5	r	Receives a Wakeup Frame It is cleared by reading this register. 1 _B RWF , Means ADM8515/X receives a wakeup frame
LS	0	r	Indicate the Current Link Status 0 _B LOFF , Link off 1 _B LON , Link on

Internal PHY Control

IPHYC Offset **Reset Value**
Internal PHY Control **7B_H** **00_H**



Field	Bits	Type	Description
EPHY	1	rw	Enable PHY 0 _B DIN , disables internal 10/100 PHY 1 _B EIN , enables internal 10/100 PHY
PHYR	0	rw	Internal PHY Reset The internal PHY is reset when this bit is written with 1 and stops reset when this bit is written with 0. 1 _B RIPHY , resets internal PHY

GPIO[5:4] Control

GPIO54C	Offset	Reset Value
GPIO[5:4] Control	7C_H	00_H

7	6	5	4	3	2	1	0
Res		G5OE	G5OV	G5IV	G4OE	G4OV	G4IV
		rw	rw	r	rw	rw	r

Field	Bits	Type	Description
G5OE	5	rw	GPIO5 Output Enable 0 _B IN , GPIO5 is used for input 1 _B OUT , GPIO5 is used for output
G5OV	4	rw	GPIO5 Output Value When GPIO5 is used for output, this value is driven to GPIO5 pin.
G5IV	3	r	GPIO5 Input Value When GPIO5 is used for input, this field reflects the status of GPIO5. Default is pulled-down.
G4OE	2	rw	GPIO4 Output Enable 0 _B IN , GPIO4 is used for input 1 _B OUT , GPIO4 is used for output
G4OV	1	rw	GPIO4 Output Value When GPIO4 is used for output, this value is driven to GPIO4 pin.
G4IV	0	r	GPIO4 Input Value When GPIO4 is used for input, this field reflects the status of GPIO4. Default is pulled-down.

GPIO[1:0] Control

GPIO10C GPIO[1:0] Control	Offset 7E _H	Reset Value 00 _H
--	----------------------------------	---------------------------------------



Field	Bits	Type	Description
G1OE	5	rw	GPIO1 Output Enable 0 _B IN , GPIO1 is used for input 1 _B OUT , GPIO1 is used for output
G1OV	4	rw	GPIO1 Output Value When GPIO1 is used for output, this value is driven to GPIO1 pin.
G1IV	3	r	GPIO1 Input Value When GPIO1 is used for input, this field reflects the status of GPIO1.
G1OE	2	rw	GPIO0 Output Enable 0 _B IN , GPIO0 is used for input 1 _B OUT , GPIO0 is used for output
G0OV	1	rw	GPIO0 Output Value When GPIO0 is used for output, this value is driven to GPIO0 pin.
G0IV	0	r	GPIO0 Input Value When GPIO0 is used for input, this field reflects the status of GPIO0.

GPIO[3:2] Control

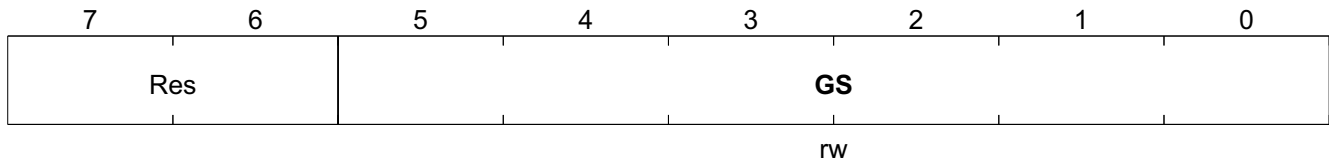
GPIO32C	Offset	Reset Value
GPIO[3:2] Control	7F_H	00_H

7	6	5	4	3	2	1	0
Res	G3OE	G3OV	G3IV	G2OE	G2OV	G2IV	
	rw	rw	r	rw	rw	r	

Field	Bits	Type	Description
G3OE	5	rw	GPIO3 Output Enable 0 _B IN , GPIO3 is used for input 1 _B OUT , GPIO3 is used for output
G3OV	4	rw	GPIO3 Output Value When GPIO3 is used for output, this value is driven to GPIO3 pin.
G3IV	3	r	GPIO3 Input Value When GPIO3 is used for input, this field reflects the status of GPIO3.
G2OE	2	rw	GPIO2 Output Enable 0 _B IN , GPIO2 is used for input 1 _B OUT , GPIO2 is used for output
G2OV	1	rw	GPIO2 Output Value When GPIO2 is used for output, this value is driven to GPIO2 pin.
G2IV	0	r	GPIO2 Input Value When GPIO2 is used for input, this field reflects the status of GPIO2.

Registers Description System Registers
TEST

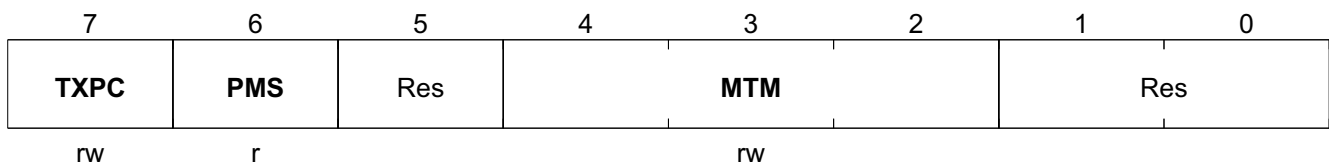
Test **Offset**
TEST **80_H** **Reset Value**
00_H



Field	Bits	Type	Description
GS	5:0	rw	Internal Probing Signal Group Selection group_sel

Test Mode

TM **Offset**
Test Mode **81_H** **Reset Value**
00_H

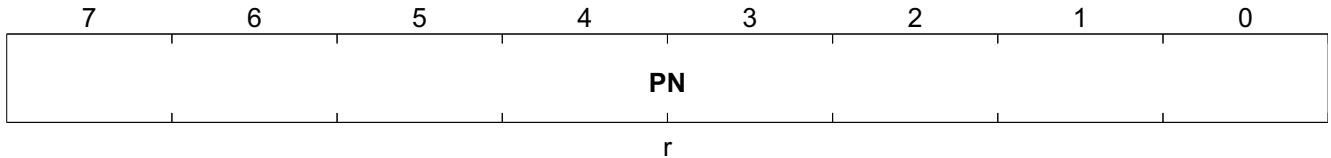


Field	Bits	Type	Description
TXPC	7	rw	TX Packet Control 0 _B TLI , transmits length in the first 2 bytes could be ignored 1 _B TLR , transmits length in the first 2 bytes is used as real data length
PMS	6	r	Power Mode Selection This bit is loaded from EEPROM 0 _B BP , Bus power 1 _B SP , Self power
MTM	4:2	rw	MII Test Mode This value could be updated from EEPROM offset 0A[4:2]. 000 _B TS , Tri-state MII pins 001 _B EM , enables MAC's MII signals to external MII pins 010 _B EPHY , enables PHY's MII signals to external MII pins 011 _B MM , Monitor mode MII

Registers Description PHY Registers

Receive Packet Number

RPN	Offset	Reset Value
Receive Packet Number	82 _H	00 _H



Field	Bits	Type	Description
PN	7:0	r	Packet Number Received packet number from last access this register. This register is controlled by Reg 02[6] to decide read clear or not.

4.2 PHY Registers

Table 25 Registers Address Space

Module	Base Address	End Address	Note
PHY Registers	0000 0000 _H	0000 0006 _H	

Table 26 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
CTL	Control	0 _H	62
STA	Status	01 _H	63
PHYI1	PHY Identifier 1	2 _H	65
PHYI2	PHY Identifier 2	3 _H	65
ANA	Auto-Negotiation Advertisement	4 _H	66
ANLPA	Auto-Negotiation Link Partner Ability	5 _H	67
ANE	Auto-Negotiation Expansion	6 _H	67

The register is addressed wordwise.

Register Access Types

4.2.1 Registers

Registers Description PHY Registers

Control

CTL Offset Reset Value
Control 0_H 1000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST	LP	SS	ANE	PD	ISO	RA	DM	CT	Res						
rwsc	rw	rw	rw	rw	rw	rwsc	rw	ro							

Field	Bits	Type	Description
RST	15	rwsc	Reset 0 _B NO, Normal operation 1 _B PR, PHY Reset
LP	14	rw	Loopback 0 _B DL, Disables loopback 1 _B EL, Enables loopback
SS	13	rw	Speed Selection 0 _B 10M, 10 Mbit/s 1 _B 100M, 100 Mbit/s
ANE	12	rw	Autonegotiation Enable 0 _B DAN, Disables auto-neg 1 _B EAN, Enables auto-neg
PD	11	rw	Power Down 0 _B NO, Normal operation 1 _B PD, Power Down
ISO	10	rw	Isolate 0 _B NO, normal operation 1 _B IPHY, isolate PHY from MII
RA	9	rwsc	Restart Autonegotiation 1 _B RAN, Restarts Auto-neg
DM	8	rw	Duplex Mode 0 _B HA, Half 1 _B FU, Full
CT	7	ro	Collision Test Not implemented

Note:

SCSelf Clearing

ResetReset this port only. This will cause the following:

1. Restart the auto-negotiation process.
2. Reset the registers to their default values. Note that this does not affect registers 20, 22, 30 or 31. These registers are not reset by this bit to allow test configurations to be written and then not affected by resetting the

Registers Description PHY Registers

port.

Note: No reset is performed to analogue sections of the port. There is also no physical reset to any internal clock synthesisers or the local clock recovery oscillator which will continue to run throughout the reset period. However since the port is restarted and autoneg re-run the process of locking the frequency of the local oscillator (slave) to the reference oscillator (master) will be repeated as it is at the start of any link initialization process.

Loopback Loop back of transmit data to receive via a path as close to the wire as possible. When set inhibits actual transmission on the wire.

Speed selection Forces speed of Phy only when auto-negotiation is disabled. The default state of this bit will be determined by a power-up configuration pin in this case. Otherwise it defaults to 1.

Auto-neg enable Defaults to pin programmed value. When cleared it allows forcing of speed and duplex settings. When set (after being cleared) it causes re-start of auto-neg process. Pin programming at power-up allows it to come up disabled and for software to write the desired capability before allowing the first negotiation to commence.

Restart Negotiation Only has effect when auto-negotiating. Restarts state machine.

Power down Has no effect in this device. Test mode power down modes may be implemented in other specific modules.

Isolate Puts RMII receive signals into high impedance state and ignores transmit signals.

Duplex mode When bit 12 is cleared (i.e. autoneg disabled), this bit forces full duplex (bit = 1) or half duplex (bit = 0)

Collision test Always 0 because collision signal is not implemented.

Status

STA	Offset	Reset Value
Status	01 _H	7849 _H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
100T 4	100F D	100H D	10FD	10HD	T2FD	T2HD	Res		MFP	ANC	RF	ANA	LS	JD	EC
ro	ro	ro	ro	ro	ro	ro	ro		ro	ro	ro/lhsc	ro	ro/lhsc	ro/lhsc	ro

Field	Bits	Type	Description
100T4	15	ro	100Base-T4 Not supported
100FD	14	ro	100Base-TX Full Duplex 0 _B , PHY is not 100BASE-X full duplex capable 1 _B , PHY is 100BASE-X full duplex capable
100HD	13	ro	100Base-TX Half Duplex 0 _B , PHY is not 100BASE-X half duplex capable 1 _B , PHY is 100BASE-X half duplex capable
10FD	12	ro	10Base-T Full Duplex 0 _B , PHY is not 10Mbit/s Full duplex capable 1 _B , PHY is 10Mbit/s Full duplex capable
10HD	11	ro	10Base-T Half Duplex 0 _B , PHY is not 10Mbit/s Half duplex capable 1 _B , PHY is 10Mbit/s Half duplex capable

Registers Description PHY Registers

Field	Bits	Type	Description
T2FD	10	ro	100BASE-T2 Full Duplex Not supported
T2HD	9	ro	100BASE-T2 half duplex Not supported
Res	8:7	ro	Reserved
MFP	6	ro	MF Preamble Suppression 0 _B , PHY cannot accept management frames with preamble suppression 1 _B , PHY can accept management frames with preamble suppression
ANC	5	ro	Auto-Negotiate Complete 0 _B , Auto-neg incompleted 1 _B , Auto-neg completed
RF	4	ro/lhsc	Remote Fault This bit will remain set until it is cleared by reading register 1 via management interface. 0 _B , No remote fault detected 1 _B , Remote fault detected
ANA	3	ro	Auto-Negotiate Ability 0 _B , PHY cannot Auto-Negotiate 1 _B , PHY can Auto-Negotiate
LS	2	ro/lhsc	Link Status 0 _B , Link is down 1 _B , Link is up
JD	1	ro/lhsc	Jabber Detect Only used in 10Base-T mode. Reads as 0 in 100Base-TX mode 1 _B , Jabber condition detect
EC	0	ro	Extended Capability 0 _B , Basic register set capabilities only 1 _B , Extended register capable.

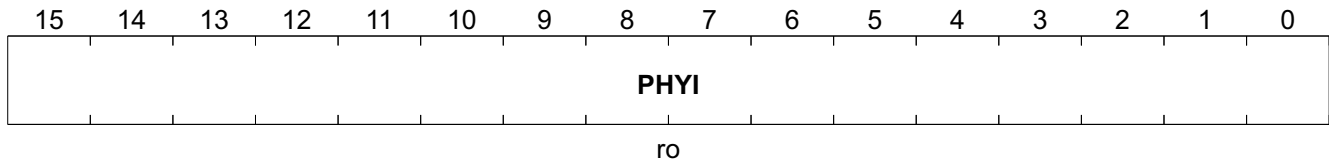
Register 2 and 3

Each PHY has an identifier, which is assigned to the device. The identifier contains a total of 32 bits, which consists of the following: 22 bits of a 24bit organizationally unique identifier (OUI) for the manufacturer; a 6-bit manufacturer's model number; a 4-bit manufacturer's revision number. For an explanation of how the OUI maps to the register, please refer to IEEE 802-1990 clause 5.1

Registers Description PHY Registers

PHY Identifier 1

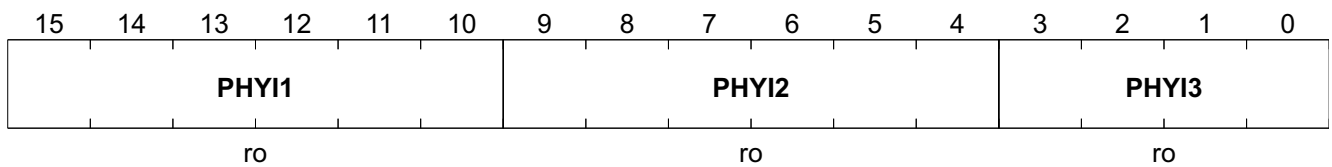
PHYI1 **Offset**
PHY Identifier 1 **2_H** **Reset Value**
001D_H



Field	Bits	Type	Description
PHYI	15:0	ro	PHY Identifier[31-16] OUI (bits 3-18)

PHY Identifier 2

PHYI2 **Offset**
PHY Identifier 2 **3_H** **Reset Value**
2411_H



Field	Bits	Type	Description
PHYI1	15:10	ro	PHY Identifier[15-10] OUI (bits 19-24)
PHYI2	9:4	ro	PHY Identifier[9-4] Manufacturer's Model Number (bits 5-0)
PHYI3	3:0	ro	PHY Identifier[3-0] Revision Number (bits 3-0); Register 3, bit 0 is LS bit of PHY Identifier

Note: This uses the OUI of Infineon-ADMtek, device type of 1 and rev 0.

Auto-Negotiation Advertisement

ANA **Offset** **Reset Value**
Auto-Negotiation Advertisement **4_H** **0001_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NP	Res	RF		NI	PAU	NI	100F D	100H D	10FD	10HD				SF	
rw		rw		ro	rw	ro	rw	rw	rw	rw				ro	

Field	Bits	Type	Description
NP	15	rw	Next Page 0 _B NNP , Device not set to use Next Page 1 _B NP , Device set to use Next Page
RF	13	rw	Remote Fault 0 _B NFD , No fault detected 1 _B RF , Local remote fault sent to link partner
NI	12:11	ro	Not Implemented Technology ability bits A7-A6
PAU	10	rw	Pause Technology ability bit A5
NI	9	ro	Not Implemented Technology ability bit A4
100FD	8	rw	100BASE-TX Full Duplex Technology ability bit A3 0 _B 100NFD , Unit is not capable of Full Duplex 1 _B 100FD , Unit is capable of Full Duplex
100HD	7	rw	100BASE-TX Half Duplex Technology ability bit A2 0 _B 100NHD , Unit is not capable of Half Duplex 100BASE-TX 1 _B 100HD , Unit is capable of Half Duplex
10FD	6	rw	10BASE-T Full Duplex Technology ability bit A1 0 _B 10NFD , Unit is not capable of Full Duplex 10BASE-T 1 _B 10FD , Unit is capable of Full Duplex 10BASE-T
10HD	5	rw	10BASE-T Half Duplex Technology ability bit A0 0 _B 10NHD , Unit is not capable of Half Duplex 10BASE-T 1 _B 10HD , Unit is capable of Half Duplex 10BASE-T
SF	4:0	ro	Selector Field Identifies type of message being sent. Currently only one value is defined.

Registers Description PHY Registers

Auto-Negotiation Link Partner Ability

The register is used to view the advertised capabilities of the link partner once auto negotiation is complete. The contents of this register should not be relied upon unless register 1 bit 5 is set (auto negotiation complete). After negotiation this register should contain a copy of the link partner's register 4. All bits are therefore defined in the same way as for register 4. All bits are readable only. This register is used for Base Page code word only. Base Page Register Format

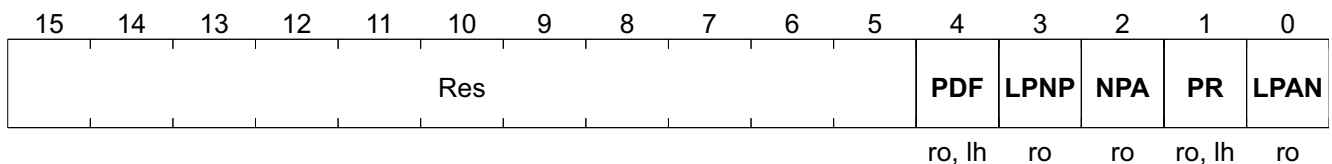
ANLPA **Offset**
Auto-Negotiation Link Partner Ability **5_H** **Reset Value**
0000_H



Field	Bits	Type	Description
NP	15	ro	Next Page 0 _B , Base Page is requested 1 _B , Link Partner is requesting Next Page function
ACK	14	ro	Acknowledge Link Partner acknowledgement bit
RF	13	ro	Remote Fault Link Partner is indicating a fault
TA	12:5	ro	Technology Ability Link Partner technology ability field.
SF	4:0	ro	Selector Field Link Partner selector field

Auto-Negotiation Expansion

ANE **Offset**
Auto-Negotiation Expansion **6_H** **Reset Value**
0004_H



Field	Bits	Type	Description
PDF	4	ro, lh	Parallel Detection Fault 0 _B NFD , No fault detected 1 _B FD , Local Device Parallel Detection Fault

USB CommandGet Register (Vendor Specific) Single/Burst Read

Field	Bits	Type	Description
LPNP	3	ro	Link Partner Next Page Able 0 _B NNP , Link Partner is not Next Page Able 1 _B NP , Link Partner is Next Page Able
NPA	2	ro	Next Page Able 0 _B , Local device is not Next Page Able 1 _B , Local device is Next Page Able
PR	1	ro, lh	Page Received 0 _B NPR , A New Page has not been received 1 _B PR , A New Page has been received
LPAN	0	ro	Link Partner Auto Negotiation Able 0 _B NAN , Link Partner is not Auto negotiation able 1 _B AN , Link Partner is Auto negotiation able

5 USB Command

5.1 Get Register (Vendor Specific) Single/Burst Read

Table 27 Setup Stage

BmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
C0	F0	0	{RegIndex[0:7], 00}	length

Table 28 Data Stage

Offset0(1B)	Offset1(1B)	Offset2(1B)
{RegIndex}	{RegIndex+1}	{RegIndex+2}

The returned total number of registers depends on the length field.

5.2 Set Register (Vendor Specific) Burst Write

Table 29 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
40	F1	0	{RegIndex[0:7], 00}	Length

Table 30 Data Stage

Offset0(1B)	Offset1(1B)	Offset2(1B)	Offset3(1B)
{RegIndex}	{RegIndex+1}	{RegIndex+2}	{RegIndex+3}

Ex. Write 44 to RegIndex = 05_H, the transfer will be

USB CommandGet Status (Device)
Table 31 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
40	F1	4400	0500	0100

If wLength > 1, more than 1 register is accessed (burst write) and mask is not supported => DataStage for 8-byte OUT transfer appears

Ex. Burst write 20 registers from RegIndex = 07_H and data from 01_D to 20_D

Table 32 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
40	F1	0000	0700	1400

- Data Stage

Table 33 1st OUT Transfer

Offset0(1B)	Offset1(1B)	Offset2(1B)	Offset3(1B)	Offset4(1B)	Offset5(1B)	Offset6(1B)	Offset7(1B)
01	02	03	04	05	06	07	08

Table 34 2nd OUT Transfer

Offset0(1B)	Offset1(1B)	Offset2(1B)	Offset3(1B)	Offset4(1B)	Offset5(1B)	Offset6(1B)	Offset7(1B)
09	0A	0B	0C	0D	0E	0F	10

Table 35 3rd OUT Transfer

Offset0(1B)	Offset1(1B)	Offset2(1B)
11	12	13

5.3 Get Status (Device)

Table 36 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength L(1B)	wLength H(1B)
80	0	0	0	2	0

Table 37 Data Stage

D[15:2]	D[1]: Remote Wakeup	D[0]: Self Powered
0	Register of remote_wakeup	1

5.4 Get Status (Interface)

Table 38 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength L(1B)	wLength H(1B)
81	0	0	0	2	0

USB CommandGet Status (EP1) Bulk IN

Table 39 Data Stage

D[15:0]
0

5.5 Get Status (EP1) Bulk IN

Table 40 Setup Stage

bmReq	bReq	wValue(2B)	wIndex L(1B)	wIndex H(1B)	wLength L(1B)	wLength H(1B)
82	0	0	81	00	2	0

Table 41 Data Stage

D[15:1]	D[0]: Halt
0	Register of ep1_halt

5.6 Get Status (EP2) Bulk OUT

Table 42 Setup Stage

bmReq	bReq	wValue(2B)	wIndex L(1B)	wIndex H(1B)	wLength L(1B)	wLength H(1B)
82	0	0	02	00	2	0

Table 43 Data Stage

D[15:1]	D[0]: Halt
0	register of ep2_halt

5.7 Get Status (EP3) Interrupt IN

Table 44 Setup Stage

bmReq	bReq	wValue(2B)	wIndex L(1B)	wIndex H(1B)	wLength L(1B)	wLength H(1B)
82	0	0	83	00	2	0

Table 45 Data Stage

D[15:1]	D[0]: Halt
0	register of ep3_halt

USB CommandGet Descriptor (Device) Total 18-byte
5.8 Get Descriptor (Device) Total 18-byte
Table 46 Setup Stage

bReq	bReq	wValue L(1B)	wValue H(1B)	wIndex(2B)	wLength L(1B)	wLength H(1B)
80	6	01	00	0	Length low	Length high

Table 47 Data Stage: wLength Field Specifies the Total byte Count to Return

Offset 0	Offset 1 (type)	Offset 2 (USB release no. L)	Offset 3 (USB release no. H)	Offset 4 (Class code)	Offset 5 (Sub Class Code)	Offset 6 (Protocol)	Offset 7 (EP0 MaxPktSize)
12(1 _B)	01(1 _B)	10/00(1 _B)	01/02(1 _B)	FF(1 _B)	FF(1 _B)	00(1 _B)	8/64(1 _B)

Table 48 *8/64 := USB 1.1/2.0

Offset 8 (vendor ID) Low	Offset 9 (vendor ID) High	Offset 10 (productID) Low	Offset 11 (productID) High	Offset 12 (releaseID) Low
(1 _B)	(1 _B)	(1 _B)	(1 _B)	01(1 _B)

Table 49 *8/64 := USB 1.1/2.0

Offset 16 (serial no.)	Offset 17 (no. of config)	Offset 13 (releaseID) High	Offset 14 (m anufacture)	Offset 15 (Product)
03(1 _B)	01(1 _B)	01(1 _B)	01(1 _B)	02(1 _B)

Default Value
***Product ID = 8515_H**
***Vendor ID = 07A6_H**
5.9 Get Descriptor (Configuration) Total 39-byte
Table 50 Setup Stage

BmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex(2B)	wLength L(1B)	wLength H(1B)
80	6	02	00	0	Length low	Length high

- Data Stage

Table 51 Configuration Descriptor

Offset 0 (Length)	Offset 1 (DscrType)	Offset 2 (TotalLength) Low	Offset 3 (TotalLength) High	Offset 4 (NumInterface)
09(1 _B)	02(1 _B)	27(1 _B)	00(1 _B)	01(1 _B)

USB CommandGet Descriptor (String) Index 0, LanguageID Code
Table 52 Configuration Descriptor

Offset 8 (MaxPower)	Offset 5 (ConfigValue)	Offset 6 (StringIndex)	Offset 7 (Attribute)
max_pwr(1 _B)	01(1 _B)	00(1 _B)	1 _B 1, powermode, remote wakeup, 5 _H 00(1 _B)

Table 53 Interface 0 Descriptor

Offset 0 (Length)	Offset 1 (DscrType)	Offset 2 (Interface Num)	Offset 3 (AltInterface)	Offset 4 (NumEP)	Offset 5 (IntfClass)	Offset 6 (IntfSubClass)	Offset 7 (IntfProtocol)	Offset 8 (StringIndex)
09(1 _B)	04(1 _B)	00(1 _B)	00(1 _B)	03(1 _B)	FF(1 _B)	FF(1 _B)	00(1 _B)	00(1 _B)

Table 54 EP1 Descriptor

Offset 0 (Length)	Offset 1 (DscrType)	Offset 2 (EPAddr)	Offset 3 (Attribute)	Offset 4 (MaxPktSize) Low	Offset 5 (MaxPktSize) High	Offset 6 (Interval)
07(1 _B)	05(1 _B)	81(1 _B)	02(1 _B) bulk	40 _H /00 _H (1 _B)	00 _H /02 _H (1 _B)	00(1 _B)

Table 55 EP2 Descriptor

Offset 0 (Length)	Offset 1 (DscrType)	Offset 2 (EPAddr)	Offset 3 (Attribute)	Offset 4 (MaxPktSize) Low	Offset 4 (MaxPktSize) High	Offset 6 (Interval)
07(1 _B)	05(1 _B)	02(1 _B)	02(1 _B) bulk	40 _H /00 _H (1 _B)	00 _H /02 _H (1 _B)	00(1 _B)

Table 56 EP3 Descriptor

Offset 0 (Length)	Offset 1 (DscrType)	Offset 2 (EPAddr)	Offset 3 (Attribute)	Offset 4 (MaxPktSize) Low	Offset 5 (MaxPktSize) High	Offset 6 (Interval)
07(1 _B)	05(1 _B)	83(1 _B)	03(1 _B) interrupt	08(1 _B)	00(1 _B)	ep3_interval(1 _B)

5.10 Get Descriptor (String) Index 0, LanguageID Code
Table 57 Setup Stage

BmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex(2B)	wLength Low(1B)	wLength High(1B)
80	06	00	03	0000	Length Low	Length High

Table 58 Data Stage

Offset0 (Length)	Offset1 (DscrType)	Offset2 (LanguageID) L	Offset3 (LanguageID) H
04(1 _B)	03(1 _B)	09(1 _B)	04(1 _B)

USB CommandGet Descriptor (String) Index 1, Manufacture

5.11 Get Descriptor (String) Index 1, Manufacture

Table 59 Setup Stage

BmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex (2B)	wLength Low(1B)	wLength High(1B)
80	06	01	03	0904	Length Low	Length High

Table 60 Data Stage

Offset0 (Length)	Offset1 (DscrType)	
length(1 _B)	03(1B)	String

5.12 Get Descriptor (String) Index 2, Product

Table 61 Setup Stage

BmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex (2B)	wLength Low(1B)	wLength High(1B)
80	06	02	03	0904	Length Low	Length High

Table 62 Data Stage

Offset 0 (Length)	Offset 1 (DscrType)	
length(1 _B)	03(1 _B)	String

5.13 Get Descriptor (String) Index 3, Serial No.

Table 63 Setup Stage

BmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex (2B)	wLength Low(1B)	wLength High(1B)
80	06	03	03	0904	Length Low	Length High

Table 64 Data Stage

Offset 0 (Length)	Offset 1 (DscrType)	
Length(1 _B)	03(1 _B)	String

5.14 Get Configuration

Table 65 Setup Stage

BmReq	bReq	wValue(2B)	wIndex(2B)	wLength Low(1B)	wLength High(1B)
80	08	0	0	1	0

Table 66 Data Stage

D[7:1]	D[0]: cfg_value
0	Register of cfg value

5.15 Get Interface

Table 67 Setup Stage

BmReq	bReq	wValue(2B)	wIndex(2B)	wLength Low(1B)	wLength High(1B)
81	0A	0	0	1	0

Table 68 Data Stage

Offset0 (AltIntf) (1B)
00

5.16 Get Descriptor (DEVICE QUALIFIER)

Table 69 Setup Stage

BmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex(2B)	wLength L(1B)	wLength H(1B)
80	6	06	00	0	Length low	Length high

Table 70 Data Stage

Offset 0 (Length)	Offset 1 (DscrType)	Offset 2 (bcdUSB)	Offset 4 (class)	Offset 5 (subclass)
0A(1 _B)	06(1 _B)	0200 _H (2 _B)	FF _H (1 _B)	FF _H (1 _B)

Table 71 Data Stage

Offset 9 (Reserved)	Offset 6 (DeviceProtocal)	Offset 7 (MaxPktSizefor other speed)	Offset 8 (No of other speed configuration)
00(1 _B)	00 _H (1 _B)	08 _H (1 _B)	01 _H (1 _B)

5.17 Get Descriptor (OTHER SPEED Configuration) Total 39-byte

Table 72 Setup Stage

BmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex(2B)	wLength L(1B)	wLength H(1B)
80	6	07	00	0	Length low	Length high

- Data Stage

USB CommandClear Feature (Device) Remote Wakeup
Table 73 Configuration Descriptor

Offset 0 (Length)	Offset 1 (DscrType)	Offset 2 (TotalLength) Low	Offset 3 (TotalLength) High	Offset 4 (NumInterface)
09(1 _B)	07(1 _B)	27(1 _B)	00(1 _B)	01(1 _B)

Table 74 Configuration Descriptor

Offset 8 (MaxPower)	Offset 5 (ConfgValue)	Offset 6 (StringIndex)	Offset 7 (Attribute)
max_pwr(1 _B)	01(1 _B)	00(1 _B)	1 _B 1, powermode, remote wakeup, 5 _H 00(1 _B)

Table 75 Interface 0 Descriptor

Offset 0 (Length)	Offset 1 (DscrType)	Offset 2 (Interface Num)	Offset 3 (AltInterface)	Offset 4 (NumEP)	Offset 5 (IntfClass)	Offset 6 (IntfSubClass)	Offset 7 (IntfProtocol)	Offset 8 (StringIndex)
09(1 _B)	04(1 _B)	00(1 _B)	00(1 _B)	03(1 _B)	FF(1 _B)	FF(1 _B)	00(1 _B)	00(1 _B)

Table 76 EP1 Descriptor

Offset 0 (Length)	Offset 1 (DscrType)	Offset 2 (EPAddr)	Offset 3 (Attribute)	Offset 4 (MaxPktSize) Low	Offset 5 (MaxPktSize) High	Offset 6 (Interval)
07(1 _B)	05(1 _B)	81(1 _B)	02(1 _B) bulk	40 _H (1 _B)	00 _H (1 _B)	00(1 _B)

Table 77 EP2 Descriptor

Offset 0 (Length)	Offset 1 (DscrType)	Offset 2 (EPAddr)	Offset 3 (Attribute)	Offset 4 (MaxPktSize) Low	Offset 4 (MaxPktSize) High	Offset 6 (Interval)
07(1 _B)	05(1 _B)	02(1 _B)	02(1 _B) bulk	40 _H (1 _B)	00 _H (1 _B)	00(1 _B)

Table 78 EP3 Descriptor

Offset 0 (Length)	Offset 1 (DscrType)	Offset 2 (EPAddr)	Offset 3 (Attribute)	Offset 4 (MaxPktSize) Low	Offset 5 (MaxPktSize) High	Offset 6 (Interval)
07(1 _B)	05(1 _B)	83(1 _B)	03(1 _B) interrupt	08(1 _B)	00(1 _B)	ep3_interval(1 _B)

5.18 Clear Feature (Device) Remote Wakeup
Table 79 Setup Stage

BmReq	bReq	wValue L(1B)	WValue H(1B)	wIndex(2B)	wLength(2B)
00	01	01	00	0	0

5.19 Set Feature (Device) Remote Wakeup
Table 80 Setup Stage

BmReq	bReq	wValue L(1B)	WValue H(1B)	wIndex(2B)	wLength(2B)
00	03	01	00	0	0

5.20 Clear Feature (EP 0, 1, 2, 3) Halt
Table 81 Setup Stage

BmReq	bReq	wValue(2B)	WIndex L(1B)	wIndex L(2B)	WLength(2B)
02	01	0000	EP no	00	0

5.21 Set Feature (EP 0, 1, 2, 3) Halt
Table 82 Setup Stage

BmReq	bReq	wValue(2B)	WIndex H(1B)	wIndex H(2B)	WLength(2B)
02	03	0000	EP no	00	0

Device should respond STALL if ENDPOINT HALT.

5.22 Set Feature (TEST MODE)
Table 83 Setup Stage

BmReq	bReq	wValue(2B)	WIndex H(1B)	wIndex H(2B)	WLength(2B)
02	03	0002	Test selector	00	0

Test selector :

00_H = reserved

01_H = Test_J

02_H = Test_K

03_H = Test_SE0_NAK

others = reserved

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 84 Absolute Maximum Rating

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{DD}	-0.3	–	3.6	V	–
Input Voltage	V_{IN}	-0.5	–	$V_{DD} + 0.5$	V	–
Output Voltage	V_{OUT}	-0.5	–	$V_{DD} + 0.5$	V	–
Storage Temperature	T_{STG}	-65	–	150	°C	–
Ambient Temperature	T_{AMB}	0	–	70	W	–
ESD Rating	V_{ESD}	–	–	2000	V	–

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

6.2 Operating Condition

Table 85 Operating Condition

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{DD}	3.0	–	3.6	V	–
USB Bus Supply Voltage	$5V_{DD}$	4.4	–	5.25	V	–

6.3 DC Specifications

6.3.1 USB Interface DC Specification

Table 86 USB Interface DC Specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input High Voltage	V_{IH}	2.0	–	–	V	–
Input Low Voltage	V_{IL}	–	–	0.8	V	–
Differential Input Sensitivity	V_{DI}	0.2	–	–	V	–
Differential Common Mode Range	V_{CM}	0.8	–	2.5	V	–

Table 86 USB Interface DC Specification (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output High Voltage	V_{CH}	2.8	–	3.6	V	–
Output Low Voltage	V_{OL}	0.0	–	0.3	V	–
Output Signal Crossover Voltage	V_{CRS}	1.3	–	2.0	V	–

6.3.2 EEPROM Interface DC Specification

Recommended Operating Conditions:

Table 87 EEPROM Interface DC Specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input High Voltage	V_{IH}	1.8	–	5.5	V	–
Input Low Voltage	V_{IL}	-0.5	–	1.0	V	–
Input Leakage Current	I_I	-1	–	+1	μ A	$0 < V_{IN} < V_{CC}$
Output High Voltage	V_{OH}	$V_{CC} - 0.2$	–	–	V	$I_{OH} = -10 \mu$ A
Output Low Voltage	V_{OL}	–	–	0.2	V	$I_{OL} = 10 \mu$ A
Input Pin Capacitance	C_{IN}	–	–	5	pF	–

6.3.3 GPIO Interface DC Specification

Table 88 GPIO Interface DC Specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input High Voltage	V_{IH}	1.8	–	5.5	V	–
Input Low Voltage	V_{IL}	-0.5	–	1.0	V	–
Input Leakage Current	I_I	± 1 nA	–	± 1	μ A	$V_{IN} 3.3$ V or 0 V
Output High Voltage	V_{OH}	2.4	–	–	V	–
Output Low Voltage	V_{OL}	–	–	0.4	V	–
Input Pin Capacitance	C_{IN}	–	–	5.64	pF	–

6.4 Timing

6.4.1 Reset Timing

ADM8515/X can be reset either by hardware, software or USB reset.

- A hardware reset is accomplished by asserting the RST# pin after powering up the device. It should have a duration of at least 100 ms to ensure the external 12 MHz crystal is in stable and correct frequency. All registers will be reset to default values.
- A software reset is accomplished by setting the reset bit (bit 3) of the Ethernet Control Register (address 01_H). This software reset will reset all registers to default values.

- When ADM8515/X sees an SE0 on USB bus for more than 2.5 s. This USB reset will reset all registers to default values.

6.4.2 EEPROM Interface Timing

Table 89 EEPROM Interface Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EESK Clock Frequency	t_{EESK}	0	–	1	MHz	–
EECS Setup Time to EESK	t_{EECSS}	0.2	–	–	μ S	–
EECS Hold Time from EESK	t_{EECSH}	0	–	–	ns	–
EEDO Hold Time from EESK	t_{EEDOH}	70	–	–	ns	–
EEDO Output Delay to “1” or “0”	t_{EEDOP}	–	–	2	μ S	–
EEDI Setup Time to EESK	t_{EEDIS}	0.4	–	–	μ S	–
EEDI Hold Time from EESK	t_{EEDIH}	0.4	–	–	μ S	–

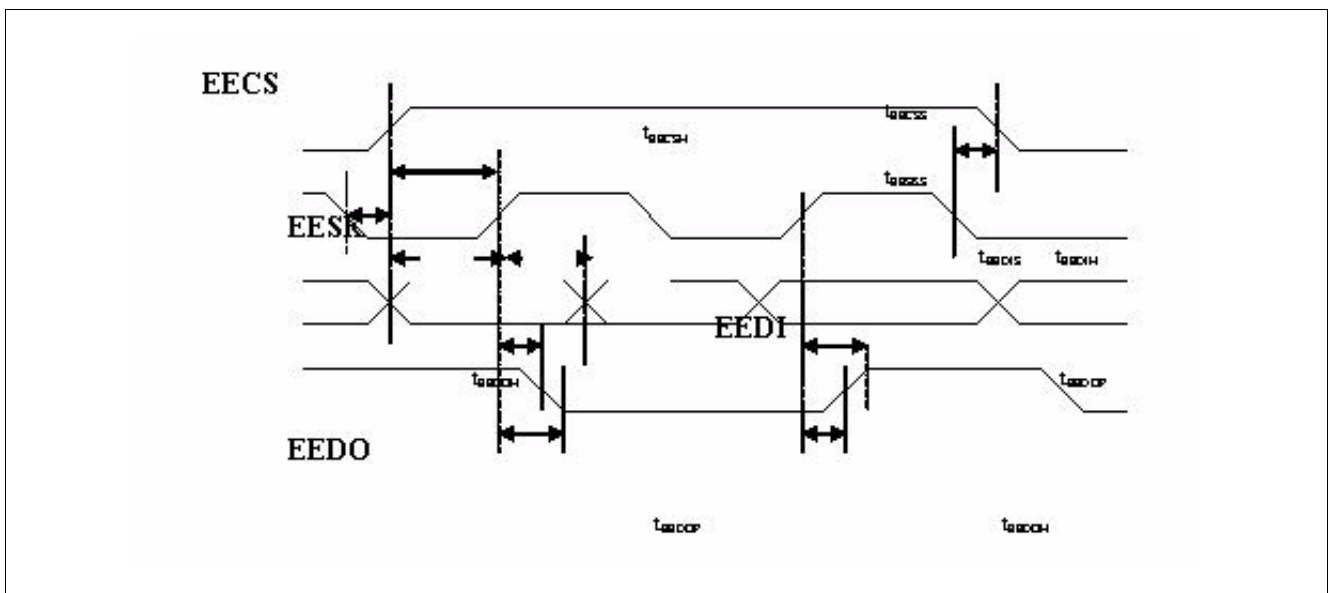


Figure 6 EEPROM Interface Timing

6.4.3 MII Interface Timing

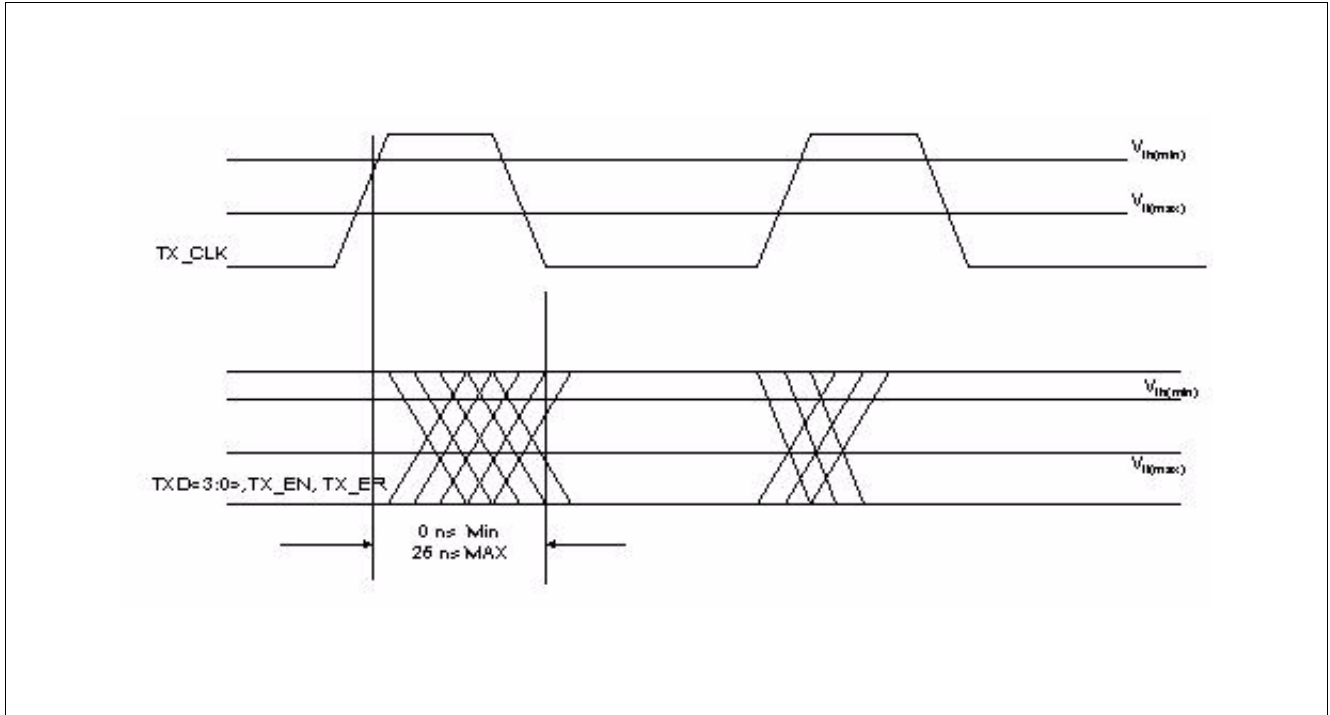


Figure 7 Transmit Signal Timing Relationships at the MII

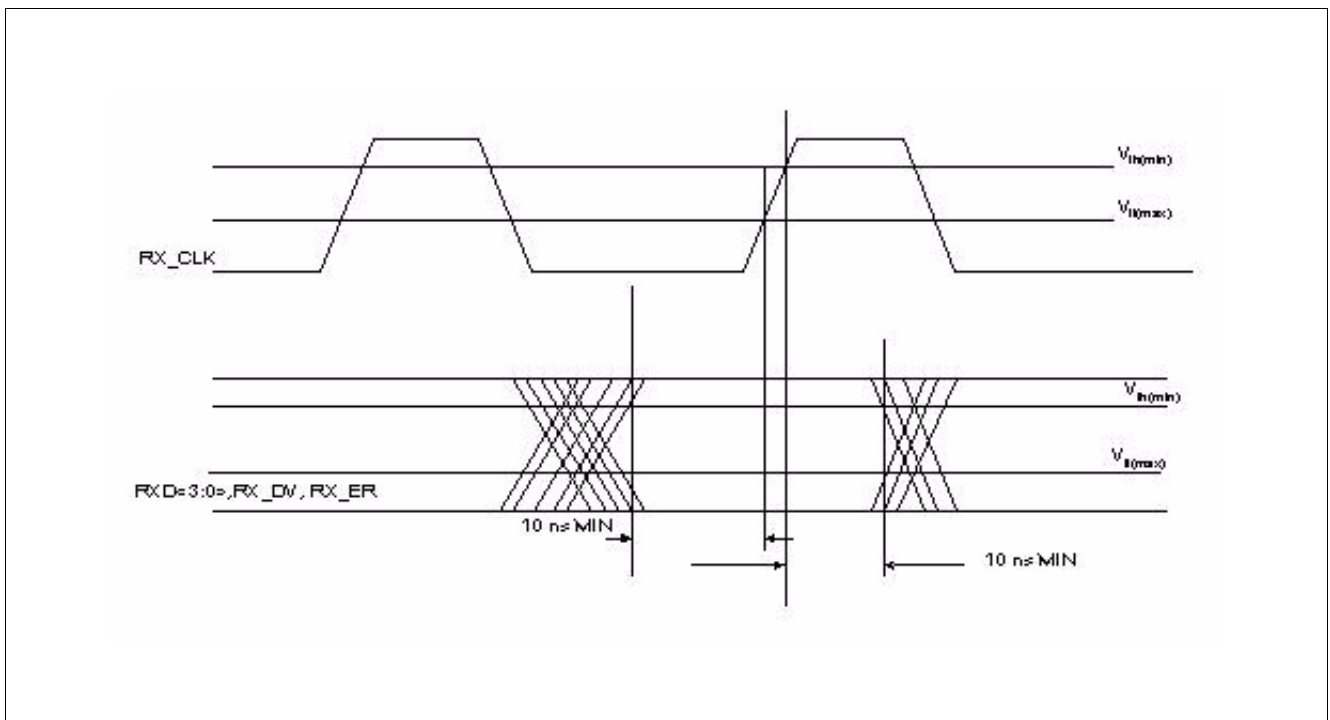


Figure 8 Received Signal Timing Relations at the MII

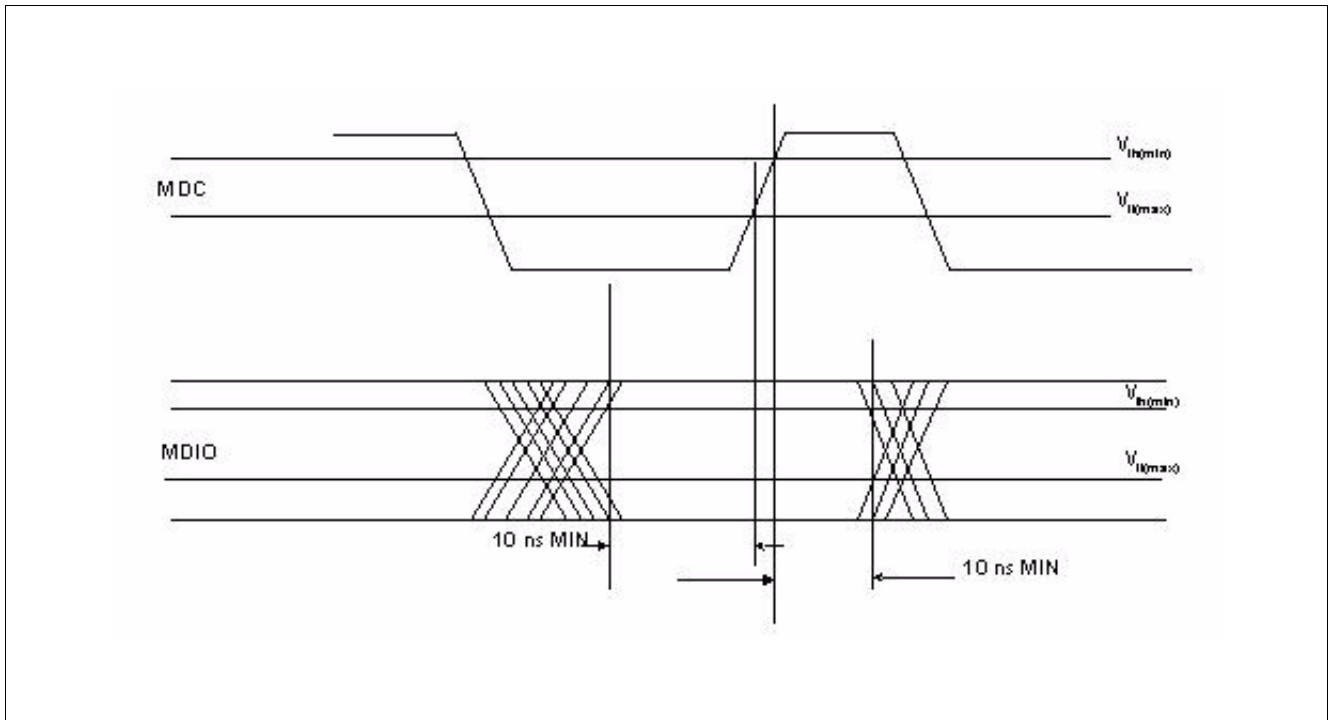


Figure 9 MDIO Sourced by STA

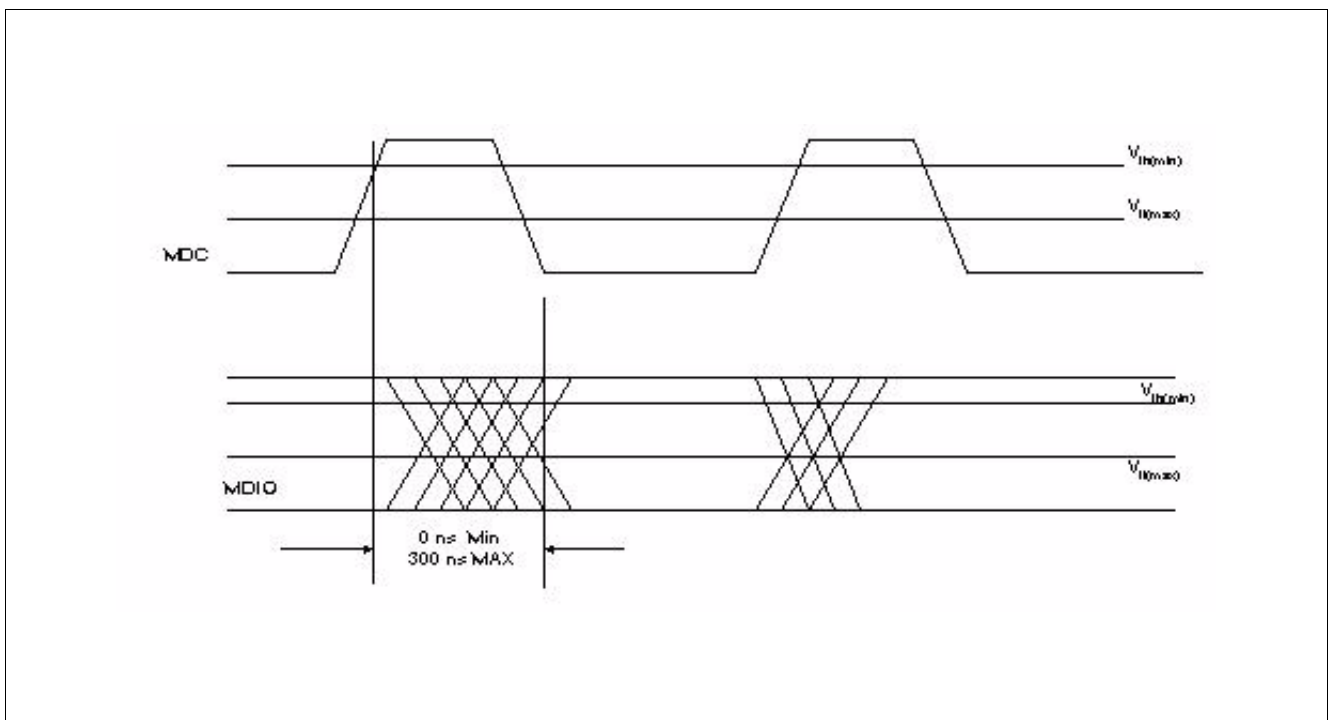


Figure 10 MDIO Sourced by PHY

7 Packaging

Package Outline of ADM8515/X

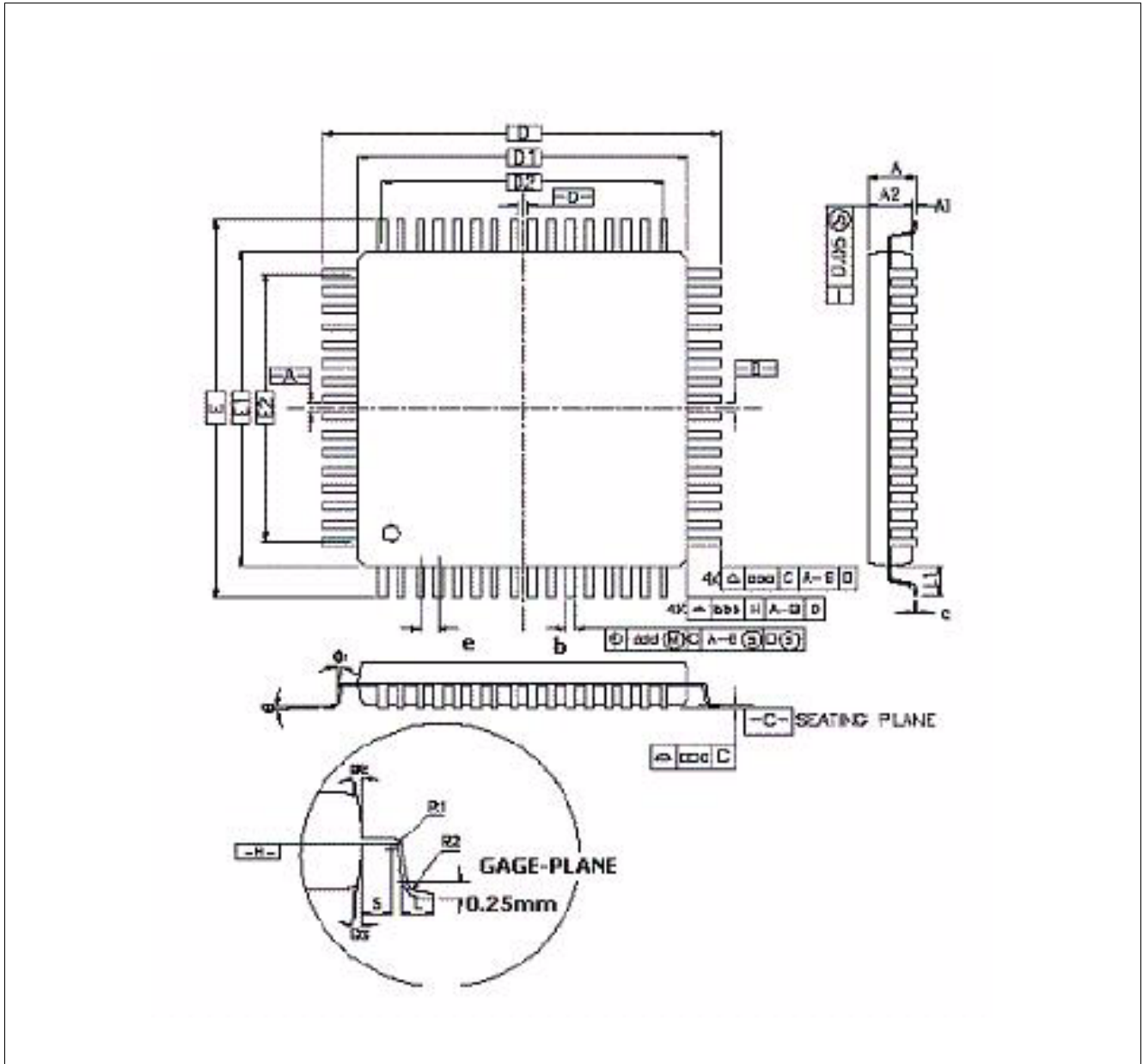


Figure 11 P-LQFP-100-1 (Plastic Low Profile Quad Flat Package)

Note: Dimensions in mm

Table 90 Dimensions for 100 Pin LQFP Package

Symbol	Millimeter (mm)			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	–	–	1.60	–	–	0.063
A ₁	0.05	–	0.15	0.002	–	0.006
A ₂	1.35	1.40	1.45	0.053	0.005	0.057
D	16.00 BSC.			0.630 BSC.		
D ₁	14.00 BSC			0.551 BSC.		
E	16.00 BSC			0.630 BSC.		
E ₁	14.00 BSC			0.551 BSC.		
R ₂	0.08	–	0.20	0.003	–	0.008
R ₁	0.08	–	–	0.003	–	–
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ ₁	0°	–	–	0°	–	–
Θ ₂	11°	12°	13°	11°	12°	13°
Θ ₃	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L ₁	1.00 Ref.			0.039 Ref.		
S	0.20	–	–	0.008	–	–
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D ₂	12.00			0.472		
E ₂	12.00			0.472		
Tolerance of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

8 Appendix

8.1 Appendix 1 EEPROM CONTENT & Example

The EEPROM contents from offset 0 to offset5 is “FF_FF_FF_FF_FF_FF”, the EEPROM isn’t programmed correctly. The default values for every field are used instead of loading from EEPROM.

Offset (byte)	Field	Description
00	node_id0	The 1st byte of Ethernet node ID.
01	node_id1	The 2nd byte of Ethernet node ID.
02	node_id2	The 3rd byte of Ethernet node ID.
03	node_id3	The 4th byte of Ethernet node ID.
04	node_id4	The 5th byte of Ethernet node ID.
05	node_id5	The 6th byte of Ethernet node ID.
06-07	signature	0x8515
08	max_pwr	The maximum USB power consumption.
09	ep3_interval	The polling interval for endpoint 3. If this value is 0, EP3 is disabled.
0A[0]	reserved	
0A[1]	usb_sel	0A[1] = 0: select external USB 2.0 transceiver 0A[1] = 1: select internal USB 2.0 transceiver.
0A[4:2]	Phy MODE	0A[4:2] = 000: tri-state MII pins
0A[6]	Bus power selection	0A[6] = 0: bus power 0A[6] = 1: self power
0A[7]	Remote wake up	0A[7] = 0: with wakeup cap 0A[7] = 1: without wakeup cap
0B[5:0]	reserved	
0B[7:6]	LED mode	Refer to Pin description
0C	Languageid_lo	The low byte of language ID.
0D	Languageid_hi	The high byte of language ID.
0E-0F	reserved	
10	manuid_lo	The low byte of manufacture ID.
11	manuid_hi	The high byte of manufacture ID.
12	proid_lo	The low byte of product ID.
13	proid_hi	The high byte of product ID.
14	manu_str_len	The length for manufacture string.
15	manu_str_offset	The word offset address of manufacture string.
16	pro_str_len	The length for product string.
17	pro_str_offset	The word offset address of product string.
18	seri_str_len	The length for serial number string.
19	seri_str_offset	The word offset address of serial number string.

Table 91 Example

Offset (byte)	Value
0000 _H	00 00 E8 00 02 2C 00 00
0008 _H	50 01 02 00 09 04 00 00
0010 _H	A6 07 15 85 0E 10 2A 20
0018 _H	0A 38 00 00 00 00 00 00
0020 _H	0E 03 41 00 44 00 4D 00
0028 _H	74 00 65 00 6B 00 00 00
0030 _H	1E 00 55 00 53 00 42 00
0038 _H	20 00 31 00 30 00 2F 00
0040 _H	2A 03 55 00 53 00 42 00
0048 _H	20 00 54 00 6F 00 20 00
0050 _H	4C 00 41 00 4E 00 20 00
0058 _H	43 00 6F 00 6E 00 76 00
0060 _H	65 00 72 00 74 00 65 00
0068 _H	72 00 00 00 00 00 00 00
0070 _H	0A 03 30 00 30 00 30 00
0078 _H	31 00 00 00 00 00 00 00

Offset (byte)	Value	Description
00-05	00_00_E8_10_46_02	NIC node ID
08	50	Maximum power 160 mA
09	01	Interrupt endpoint 3 polling interval 1ms
0A	02	Isochronous endpoint disable, select internal USB transceiver, use bus power. Use internal Ethernet PHY, Wake on LAN enable
0C-0D	0904	Language ID 0409
10-11	A607	Manufacture ID 07A6
12-13	8515	Product ID 8515
14	0E	Manufacture string length 0E bytes
15	10	Manufacture string starts from word offset 10 _H , thus byte offset 20 _H .
16	1E	Product string length 1E bytes
17	18	Product string starts from word offset 18 _H , thus byte offset 30 _H .
18	0A	Serial number string length 0A bytes
19	38	Serial number string starts from word offset 38 _H , thus byte offset 70 _H .
20-2E	0E 03 41 00 44 00 4D 00 74 00 65 00 6B 00	0E:descriptor size 14 bytes 03: string descriptor 41.....: UNICODE encoded string

Appendix

Offset (byte)	Value	Description
30-4E	1E 03 55 00 53 00 42 0020 00.....	1E:descriptor size 30 bytes 03: string descriptor 55.....: UNICODE encoded string
50-5A	0A 03 30 00 30 00 30 0031 00	0A: descriptor size 10 bytes 03: string descriptor 30.....: UNICODE encoded string

Terminology

A	
ACK	Acknowledge
B	
BIST	Built In Self Test
C	
COL	Collision
CRC	Cyclic Redundancy Check
CRS	Carrier Sense
D	
DC	Direct Current
DM	Differential Minus
DP	Differential Plus
E	
EP	End Point
ESD	Electro Static Discharge
F	
FIFO	First In First Out
FLP	First Link Pulse
G	
GPIO	General Purpose Input Output
H	
HW	Hardware
I	
I/O	Input/Output
IA	Information Appliance
ISI	Inter-symbol Interface
L	
LAN	Local Area Network
LED	Light Emitting Diode
LH	Latch High
LQFP	Low Profile Quad Flat Package
LS	Least Significant Bit
M	
MAC	Media Access Controller
MDC	Management Data Clock
MDIO	Management Data Input/Output
MFG	Manufacture Program
MII	Media Independent Interface
N	
NAK	Not Acknowledge
NLP	Normal Link Pulse

O	
OS	Operating System
OUI	Organizationally Unique Identifier
P	
P	Power Pin
PHY	Physical Layer
PIE	Parallel Interface Engine
PMD	Physical Medium Dependent
R	
RX	Receive
RXCLK	Receive Clock
RXD	Receive Data
RXDV	Receive Data Valid
S	
SQE	Signal Quality Error
SW	Software
T	
TX	Transmit
TXCLK	Transmit Clock
TXD	Transmit Data
TXIN	Transmit Input Negative
TXIP	Transmit Input Positive
U	
USB	Universal Serial Bus
UTMI	USB 2.0 Transceiver Macrocell Interface
V	
VDD	Voltage
VIN	Voltage In
VOOUT	Voltage out
W	
WAN	Wide Area Network
X	
XCVR	Transceiver
xDSL	A/S/V DSL

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