MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Advance Information

Four 32K x 9-Bit Synchronous Dual I/O FAST Static RAM Multichip Module with Parity Checker

462110

The 462110 multichip module uses four 62110 FAST Static random access memory die. Each 62110 die is a 294,912 bit synchronous static random access memory organized as 32,768 words of 9 bits, fabricated using Motorola's high performance silicon gate CMOS technology. Each die integrates a 32K x 9 SRAM core with advanced peripheral circuitry consisting of address registers, two sets of input data registers, two sets of output latches, active high and active low chip enables, and a parity checker. The RAM checks odd parity during RAM read cycles. The data parity error ($\overline{DPE}$) output is an open drain type output which indicates the result of this check. This module has increased output drive capability supported by multiple power pins.

The multichip module has both asynchronous and synchronous inputs. Asynchronous inputs include the processor output enable ($\overline{POE}$), system output enable ($\overline{SOE}$), and the clock (K).

The address (A_0–A_{14}) and chip enable ($\overline{E}_1$–$\overline{E}_4$ and E_2) inputs are synchronous and are registered on the falling edge of K. Write enable ($\overline{W}$), processor input enable ($\overline{PIE}$) and system input enable ($\overline{SIE}$) are registered on the rising edge of K. Writes to the RAM are self-timed.

All data inputs/outputs, PDQ_0–PDQ_{31}, SDQ_0–SDQ_{31}, $PDQP_1$–$PDQP_4$, and $SDQP_1$–$SDQP_4$ have input data registers triggered by the rising edge of the clock. These pins also have three-state output latches which are transparent during the high level of the clock and latched during the low level of the clock.

This module has a special feature which allows data to be passed through the RAM between the system and processor ports in either direction. This streaming is accomplished by latching in data from one port and asynchronously output enabling the other port. It is also possible to write to the RAM while streaming.

The 462110 is available in a 420–pin ceramic Low Cost Land Grid Array (LGA) package. This single packaged multichip module provides a 3x space savings over the multiple packaged solution.

This module is ideally suited for pipelined systems and systems with multiple data buses and multi-processing systems, where a local processor has a bus isolated from a common system bus.

- Single 5 V ± 10% Power Supply
- Fast Access and Cycle Times: 17/25/35 ns Max
- High Density Land Grid Array package with heat spreader
- Additional power supply pins have been utilized for maximum performance
- Self–Timed Write Cycles
- Clock Controlled Output Latches
- Low Profile Package is 25 mm (1.0") square and 2.9 mm (.144") high
- Address, Chip Enable, and Data Input Registers
- Common Data Inputs and Data Outputs
- Dual I/O for Separate Processor and Memory Buses
- Separate Output Enable Controlled Three–State Outputs
- Odd Parity Checker during Reads
- Open Drain Output on Data Parity Error ($\overline{DPE}$) Allowing Wire–ORing of Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- Active High and Low Chip Enables for Easy Memory Depth Expansion

CPTO
Commercial Plus Technologies Operation

AVAILABLE AS
1)	JAN:	N/A
2)	SMD:	N/A
3)	883:	N/A
4)	CMP:	462110-XX/*

*See Commercial Plus and Avionics Options:
(BR914/D)

XX = Speed in ns (15, 17, 20)

PIN NAMES and FUNCTION

$A_0 - A_{14}$	Address Inputs
K	Clock Inputs
$\overline{W}$	Write Enable
$\overline{E}_1 - \overline{E}_4$	Active Low Chip Enable
E_2	Active High Bussed Chip Enable
$\overline{PIE}$	Processor Input Enable
$\overline{SIE}$	System Input Enable
$\overline{POE}$	Processor Output Enable
$\overline{SOE}$	System Output Enable
$\overline{DPE}_1 - \overline{DPE}_4$	Data Parity Error
$PDQ_0 - PDQ_3$	Processor Data I/O
$PDQP_0 - PDQ_4$	Processor Data Parity
$SDQ_0 - SDQ_{31}$	System Data I/O
$SDQP_1 - SDQP_4$	System Data Parity
V_{CC}	+ 5.0 Power Supply
V_{SS}	Ground

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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Rev. 1

BLOCK DIAGRAM
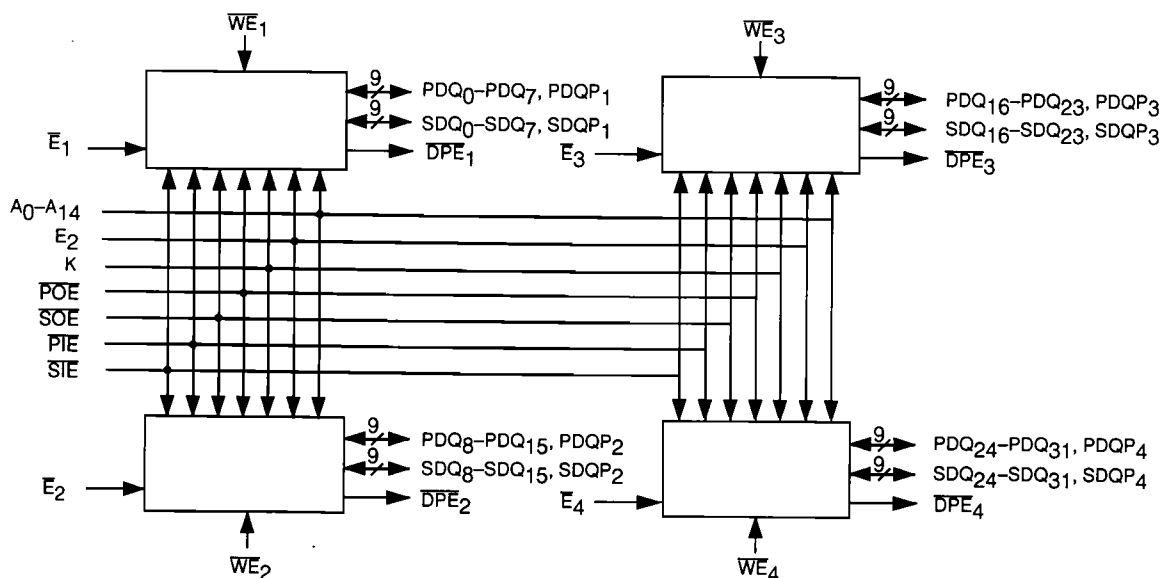
FUNCTIONAL TRUTH TABLE (See Notes 1 and 8)

$\overline{W}$	$\overline{PIE}$	$\overline{SIE}$	$\overline{POE}$	$\overline{SOE}$	Mode	Memory Subsystem Cycle	PDQ_{0-31}, $PDQP_{1-4}$ Output	SDQ_{0-31}, $SDQP_{1-4}$ Output	$\overline{DPE}$	Notes
1	1	1	0	1	Read	Processor Read	Data Out	High–Z	Parity Out	2, 3
1	1	1	1	0	Read	Copy Back	High–Z	Data Out	Parity Out	2, 3
1	1	1	0	0	Read	Dual Bus Read	Data Out	Data Out	Parity Out	2, 3
1	X	X	1	1	Read	NOP	High–Z	High–Z	1	–
X	0	0	X	X	N/A	NOP	High–Z	High–Z	1	4
0	0	1	1	1	Write	Processor Write Hit	Data In	High–Z	1	5
0	1	0	1	1	Write	Allocate	High–Z	Data In	1	–
0	0	1	1	0	Write	Write Through	Data In	Stream Data	1	6
0	1	0	0	1	Write	Allocate With Stream	Stream Data	Data In	1	6
1	0	1	1	0	N/A	Cache Inhibit Write	Data In	Stream Data	1	6
1	1	0	0	1	N/A	Cache Inhibit Read	Stream Data	Data In	1	6
0	1	1	X	X	N/A	NOP	High–Z	High–Z	1	4
X	0	1	0	0	N/A	Invalid	Data In	Stream	1	7
X	0	1	0	1	N/A	Invalid	Data In	High–Z	1	7
X	1	0	0	0	N/A	Invalid	Stream	Data In	1	7
X	1	0	1	0	N/A	Invalid	High–Z	Data In	1	7

NOTES:

1. A '0' represents an input voltage $\geq V_{IL}$ and a '1' represents an input voltage $\geq V_{IH}$. All inputs must satisfy the specified setup and hold times for the falling or rising edge of K. Some entries in this truth table represent latched values. This table assumes that a chip is selected (for example, $\overline{E}_{1-4}=0$ and $E_2 = 1$) and V_{CC} current is equal to I_{CCA} of the selected die. If this is not true, the chip will be in standby mode, the V_{CC} current will equal I_{SB1} or I_{SB2}. $\overline{DPE}$ will default to 1 and all RAM outputs will be in High–Z. Other possible combinations of control inputs not covered by this note or the table above are not supported and the RAM's behavior is not specified.
2. A read cycle is defined as a cycle where data is driven on the internal data bus by the RAM.
3. $\overline{DPE}$ is registered on the rising edge of K at the beginning of the following clock cycle.
4. No RAM cycle is performed.
5. A write cycle is defined as a cycle where data is driven onto the internal data bus through one of the data I/O ports (PDQ_0–PDQ_{31} and $PDQP_{1-4}$ or SDQ_0–SDQ_{31} and $SDQP_{1-4}$), and written into the RAM.
6. Data is driven on the internal data bus by one I/O port through its data input register and latched into the data output latch of the other I/O port.
7. Data contention will occur.
8. If either $\overline{IE}$ signal is sampled low on the rising edge of clock, the corresponding $\overline{OE}$ is a don't care, and the corresponding outputs are High–Z.

PARITY CHECKER

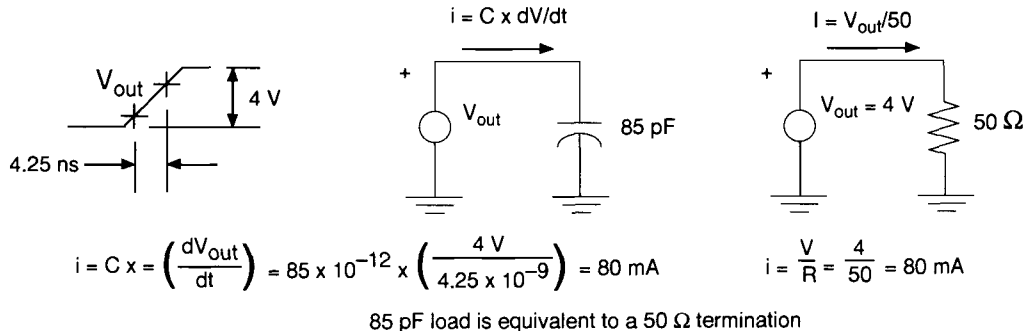| Parity Scheme	$\overline{DPE}$
$\overline{E}_1 = V_{IH}$ and/or $\overline{E}_2 = V_{IL}$	1
RAMP = $\overline{RAM0 \oplus RAM1 \oplus \ldots RAM7}$	1
RAMP ≠ $\overline{RAM0 \oplus RAM1 \oplus \ldots RAM7}$	0

NOTE: RAMP, $\overline{RAM0}$, $\overline{RAM1}$..., refer to the data that is present on the RAM's internal bus, not necessarily data that resides in the RAM array. $\overline{DPE}$ is always delayed one clock, and is registered on the rising edge of K at the beginning of the following clock cycle (see AC CHARACTERISTICS).

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. This device contains circuitry that will ensure the output devices are in High–Z at power up.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 70°C)	P_D	4.8	W
Temperature Under Bias	T_{bias}	–10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

CAPACITIVE LOAD EQUIVALENT RESISTANCE

$$i = C x = \left(\frac{dV_{out}}{dt}\right) = 85 \times 10^{-12} \times \left(\frac{4\,V}{4.25 \times 10^{-9}}\right) = 80\,mA \qquad i = \frac{V}{R} = \frac{4}{50} = 80\,mA$$

85 pF load is equivalent to a 50 Ω termination

AC TEST LOADS
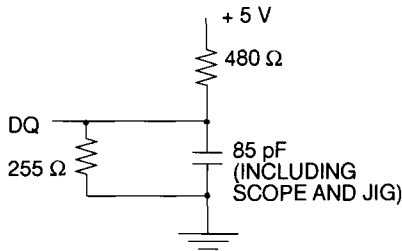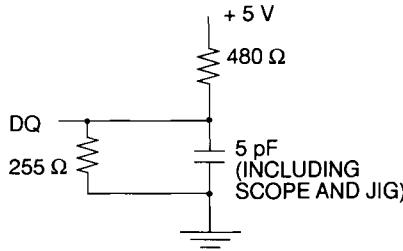
Figure 1A

Figure 1B
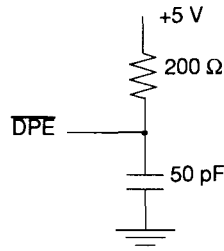
Figure 1C

DC OPERATING CONDITIONS AND CHARACTERISTICS
(V_{CC} = 5.0 V $\pm$ 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ}$ = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	–0.5*	0.0	0.8	V

*V_{IL} (min) = - 3.0 V ac (pulse width $\leq$ 20 ns)

DC CHARACTERISTICS

Parameters	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC}	$I_{lkg(I)}$	–	–	±4.0	µA
Output Leakage Current ($\overline{POE}$, $\overline{SOE}$ = V_{IH})	$I_{lkg(O)}$	–	–	±4.0	µA
AC Supply Current (All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} $\geq$ 3.0 V, I_{out} = 0 mA, Cycle Time $\geq$ t_{KHKH} min) MCM62110–15: t_{KHKH} = 15 ns MCM62110–17: t_{KHKH} = 17 ns MCM62110–20: t_{KHKH} = 20 ns	I_{CCA}	– – –	680 720 760	760 760 760	mA
TTL Standby Current (V_{CC} = Max, $\overline{E}_1$ = V_{IH} or E_2 = V_{IL})	I_{SB1}	–	–	160	mA
CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E}_1$ = V_{IH} or E2 = V_{IL}, $V_{in} \leq V_{SS}$ + 0.2 V or $\geq V_{CC}$ – 0.2V)	I_{SB2}	–	–	120	mA
Output Low Voltage (I_{OL} = + 8.0 mA, $\overline{DPE}$: I_{OL} = + 23.0 mA)	V_{OL}	–	–	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	–	–	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (all Pins Except I/Os)	C_{in}	8	12	pF
Input/Output Capacitance (PDQ$_0$–PDQ$_{31}$, SDQ$_0$–SDQ$_{31}$, PDQP$_{1-4}$, SDQP$_{1-4}$)	$C_{I/O}$	20	28	pF
Data Parity Error Output Capacitance ($\overline{DPE}$)	C_{out} ($\overline{DPE}$)	20	28	pF

PAD INTERCONNECTION LIST

Pin Function	ARRAY PAD				ARRAY PAD				Pin Function
	U1	U2	U3	U4	U1	U2	U3	U4	
Clk	Z12	←	←	←	A13	←	←	←	A9
$\overline{WE}$	M3	C17	V22	X9	A12	←	←	←	A8
$\overline{POE}$	Z14	←	←	←	A11	←	←	←	A7
$\overline{SOE}$	Z15	←	←	←	A10	←	←	←	A5
$\overline{PIE}$	Z16	←	←	←	A9	←	←	←	A3
$\overline{SIE}$	Z17	←	←	←	A8	←	←	←	A1
E	U3	←	←	←	E3	F22	N22	P2	SDQ0
$\overline{E}$	M2	L24	U23	T3	F2	G22	N23	P1	PDQ0
PDQ7	M1	K22	U22	S3	G2	H22	N24	Q1	SDQ2
SDQ7	L3	J23	T23	R3	H1	J22	P22	R2	PDQ2
PDQ5	K2	J24	S23	Q3	H2	K23	Q24	R1	SDQ4
SDQ5	K3	H23	R24	Q2	J1	K24	Q22	S2	PDQ4
PDQ3	J3	H24	R23	P3	J2	L22	R22	S1	SDQ6
SDQ3	H3	G23	Q23	N1	K1	M24	S22	T2	PDQ6
PDQ1	G3	F23	P24	N2	L1	M23	S24	U2	SDQP
SDQ1	F3	E22	P23	N3	L2	M22	T22	V3	PDQP
A14	A17	←	←	←	Z8	←	←	←	A0
A13	A16	←	←	←	Z9	←	←	←	A2
A12	A15	←	←	←	Z10	←	←	←	A4
A11	B13	←	←	←	Z11	←	←	←	A6
A10	A14	←	←	←	Y9	Y17	Y17	Y16	$\overline{DPE}$

Note: (←) indicates a bussed connection.
V_{CC}: B7, B18, Y7, Y18
Gnd: B6, B19, H4, H21, S21, Y6, Y19

PAD ARRAY DIAGRAM

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462110/D