2X20W Stereo Digital Audio Amplifier with DRC

Features

- 16/18/20/24-bit input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting)
  Loudspeaker: 94dB (PSNR), 106dB (DR) @24V
- Multiple sampling frequencies (Fs)
  32kHz / 44.1kHz / 48kHz and
  64kHz / 88.2kHz / 96kHz and
  128kHz/176.4kHz/192kHz
- System clock = 64x, 128x, 256x, 384x, 512x, 768x, 1024x Fs
  256x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  128x~512x Fs for 64kHz / 88.2kHz / 96kHz
  64x~256x Fs for 128kHz/176.4kHz/192kHz
- Supply voltage
  3.3V for digital circuit
  10V~26V for loudspeaker driver
- Loudspeaker output power for 24V
  10W x 2CH into 8Ω @0.16% THD+N for stereo
  15W x 2CH into 8Ω @0.18% THD+N for stereo
  20W x 2CH into 8Ω @0.24% THD+N for stereo
- Sounds processing including:
  Volume control (+24dB~-103dB, 0.125dB/step)
  Dynamic range control
  Power clipping
  Channel mixing
  User programmed noise gate with hysteresis window
  DC-blocking high-pass filter
- Anti-pop design
- Short circuit and over-temperature protection
- I^2C control interface
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage detection
- Power saving mode
- Dynamic temperature control

Applications

- TV audio
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio

Description

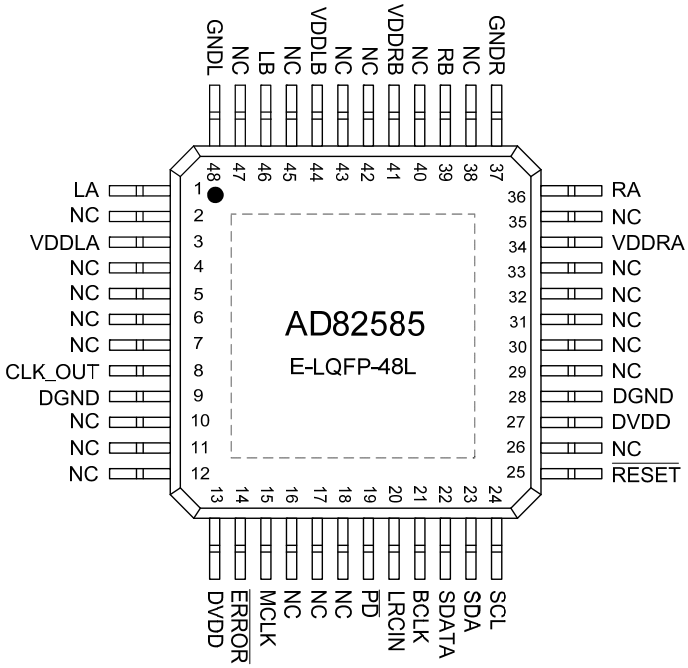
AD82585 is a digital audio amplifier capable of driving a pair of 8Ω, 20W speaker which operate with play music at a 24V supply without external heat-sink or fan requirement.

Using I^2C digital control interface, the user can control AD82585's input format selection, mute and volume control functions. AD82585 has many built-in protection circuits to safeguard AD82585 from connection errors.

Ordering Information

Product ID	Package	Packing / MPQ	Comments
AD82585-LG48NAY	E-LQFP-48L (7x7 mm)	2.5K Units / Small Box (250 Units / Tray, 10 Trays / Small Box)	Green

Pin Assignment (Top View)



Pin Description

PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	LA	O	Left channel output A.	
2	NC		Not connected.	
3	VDDLA	P	Left channel supply A.	
4	NC		Not connected.	
5	NC		Not connected.	
6	NC		Not connected.	
7	NC		Not connected.	
8	CLK_OUT	O	Clock output from PLL.	TTL output buffer
9	DGND	P	Digital ground.	
10	NC		Not connected.	
11	NC		Not connected.	
12	NC		Not connected.	
13	DVDD	P	Digital Power.	
14	$\overline{\text{ERROR}}$	O	Error status, low active.	Open-drain output
15	MCLK	I	Master clock input.	Schmitt trigger TTL input buffer
16	NC		Not connected.	
17	NC		Not connected.	
18	NC		Not connected.	
19	$\overline{\text{PD}}$	I	Power down, low active	Schmitt trigger TTL input buffer

20	LRCIN	I	Left/Right clock input (Fs).	Schmitt trigger TTL input buffer
21	BCLK	I	Bit clock input (64Fs).	Schmitt trigger TTL input buffer
22	SDATA	I	Serial audio data input.	Schmitt trigger TTL input buffer
23	SDA	I/O	I^2C bi-directional serial data.	Schmitt trigger TTL input buffer
24	SCL	I	I^2C serial clock input.	Schmitt trigger TTL input buffer
25	$\overline{\text{RESET}}$	I	Reset, low active.	Schmitt trigger TTL input buffer
26	NC		Not connected.	
27	DVDD	P	Digital power.	
28	DGND	P	Digital Ground.	
29	NC		Not connected.	
30	NC		Not connected.	
31	NC		Not connected.	
32	NC		Not connected.	
33	NC		Not connected.	
34	VDDRA	P	Right channel supply A.	
35	NC		Not connected.	
36	RA	O	Right channel output A.	
37	GNDR	P	Right channel ground.	
38	NC		Not connected.	
39	RB	O	Right channel output B.	
40	NC		Not connected.	
41	VDDRB	P	Right channel supply B.	
42	NC		Not connected.	
43	NC		Not connected.	
44	VDDLB	P	Left channel supply B.	
45	NC		Not connected.	
46	LB	O	Left channel output B.	
47	NC		Not connected.	
48	GNDL	P	Left channel ground.	