Ordering number : ENA0584

SANYO

SANYO Semiconductors

DATA SHEET

LV5254LG — Bi-CMOS LSI Inverting Charge Pump Regulator IC

Overview

The LV5254LG is an inverting charge pump regulator IC.

Functions

- Inverting charge pump regulator

Specifications

Absolute Maximum Ratings at Ta = 25°C, SGND and PGND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Input supply voltage	V_{DD} max	$SV_{DD} = PV_{DD}$	6.5	V
VS pin input voltage	VS max		6.5	V
STBY pin input voltage	STBY max		6.5	V
S1 and S2 pin input voltage	S1, S2 max		6.5	V
Maximum output current	I_{OUT}		110	mA
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-40 to +125	°C

Recommended Operating Conditions at Ta = 25°C, SGND and PGND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Input supply voltage	V_{DD}	$SV_{DD} = PV_{DD}$	3.5 to 6	V
VS pin input voltage	VS		1 to 4.5	V
Output current	I_{OUT}		100	mA

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Electrical Characteristics

(a) Electrical Characteristics

Ta = 25°C, SV_{DD} and PV_{DD} = 4.6V, SGND and PGND = 0V, CLK = 2MHz, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output ripple	Vrp	C2, C5 = 1μF, I_O = 60mA		20		mVp-p
Standby mode V_{DD} current	I_{dd}stby				1	μA
Operating V_{DD} current 1	I_{dd}ope1	I_O = 0mA		2.2		mA
Operating V_{DD} current 2	I_{dd}ope2	I_O = 60mA		3.2		mA
Power efficiency	Peff	V_{DD} = 4.6V, V_{OUT} = -2.8V, I_{OUT} = 60mA		57.5		%
Reference voltage	V_{REF}		1.262	1.300	1.339	V
Overcurrent protection threshold current	I_{OCP}		115			mA
Overcurrent protection latch off wait time	t_{OCP}	Fclk = 2MHz		6		ms
Regulator output on time	tregon	Fclk = 2MHz		3.5		ms
Internal clock frequency*	fclk			2		MHz
Thermal shutdown circuit operating temperature	TSD	Design guarantee		170		°C
V_{OUT} discharge resistance	RDIS			650		Ω
VS pin input resistance	RVS		180	280	480	kΩ
STBY pin pull-down resistance	RSHD		100	170	300	kΩ
STBY pin control voltage	V_{th}H		1.6		V_{DD}	V
	V_{th}L		0		0.3	V
S1 and S2 pin control voltage	V_{th}H		0.7V_{DD}		V_{DD}	V
	V_{th}L		0		0.3	V

* : The charge pump operating frequency, Fcp, is the internal clock frequency divided by two, i.e. Fclk/2.

(b) Output Characteristics

Ta = 25°C, SV_{DD} and PV_{DD} = 4.6V, SGND and PGND = 0V, CLK = 2MHz, unless otherwise specified.

Fixed Output Voltage (Vout = -2.8V) Mode

Outputs a fixed voltage of -2.8V determined by an internal resistor.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input supply voltage	V_{DD}	SV_{DD} = PV_{DD}	4.37		4.83	V
Output voltage precision	V_{OUT}	V_{DD} = +4.37 to +4.83V I_{OUT} = 60mA	-2.884	-2.8	-2.716	V
Maximum output current	I_{OUT}	V_{DD} = +4.37 to +4.83V V_{OUT} = -2.8V			70	mA

VS Mode

Outputs a voltage that is -1 times the voltage VS input to the VS pin.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
VS pin input voltage	VS		1		4.5	V
VS pin output voltage range	V_{OUT}	*1	-4.5		-1	V
Output voltage precision		VS = 1 to 2V, I_{OUT} = 0 to 60mA	-1.05VS	-VS	-0.95VS	V
Output voltage precision		VS = 2 to 4.5V, I_{OUT} = 0 to 60mA	-1.03VS	-VS	-0.97VS	V

External Setting Mode

Outputs a voltage determined by external resistors and the external reference voltage.

See page 8, External Setting Mode Applications and the Output Voltage Setting Method for the method for setting the V_{OUT} voltage.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output voltage range	V_{OUT}	*1	-4.5		-1	V
FB pin voltage	VFB	V_{DD} = 5V, I_{OUT} = 0 to 100mA	-5		20	mV
FB pin current	IFB	V_{DD} = 5V, I_{OUT} = 0 to 100mA		70	200	nA

*1 : The V_{OUT} range that can be set and the current drive capacity of the charge pump regulator are, in principle, determined by the relationship between the values of the V_{DD} voltage and the set voltage. (See the "Relationship Between the Input and Output Voltages") Contact your SANYO Semiconductors representative for more detailed information.

Logic Function Tables

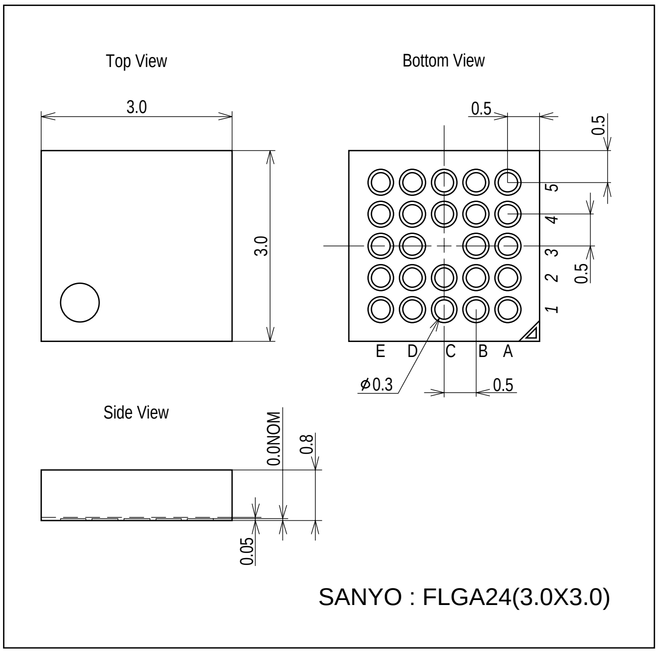
The pins S1 and S2 must be connected to V_{DD} (high) or ground (low) according to the mode to be used.

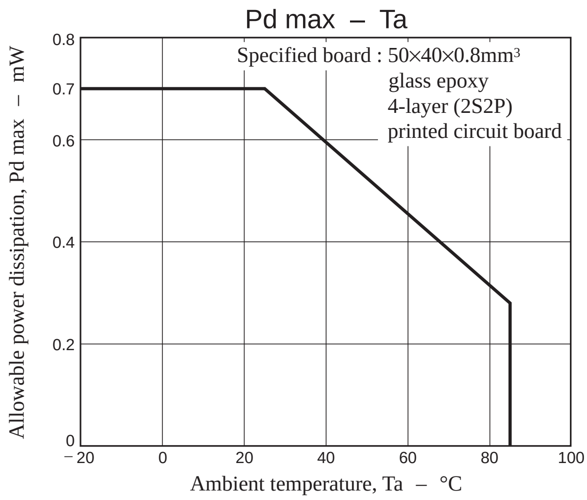
Mode	Description	S1	S2
Mode 1	Outputs a fixed voltage of -2.8V determined by an internal resistor.	High	Low
Mode 2	Outputs a voltage that is -1 times the voltage VS input to the VS pin.	Low	High
Mode 3	Outputs a voltage determined by an external resistor and the external reference voltage.	High	High

Package Dimensions

unit : mm (typ)

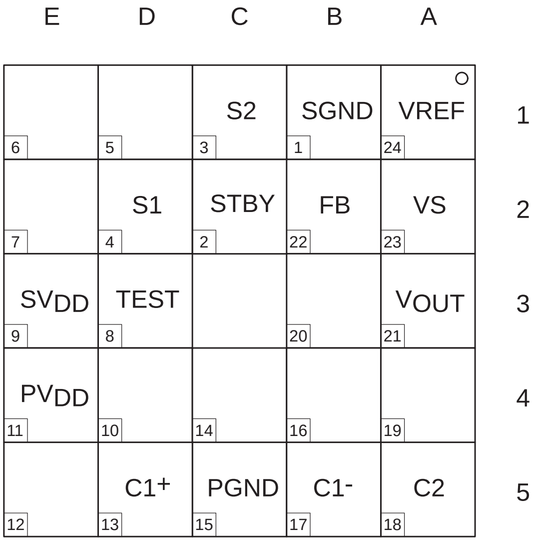
3330





Pin Assignment

FLGA24 (3mm×3mm)



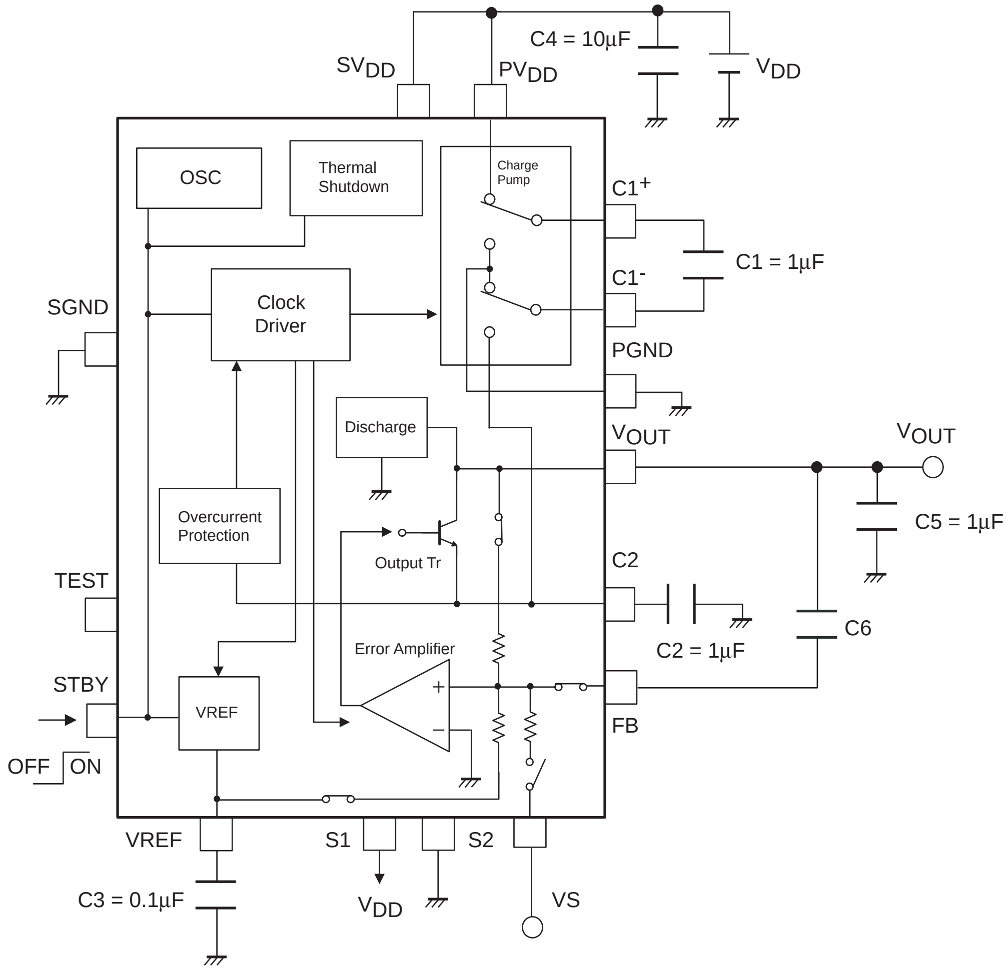
TOP VIEW

Pin Descriptions

Pin No.	Pin	Functions
9	SV_{DD}	Small signal system V_{DD}
11	PV_{DD}	Power system V_{DD}
1	SGND	Small signal system ground
15	PGND	Power system ground
13	$C1^{+}$	Inversion capacitor connection (driver side)
17	$C1^{-}$	Inversion capacitor connection (charge transfer side)
18	C2	Charge pump output
21	V_{OUT}	Regulator output
24	VREF	Band gap voltage output
22	FB	Feedback pin
23	VS	VS mode output setting
2	STBY	Standby mode control
4	S1	Sensing mode selection 1
3	S2	Sensing mode selection 2
8	TEST	Test mode enable (normally not used)

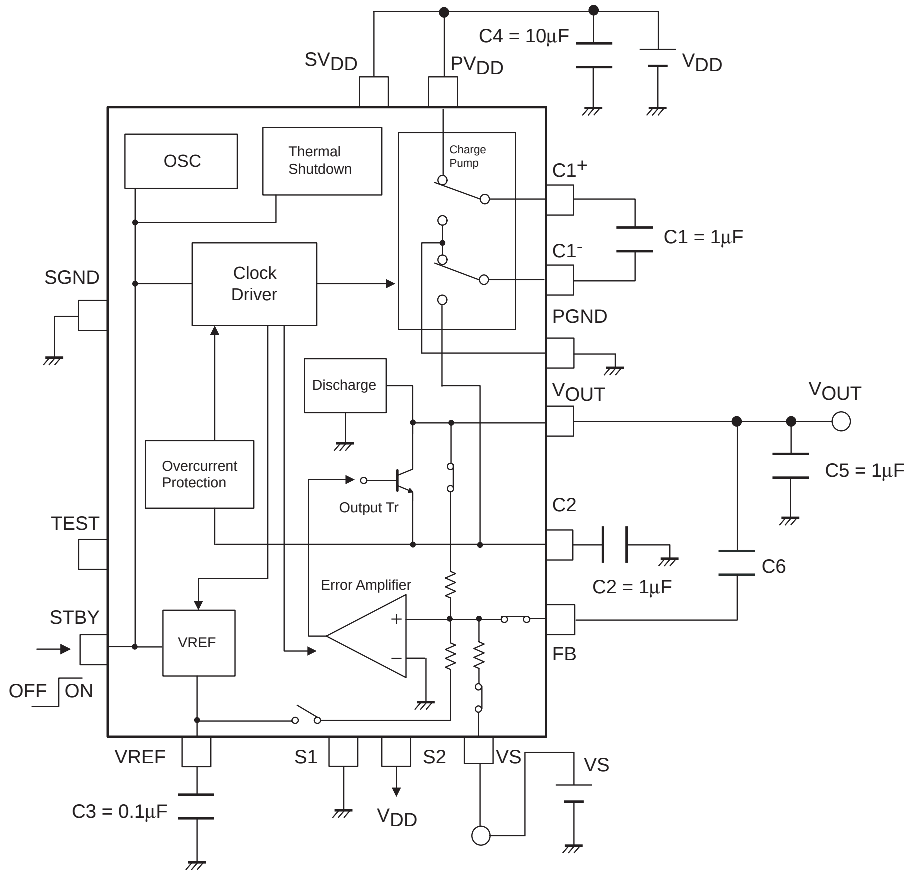
* : The test mode enable pin must be left open. (There is a built-in pull-down resistor, and this pin should always be low.)

Block Diagram and Application Circuit Example 1 (Internal fixed-voltage mode)

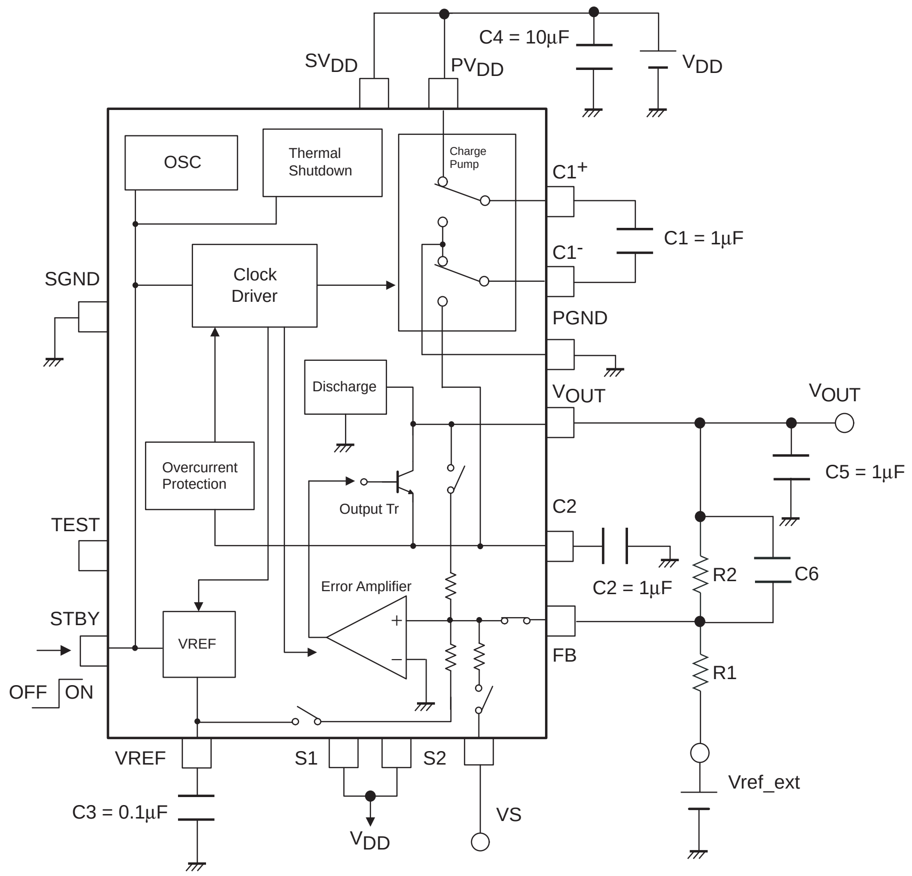


- Use ceramic capacitors for the external capacitors and connect them as close as possible to the IC. We recommend using class B devices with excellent temperature characteristics.)
- Use capacitors with the same values for the charge pump capacitors C1 and C2.
  We recommend a capacitance of 1µF for C1 and C2. (See figure 4 on page 10)
- SV_{DD} and PV_{DD} must be at the same potential. Short them together with the shortest possible line and use a ceramic capacitor with a value of 1µF or greater for C4 (which is inserted between this point and PGND). C4 must be mounted as close as possible to the IC.
- C6 is a phase compensation capacitor. It is required for stable regulator operation.

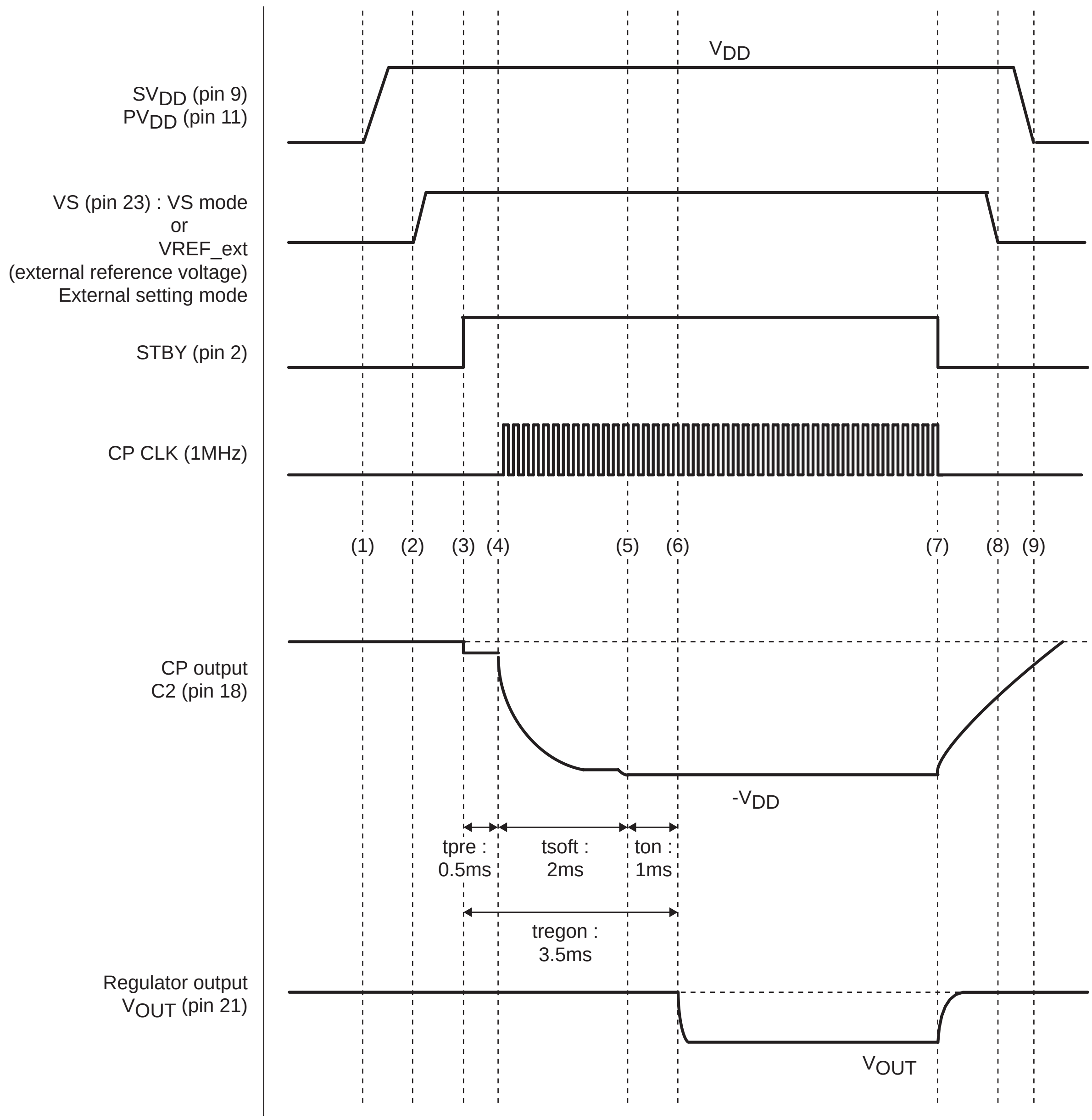
Application Circuit Example 2 (VS mode)



Application Circuit Example 3 (External setting mode)



Recommended Power On and Off Sequences



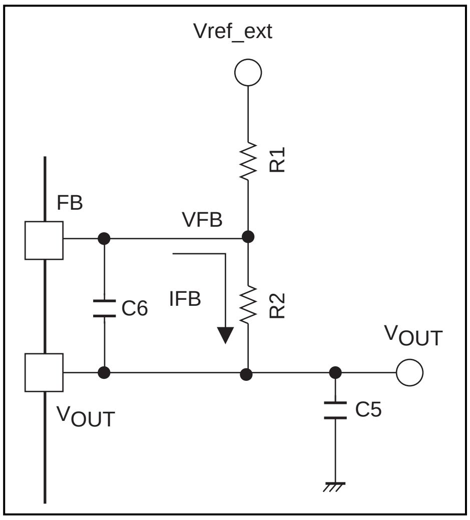
(1) Apply the V_{DD} voltage to the SV_{DD} and PV_{DD} pins.
(2) If VS mode is used, apply the VS voltage. If external setting mode is used, apply the external reference voltage.
(3) Start pre-charging the flying capacitor with a high-level input to the STBY pin.
(4) Start charging the pump-up capacitor with the charge pump sub-driver (soft start).
(5) Switch to the charge pump driver. This starts charging of the pump-up capacitor by the main driver.
(6) Regulator output starts.
(7) Stop IC drive by applying a low-level input to the STBY pin to start V_{OUT} output discharge operation by the internal discharge transistor. (This operates when the STBY pin is low.)
(8) If VS mode is used, shut down the VS voltage, and if external setting mode is used, shut down the external reference voltage.
(9) Shut down the V_{DD} voltage.

Overcurrent Protection Operation

This IC includes a function that protects against overcurrent in V_{OUT}. If the V_{OUT} output is shorted and a large current flows, the IC will latch and stop the output. To recover from this stopped state, set the STBY pin low and then set it high again.

External Setting Mode Applications and the Output Voltage Setting Method

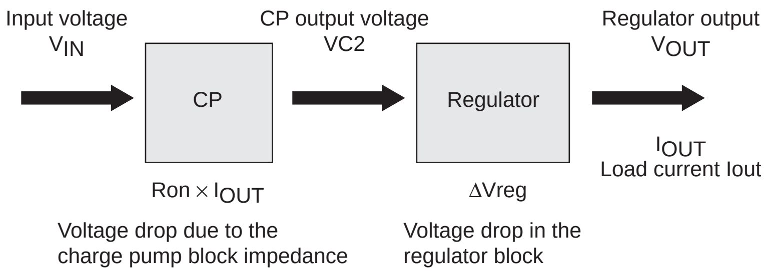
In the LV5254's external setting mode, the output voltage is set by the external resistors R1 and R2 and by the external reference voltage, Vref_ext. In this mode, the output voltage is expressed by equation (1). The second term in equation (1) is the error amplifier's offset component and the third term is the offset component due to the feedback current. The voltage precision achieved by an application can be determined by considering the tolerances of the parameters in equation (1).



$$V_{OUT} = -\frac{R2}{R1}\cdot Vref\_ext + \frac{R1+R2}{R1}\cdot VFB - R2\cdot IFB \cdots (1)$$

Relationship Between the Input and Output Voltages

Equation (2) gives the relationship between the input voltage and output voltage. In the LV5254, a charge pump circuit generates VC2, which is the V_{IN} level inverted, and generates the output voltage V_{OUT} by regulating that inverted voltage. In this case, due to the charge pump block impedance Ron, the voltage drop $I_O \times$ Ron (where I_O is the load current) is generated. (* Here we are ignoring the capacitor loss components in the charge pump capacitors C1 and C2.) The LV5254's current capacity is expressed by equation (3). At this time, the impedance Ron increases with temperature. Thus the current capacity decreases with increasing temperature.



$$V_{OUT} = VC2 + \Delta Vreg = (-V_{IN} + Ron \times I_{OUT}) + \Delta Vreg \cdots (2)$$

V_{OUT} : Output voltage, V_{IN} : Input voltage, I_{OUT} : Load current, Ron : Charge pump block impedance, ΔVreg : Regulator voltage drop

$$I_O\,[max] = (V_{IN} + V_{OUT} - \Delta Vreg\,[min]) / Ron \cdots (3)$$

I_O [max] : Maximum load current, ΔVreg [min] : Minimum regulator voltage drop

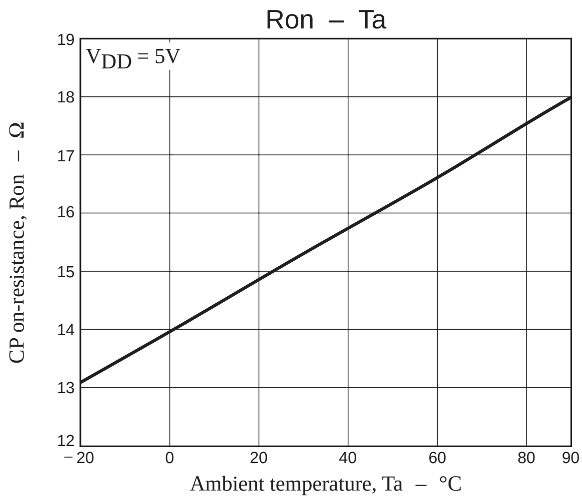


Figure 1 : Charge Pump Block Impedance Temperature Characteristics : Assumed Worst Case (C1, C2 = 1µF)

Next, consider figure 2, which shows the relationship between the input voltage V_{IN} and the charge pump block impedance Ron at Ta = 85°C, which is the maximum temperature for which operation is guaranteed. At Ta = 85°C, if ΔVreg [min] = 0.3V (inferred worst case value), the LV5254's maximum output current can be expressed as equation (4).

$$I_O\ [max] = (V_{IN}+V_{OUT}-0.3) / Ron \cdots (4)$$

The current capacity shown in figure 3 can be determined from the characteristics in figure 2 when V_{OUT} is set to be -3V.

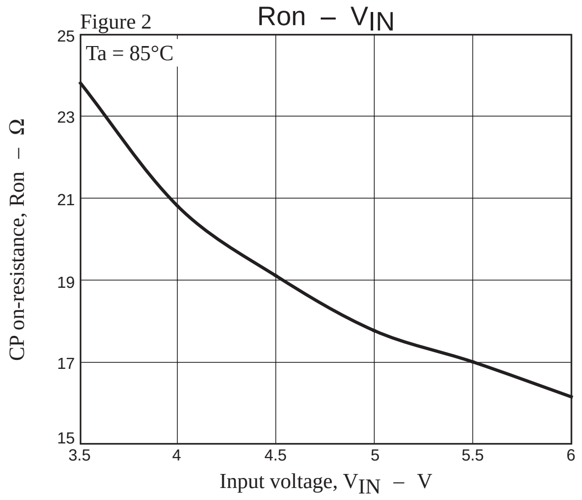


Figure 2 : Charge Pump Block Impedance - Input Voltage Characteristics (Ta = 85°C) : Assumed Worst Case (C1, C2 = 1μF)

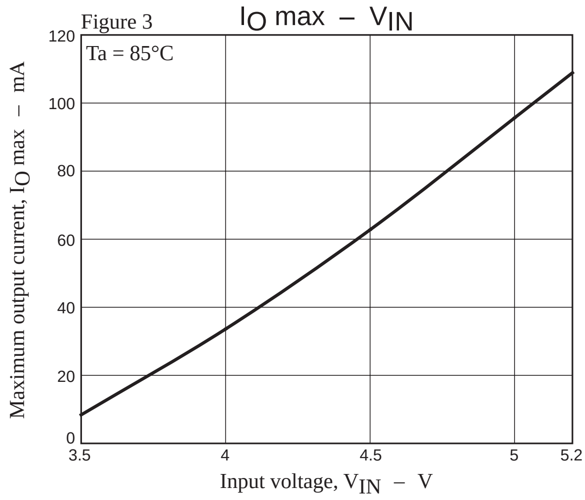


Figure 3 : Maximum Output Current - Input Voltage Characteristics when V_{OUT} = -3V (Ta = 85°C) : Assumed Worst Case (C1, C2 = 1μF)

Caution : The characteristics values presented in this reference documentation are nothing other than inferred worst-case values. No guarantee or warranty is made with respect to these values.

Loss in the Charge Pump Capacitors

Voltage loss occurs in the pump capacitors C1 and C2 in the charge pump circuit. Figure 4 shows the charge pump output vs. load current characteristics (with the C1 and C2 value as a parameter) at room temperature when V_{DD} = 5V. Note that the load regulation becomes worse as the value of the capacitors C1 and C2 is reduced. To minimize the loss in these capacitor, we recommend using a value of 1μF for C1 and C2.

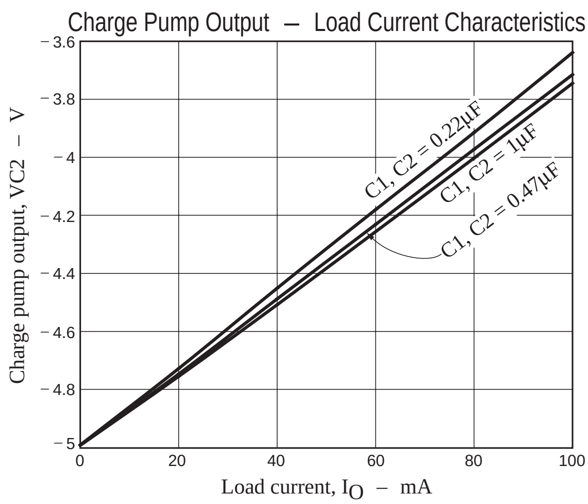
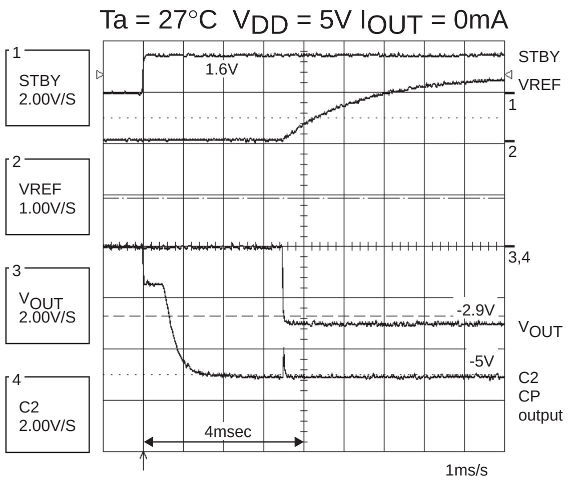


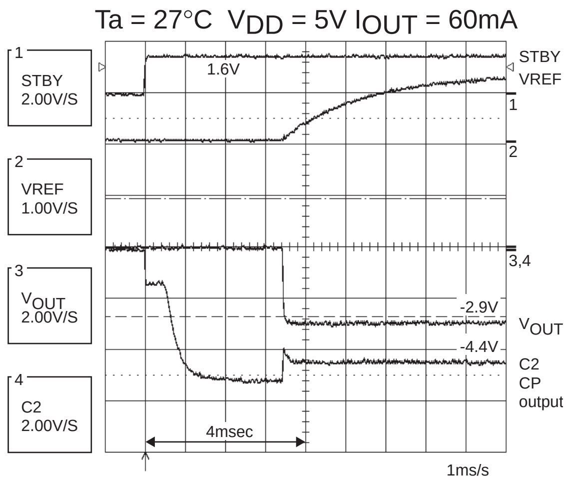
Figure 4 : Charge Pump Output - Load Current Characteristics when V_{DD} = 5V, data provided for reference purposes.

IC start and stop

1. Startup waveform (External setting mode)

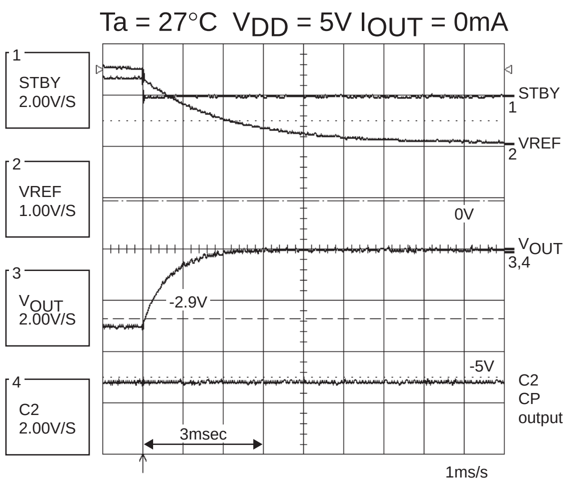


(a) No load - Startup waveform

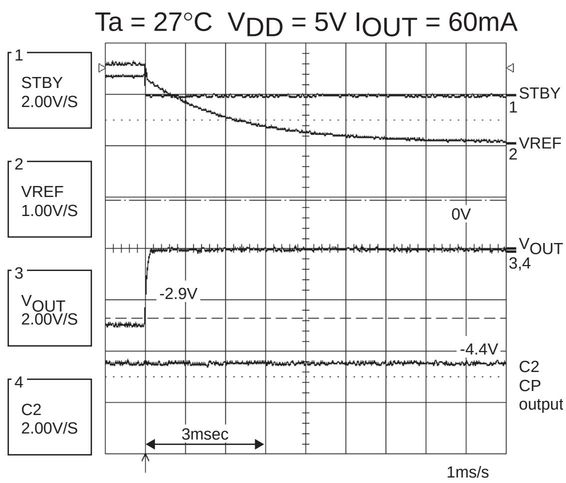


(b) 50Ω - Startup waveform

2. Falling waveform (External setting mode)

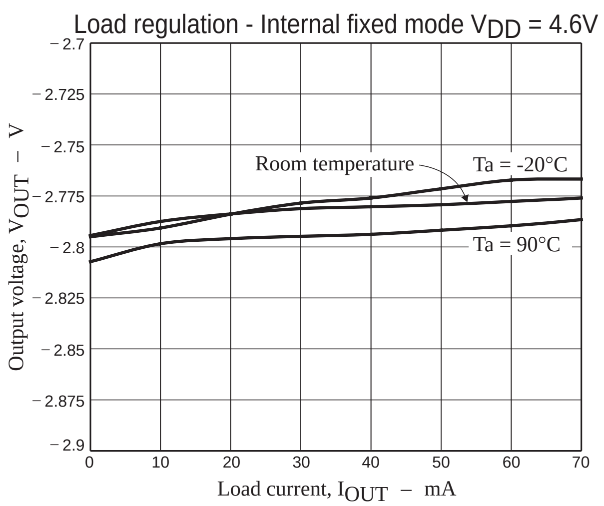


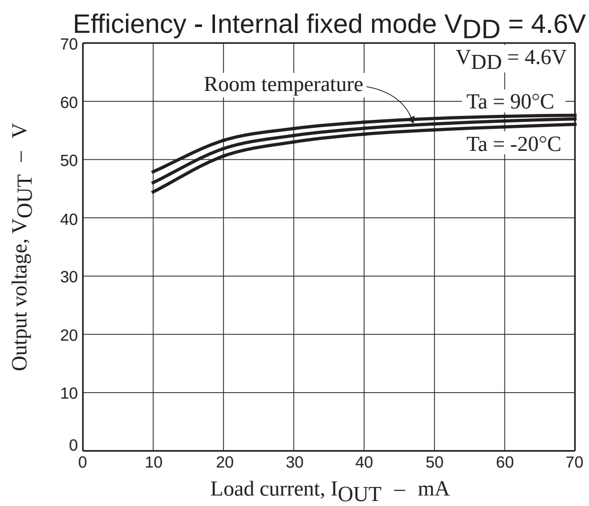
(a) No load - Falling waveform



(b) 50Ω - Falling waveform

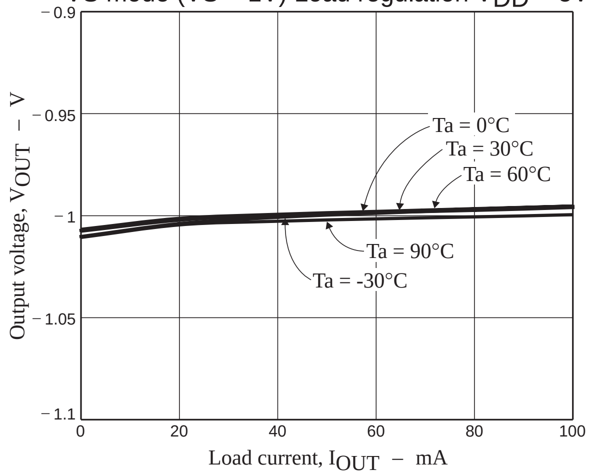
Internal fixed mode - Regulator



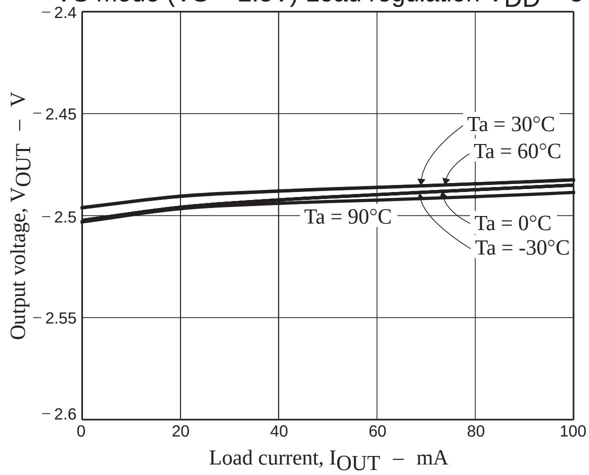


VS mode - Regulator

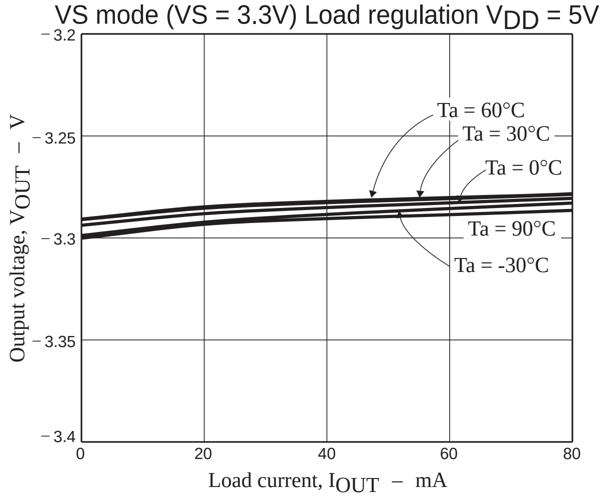
VS mode (VS = 1V) Load regulation V_{DD} = 5V



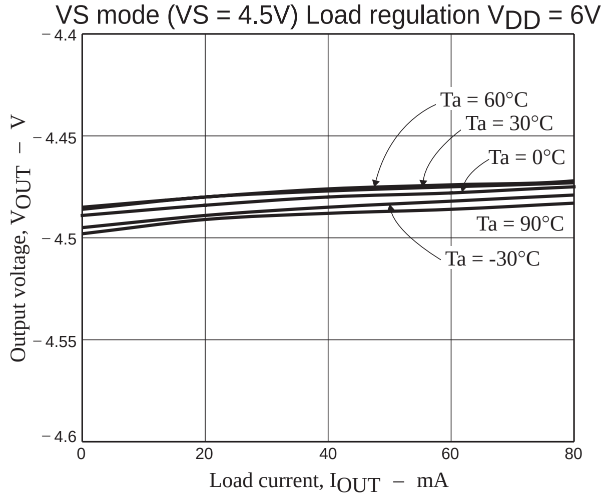
VS mode (VS = 2.5V) Load regulation V_{DD} = 5V



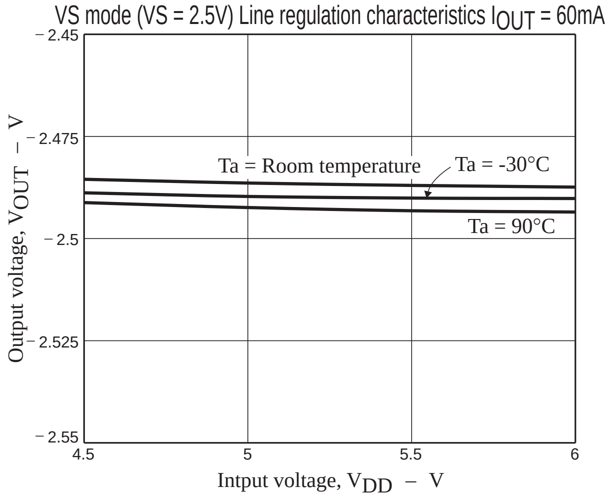
VS mode (VS = 3.3V) Load regulation V_{DD} = 5V



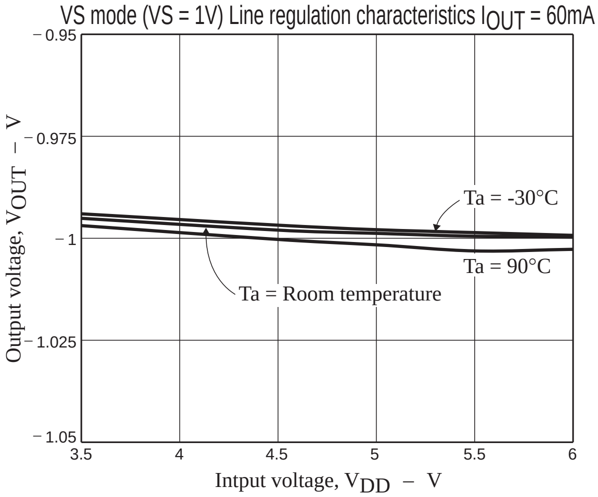
VS mode (VS = 4.5V) Load regulation V_{DD} = 6V



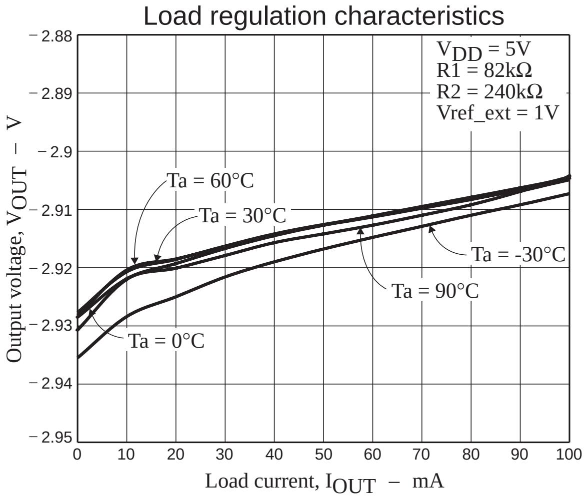
VS mode (VS = 2.5V) Line regulation characteristics I_{OUT} = 60mA

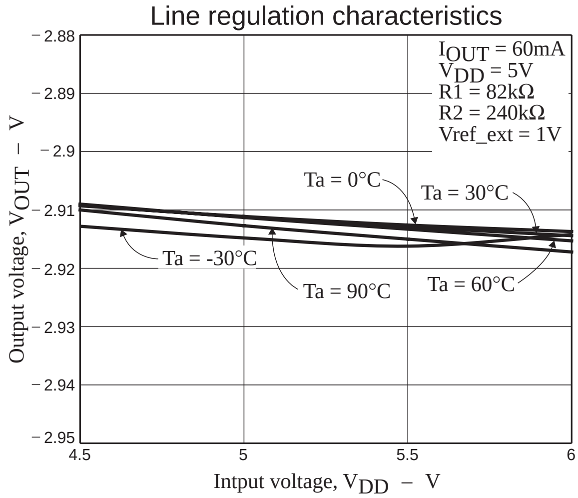


VS mode (VS = 1V) Line regulation characteristics I_{OUT} = 60mA

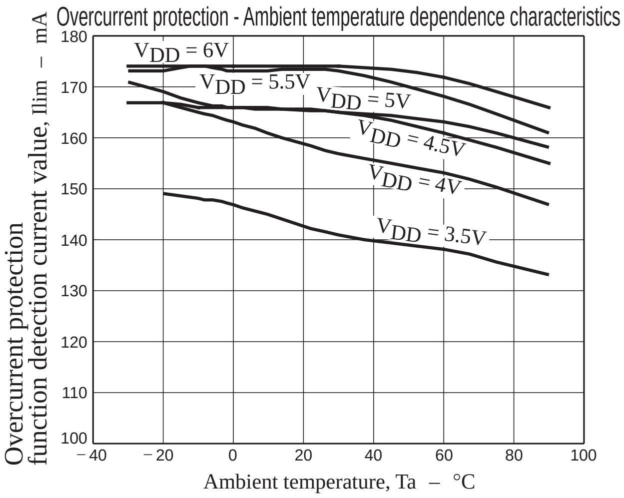


External Setting Mode Applications and the Output Voltage Setting Method





Overcurrent protection function detection current value



This catalog provides information as of March, 2007. Specifications and information herein are subject to change without notice.