Intel® IXF1110 10-Port Gigabit Ethernet Media Access Controller

Preliminary Datasheet

The Intel® IXF1110 is a 10-port Ethernet Media Access Controller (MAC) that supports IEEE 802.3 1000 Mbps applications. The device supports a System Packet Interface Level 4 Phase 2 (SPI4-2) system interface to the network processor or ASIC, and implements an internal Serializer/Deserializer (SerDes) to allow direct connection to optical modules. The integration of the SerDes functionality reduces PCB real-estate and system-cost requirements.

Applications

In general, the IXF1110 is appropriate for high-end switching applications where MAC and SerDes functions are not integrated into the system ASIC.

- High-End Optical Ethernet Switches
- Multi-Service Optical Ethernet Switches
- High-End Ethernet LAN/WAN Routers

Product Features

- Supports 10 independent 1000 Mbps full-duplex Ethernet MAC ports
- System Packet Interface Level 4 Phase 2 (SPI4-2)
  - —Capable of data transfers from 10.24 Gbps up to 12.8 Gbps
  - —Supports dynamic phase alignment
  - —Integrated termination
- SerDes interface with GBIC for Ethernet physical connectivity
  - —Integrated termination
  - —I^2C Read/Write capability
- 32-bit CPU interface
- RMON statistics
- JTAG boundary scan capable
- Compliance with IEEE 802.3x Standard for flow control
- Jumbo frame support for 9.6 KB packets
- .18 µ CMOS process technology
- Supports IEEE 802.3 fiber auto-negotiation, including forced mode
- SFF-8053, Revision 5.5 compatible
- Internal 17.0 KB receive FIFO and 4.5 KB transmit FIFO per channel
- Independent enable/disable of any port
- Detection of overly large packets
- Error counters for dropped and errored packets
- CRC calculation and error detection
- Programmable option to:
  - —Filter packets with errors
  - —Filter, broadcast, multicast, and unicast address packets
  - —Automatically pad transmitted packets less than the minimum frame size
- 552-Ceramic Ball Grid Array (CBGA)
- 1.8 V and 2.5 V operation
- Power consumption: 490 mW per-port typical

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Contents

Figures

Tables

Revision History

Revision: 004 Revision Date: December 6, 2002	
Page #	**Description**
1	Modified first paragraph Modified first line under Applications. Added text under Product Features on title page.
23	Modified Figure 5 “Power Sequencing Diagram”
25	Modified third bullet and last paragraph under Section 3.1.1, “General Description”.
25	Changed heading from “Features” to Section 3.1.2, “MAC Functions”.
26	Modified Section 3.1.2.3.1, “Filter on Unicast Packet Match”, Section 3.1.2.3.2, “Filter on Multicast Packet Match”, Section 3.1.2.3.3, “Filter Broadcast Packets”.
28	Modified text under Section 3.1.3, “Fiber Operation”.
28	Modified text under Section 3.1.4, “Auto-Negotiation”.
29	Added Section 3.1.5, “Forced Mode Operation”.
32	Changed heading from IXF1110 Advantages to Section 3.1.7.3, “Additional Statistics”.
n/a	Deleted old Table 9: Interface Timing
41	Modified Section 3.2.2.7, “DIP4_UnLock” and Section 3.2.2.8, “DIP4_Lock”.
42	Modified Section 3.2.2.10, “MaxBurst2” (MaxBurst1 to MaxBurst2).
53	Modified Section 3.4.5, “I^2C Module Configuration Interface” (read only to Read/Write capable).
53	Section 3.4.5.1.2, “Write Access Operation Example”: changed READ to WRITE for item numbers 4 and 5; modified note.
59	Modified Section 3.4.5.4.6, “Random Read Operation”
59	Added Section 3.4.5.4.7, “Byte Write Operation”.
68	Modified Section 3.7.5, “LED Clock”: changed 500 MHz to 720 MHz.
70	Modified Section 4.2, “Reset and Initialization”: changed 220 us to 4.11 ms in third paragraph.
84	Modified Table 29 “Hardware Reset Timing Parameters”: changed min value for Reset Recovery Time.
88	Modified Figure 37 “SPI4-2 Transmit FIFO Status Bus Timing Diagram” and Table 33 “SPI4-2 Transmit FIFO Status Bus Timing Parameters”: modified Parameters.
89	Modified Figure 38 “SPI4-2 Receive FIFO Status Bus Timing Diagram” and Table 34 “SPI4-2 Receive FIFO Status Bus Timing Parameters”: modified Parameters.
97	Added JTAG Register to Table 39 “Global Status and Configuration Register Map”.
110	Modified RxSymbolErrors description in Table 63 “MAC RX Statistics Registers (Addr: Port_Index + 0x20 - Port_Index + 0x39)”.
101	Modified Table 44 “GBIC Block Register Map”.
110	Added notes to RxRuntErrors and RxShortErrors Description in Table 63 “MAC RX Statistics Registers (Addr: Port_Index + 0x20 - Port_Index + 0x39)” (fiber only).
120	Modified Table 69 “LED Flash Rate Register (Addr: 0x50A)”.
122	Added Table 71 “JTAG ID Revision Register (Addr: 0x50C)”.
134	Changed Default value in Table 79 “TX FIFO MAC Transfer Threshold Ports 0 to 9 (Addr: 0x614 - 0x61D)”.
141	Modified bits 12 and 28 descriptions in Table 85 “SPI4-2 RX Calendar Register (Addr: 0x702)”

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142	Changed default value for bits 15:8 in Table 86 “SPI4-2 TX Synchronization Register (Addr: 0x703)”.
145	Modified into two tables: Table 92 “I^2C Control Register Ports 9-0 Register (Addr: 0x79B)” and Table 93 “I^2C Data Register Ports 9-0 Register (Addr: 0x79C)”
148	Added marking diagram under Section 7.2.1, “Markings”.

Revision: 003 Revision Date: October 7, 2002	
Page #	**Description**
1	Modified Product Features on front page: Added “Integrated termination” under SPI4-2 Interface
1	Added “Integrated termination” under SerDes Interface
23	Added new section: Section 2.2, “Power Sequencing” including Figure 5 “Power Sequencing Diagram” and Table 4 “Power Sequencing”.
26	Added Note under Section 3.1.2.3, “Filtering of Receive Packets” regarding jumbo frames.
28	Modified text under Section 3.1.4, “Auto-Negotiation”.
29	Modified text under Section 3.1.6, “Jumbo Packet Support”.
31	Modified Table 7 “RMON Additional Statistics Registers”.
36	Added new section: Section 3.2.1.1, “Control Words”, including Table 9 “Control Word Format” and Table 10 “Control Word Definitions”.
38	Added new section: Section 3.2.1.2, “DIP4”.
44	Modified Figure 12 “FIFO Status State Diagram”.
48	Modified second paragraph under Section 3.3.3.1, “Transmitter Operational Overview”.
66	Updated Table 23 “Read Timing Diagram - Asynchronous Interface” and Table 24 “Write Timing Diagram - Asynchronous Interface”.
67	Added bullet to Section 3.7.2, “SPI4-2 Receive and Transmit Data Path Clocks”: “TSCLK frequency is 1/4 TDCLK frequency.”
70	Removed second “Note” under Section 4.2, “Reset and Initialization”.
70	Added new section Section 4.3, “Optical Module Connections to the IXF1110” including: Table 18 “SFP-to-IXF1110 Connection” and Figure 26 “SFP-to-IXF1110 Connection Diagram”; Table 19 “SFF-to-IXF1110 Connection” and Figure 27 “SFF-to-IXF1110 Connection Diagram”; Table 20 “1 x 9-to-IXF1110 Connection” and Figure 28 “1 x 9-to-IXF1110 Connection”.
78	Added Note 2 to Table 23 “2.5 V LVTTL and CMOS I/O Electrical Characteristics”.
84	Modified Table 29 “Hardware Reset Timing Parameters”: Min value of Reset Recovery Time.
84	Modified Table 29 “Hardware Reset Timing Parameters”: Reset Pulse Wide Min = 100 ns. Reset Recovery Time Min = 220 µs.
86/87	Modified Table 31 “Transmitter Characteristics” and Table 32 “Receiver Characteristics”. Added introductory text.
97	Modified Table 39 “Global Status and Configuration Register Map”.
94	Added text to bits 9:0 description under Table 50 – “Specified in multiples of 512 bit times.

Revision: 003 Revision Date: October 7, 2002	
Page #	**Description**
94	Added text to bits 9:0 description under Table 51 – “Specified in multiples of 512 bit times.
103	Added text to bits 9:0 description under Table 51 “IPG Transmit Time Register (Addr: Port_Index + 0x0C)” – “Specified in multiples of 512 bit times.
103	Added text to bits 15:0 description under Table 52 “Pause Threshold Register (Addr: Port_Index + 0x0E)” – “Specified in multiples of 512 bit times.
105	Changed subclause number for Register Description under Table 57 “RX Config Word Register (Addr: Port_Index + 0x16)”. Bits 13:12: Added to bit description. Changed default values for bits 8:5.
106	Modified Table 59 “Diverse Config Register (Addr: Port_Index + 0x18)” – bits 15:9, 8, 4:0 are now reserved. Modified bit 5 name and description; added “1 = Normal operation.” Added note.
107	Added “table note 3” to Table 60 “RX Packet Filter Control Register (Addr: Port_Index + 0x19)”.
114	Table 64 “MAC TX Statistics Registers (Addr: Port_Index + 0x40 - Port_Index + 0x58)”: Changed “TXOctetsTransmittedOK” to “TXOctetsTotalOK”. TxPkts1519toMaxOctets: changed 1526 to 1523.
118	Modified Register Description under Table 65 “Port Enable Register (Addr: 0x500)”: Change “Setting the bit to 0 de-asserts the reset.” to “Setting the bit to 0 disables the port.”
120	Modified Table 68 “LED Control Register (Addr: 0x509)”: Bit 0: Changed “LED Control” to “LED_SEL_mode”.
140	Modified bit 31 description under Table 83 “SPI4-2 RX Burst Size Register (Addr: 0x700)”.
141	Modified Table 85 “SPI4-2 RX Calendar Register (Addr: 0x702)”: Modified descriptions for bits 19:16, 11:8, and 3:0.
142	Modified Table 86 “SPI4-2 TX Synchronization Register (Addr: 0x703)”: Added new description for bits 7:4.

Revision: 002 Revision Date: July 2002	
Page #	**Description**
20	Modified Figure 8 “IXF1110 552-Ball CBGA Assignments (Top View)”.
22	Modified Table 1 “IXF1010/IXF1110 Signal Pins”.
31	Modified Table 3 “IXF1110 Power Supply Signal Descriptions”.
28	Added Section 3.1.4, “Jumbo Packet Support”.
30	Replaced Section 3.1.5, “RMON Statistics Support”.
46	Added Figure 12 “IXF1010/IXF1110 SPI4-2 Interfacing with the Network Processor or Forwarding Engine”.
62	Modified sections under Section 3.7, “Clocks”.
66	Added Section 4.3, “Extras and Back up”.
89	Modified all register maps under Section 6.5, “Memory Map”.

Related Documents

Title	Order
IXF1010 and IXF1110 10-Port Gigabit Ethernet Media Access Controllers Design and Layout Guide	250676
IXF1110 Demo Board Development Kit Manual	250807
SPI4 Phase 2 Performance in Gigabit Ethernet Media Access Controllers Application Note	250643
Interfacing with IXF1010 and IXF1110 10-Port Gigabit Ethernet Media Access Controllers Application Note	250856
IXF1110 Thermal Design Considerations Application Note	250289
Flow Control in IXF1010 and IXF1110 10-Port Gigabit Ethernet Media Access Controllers Application Note	250236

1.0 General Description

The Intel® IXF1110 is a 10-port 1000 Mbps Ethernet Media Access Controller (MAC). The 10 Gigabit interface to the network processor is supported through a System Packet Interface Level 4 Phase 2 (SPI4-2), while the media interface is an integrated Serializer/Deserializer (SerDes). Figure 1 illustrates the IXF1110 block diagram and Figure 2 represents the IXF1110 system block diagram.

Figure 1. IXF1110 Block Diagram

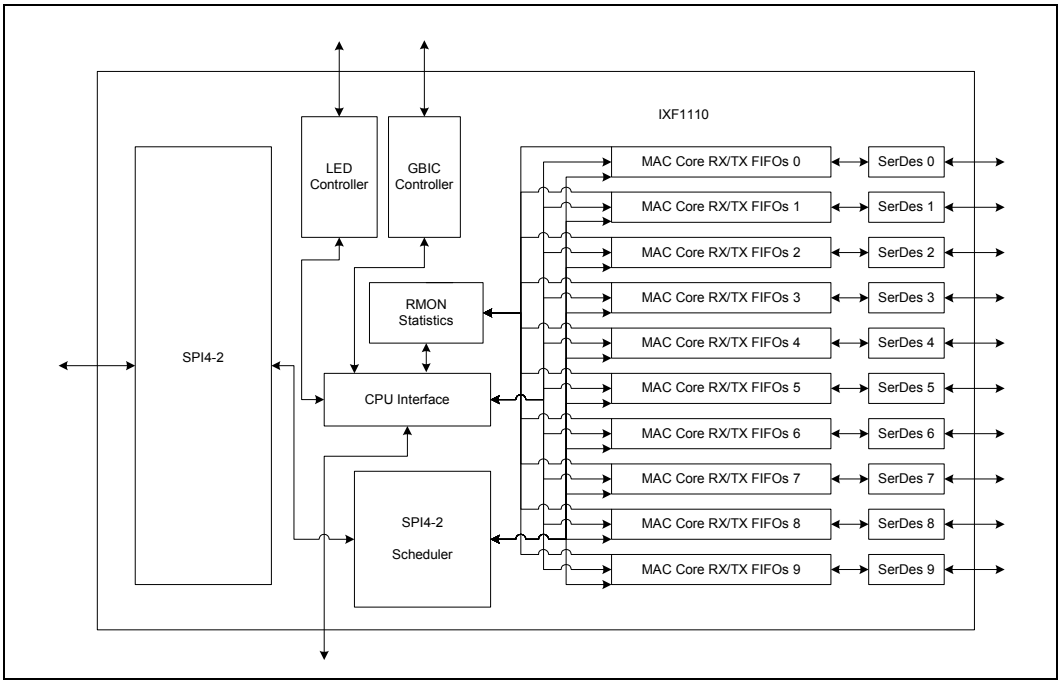


Figure 2. Intel® IXF1110 System Block Diagram

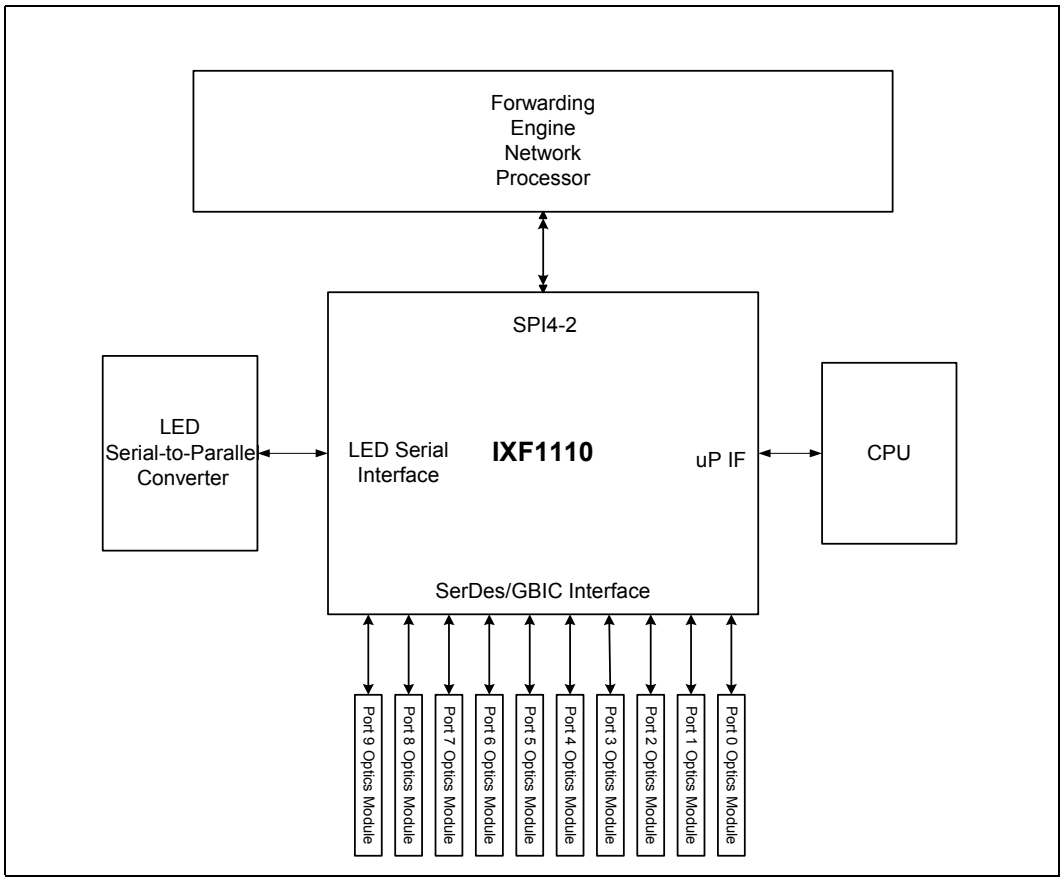
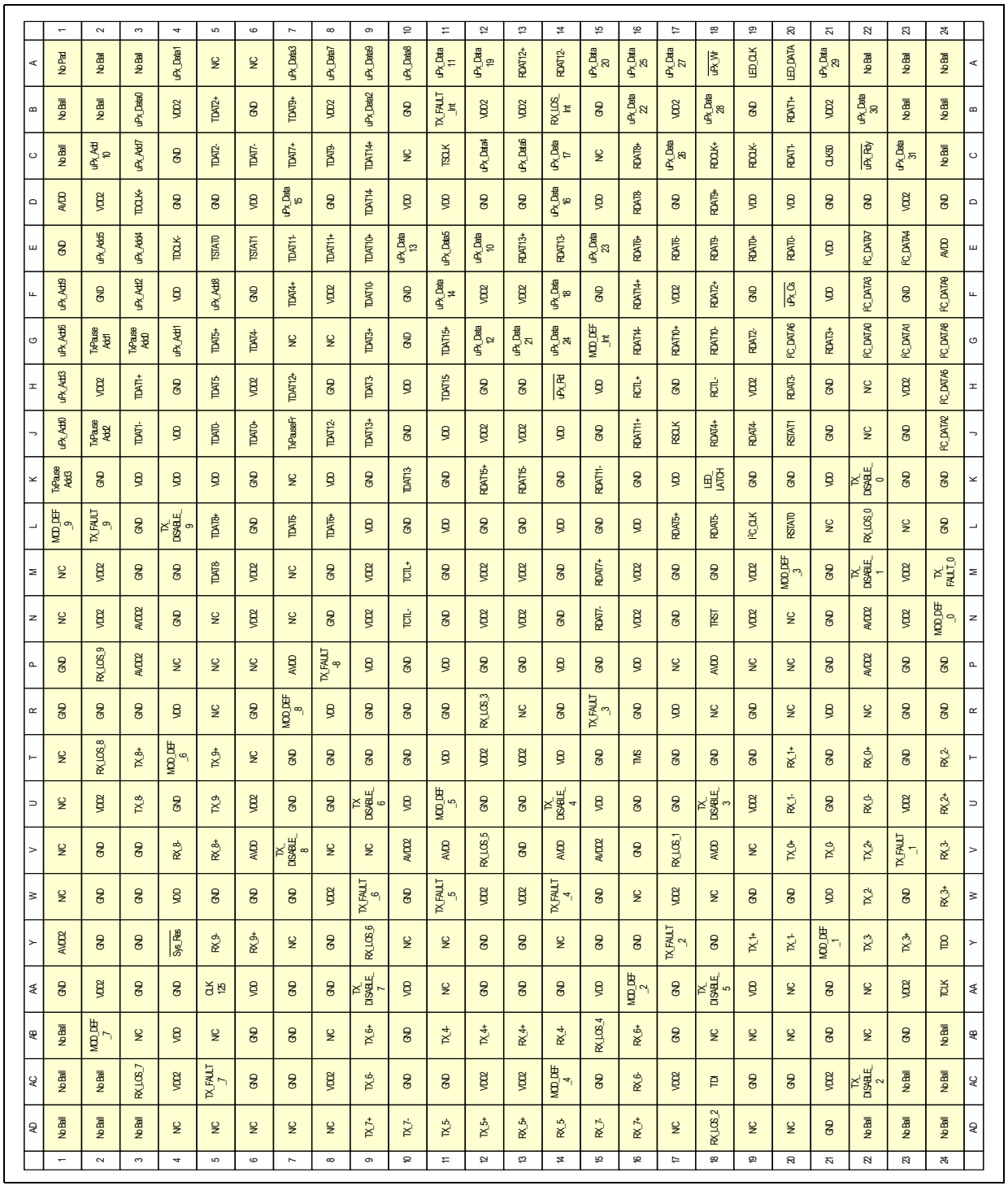


Figure 3 provides the physical layout of the balls, labeled with their ball number (matrix layout) and signal name.

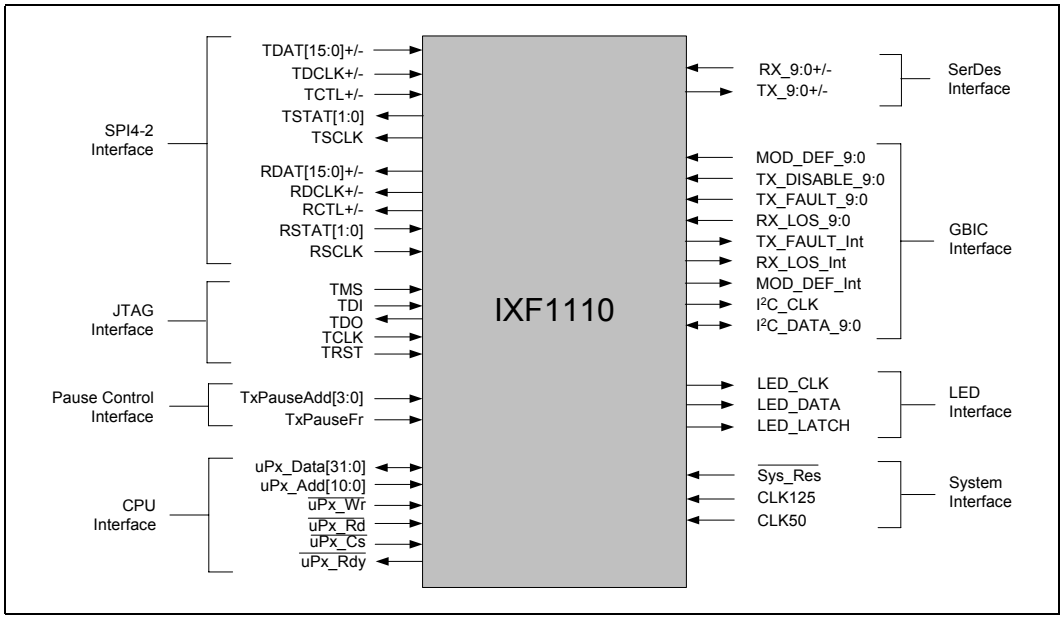
Figure 3. IXF1110 552-Ball CBGA Assignments (Top View)



2.0 Pin Assignments and Signal Descriptions

Figure 4 and Table 1 through Table 3 on page 23 provide the signal pins used by the IXF1110

Figure 4. IXF1110 Pinout Diagram



2.1 Signal Name Conventions

Signal names may contain either a port designation (media interface) or a serial designation (System Interface). Signal naming conventions are as follows:

Port Designation. Individual signals that apply to a particular port are designated by the Signal Mnemonic, immediately followed by an underscore and the Port Designation. For example, GBIC Serial Data signals would be identified as I^2C_DATA_0, I^2C_DATA_1, etc.

Serial Designation. A set of signals that are not tied to any specific port are designated by the Signal Mnemonic, followed by a bracketed serial designation. For example, SPI4-2 Transmit Data Bus signals would be identified as TDAT[15:0].

Table 1. IXF1110 Signal Pins

Ball Designator	Signal Name	Type	Standard	Signal Description
SPI4-2 Interface				
G11, H11 C9, D9 J9, K10 H7, J8 E8, E7 E9, F9 B7, C8 L5, M5 C7, C6 L8, L7 G5, H5 F7, G6 G9, H9 B5, C5 H3, J3 J6, J5	TDAT15+/- TDAT14+/- TDAT13+/- TDAT12+/- TDAT11+/- TDAT10+/- TDAT9+/- TDAT8+/- TDAT7+/- TDAT6+/- TDAT5+/- TDAT4+/- TDAT3+/- TDAT2+/- TDAT1+/- TDAT0+/-	Input	LVDS	**Transmit Data Bus:** Carries payload data and in-band control words to the IXF1110 link-layer device. Internally terminated differentially with 100 Ω.
D3, E4	TDCLK+, TDCLK-	Input	LVDS	**Transmit Data Clock:** Clock associated with TDAT[15:0] and TCTL. Data and control lines are driven off the rising and falling edges of the clock. Internally terminated differentially with 100 Ω.
M10, N10	TCTL+, TCTL-	Input	LVDS	**Transmit Control:** TCTL is High when a control word is present on TDAT[15:0]. Otherwise, TCTL is Low. Internally terminated differentially with 100 Ω.
C11	TSCLK	Output	2.5 V LVTTL	**Transmit Status Clock:** Clock associated with TSTAT [1:0]. Frequency is equal to one-quarter TDCLK.
E6, E5	TSTAT1, TSTAT0	Output	2.5 V LVTTL	**Transmit FIFO Status:** Carries round-robin FIFO status information, along with associated error detection and framing.
K12, K13 F16, G16 E13, E14 A13, A14 J16, K15 G17, G18 D18, E18 C16, D16 M15, N15 E16, E17 L17, L18 J18, J19 G21, H20 F18, G19 B20, C20 E19, E20	RDAT15+/- RDAT14+/- RDAT13+/- RDAT12+/- RDAT11+/- RDAT10+/- RDAT9+/- RDAT8+/- RDAT7+/- RDAT6+/- RDAT5+/- RDAT4+/- RDAT3+/- RDAT2+/- RDAT1+/- RDAT0+/-	Output	LVDS	**Receive Data:** Carries payload data and in-band control from the IXF1110 link-layer device.

Table 1. IXF1110 Signal Pins (Continued)

Ball Designator	Signal Name	Type	Standard	Signal Description
C18, C19	RDCLK+, RDCLK-	Output	LVDS	**Receive Data Clock:** Clock associated with RDAT[15:0] and RCTL. Data and control lines are driven off the rising and falling edges of the clock.
H16, H18	RCTL+, RCTL-	Output	LVDS	**Receive Control:** RCTL is High when a control word is present on RDAT[15:0]. Otherwise, RCTL is Low.
J17	RSCLK	Input	2.5 V LVTTL	**Receive Status Clock:** Clock associated with RSTAT[1:0].
J20, L20	RSTAT1, RSTAT0	Input	2.5 V LVTTL	**Receive FIFO Status:** Carries round-robin FIFO status information, along with associated error detection and framing.
SerDes Interface				
T5, U5 T3, U3 AD9, AD10 AB9, AC9 AD12, AD11 AB12, AB11 Y23, Y22 V22, W22 Y19, Y20 V20, V21	TX_9+/- TX_8+/- TX_7+/- TX_6+/- TX_5+/- TX_4+/- TX_3+/- TX_2+/- TX_1+/- TX_0+/-	Output	LV PECL	**Transmit Differential Output:** Carries the 1.25 GHz data to the optics module. These lines can be AC- or DC-coupled. By default, these lines are AC-coupled internally. This can be changed (see Table 87, “TX and RX AC/DC Coupling Selection Register (Addr: 0x780)” on page 142).
Y6, Y5 V5, V4 AD16, AD15 AB16, AC16 AD13, AD14 AB13, AB14 W24, V24 U24, T24 T20, U20 T22, U22	RX_9+/- RX_8+/- RX_7+/- RX_6+/- RX_5+/- RX_4+/- RX_3+/- RX_2+/- RX_1+/- RX_0+/-	Input	LV PECL	**Receive Differential Input:** Carries the 1.25 GHz data from the optics module. Internally terminated differentially with 100 Ω. These lines can be AC- or DC-coupled. By default, these lines are AC-coupled internally. This can be changed (see Table 87, “TX and RX AC/DC Coupling Selection Register (Addr: 0x780)” on page 142).
CPU Interface				
C2 F1 F5 C3 G1 E2 E3 H1 F3 G4 J1	uPx_Add10 uPx_Add9 uPx_Add8 uPx_Add7 uPx_Add6 uPx_Add5 uPx_Add4 uPx_Add3 uPx_Add2 uPx_Add1 uPx_Add0	Input	2.5 V CMOS	**Address bus:** 11-bit address bus
F20	$\overline{\text{uPx\_Cs}}$	Input	2.5 V CMOS	**Chip Select Signal:** Active Low chip select

Table 1. IXF1110 Signal Pins (Continued)

Ball Designator	Signal Name	Type	Standard	Signal Description
C23 B22 A21 B18 A17 C17 A16 G14 E15 B16 G13 A15 A12 F14 C14 D14 D7 F11 E10 G12 A11 E12 A9 A10 A8 C13 E11 C12 A7 B9 A4 B3	uPx_Data31 uPx_Data30 uPx_Data29 uPx_Data28 uPx_Data27 uPx_Data26 uPx_Data25 uPx_Data24 uPx_Data23 uPx_Data22 uPx_Data21 uPx_Data20 uPx_Data19 uPx_Data18 uPx_Data17 uPx_Data16 uPx_Data15 uPx_Data14 uPx_Data13 uPx_Data12 uPx_Data11 uPx_Data10 uPx_Data9 uPx_Data8 uPx_Data7 uPx_Data6 uPx_Data5 uPx_Data4 uPx_Data3 uPx_Data2 uPx_Data1 uPx_Data0	Input/ Output	2.5 V CMOS	**Bi-directional data bus:** 32-bit bi-directional data bus
A18	$\overline{\text{uPx\_Wr}}$	Input	2.5 V CMOS	**Write Strobe:** Active Low Write strobe
H14	$\overline{\text{uPx\_Rd}}$	Input	2.5 V CMOS	**Read Strobe:** Active Low Read strobe
C22	$\overline{\text{uPx\_Rdy}}$	Open Drain Output	2.5 V CMOS	**Cycle complete indicator:** Indicates that Read or Write is complete
Pause Control Interface				
J7	TxPauseFr	Input	2.5 V CMOS	**Pause Strobe:** Indicates when a Pause frame is to be sent
K1 J2 G2 G3	TxPauseAdd3 TxPauseAdd2 TxPauseAdd1 TxPauseAdd0	Input	2.5 V CMOS	**Pause Address Bus:** Selects the port for the Pause frames
GBIC Interface				
L2 P8 AC5 W9 W11 W14 R15 Y17 V23 M24	TX_FAULT_9 TX_FAULT_8 TX_FAULT_7 TX_FAULT_6 TX_FAULT_5 TX_FAULT_4 TX_FAULT_3 TX_FAULT_2 TX_FAULT_1 TX_FAULT_0	Input	2.5 V CMOS	**Transmitter Fault:** Input used to determine when there is a GBIC transmitter fault.

Table 1. IXF1110 Signal Pins (Continued)

Ball Designator	Signal Name	Type	Standard	Signal Description
P2 T2 AC3 Y9 V12 AB15 R12 AD18 V17 L22	RX_LOS_9 RX_LOS_8 RX_LOS_7 RX_LOS_6 RX_LOS_5 RX_LOS_4 RX_LOS_3 RX_LOS_2 RX_LOS_1 RX_LOS_0	Input	2.5 V CMOS	**Receiver Loss of Signal:** Input used to determine when the GBIC receiver loses synchronization.
L1 R7 AB2 T4 U11 AC14 M20 AA16 Y21 N24	MOD_DEF_9 MOD_DEF_8 MOD_DEF_7 MOD_DEF_6 MOD_DEF_5 MOD_DEF_4 MOD_DEF_3 MOD_DEF_2 MOD_DEF_1 MOD_DEF_0	Input	2.5 V CMOS	**Module Definition:** Input used to determine when a GBIC module is present.
L4 V7 AA9 U9 AA18 U14 U18 AC22 M22 K22	TX_DISABLE_9 TX_DISABLE_8 TX_DISABLE_7 TX_DISABLE_6 TX_DISABLE_5 TX_DISABLE_4 TX_DISABLE_3 TX_DISABLE_2 TX_DISABLE_1 TX_DISABLE_0	Open Drain Output	2.5 V CMOS	**Transmitter Disable:** Output used to disable a GBIC module transmitter. External pull-up resistor usually resident in a GBIC module is required for proper operation.
B11	TX_FAULT_Int	Open Drain Output	2.5 V CMOS	**Transmitter Fault interrupt:** Open drain output interrupt to signal a TX_FAULT condition.
B14	RX_LOS_Int	Open Drain Output	2.5 V CMOS	**Receiver Loss of Signal Interrupt:** Open drain output interrupt to signal an RX_LOS condition.
G15	MOD_DEF_Int	Open Drain Output	2.5 V CMOS	**Module Definition Interrupt:** Open drain output interrupt to signal a MOD_DEF condition.
L19	I^2C_CLK	Output	2.5 V CMOS	**I^2C Reference Clock:** Clock used for I^2C bus interface.
F24 G24 E22 G20 H24 E23 F22 J24 G23 G22	I^2C_DATA_9 I^2C_DATA_8 I^2C_DATA_7 I^2C_DATA_6 I^2C_DATA_5 I^2C_DATA_4 I^2C_DATA_3 I^2C_DATA_2 I^2C_DATA_1 I^2C_DATA_0	Input/ Output	2.5 V CMOS	**I^2C Data Bus:** Data I/O for the I^2C bus interface.
LED Interface				
A19	LED_CLK	Output	2.5 V CMOS	**LED Clock:** Clock output for the LED block.

Table 1. IXF1110 Signal Pins (Continued)

Ball Designator	Signal Name	Type	Standard	Signal Description
A20	LED_DATA	Output	2.5 V CMOS	**LED Data:** Data output for the LED block.
K18	LED_LATCH	Output	2.5 V CMOS	**LED Latch:** Latch enable for the LED block.
JTAG Interface				
AA24	TCLK	Input	2.5 V CMOS	**JTAG Test Clock:** Reference clock for JTAG.
T16	TMS	Input	2.5 V CMOS	**JTAG Test Mode Select:** Selects test mode for JTAG.
AC18	TDI	Input	2.5 V CMOS	**JTAG Test Data Input:** Test data sampled with respect to the rising edge of TCK.
N18	TRST	Input	2.5 V CMOS	**JTAG Test Reset:** Reset input for JTAG test.
Y24	TDO	Output	2.5 V CMOS	**JTAG Test Data Output:** Test data driven with respect to the falling edge of TCK.
System Interface				
AA5	CLK125	Input	2.5 V CMOS	**125 MHz Reference Clock:** Input clock to PLL.
C21	CLK50	Input	2.5 V CMOS	**SPI4-2 Reference Clock:** Input clock to SPI4-2 RX PLL. Input range is 40 MHz to 50 MHz. This clock multiplied by eight must equal the required SPI4-2 data clock frequency.
Y4	$\overline{\text{Sys\_Res}}$	Input	2.5 V CMOS	**System Reset:** System hard reset (active Low).

Table 2. IXF1110 Power Supply Signal Descriptions

Ball #	Signal Name	Type	Standard	Signal Description
D1, E24, P7, P18, V6, V11, V14, V18	AVDD	–	–	**1.8 V Analog Power Supply:** 1.8 V supply for analog circuits.
N3, N22, P3, P22, V10, V15, Y1	AVDD2		–	**2.5 V Analog Power Supply:** 2.5 V supply for analog circuits.
D6, D10, D11, D15, D19, D20, E21, F4, F21, H10, H15, J4, J11, J14, K3, K4, K5, K8, K17, K21, L9, L11, L14, L16, P9, P11, P14, P16, R4, R8, R17, R21, T11, T14, U10, U15, W4, W21, AA6, AA10, AA15, AA19, AB4	VDD	–	–	**1.8 V Digital Power Supply:** 1.8 V core supply.
B4, B8, B12, B13, B17, B21, D2, D23, F8, F12, F13, F17, H2, H6, H19, H23, J12, J13, M2, M6, M9, M12, M13, M16, M19, M23, N2, N6, N9, N12, N13, N16, N19, N23, T12, T13, U2, U6, U19, U23, W8, W12, W13, W17, AA2, AA23, AC4, AC8, AC12, AC13, AC17, AC21	VDD2	–	–	**2.5 V Digital Power Supply:** 2.5 V I/O supply.
B6, B10, B15, B19, C4, D4, D5, D8, D12, D13, D17, D21, D22, D24, E1, F2, F6, F10, F15, F19, F23, G10, H4, H8, H12, H13, H17, H21, J10, J15, J21, J23, K2, K6, K9, K11, K14, K16, K19, K20, K23, K24, L3, L6, L10, L12, L13, L15, L24, M3, M4, M8, M11, M14, M17, M18, M21, N4, N8, N11, N14, N17, N21, P1, P10, P12, P13, P15, P21, P23, P24, R1, R2, R3, R6, R9, R10, R11, R14, R16, R19, R23, R24, T7, T8, T9, T10, T15, T17, T18, T19, T21, T23, U4, U7, U8, U12, U13, U16, U17, U21, V2, V3, V13, V16, W2, W3, W5, W6, W7, W10, W15, W19, W20, W23, Y2, Y3, Y8, Y12, Y13, Y15, Y16, Y18, AA1, AA3, AA4, AA7, AA8, AA12, AA13, AA14, AA17, AA21, AB6, AB7, AB10, AB17, AB21, AB23, AC6, AC7, AC10, AC11, AC15, AC19, AC20, AD21	GND	–	–	**Ground:** Ground return for all signals.

Table 3. IXF1110 Unused Balls/Reserved

Ball #	Signal Name	Type	Standard	Signal Description
A5, A6, C10, C15, G7, G8, H22, J22, K7, L21, L23, M1, M7, N1, N5, N7, N20, P4, P5, P6, P17, P19, P20, R5, R13, R18, R20, R22, T1, T6, U1, V1, V8, V9, V19, W1, W16, W18, Y7, Y10, Y11, Y14, AA11, AA20, AA22, AB3, AB5, AB8, AB18, AB19, AB20, AB22, AD4, AD5, AD6, AD7, AD8, AD17, AD19, AD20	N/C	–	–	No connection.
A2, A3, A22, A23, A24, B1, B2, B23, B24, C1, C24, AB1, AB24, AC1, AC2, AC23, AC24, AD1, AD2, AD3, AD22, AD23, AD24	No Ball	–	–	Balls removed from substrate.
A1	No Pad	–	–	Pad removed from substrate.

2.2 Power Sequencing

Correct operation requires a power-up and power-down sequence. Failure to follow this sequence can result in damage to the device. The sequence described in this section covers digital and analog supplies for the device.

Ensure that the 1.8 V supplies (VDD/AVDD) are applied and stable prior to the application of the 2.5 V supplies (VDD2/AVDD2).

Note: If the 2.5 V supplies (VDD2/AVDD2) exceed the 1.8 V core supplies (VDD/AVDD) by more than 2.0 V during power-up or power-down, damage can occur to the ESD structures within the Analog IOs.

Since the power-down sequence is the reverse of the power-up sequence, remove the 2.5 V supplies (VDD2/AVDD2) prior to the removal of the 1.8 V core supplies (VDD/VDD2).

Figure 5. Power Sequencing Diagram

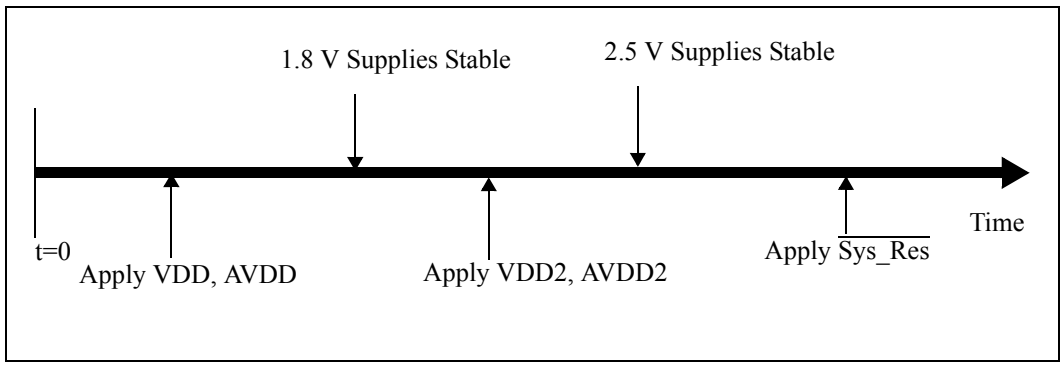


Table 4. Power Sequencing

Power Supply	Power-Up Order	Time Delta to Next Supply[1]	Description
VDD, AVDD	First	0	1.8 V supplies
VDD2, AVDD2	Second	10 µs	2.5 V supplies

1. The value of 10 µs given is a nominal value only. The exact time difference between the application of the 2.5 V analog supply will be determined by a number of factors dependent on the power management method used. The key requirement that must be met to avoid damage to the device is that the AVDD2 supply must not exceed the VDD supply by more than 2 V at any time during the power-up or power-down sequence.

3.0 Functional Descriptions

3.1 Media Access Controller

3.1.1 General Description

The Intel® IXF1110 main functional block consists of a 1000 Mbps Ethernet Media Access Controller (MAC), supporting the following features:

- 1000 Mbps full-duplex operation
- Independent enable/disable of any port
- Detection of length error or overly large packets
- RMON statistics and error counters
- Cyclic Redundancy Check (CRC) calculation and error detection
- Programmable option to:
  - Filter packets with errors
  - Filter, broadcast, multicast, and unicast address packets
  - Automatically pad transmitted packets less than the minimum frame size
- Compliance with IEEE 802.3x Standard for Flow Control (symmetric pause capability)

The MAC is fully integrated, designed for use with Ethernet 802.3 Frame types, and is compliant with all of the required IEEE 802.3 MAC requirements.

The MAC adds preamble and Start-of-Frame Delimiter (SFD) to all frames sent to it (transmit path) and removes preamble and SFD on all frames received by it (receive path). A CRC check is also applied to all transmit and receive packets. Packets with a bad CRC are marked, counted in the statistics block, and may be optionally dropped or sent to the SPI4-2 interface.

3.1.2 MAC Functions

Section 3.1.2.1, “Padding of Undersized Frames on Transmit” on page 25 through Section 3.1.2.4, “PAUSE Command Frames” on page 28 cover the MAC functions.

3.1.2.1 Padding of Undersized Frames on Transmit

The padding feature allows Ethernet frames smaller than 64 bytes to be transferred across the SPI4-2 interface and automatically padded up to 64 bytes by the MAC. This feature is enabled by setting bit 7 of the Diverse Config Register = 1 (Address Port_Index + 0x18h). See Table 59 on page 106.

3.1.2.2 Automatic CRC Generation

The Automatic CRC Generation is used in conjunction with the padding feature to generate and append a correct CRC to any incoming frame from the SPI4-2 interface. This feature is enabled by setting bit 6 of the Diverse Config Register = 1 (Address Port_Index + 0x18h) (see Table 59 on page 106).

Note: When padding of undersized frames on transmit is enabled, the automatic CRC generation must be enabled for proper operation of the IXF1110.

3.1.2.3 Filtering of Receive Packets

This feature allows the MAC to filter receive packets under various conditions and drop the packets via an interaction with the Receive FIFO control.

Note: Jumbo frames (1519 - 9600 bytes) matching the filter conditions, which would cause the frame to be dropped by the RX FIFO, are not dropped. Instead, jumbo frames that are expected to be dropped by the RX FIFO, based on the filter settings in Table 60, "RX Packet Filter Control Register (Addr: Port_Index + 0x19)" on page 107, are sent across the SPI4-2 interface as an EOP abort frame. Jumbo frames matching the filter conditions are not counted in the RX FIFO Number of Frames Removed Register because they are not removed by the RX FIFO. Only standard packet sizes (64 - 1518 bytes) meeting the filter conditions set in the "RX Packet Filter Control Register (Addr: Port_Index + 0x19)" are actually dropped by the RX FIFO and counted in the RX FIFO Number of Frames Removed.

3.1.2.3.1 Filter on Unicast Packet Match

This feature is enabled when bit 0 of the RX Packet Filter Control Register = 1. Any frame received in this mode containing a Unicast Destination Address which does not match the Station Address is marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all unicast frames are sent to the SPI4-2 interface.

3.1.2.3.2 Filter on Multicast Packet Match

This feature is enabled when bit 1 of the RX Packet Filter Control Register = 1. Any frame received in this mode containing a Multicast Destination Address which does not match the Port Multicast Address is marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable register = 1. Otherwise, all multicast frames are sent to the SPI4-2 interface.

3.1.2.3.3 Filter Broadcast Packets

This feature is enabled when bit 2 of the RX Packet Filter Control Register = 1. Any broadcast frame received in this mode is marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all broadcast frames are sent to the SPI4-2 interface.

3.1.2.3.4 Filter VLAN Packets

This feature is enabled when bit 3 of the RX Packet Filter Control Register = 1. VLAN frames received in this mode are marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all VLAN frames are sent to the SPI4-2 interface.

3.1.2.3.5 Filter PAUSE Packets

This feature is enabled when bit 4 of the RX Packet Filter Control Register = 0. PAUSE frames received in this mode are marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all PAUSE frames are sent to the SPI4-2 interface.

Table 5. Pause Packets Drop Enable Behavior

Pause Frame Pass	Frame Drop En	Actions
1	0	Packets are passed to the SPI4-2 interface. They are not marked as bad and are sent to the switch or Network Processor.
0	0	Packets are marked as bad but not dropped in the RX FIFO. These packets are sent to the SPI4-2 interface, but with an EOP Abort code to the switch or Network Processor.
1	1	Packets are not marked as bad and sent to the switch or Network Processor, regardless of the Frame Drop En setting.
0	1	PAUSE Packets are marked as bad, are dropped in the RX FIFO, and never appear at the SPI4-2 interface.

3.1.2.3.6 Filter CRC Errored Packets

This feature is enabled when bit 5 of the RX Packet Filter Control Register = 0. Frames received with an errored CRC are marked as bad frames and may optionally be dropped in the RX FIFO. Otherwise, the frames are sent to the SPI4-2 interface and may be dropped by the switch or system controller (see Table 6).

Table 6. CRC Errored Packets Drop Enable Behavior

CRC Errored PASS	Frame Drop En	Actions
1	0	Packets are passed to the SPI4-2 interface. They are not marked as bad and are sent to the switch or Network Processor.
0	0	Packets are marked as bad but not dropped in the RX FIFO. These packets are sent to the SPI4-2 interface, but with an EOP Abort code to the switch or Network Processor.
1	1	Packets are not marked as bad and are sent to the switch or Network Processor regardless of the Frame Drop En setting.
0	1	CRC errored packets are marked as bad, dropped in the RX FIFO, and never appear at the SPI4-2 interface.

3.1.2.4 PAUSE Command Frames

The MAC acts on any PAUSE command frames received from the link partner by checking the entire frame and verifying that it is a valid PAUSE control frame addressed to either the Multicast Address (01-80-c2-00-00-01 as specified in IEEE 802.3, Annex 31B) or the Station Address. If the PAUSE frame is valid, the Transmit side of the MAC pauses for the required number of Pause Quanta, as specified in IEEE 802.3u, Clause 31 (see Table 5).

Note: PAUSE does not begin until completion of the frame currently being transmitted.

3.1.3 Fiber Operation

The data path in the MAC is an internal 10-bit interface, as described in the IEEE 802.3z Standard. It is connected directly to an internal SerDes block for Serialization/Deserialization and transmission/reception on the fiber medium to/from the link partner.

The MAC contains all the PCS (8B/10B encoding and 10B/8B decoding) required to encode and decode the data. The MAC also supports auto-negotiation per the IEEE 802.3z Standard via access to the TX Config Word, RX Config Word, and Diverse Config Registers (see Table 57 on page 105, Table 58 on page 106, and Table 59 on page 106).

By default, IXF1110 auto-negotiation is disabled by Register bit 5 (AN_enable) of the "Diverse Config Register (Addr: Port_Index + 0x18)". When auto-negotiation is disabled, the IXF1110 can operate in forced mode, which is 1000 Mbps full duplex only. This is equivalent to entering the state AN_DISABLE_LINK_OK as described in Figure 37-6 of IEEE 802.3. The IXF1110 can pass packets when auto-negotiation is disabled only when the internal Synchronization State Machine indicates that the sync_status is OK as described in Figure 36-9 of IEEE 802.3.

Note: Packet IPG must contain a minimum of three consecutive /I1/ or /I2/ ordered sets per IEEE 802.3 for correct operation.

Note: In forced mode, the TX SPI4-2 status bus (TSTAT[1:0]) is held in the SATISFIED state until sync_status is OK. This prevents the TX FIFO from being filled prior to transmission of packets.

3.1.4 Auto-Negotiation

In the IXF1110, auto-negotiation is carried out by an internal state machine within the MAC. The IXF1110 is fully IEEE 802.3z standard compliant.

There are three registers involved in this auto-negotiation process: RX Config Word, TX Config Word, and Diverse Config:

- The RX Config Word Register performs the operation of the Auto-Negotiation Link Partner Ability Register (see Table 57, "RX Config Word Register (Addr: Port_Index + 0x16)" on page 105)
- The TX Config Word Register performs the operation of the Auto-Negotiation Advertisement Register (see Table 58, "TX Config Word Register (Addr: Port_Index + 0x17)" on page 106
- The Diverse Config Register enables auto-negotiation (see Table 59, "Diverse Config Register (Addr: Port_Index + 0x18)" on page 106)

The TX Config Word Register must be written to program the modes advertised. The Diverse Config Register bit 5 (AN_enable) must be written to enable auto-negotiation. The RX Config Word Register must be polled to determine when auto-negotiation is complete and to determine the link mode. The following MAC registers must be programmed to match the results upon completion:

- Link: Table 66, "Link LED Enable Register (Addr: 0x502)" on page 119 (Addr: 502)
- Flow Control: If the link partner does not support flow control, the FC Enable Register (Addr: Port Index + 0x12) must be updated to reflect this change (see Table 54, "FC Enable Register (Addr: Port_Index + 0x12)" on page 104

To restart auto-negotiation, bit 5 of the Diverse Config Register (AN_enable) must be de-asserted, then re-asserted.

3.1.5 Forced Mode Operation

The fiber operation of the MAC can be forced to operated at 1000 Mbps, full duplex without completion of the auto negotiation function. In this mode, the receive path of the MAC must achieve synchronization with the link partner. Once this has been achieved, the transmit path of the MAC will be enabled to allow data transmission, which is known as "forced mode" operation. Forced mode is limited to operation with a link partner that operates with a full-duplex link at a speed of 1000 Mbps.

Forced mode is enabled by Register bit 5 (AN_enable) in the "Diverse Config Register (Addr: Port_Index + 0x18)". By default, the IXF1110 is set to forced mode operation.

3.1.6 Jumbo Packet Support

The IXF1110 supports the concept of jumbo frames. The jumbo frame length is dependent on the application, and the IXF1110 design has been optimized for 9.6 K jumbo frame length. Lengths larger than this can be programmed, but will limit system performance.

The value programmed into the Max Frame Size Register (Addr: Port_Index + 0x0F) determines the maximum length frame size the MAC can receive or transmit without activating any error counters, and without truncation.

The Max Frame Size Register (Addr: Port_Index + 0x0F) bits 13:0 set the frame length. The default value programmed into this register is 0x05EE (1518). The value is internally adjusted by +4 if the frame has a VLAN tag. The overall programmable maximum is 0x3FFF or 16383 bytes. The register should be programmed to 0x2667 for the 9.6 K length jumbo frame for which the IXF1110 is optimized.

The RMON counters are also affected for jumbo frame support as follows:

RX Statistics:

- RXOctetsTotalOK (Addr: Port_Index + 0x20)
- RXPkts1519toMaxOctets (Addr: Port_Index + 0x2B)
- RXFCSErrors (Addr: Port_Index + 0x2C)
- RXDataError (Addr: Port_Index + 0x02E)
- RXAlignErrors (Addr: Port_Index + 0x2F)

- RXLongErrors (Addr: Port_Index + 0x30)
- RXJabberErrors (Addr: Port_Index + 0x31)
- RXVeryLongErrors (Addr: Port_Index + 0x34)

TX Statistics:

- TXOctetsTotalOK (Addr: Port_Index + 0x40)
- TxPkts1519toMaxOctets (Addr: Port_Index + 0x4B)
- TxExcessiveLengthDrop (Addr: Port_Index + 0x53)
- TXCRCError (Addr: Port_Index + 0x56)

The IXF1110 device checks the CRC for all legal length jumbo frames (frames between 1519 and the Max Frame Size). On transmission, the MAC can be programmed to append the CRC to the frame or check the CRC and increment the appropriate counter. On reception, the MAC transmits these frames across the SPI4-2 interface (jumbo frames with a bad CRC cannot be dropped and are sent across the SPI4-2 interface). If the receive frame has a bad CRC, the appropriate counter is incremented and the EOP Abort code is set in the SPI4-2 control word.

Jumbo frames also impact flow control. The maximum frame size needs to be taken into account when determining the FIFO watermarks. The current transmission must be completed before a Pause frame can be transmitted (needed when the receiver FIFO high watermark has been exceeded). If the current transmission is a jumbo frame, the delay may be significant and increase data loss due to insufficient available FIFO space.

3.1.7 RMON Statistics Support

3.1.7.1 RMON Statistics

The IXF1110 supplies RMON statistics via the CPU interface. These statistics are available in the form of counter values that can be accessed at specific addresses in the IXF1110 memory map. Once read, these counters automatically reset and begin counting from zero. A separate set of RMON statistics is available for each MAC device in the IXF1110.

Implementation of the RMON Statistics block is similar to the functionality provided by existing Intel switch and router products. This implementation allows the IXF1110 to provide all of the RMON Statistics group as defined by RFC2819.

The IXF1110 supports the RMON RFC2819 Group 1 statistics counters. Table 7 notes the differences and additional statistics registers supported by the IXF1110 that are outside the scope of the RMON RFC2819 document.

Table 7. RMON Additional Statistics Registers

RMON Ethernet Statistics Group 1 Statistics	Type	IXF1110 Equivalent Statistics	Type	Definition of RMON Versus IXF1110 Documentation
etherStatsIndex	Integer32	N/A	N/A	N/A
etherStatsDataSource	OBJECT IDENTIFIER	N/A	N/A	N/A
etherStatsDropEvents	Counter32	RX/TX FIFO Number of Frames Removed	Counter 32	See table note 1.
etherStatsOctets	Counter32	RXOctetsTotalOK RXOctetsBad TXOctetsTotalOK TXOctetsBad	Counter 32	**Note:** The IXF1110 has two counters for RX and TX that use different naming conventions for total Octets and Octets bad. These counters need to be combined to meet the RMON spec.
etherStatsPkts	Counter32	RX/TXUCPkts RX/TXBCPkts RX/TXMCPkts	Counter 32	**Note:** The IXF1110 has three counters for etherStatsPkts that need to be combined to give the total packets as defined by the RMON spec.
etherStatsBroadcastPkts	Counter32	RX/TXBCPkts	Counter 32	OK
etherStatsMulticastPkts	Counter32	RX/TXMCPkts	Counter 32	See table note 2.
etherStatsCRCAlignErrors	Counter32	RXAlignErrors RXFCSErrors TXCRCError	Counter 32	**Note:** The IXF1110 has two counters for alignment and CRC errors for the RX side only. The IXF1110 has CRCError for the TX side.

1. The RMON spec requires that this is, "The total number of events where packets were dropped by the probe due to a lack of resources. Note that this number is not necessarily the number of packets dropped; it is the number of times this condition has been detected." The RX/TX FIFO Number of Frames Removed Register in the IXF1110 supports this and will increment when either an RX or TXFIFO has over flowed. If any IXF1110 programmable packet filtering is enabled, the RX/TX Number of Frames Removed Register increments with every frame removed in addition to the existing frames counted due to FIFO overflow.
2. The IXF1110 has an extra counter RX/TXUCPkts that can be used.
3. The IXF1110 has an extra counter RX/TXPktstoMaxOctets that can be used in addition to the RMON stats. This is required to accommodate the Jumbo packet frames requirement.

Table 7. RMON Additional Statistics Registers (Continued)

etherStatsOversizePkts	Counter32	RXLongErrors TXExcessiveLengthDrop	Counter 32	OK
etherStatsJabbers	Counter32	RXJabberErrors	Counter 32	OK
etherStatsCollisions	Counter32	TXSingleCollisions TXMultipleCollisions TXLateCollisions TXTotalCollisions	Counter 32	OK **Note:** Registers exist on the TX side but should not increment since the IXF1110 only supports full-duplex.
etherStatsPkts64Octets	Counter32	RX/TXPkts64Octets	Counter 32	OK
etherStatsPkts65to127Octets	Counter32	RX/TXPkts65to127Octets	Counter 32	OK
etherStatsPkts128to255Octets	Counter32	RX/TXPkts128to255Octets	Counter 32	OK
etherStatsPkts256to511Octets	Counter32	RX/TXPkts256to511Octets	Counter 32	OK
etherStatsPkts512to1023Octets	Counter32	RX/TXPkts512to1023Octets	Counter 32	OK
etherStatsPkts1024to1518Octets	Counter32	RX/TXPkts1024to1518Octets	Counter 32	See table note 3.
etherStatsOwner	OwnerString	N/A	N/A	N/A
etherStatsStatus	EntryStatus	N/A	N/A	N/A

1. The RMON spec requires that this is, "The total number of events where packets were dropped by the probe due to a lack of resources. Note that this number is not necessarily the number of packets dropped; it is the number of times this condition has been detected." The RX/TX FIFO Number of Frames Removed Register in the IXF1110 supports this and will increment when either an RX or TXFIFO has over flowed. If any IXF1110 programmable packet filtering is enabled, the RX/TX Number of Frames Removed Register increments with every frame removed in addition to the existing frames counted due to FIFO overflow.
2. The IXF1110 has an extra counter RX/TXUCPkts that can be used.
3. The IXF1110 has an extra counter RX/TXPktstoMaxOctets that can be used in addition to the RMON stats. This is required to accommodate the Jumbo packet frames requirement.

3.1.7.2 Conventions

The following conventions are used throughout the RMON MIB and its companion documents.

- **Good Packets**: Error-free packets that have a valid frame length. For example, on Ethernet, good packets are error-free packets that are between 64 octets long and 1518 octets long. They follow the form defined in IEEE 802.3, Section 3.2.
- **Bad Packets**: Packets that have proper framing and are therefore recognized as packets, but contain errors within the packet or have an invalid length. For example, on Ethernet, bad packets have a valid preamble and SFD, but have a bad CRC, or are either shorter than 64 octets or longer than 1518 octets.

3.1.7.3 Additional Statistics

The following lists additional IXF1110 registers that support features not documented in RMON.

- MAC (flow) control frames
- VLAN tagged frames
- Sequence errors
- Symbol errors
- CRC errors

These additional counters allow for additional differentiation over and above standard RMON probes.

Note: A packet transfer with an invalid 10-bit symbol will not always update the statistics registers correctly.

- **Behavior:** The IXF1110 8B10B decoder substitutes a valid code word octet in its place. The packet transfer is aborted and marked as bad. The new internal length of the packet is equal to the byte position where the invalid symbol was. No packet fragments are seen at the next packet transfer.
- **Issue:** If the invalid 10-bit code is inserted in a byte position of 64 or greater, expected RX statistics are reported. However, if the invalid code is inserted in a byte position of less than 64, expected RX statistics are not stored.

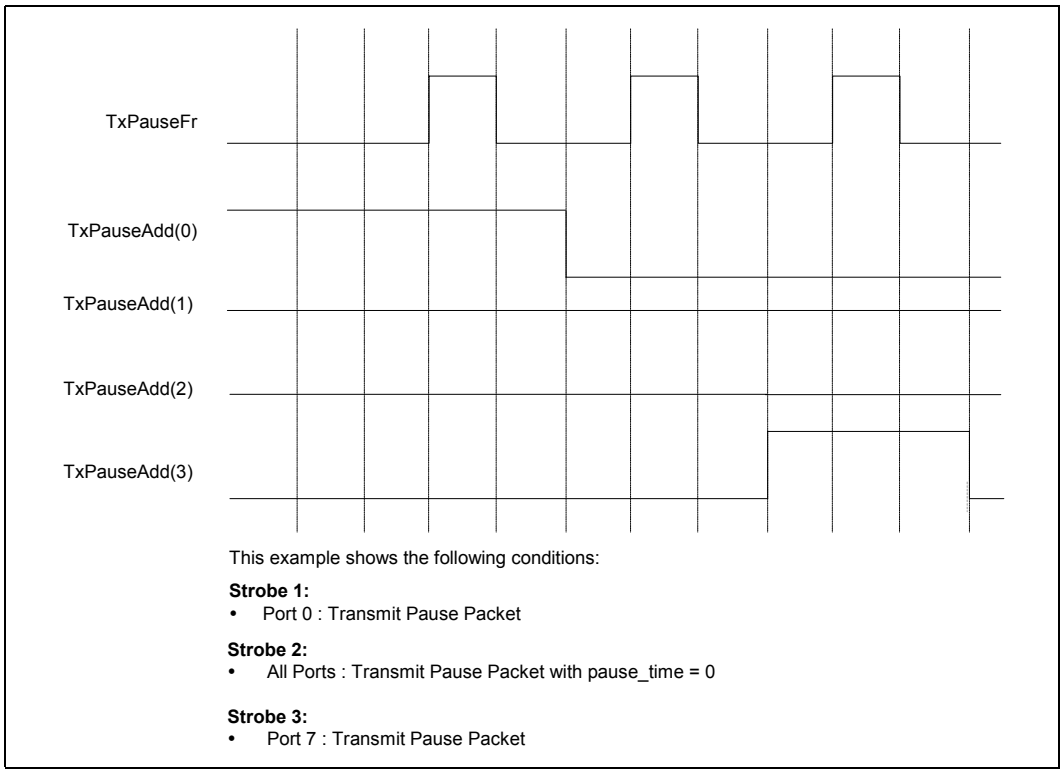
3.1.8 Transmit Pause Control Interface

The Transmit Pause Control interface is completely asynchronous. It consists of four address signals (TxPauseAdd[3:0]) and a strobe signal (TxPauseFr). The required address for this interface operation is placed on the TxPauseAdd[3:0] pins and the TxPauseFr is pulsed High and then returned Low. Refer to Figure 32, “Transmit Pause Control Interface Diagram” on page 83 and Table 27, “Transmit Pause Control Interface Parameters” on page 83. The valid decodes for the TxPauseAdd[3:0] signals are shown in Table 8. Figure 6 illustrates the transmit pause control interface.

Table 8. Valid Decodes for TxPauseAdd[3:0]

TxPauseAdd[3:0]	Operation of Tx Pause Interface
00h	Sends out a PAUSE frame on every port with a pause_time = ZERO (cancels all previous pause commands).
01h to 0Ah	Sends a PAUSE frame out on the selected port with pause_time = to the value programmed into that port’s register set
0Bh to 0Eh	Reserved. These are invalid decodes and should not be used. The Tx Pause Interface will not operate under these conditions.
0Fh	Sends a PAUSE frame out on every port with pause_time = to the value programmed into that ports register set.

Figure 6. Transmit Pause Control Interface



This example shows the following conditions:

Strobe 1:
- Port 0 : Transmit Pause Packet

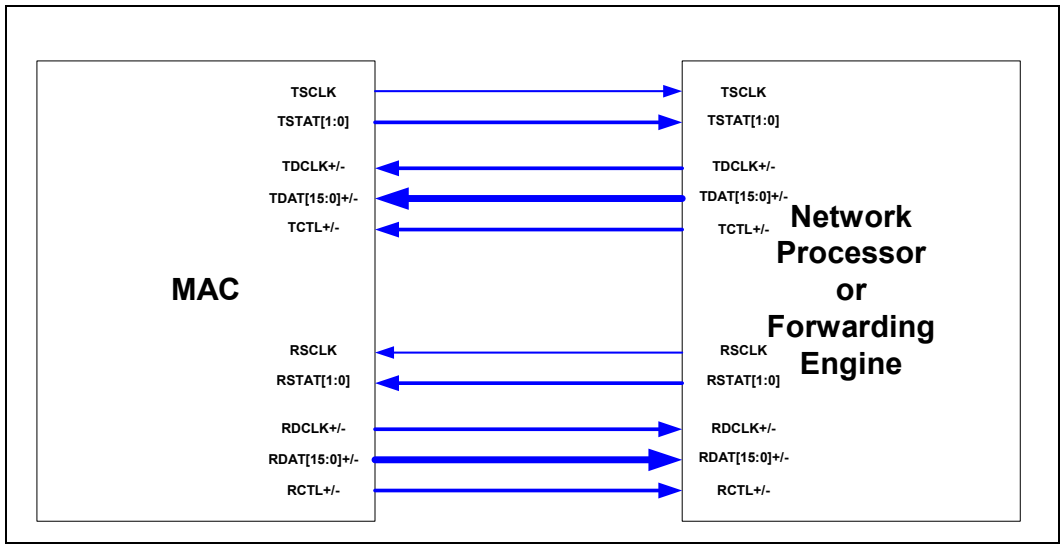
Strobe 2:
- All Ports : Transmit Pause Packet with pause_time = 0

Strobe 3:
- Port 7 : Transmit Pause Packet

3.2 System Packet Interface Level 4 Phase 2

The System Packet Interface Level 4 Phase 2 (SPI4-2) provides a high-speed connection to a network processor or an ASIC. The interface implemented on the IXF1110 operates at data rates up to 12.8 Gbps and supports up to ten 1 Gbps MAC channels. The data path is 16 lanes wide in each direction, with each lane operating from 640 Mbps up to 800 Mbps. Port addressing, start/end packet control, and error control codes are all transferred "in-band" on the data bus. In-band addressing supports up to 10 ports. Separate transmit and receive FIFO status lines are used for flow control. By keeping the FIFO status information out-of-band, the transmit and receive interfaces may be de-coupled to operate independently. Figure 7 provides an overview of the IXF1110 SPI4-2 interface.

Figure 7. IXF1110 SPI4-2 Interfacing with the Network Processor or Forwarding Engine



3.2.1 Data Path

Transfer of complete packets or shorter bursts is controlled by the programmed MaxBurst1 or MaxBurst2 in conjunction with the FIFO status bus. The maximum configured payload data transfer size must be a multiple of 16 bytes. Control words are inserted between burst transfers only. Once a transfer begins, data words are sent uninterrupted until an end-of-packet, or until a multiple of 16 bytes is reached as programmed in MaxBurst1 and MaxBurst2. The interval between the end of a given transfer and the next payload control word (marking the start of another transfer) consists of zero or more idle control words and/or training patterns.

Note: The system designer should be aware that the MAC Transfer Threshold Register must be set to a value which exceeds MaxBurst1 number of bytes. Otherwise, a TX FIFO under-run may result.

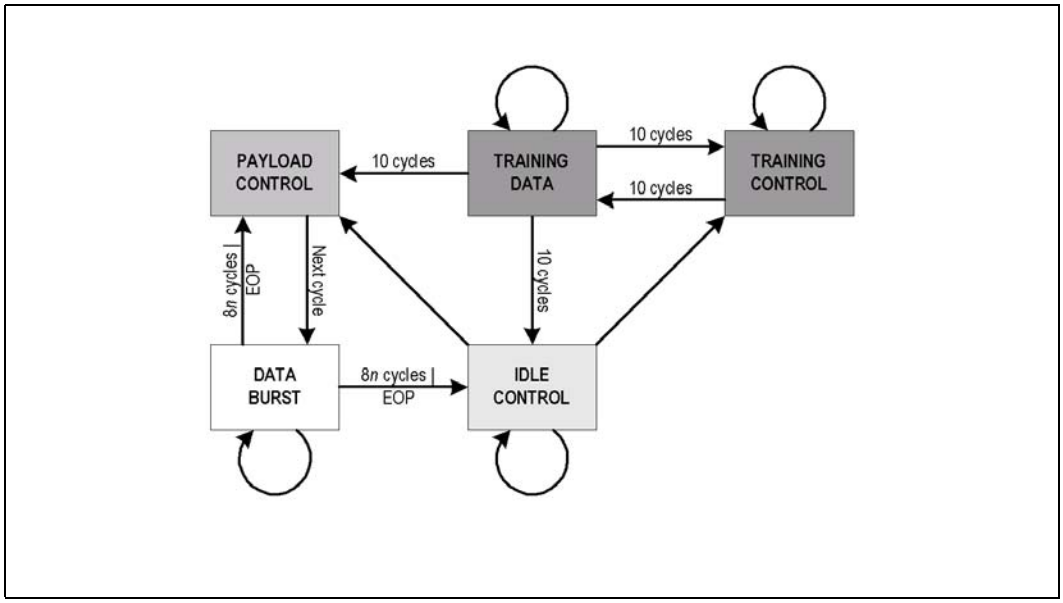
The minimum and maximum supported packet lengths are determined by the application. Because the IXF1110 is targeted at the Ethernet environment, the minimum frame size is 64 bytes and the maximum frame size is 1522 bytes for VLAN packets (1518 bytes for non-VLAN packets). For larger frames, adjust the Max Frame Size Register value, seen in Table 53 on page 104. For ease of implementation, successive start-of-packets must occur not less than eight cycles apart, where a cycle is one control or data word. The gap between shorter packets is filled with idle control words.

Note: Data packets with frame lengths less than 64 bytes should not be transferred to the IXF1110 unless packet padding is enabled. If this rule is disregarded, unwanted fragments may be generated on the network at the SerDes interface.

Figure 8 on page 36 shows cycle-by-cycle behavior of the data path for valid state transitions. The states correspond to the type of words transferred on the data path. Transitions from the "Data Burst" state (to "Payload Control" or "Idle Control") are possible only on the integer multiples of eight cycles (corresponding to multiples of 16-byte segmentations) or upon end-of-packet. A data burst must immediately follow a payload control word on the next cycle. Arcs not annotated correspond to single cycles.

In the IXF1110, the RX FIFO Status channel operates in a "pessimistic mode." It is termed as pessimistic because it has the longest latency and largest impact on usable bandwidth. However, as a DIP-2 check error is a rare event, there will be no 'real world' effect on bandwidth utilization and no possibility of data loss. For example, if there is a DIP-2 check error found, all previously granted credits are cancelled and the internal status for each channel is set to SATISFIED. Any current data burst in transmission is completed. No new credits are granted until a complete FIFO status cycle has been received and validated by a correct DIP-2 check. This is the only method of operation that can eliminate the possibility of an overrun in the link partner device.

Figure 8. Data Path State Diagram



3.2.1.1 Control Words

A common control word format is used in both the transmit and receive interfaces. Table 9 describes the fields in the control word. When inserted in the data path, the control word is aligned such that its MSB is sent on the MSB of the transmit or receive data lines. A payload control word that separates two adjacent burst transfers contains status information pertaining to the previous transfer and the following transfer. Table 10 provides a list of control-word definitions.

Table 9. Control Word Format

Bit Position	Label	Description
15	Type	Control Word Type. Set to either of the following values: 1: payload control word (payload transfer will immediately follow the control word). 0: idle or training control word.
14:13	EOPS	End-of-Packet (EOP) Status. Set to the following values according to the status of the immediately preceding payload transfer. 0 0: Not an EOP. 0 1: EOP Abort (application-specific error condition). 1 0: EOP Normal termination, 2 bytes valid. 1 1: EOP Normal termination, 1 byte valid. EOPS is valid in the first control word following a burst transfer. It is ignored and set to “0 0” otherwise.
12	SOP	Start-of-Packet. Set to 1 if the payload transfer immediately following the control word corresponds to the start of a packet. Set to 0 otherwise. Set to 0 in all idle and training control words.
11:4	ADR	Port Address. 8-bit port address of the payload data transfer immediately following the control word. None of the addresses are reserved (all are available for payload transfer). Set to all zeroes in all idle control words. Set to all ones in all training control words.
3:0	DIP-4	4-bit Diagonal Interleaved Parity. 4-bit odd parity computed over the current control word and the immediately preceding data words (if any) following the last control word.

Table 10. Control Word Definitions

	Bit [15:12]	Next Word Status	Prior Word Status	Meaning
0	0000	Idle	Continued	Idle, not EOP, training control word
1	0001	Reserved	Reserved	Reserved
2	0010	Idle	EOP w/abort	Idle, Abort last packet
3	0011	Reserved	Reserved	Reserved
4	0100	Idle	EOP w/ 2 bytes	Idle, EOP with 2 bytes valid
5	0101	Reserved	Reserved	Reserved
6	0110	Idle	EOP w/ 1 byte	Idle, EOP with 1byte valid
7	0111	Reserved	Reserved	Reserved
8	1000	Valid	None	Valid, no SOP, no EOP
9	1001	Valid/SOP	None	Valid, SOP, no EOP
A	1010	Valid	EOP w/abort	Valid, no SOP, abort
B	1011	Valid/SOP	EOP w/abort	Valid, SOP, abort
C	1100	Valid	EOP w/ 2 bytes	Valid, no SOP, EOP with 2 bytes valid

Table 10. Control Word Definitions (Continued)

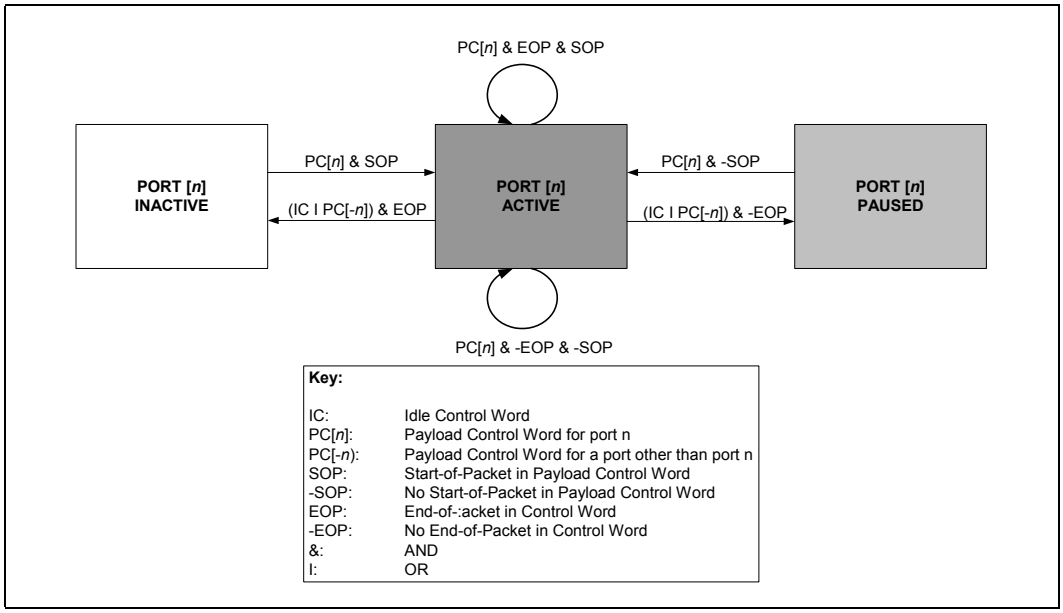
	Bit [15:12]	Next Word Status	Prior Word Status	Meaning
D	1101	Valid	EOP w/ 2 bytes	Valid, SOP, EOP with 2 bytes valid
E	1110	Valid	EOP w/ 1 byte	Valid, no SOP, EOP with 1byte valid
F	1111	Valid	EOP w/ 1 byte	Valid, SOP, EOP with 1byte valid

The SPI4-2 specification details all available Payload Control Words and should be used to reference the specific meaning of each. The IXF1110 supports all required functions per this specification. However, there are various specifics in the way certain Control Words affect the balance of the IXF1110 operation, such as how the device deals with EOP Aborts.

The SPI4-2 specification allows the EOP Abort Payload Control word, which signals that the data associated with a particular frame is errored and should be dropped, or errored and dropped by the far-end link partner. In the IXF1110, all TX SPI4-2 transfers that end with an EOP Abort code have the TX SerDes CRC corrupted. This is true regardless of the MAC configuration.

Figure 9 shows per-port state transitions at control-word boundaries. At any given time, a port may be active (sending data), paused (not sending data but pending the completion of an outstanding packet), or inactive (not sending data, no outstanding packet).

Figure 9. Per-Port State Diagram with Transitions at Control Words



3.2.1.2 DIP4

Figure 10 shows the range over which the Diagonal Interleaved Parity (DIP-4) parity bits are computed. A functional description of calculating the DIP-4 code is given as follows. Assume that the stream of 16-bit data words are arranged as shown in Figure 11, MSB at the left most column, time moving downward. (The first word received is at the top of the figure; the last word is at the bottom of the figure.) The parity bits are generated by summing diagonally (in the control word, the space occupied by the DIP-4 code (bits a, b, c, d) is set to all 1s during encoding). The first 16-bit result is split into two bytes, which are added to each other modulo-2 to produce an 8-bit result.

The 8-bit result is then divided into two 4-bit nibbles, which are added to each other modulo-2 to produce the final DIP-4 code. The procedure described applies to either parity generation on the Rx path or to check parity on the Tx path.

Figure 10. DIP-4 Calculation Boundaries

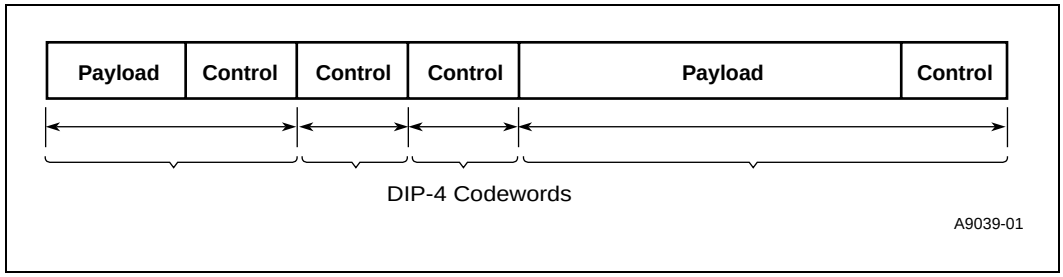
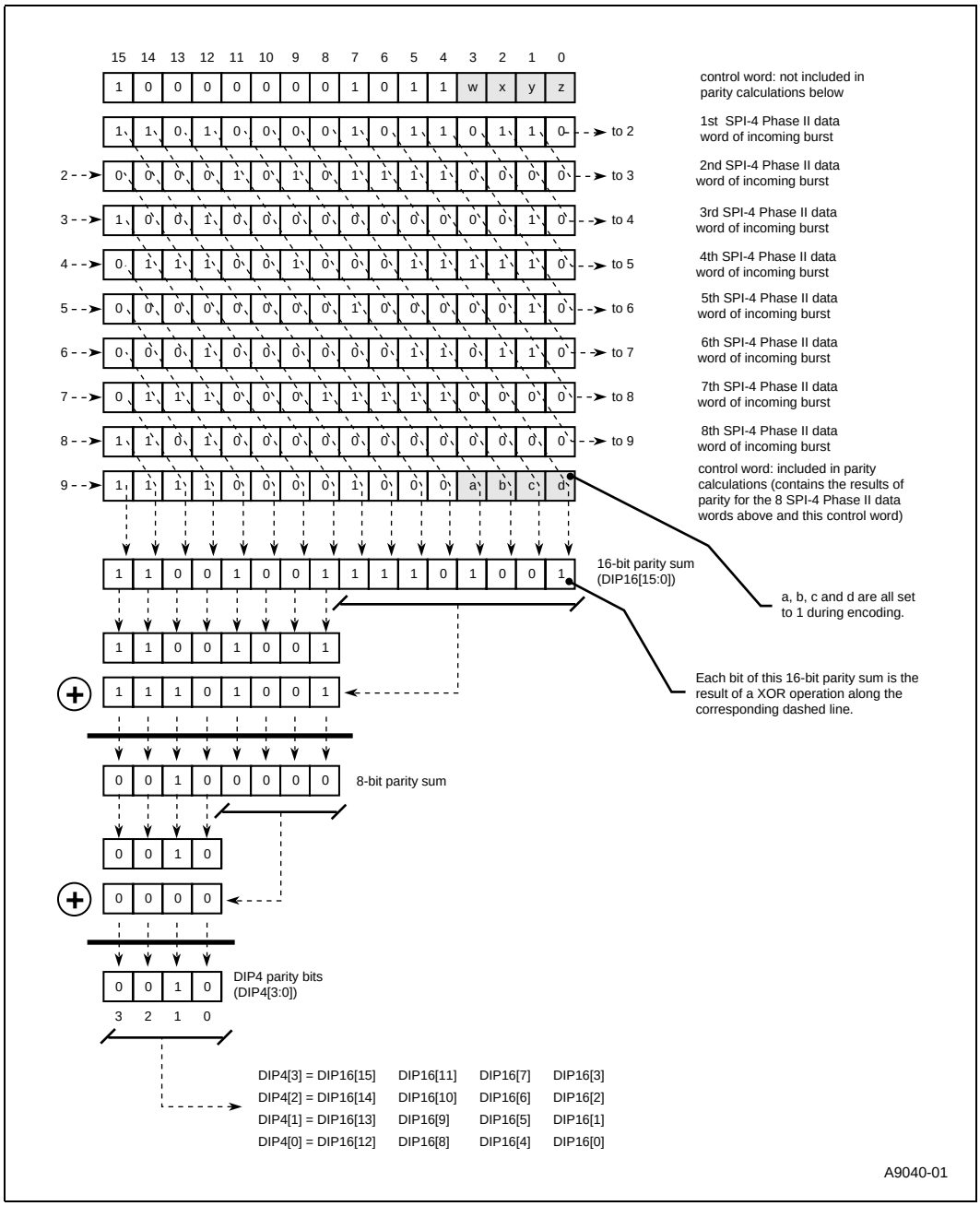


Figure 11. DIP-4 Calculation Algorithm



3.2.2 Start-Up Parameters

3.2.2.1 CALENDAR_LEN

CALENDAR_LEN specifies the length of each calendar sequence. As the IXF1110 is a 10-port device, CALENDAR_LEN is fixed at 10 for both TX and RX data paths.

3.2.2.2 CALENDAR_M

CALENDAR_M specifies the number of times the calendar port status sequence is repeated between the framing and DIP2 cycle of the calendar sequence.

In the IXF1110, the TX path CALENDAR_M is fixed at 1; thus, the port status for ports 0 - 9 will be transmitted only once between the framing and DIP2 cycle of the calendar sequence.

In the IXF1110, the RX path CALENDAR_M is configurable. The default value of expected RX CALENDAR_M is 1 as per the TX path. In Table 85, "SPI4-2 RX Calendar Register (Addr: 0x702)" on page 141, bits 3 to 0 specify CAL_M, which is the number of times the calendar sequence will be repeated over the default value of 1.

The default value for CAL_M is 0, thus the default value of both Tx and RX CALENDAR_M parameters is 1.

3.2.2.3 DIP2_Thr

DIP2_Thr is a parameter specifying the number of consecutive correct DIP2s required by the RX SPI4-2 to validate a calendar sequence and therefore terminate sending training sequences. In Table 85, "SPI4-2 RX Calendar Register (Addr: 0x702)" on page 141, bits 19 to 16 specify this parameter. The default value for DIP2_Thr is 1.

3.2.2.4 Loss_Of_Sync

Loss_of_Sync is a parameter specifying the number of consecutive framing calendar cycles required to indicate a loss of synchronization and therefore restart training sequences. Table 85, "SPI4-2 RX Calendar Register (Addr: 0x702)" on page 141, bits 11 to 8 specify this parameter. The default value for Loss_Of_Sync is three.

3.2.2.5 DATA_MAX_T

DATA_MAX_T is an RX SPI4-2 parameter specifying the interval between transmission of periodic training sequences. In Table 84, "SPI4-2 RX Training Register (Addr: 0x701)" on page 140, bits 15 to 0 specify this parameter. The default value for DATA_MAX_T is 0x0000, which disables periodic training sequence transmission.

3.2.2.6 REP_T

REP_T is an RX SPI4-2 parameter specifying the number of repetitions of the training sequence to be scheduled every DATA_MAX_T interval. In Table 84, "SPI4-2 RX Training Register (Addr: 0x701)" on page 140, bits 23 to 16 specify this parameter. The default value for REP_T is 0x00.

3.2.2.7 DIP4_UnLock

DIP4_UnLock is a TX SPI4-2 parameter specifying the number of consecutive incorrect DIP4 fields to be detected in order to declare loss of synchronization and drive TSTAT[1:0] bus with framing. In Table 86, "SPI4-2 TX Synchronization Register (Addr: 0x703)" on page 142, bits 15 to 8 specify this parameter. The default value for DIP4_UnLock is 0x4.

3.2.2.8 DIP4_Lock

DIP4_Lock is a TX SPI4-2 parameter specifying the number of consecutive correct DIP4 fields to be detected in order to declare synchronization achieved and enable the calendar sequence. In Table 86, "SPI4-2 TX Synchronization Register (Addr: 0x703)" on page 142, bits 7 to 0 specify this parameter. The default value for DIP4_Lock is 0x20.

3.2.2.9 MaxBurst1

MaxBurst1 is an RX SPI4-2 parameter specifying the maximum number of 16 byte blocks that may be transmitted when the associated FIFO status indicates "starving". Bits 24 to 16 of the SPI4-2 RX Burst Size Register specify this parameter. The default value for MaxBurst1 is 0x006, indicating a MaxBurst1 of 96 bytes [see Section 83, "SPI4-2 RX Burst Size Register (Addr: 0x700)" on page 140].

3.2.2.10 MaxBurst2

MaxBurst2 is an RX SPI4-2 parameter specifying the maximum number of 16 byte blocks that may be transmitted when the associated FIFO status indicates "hungry". Bits 8 to 0 of the SPI4-2 RX Burst Size Register specify this parameter. The default value for MaxBurst2 is 0x002, indicating a MaxBurst2 of 32 bytes (see Section 83, "SPI4-2 RX Burst Size Register (Addr: 0x700)" on page 140).

3.2.3 Training Sequence for Dynamic Phase Alignment (Data Path De-skew)

3.2.3.1 Training at Start-up

The SPI4-2 Specification states that on power-up or after a reset, the training sequence (as defined in the SPI4-2 Specification) is sent indefinitely by the source side until it receives valid FIFO status on the FIFO bus. The specification also states that it is possible for the bus de-skew to be completed after one training sequence takes place. It is unlikely that the bus can be de-skewed in a single training sequence because of the presence of both random and deterministic jitter. The only way to account for the random element is to determine an average over repeated training sequences. Since the required number of repeats is dependent on several characteristics of the system in which the IXF1110 is being used, power on training (or training following loss of synchronization) will continue until synchronization is achieved and the calendar is provisioned. The length of power on training will not be a fixed number of repeats.

The number of training sequence repeats could be fairly large (16, 32, or 64). If this is necessary every time training is required, a significant use of interface bandwidth is needed just to train and de-skew the data path. This is only done at power-up or reset for an optimal starting point interface. After this, periodic training provides a better adjustment and a substantially lower bandwidth overhead.

3.2.3.2 Periodic Training

A scheduled training sequence is sent at least once every pre-configured bounded interval (DATA_MAX_T) on both the transmit and receive paths. These training sequences are used by the receiving end of each interface for de-skewing bit arrival times on the data and control lines. The sequence allows the receiving end to correct for relative skew difference of up to +/- 1 bit time. The

training sequence consists of one (1) idle control word followed by one or more repetitions of a 20-word training pattern consisting of 10 (repeated) training-control words followed by 10 (repeated) training-data words.

The initial idle control word removes dependencies of the DIP-4 in the training control words from preceding data words. Assuming a maximum of +/- bit time alignment jitter on each line, and a maximum of +/- bit time relative skew between lines, there are at least eight bit times when a receiver can detect a training control word prior to de-skew. The training data word is chosen to be orthogonal to the training control word. In the absence of bit errors in the training pattern, a receiver should be able successfully to de-skew the data and control lines with one training pattern. The sending side of the data path on both the transmit and receive interfaces must schedule the training sequence at least once every DATA_MAX_T cycles.

Note: DATA_MAX_T may be set to zero, disabling periodic training on the interface (refer to Table 84, "SPI4-2 RX Training Register (Addr: 0x701)" on page 140). This is done when a system shows very little drift during normal operation, and no fine-grain correction on an on-going basis is needed. This allows the maximum possible bandwidth for data transfer. The transmit and receive interface training sequences are scheduled independently.

3.2.3.3 Training in a Practical Implementation

The OIF Standard states that it should be possible to train and de-skew the data input in a single training cycle. However, from the research carried out and the variances in jitter and skew due to board layout and clock tolerance issues, some sort of averaging over several repeated training patterns is required to reliably determine the optimal point at which to capture the incoming data. This is true for both static alignment and dynamic phase alignment. Therefore, several training patterns are required for an average. The more training patterns, the more accurate the average.

The de-skew circuit in the IXF1110 uses dynamic phase alignment with a typical averaging requirement of 32 training patterns required to deliver a reliable result. During power-on training, an unlimited number of training cycles is sent by the data sourcing device. (The standard states that training must be sourced until a calendar has been provisioned.) In the IXF1110, the de-skew circuit waits until completion of its programmed average over the training patterns, ensuring that the required number of good DIP-4s is seen. Only then is a calendar provisioned.

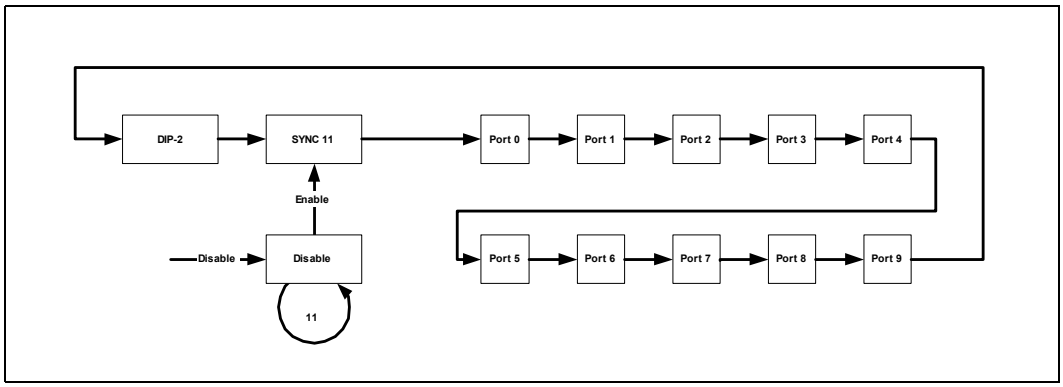
During periodic training, it is important to ensure that the training result is no less accurate than that already used for the initial decision during power-on training. Thus, a similar number of training cycles must be averaged over (32). This could make the overhead associated with periodic training large if it is required to be carried out too often. We therefore recommend that periodic training be scheduled infrequently (DATA_MAX_T = a large number) and that the number of repetitions of training be = 32(α).

3.2.4 FIFO Status Channel

FIFO status information is sent periodically over the TSTAT link from the IXF1110 to the upper layer processor device, and over the RSTAT link from the upper layer processor to the IXF1110. The status channels operate independently.

Figure 12 shows the operation of the FIFO status channel. The sending side of the FIFO status channel is initially in the DISABLE state and sends the "1 1" pattern repeatedly. When FIFO status transmission is enabled, there is a transition to the SYNC state and the "1 1" framing pattern is sent. FIFO status words are then sent according to the calendar sequence, repeating the sequence CALENDAR_M times, followed by the DIP-2 code.

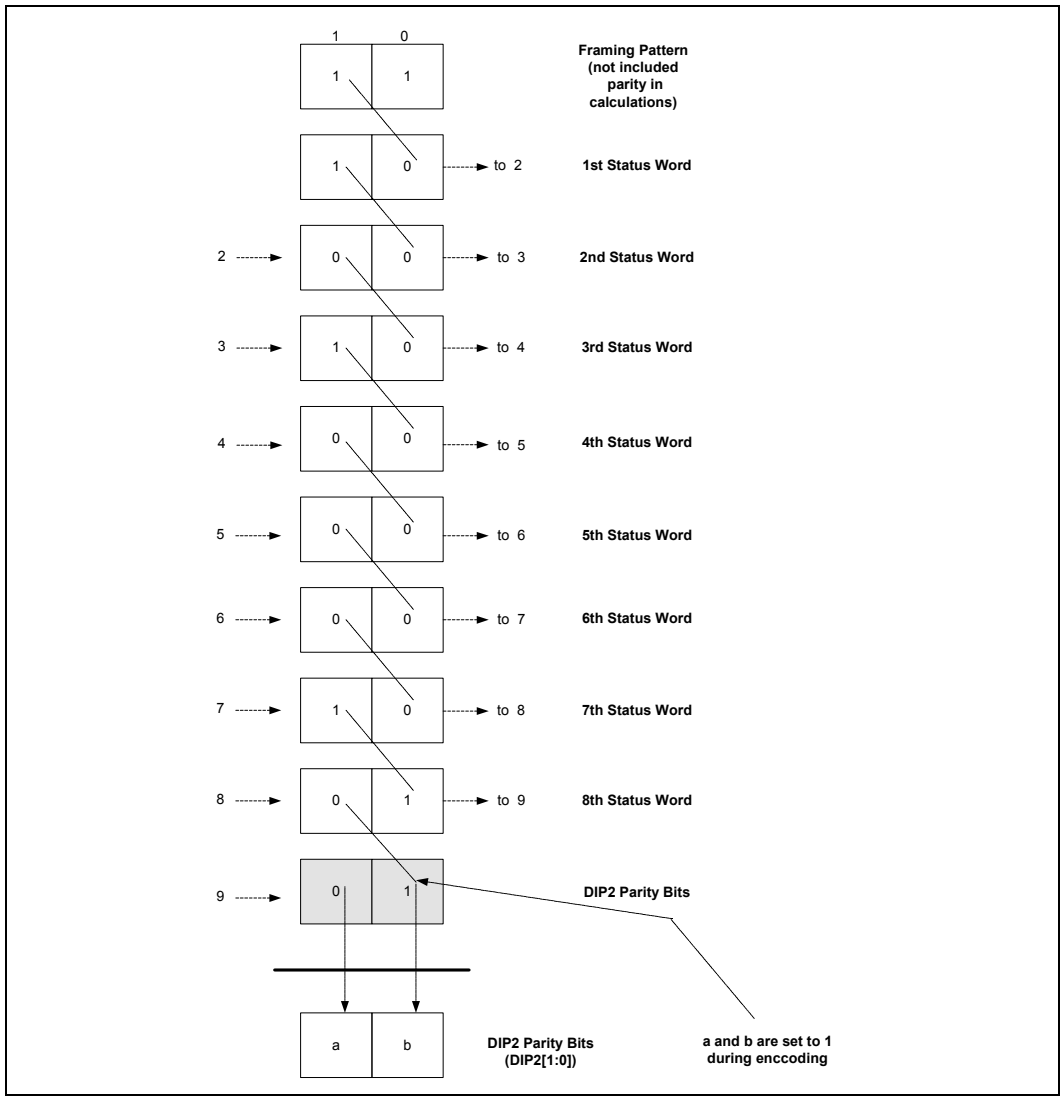
Figure 12. FIFO Status State Diagram



The FIFO status of each port is encoded in a 2-bit data structure, which is defined in Table 11, "FIFO Status Format" on page 46. The most significant bit of each port status is sent over TSTAT[1]/RSTAT[1] and the least significant bit is sent over TSTAT[0]/RSTAT[0]. The "1 1" pattern is reserved for In-band framing, which must be sent once prior to the start of the FIFO status sequence.

Immediately before the "1 1" framing pattern, a DIP-2 odd parity checksum is sent at the end of each complete sequence. The DIP-2 code is computed diagonally over TSTAT[1]/RSTAT[1] and TSTAT[0]/RSTAT[0] for all preceding FIFO status indications sent after the last "1 1" framing pattern, as shown in Figure 13 on page 45. The first word is at the top of the figure and the last word is at the bottom. The parity bits are computed by summing diagonally. Bits a and b in line 9 correspond to the space occupied by the DIP-2 parity bits and are set to 1 during encoding. The "1 1" framing pattern is not included in the parity calculation. The procedure described applies to either parity generation on the egress path or to check parity on the ingress path.

Figure 13. Example of DIP-2 Encoding



When the parity bits mimic the “1 1” pattern, the receiving end still frames successfully by syncing onto the last cycle in a repeated “1 1” pattern, and by making use of the configured sequence length when searching for the framing pattern.

To permit more efficient FIFO utilization, the MaxBurst1 and MaxBurst2 credits are granted and consumed in increments of 16-byte blocks. For any given port, these credits correspond to the most recently received FIFO status. They are not cumulative and supersede previously granted credits for the given port. A burst transfer shorter than 16 bytes (for example, an end-of-packet fragment) consumes an entire 16-byte credit.

A continuous stream of repeated “1 1” framing patterns indicates a disabled status link. For example, it may be sent to indicate that the data path de-skew is not yet completed or confirmed. When a repeated “1 1” pattern is detected, all outstanding credits are cancelled and set to zero.

Table 11. FIFO Status Format

MSB	LSB	Description
1	1	Reserved for framing or to indicate a disabled status link.
1	0	SATISFIED: Indicates that the corresponding port's FIFO is almost full. When SATISFIED is received, only transfers using the remaining previously granted 16-byte blocks (if any) may be sent to the corresponding port until the next status update. No additional transfers to that port are permitted while SATISFIED is indicated.
0	1	HUNGRY: When HUNGRY is received, transfers for up to MaxBurst2 16-byte blocks, or the remainder of what was previously granted (whatever is greater), may be sent to the corresponding port until the next status update.
0	0	STARVING: Indicates that buffer underflow is imminent in the corresponding PHY port. When STARVING is received, transfers for up to MaxBurst1 16-byte blocks may be sent to the corresponding port until the next status update

The indicated FIFO status is based on the latest available information. A STARVING indication provides additional feedback information, so that transfers are scheduled accordingly. Applications that do not distinguish between HUNGRY and STARVING may only examine the most significant FIFO status bit.

Note: If a port is disabled on the IXF1110, FIFO status for the port is set to SATISFIED to avoid the possibility of any data being sent to it by the controlling device. This applies to the IXF1110 transmit path.

Upon reset, the FIFOs in the data path receiver are emptied, and any outstanding credits are cleared in the data path transmitter. After reset, and before active traffic is generated, the data transmitter sends continuous training patterns. Transmission of the training patterns continues until valid information is received on the FIFO Status Channel. The receiver ignores all incoming data until it has observed the training pattern and acquired synchronization with the data. Synchronization may be declared after a provisional number of consecutive correct DIP-4 code words is seen. Loss of synchronization may be reported after a provisional number of consecutive DIP-4 code words is detected. [For details, see Table 86, “SPI4-2 TX Synchronization Register (Addr: 0x703)” on page 142.]

As stated above, the DIP-4 thresholds are programmable. However, there is a potential issue where it is possible that a given link showing DIP-4 errors may never lose synchronization and re-train to fix the issue. This would mean an on-going and potentially significant loss of data on the link affecting all ports transferring data at that time.

This issue may be seen in two instances:

- During training (most likely periodic training)
- During data transfers where each of the data transfers (MaxBurst1 or MaxBurst2) are separated by more than one idle control word

The mechanism for both issues is the same because data will not change during a repeated period of the same control word being transmitted on the link. If there have been some consecutive DIP-4 errors, they will be incremented towards the Loss-of-Sync threshold. This is most likely to occur from a path requiring de-skew. If either a stream of idles or training control words follow the burst and the DIP-4 associated with each of the words is checked, only the first one and the last one will be seen as invalid. Any other control words in the middle will be seen as having a valid DIP-4 and will reset the Loss-of-Sync threshold counter back to zero.

In order to avoid this, the IXF1110 has altered the way in which the check is done for idle control words and training control words. We now only validate the first occurrence of the DIP-4 in both training control words and idle control words for correctness. We do still check each of the words but only use the first occurrence to clear the DIP-4 error counter. Any DIP-4 error in any of these words is still counted towards the Loss-of-Sync threshold counter. It is now impossible to mask the DIP-4 error on our interface.

3.2.5 DC Parameters

For DC parameters on the SPI4-2 interface, please refer to Figure 23, “2.5 V LVTTL and CMOS I/O Electrical Characteristics” on page 78 and Figure 24, “LVDS I/O Electrical Characteristics” on page 78.

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3.3 SerDes Interface

3.3.1 Introduction

The following sections describe the operations supported by each SerDes interface, the configurable options, and register bits that control these options. (A full list of the register addresses and full bit definitions are found in the Register Map (Table 43, “SerDes Block Register Map” on page 101).

The IXF1110 includes ten SerDes interfaces that allow direct connection to optical modules and remove the requirement for external SerDes devices. This increases integration, which reduces the PCB real-estate, reduces both silicon and manufacturing costs, and improves reliability.

Each SerDes interface is identical and fully compliant with the relevant IEEE 802.3 Specifications, including auto-negotiation. Each port is also compliant with and supports the requirements of the SFF Committee Gigabit Interface Converter (GBIC) Standards (SFF-8053, revision 5.5).

3.3.2 Features

The SerDes cores are designed to operate in point-to-point data transmission applications. While the core can be used across various media types, such as PCB or backplanes, it is configured specifically for use in 1000BASE-X Ethernet fiber applications in the IXF1110. The following features are supported.

- 10-bit data path, which connects to the output/input of the 8B/10B encoder/decoder PCS that resides in the MAC controller
- Data frequency of 1.25 GHz
- Low power: <200 mW per SerDes channel
- Asynchronous clock data recovery

3.3.3 Functional Description

3.3.3.1 Transmitter Operational Overview

The transmit section of the IXF1110 has to serialize the Ten Bit Interface (TBI) data from the IXF1110 MAC section and outputs this data at 1.25 GHz differential PECL signal levels. The 1.25 GHz differential PECL signals are compliant with the SFF-8053 Specification for GBIC Rev 5.5.

The transmitter section takes the contents of the data register within the MAC and synchronously transfers the data out, ten bits at a time – Least Significant Bit (LSB) first, followed by the next Most Significant Bit (MSB). When these ten bits have been serialized and transmitted, the next word of 10-bit data from the MAC is ready to be serialized for transmission.

The data is transmitted by the high-speed current mode differential PECL output stage using an internal 1.25 GHz clock generated from the 125 MHz clock input.

3.3.3.2 Receiver Operational Overview

The receiver structure performs Clock and Data Recovery (CDR) on the incoming serial data stream. The quality of this operation is a dominant factor for the Bit Error Rate (BER) system performance. Feed forward and feedback controls are combined in one receiver architecture for enhanced performance. The data is over-sampled and a digital circuit detects the edge position in the data stream. A signal is not generated if an edge is not found. A feedback loop takes care of low-frequency jitter phenomenon of unlimited amplitude, while a feed forward section suppresses high-frequency jitter having limited amplitude. The static edge position is held at a constant position in the over-sampled by a constant adjustment of the sampling phases with the early and late signals.

3.4 Gigabit Interface Converter

3.4.1 Introduction

This section describes the connection of the IXF1110 ports to a Gigabit Interface Converter (GBIC) module, and the connections supported for correct operation are detailed. The registers used to write control and read status information are documented (refer to Section 6.5.9, “GBIC Block Register Overview” on page 144).

The GBIC interface allows the IXF1110 a seamless connection to the GBIC modules that form the system’s physical media connection, eliminating the need for any FPGAs or CPUs to process data. All required information of the GBIC modules is available to the system CPU via the IXF1110 CPU interface, leading to a more integrated, reliable, and cost-effective system.

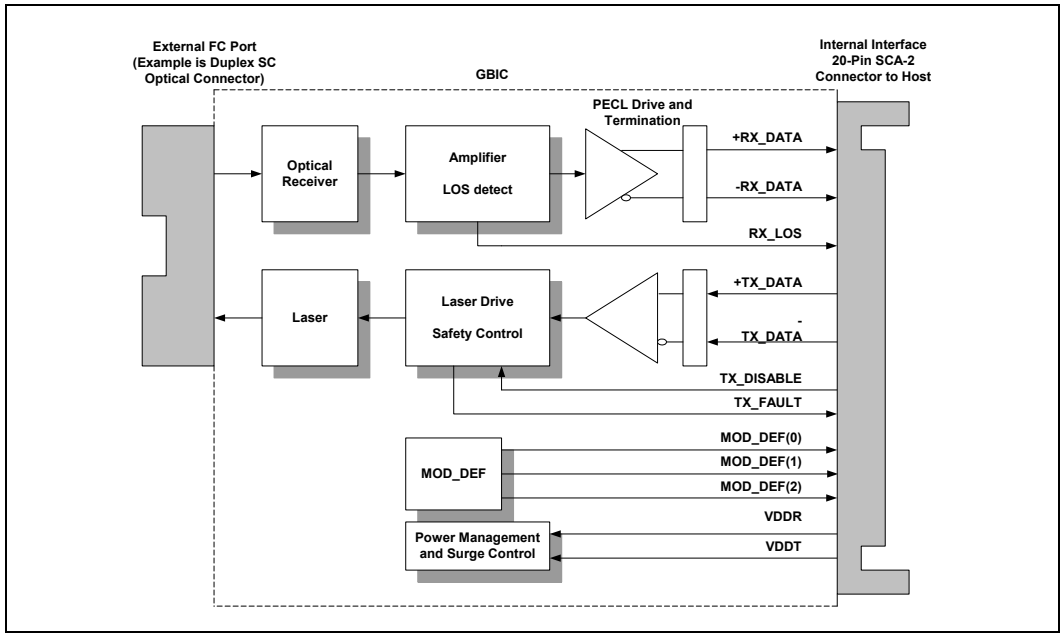
3.4.2 GBIC Description

GBICs were originally designed for fiber channel applications using the Fiber Channel Arbitrated Loop (FC-AL). The design is practical for point-to-point fiber channel implementations and for other high-performance serial technologies, including 1000 Mbps Ethernet.

There are specific mechanical and electrical requirements for the size, form factor, and connections supported on all GBICs. There are also specific requirements for each GBIC that supports a particular media requirement or interface configuration. These requirements are detailed in relevant specifications or manufacturers' datasheets.

The IXF1110 supports all the functions required for full compatibility with GBIC modules supporting the SFF Type 4 Module (refer to SFF-8053, revision 5.5). Figure 14 provides typical GBIC module functionality.

Figure 14. Typical GBIC Module Functional Diagram



3.4.3 IXF1110 Supported GBIC Interface Signals

For GBIC interface operation, three supported signal subgroups are required, allowing a more explicit definition of each function and implementation. The three subgroups are as follows:

- High-Speed Serial Interface
- Low-Speed Status Signaling Interface
- I^2C Module Configuration Interface

Table 12 provides descriptions for IXF1110-to-GBIC module connection pins.

Table 12. IXF1110-to-GBIC Connections

IXF1110 Pin Names	GBIC Module Pin Name	Description	Notes
TX_9:0+	+TX_DAT	Transmit Data, Differential PECL	Output from the IXF1110
TX_9:0-	-TX_DAT		
RX_9:0+	+RX_DAT	Receive Data, Differential PECL	Input to the IXF1110
RX_9:0-	-RX_DAT		

Table 12. IXF1110-to-GBIC Connections (Continued)

IXF1110 Pin Names	GBIC Module Pin Name	Description	Notes
I^2C_CLK	MOD_DEF(1)	I^2C_CLK Output from IXF1110 (SCL)	Output from the IXF1110
I^2C_DATA_9:0	MOD_DEF(2)	I^2C_DATA I/O (SDA)	Input/Output
MOD_DEF_9:0	MOD_DEF(0)	MOD_DEF(0) should be TTL Low level during normal operation.	Input to the IXF1110
TX_DISABLE_9:0	TX_DISABLE	Transmitter Disable, Logic High, Open collector compatible	Output from the IXF1110
TX_FAULT_9:0	TX_FAULT	Transmitter Fault, Logic High, Open collector compatible	Input to the IXF1110
RX_LOS_9:0	RX_LOS	Receiver Loss of Signal, Logic High, Open collector compatible	Input to the IXF1110

3.4.4 Functional Descriptions

3.4.4.1 High-Speed Serial Interface

These signals are responsible for transfer of the actual data at 1.25 Gbps. The data is 8B/10B encoded and transmitted differentially at PECL levels per the required specifications. This interface may be either AC or DC coupled (see Table 43, “SerDes Block Register Map” on page 101).

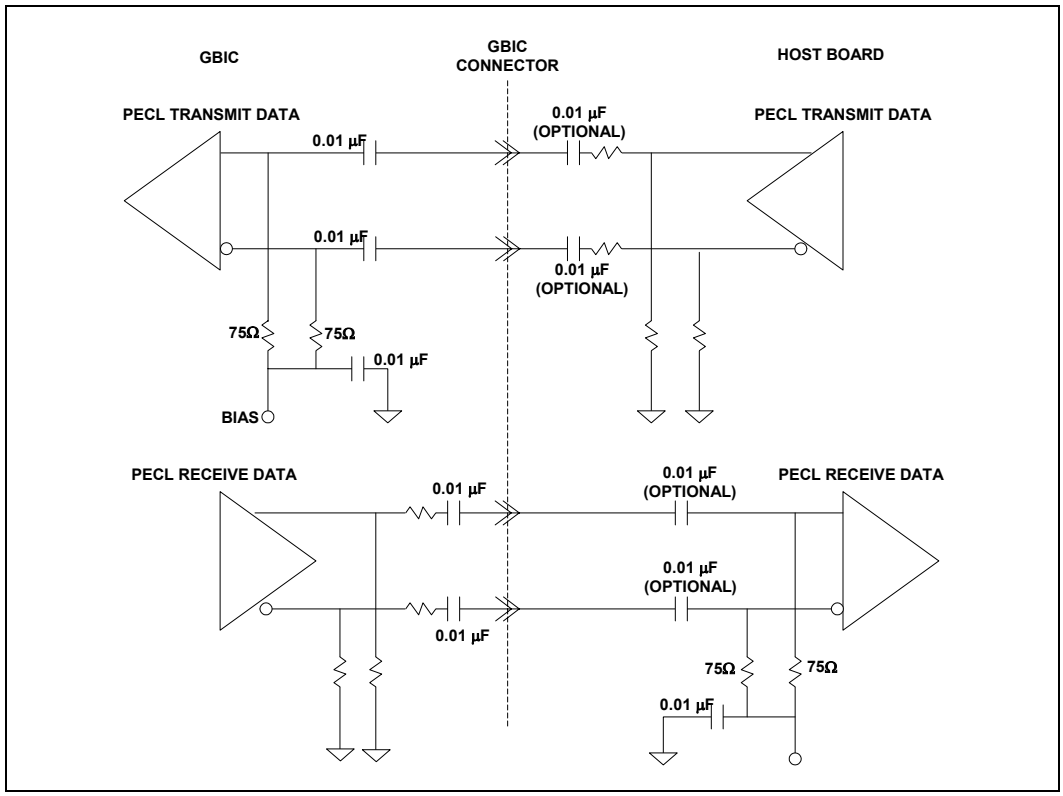
The signals required to implement the high-speed serial interface are:

- TX_9:0+
- TX_9:0-
- RX_9:0+
- RX_9:0-

Figure 15 shows a generic high-speed serial interface implementation (AC-coupled).

Note: The IXF1110 has integrated termination, thus all the components shown on the host board are not required.

Figure 15. Data Path Connection and Termination



3.4.4.2 Low-Speed Status Signaling Interface

The following low-speed signals indicate the state of the line via the GBIC module:

- MOD_DEF_9:0
- TX_FAULT_9:0
- RX_LOS_9:0
- TX_DISABLE_9:0
- MOD_DEF_Int
- TX_FAULT_Int
- RX_LOS_Int

3.4.4.2.1 MOD_DEF_9:0

These signals are direct inputs to the IXF1110 and are pulled to a logic Low level during normal operation, indicating that a module is present for each channel, respectively. If a module is not present, a logic High is received, which is achieved by a pull-up resistor on the IXF1110 pad.

The status of each bit (one for each port) is found in bits 9:0 of the GBIC Status Register (refer to Table 90, "GBIC Status Register Ports 0-9 (Addr: 0x799)" on page 144). Any change in the state of these bits causes a logic Low level on the MOD_DEF_Int output if this operation is enabled.

3.4.4.2.2 TX_FAULT_9:0

These 10 pins are inputs to the IXF1110. These signals are pulled to a logic Low level by the GBIC module during normal operation, which indicates no fault condition exists. If a fault is present, a logic High is received via the use of a pull-up resistor on the IXF1110 pad.

The status of each bit (one for each port) can be found in bits 19:10 of the GBIC Status Register (see Table 90, "GBIC Status Register Ports 0-9 (Addr: 0x799)" on page 144). Any change in the state of these bits causes a logic Low level on the TX_FAULT_Int output if this operation is enabled.

3.4.4.2.3 RX_LOS_9:0

These 10 pins are inputs to the IXF1110. During normal operation, these signals are pulled to a logic Low level by the GBIC module, which indicates that no Loss-of-Signal exists. If a Loss-of-Signal occurs, a logic High is received on these inputs via the use of a pull-up resistor on the IXF1110 pad.

The status of each bit (one for each port) is found in GBIC Status Register bits 29:20 (see Table 90 on page 144). Any change in the state of these bits causes a logic Low level on the RX_LOS_Int output if this operation is enabled.

3.4.4.2.4 TX_DISABLE_9:0

These 10 pins are outputs from the IXF1110. During normal operation, these signals are pulled to a logic Low level by the IXF1110, indicating that the GBIC transmitter is enabled. If the GBIC module transmitter is disabled, these signals are switched to a logic High level. On the IXF1110, these outputs are open-drain types and pulled up by the 4.7k to 10k pull-up resistor at the GBIC module. Each of these signals is controlled via GBIC Control Register bits 9:0, respectively (see Table 91 on page 144).

3.4.4.2.5 MOD_DEF_Int

MOD_DEF_Int is a single output, open-drain type signal, and is active Low. A change in state of any of the MOD_DEF_9:0 inputs causes this signal to switch Low and remain in this state until a Read of the GBIC Status Register takes place (see Table 90 on page 144). The signal then returns to an inactive state.

Note: The MOD_DEF_9:0 inputs shown in Table 90, "GBIC Status Register Ports 0-9 (Addr: 0x799)" on page 144 are synchronized with an internal system clock. This results in a delay from the time the signal is active to the register bit and/or interrupt being set.

3.4.4.2.6 Tx_FAULT_Int

TX_FAULT_Int is a single output, open-drain type signal, and is active Low. A change in state of any of the TX_FAULT_9:0 inputs causes this signal to switch Low and remain in this state until a Read of the GBIC Status Register takes place (see Table 90 on page 144). The signal then returns to an inactive state.

Note: The TX_FAULT_9:0 inputs shown in Table 90, "GBIC Status Register Ports 0-9 (Addr: 0x799)" on page 144 are synchronized with an internal system clock. This results in a delay from the time the signal is active to the register bit and/or interrupt being set.

3.4.4.2.7 RX_LOS_Int

RX_LOS_Int is a single output, open-drain type signal, and is active Low. A change in state of any of the Rx_LOS_9:0 inputs causes this signal to switch Low and remain in this state until a Read of the GBIC Status register has taken place. The signal then returns to an inactive state.

Note: The RX_LOS_9:0 inputs shown in Table 90, "GBIC Status Register Ports 0-9 (Addr: 0x799)" on page 144 are synchronized with an internal system clock. This results in a delay from the time the signal is active to the register bit and/or interrupt being set.

Note: MOD_DEF_Int, TX_FAULT_Int, and RX_LOS_Int are open-drain type outputs. With the three signals on the device, the system can decide which GBIC Status Register bits to look at to identify the interrupt condition source port. However, this is achieved at the expense of two device pins.

In systems that cannot support multiple interrupt signals (applications that do not have extra hardware pins), these three outputs can be connected to a single pull-up resistor and used as a single interrupt pin.

3.4.5 I^2C Module Configuration Interface

The I^2C interface is supported on Type 4 SFF GBIC modules. Details of the operation are found in SFF-8053, Revision 5.5, Annex D, Module Definition "4" GBIC (Serial Identification). This document details the contents of the registers and addresses accessible on a given GBIC module supporting this interface.

SFF-8053 identifies up to 512 8-bit registers that are accessible in each GBIC. The GBIC interface is Read/Write capable and supports either sequential or random access to the 8-bit parameters. The maximum clock rate of the interface is 100 kHz. All address select pins on the internal E^2PROM are tied Low to give a device address equal to zero (00h).

The specific interface in the IXF1110 supports only a subset of the full I^2C interface, and only the features required to support the GBIC modules are implemented, leading to the following support features:

- Single I^2C_CLK pin connected to all GBIC modules, and implemented to save unnecessary pin use.
- Ten per-port I^2C_DATA pins (I^2C_DATA_9:0) are required due to the GBIC module requirement that all modules must be addressed as 00h.
- Due to the single internal GBIC controller, only one GBIC module may be accessed at any one time. Fiber GBIC accesses contains a single register Read. Since these register accesses will most likely be done during power-up or discovery of a new module, these restrictions should not affect normal operation.
- The I^2C interface also supports byte write accesses to the full address range.

3.4.5.1 General Description

In the IXF1110, the entire I²C interface is controlled through separate I²C Control and Data Registers (see Table 93 on page 146). The general operation is described below.

The I²C Control Register is divided into the following sections:

- Port Address Error
- Write Protect Error bit
- No Acknowledge Error bit
- I²C Enable bit
- I²C Start Access bit
- Write Access Complete bit
- Read DataValid bit
- 4-bit Port Address Select
- Read/Write access select
- 4-bit Device ID
- 11-bit Register Address

The I²C Data Register is divided into the following sections:

- 8-bit Write Data
- 8-bit Read Data

The 4-bit Device ID field defaults to Ah, this value is compatible with standard fiber GBIC based on the Atmel Serial E²Prom family. I²C accesses to non-Atmel compatible devices will require to update this field with the appropriate value.

The 11-bit Register Address is split into two sub-fields:

- Bits [10:8] must be set to 0h to be compatible with standard fiber GBIC. Alternatively these bits can be set to 1h - 7h to permit access to seven other I²C component on the same bus.
- Bits [7:0] specify the particular location to be accessed within the device specified by the Device ID field and Register Address[10:8].

Initiating an access where the 4-bit Port Address field to a value > 9h will not generate an I²C access. Instead the Port Address Error will be set.

Initiating a write access where the Device ID field = Ah and the Register Address[10:8] = 0h will generate an I²C access. In addition the Write Protect Error bit will be set to indicate a write has been initiated to the write protected Fiber GBIC.

3.4.5.1.1 Read Access Operation Example

Read the data stored at Port 5 (Port Address Select), Register 000h (Data Address Select).

1. Program the "I2C Data Register Ports 9-0 Register (Addr: 0x79C)" with the following information:
   a. Enable I^2C Block by setting bit 25 to '1'.
   b. Set the port to be accessed by setting bits [19:16] to 5h.
   c. Select a READ access by setting bit 15 to '1'.
   d. Set the Device ID, bits [14:11] to be Ah (Atmel compatible).
   e. Set the 11-bit Register Address, bits [10:0] to 000h.
   f. Initiate the I^2C transfer by setting bit 24 to '1'.

   All other bits in this register should be written with the value '0'.

   This data is written into the I^2C Control Register in a single cycle via the CPU interface.
2. When this register is written and the I^2C Start bit is at a Logic 1, the I^2C access state machine examines the Port Address Select and enables the I^2C_DATA_0:9 output for the selected port.
3. The state machine uses the data in the Device ID and Register Address fields to build the data frame to be sent to the GBIC.
4. The I^2C DATA_READ_FSM internal state machine takes over the task of transferring the actual data between the IXF1110 and the selected GBIC (refer to the details in Section 3.4.5.2, "I2C Protocol Specifics" on page 56).
5. The I^2C DATA_READ_FSM internal state machine places the received data into the Read_Data field, bits [7:0] of the I^2C Data Register, and sets the Read Data Valid bit, bit 20 of the I^2C Control Register to '1' to signify that the Read data is valid.
6. The data is read through the CPU interface. The CPU must poll the Read Data Valid bit until it is set to '1. Only once this bit is set, it is safe to read the data in the I^2C Data Register.

3.4.5.1.2 Write Access Operation Example

Write the data to Port 9 (Port Address Select), Register 0FFh (Data Address Select).

1. Program the "I2C Data Register Ports 9-0 Register (Addr: 0x79C)" with the following information:
   a. Enable I^2C Block by setting bit 25 to '1'.
   b. Set the port to be accessed by setting bits [19:16] to 5h.
   c. Select a WRITE access by setting bit 15 to '0'.
   d. Set the Device ID, bits [14:11] to be Ah (Atmel compatible).
   e. Set the 11-bit Register Address, bits [10:0] to 0FFh.
   f. Initiate the I^2C transfer by setting bit 24 to '1'.

   All other bits in this register should be written with the value '0'.

   This data is written into the I^2C Control Register in a single cycle via the CPU interface.
2. When this register is written and the I^2C Start bit is at a Logic 1, the I^2C access state machine examines the Port Address Select and enables the I^2C_DATA_0:9 output for the selected port.
3. The state machine uses the data in the Device ID and Register Address fields to build the data frame to be sent to the GBIC.
4. The I^2C DATA_WRITE_FSM internal state machine takes over the task of transferring the actual data between the IXF1110 and the selected GBIC (refer to the details in Section 3.4.5.2, "I2C Protocol Specifics" on page 56).
5. The I^2C DATA_WRITE_FSM internal state machine uses the data from the Write_Data field, bits [23:16] of the I^2C Data Register, and sets the Write_Complete bit, bit 22 of the I^2C Control Register to '1' to signify that the Write Access is complete.
6. The data is written through the CPU interface. The CPU must poll the Write_Complete bit until it is set to '1. Only once this bit is set, it is safe to request a new access.

Note: Only one GBIC I^2C access sequence can be run at any given time. If a second Write is carried out to the I^2C Control Register before a result is returned for the previous Write, the data for the first Write is lost. To ensure no data is lost, make sure Write complete = 1 before starting the next Write sequence.

3.4.5.2 I^2C Protocol Specifics

This section describes the I^2C protocol behavior supported by the IXF1110, which is controlled by an internal state machine. Specific protocol states are defined below, with an additional description of the hardware pins used on the interface.

The Serial Clock Line (I^2C_CLK) is an IXF1110 output. The serial data is synchronous with this clock and is driven off the rising edge by the IXF1110 and off the falling edge by the GBIC module. The IXF1110 has only one I^2C_CLK line that drives all of the GBIC modules. I^2C_CLK runs continuously when enabled (I^2C Enable = 01h0).

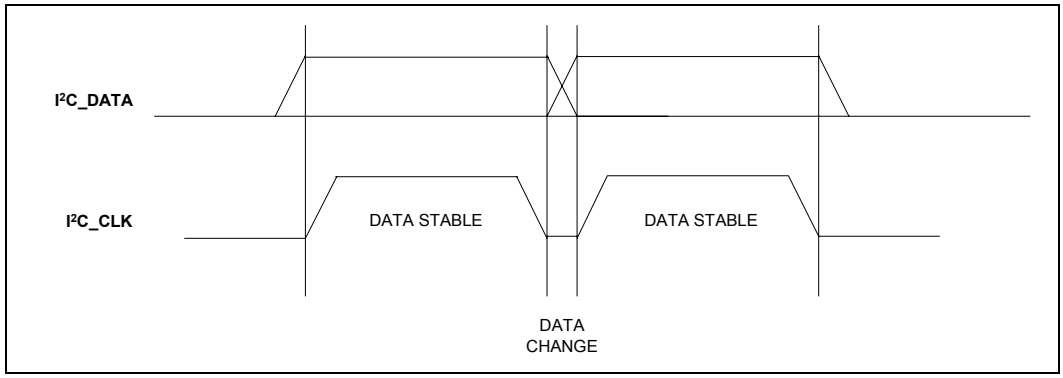
The Serial Data (I^2C_DATA_0:9) pins (one per port) are bi-directional for serial data transfer, and are open drain.

3.4.5.3 Port Protocol Operation

3.4.5.4 Clock and Data Transitions

The I²C_DATA is normally pulled High with an extra device. Data on the I²C_DATA pin changes only during the I²C_CLK Low time periods (see Figure 16). Data changes during I²C_CLK High periods indicate a start or stop condition.

Figure 16. Data Validity Timing Diagram



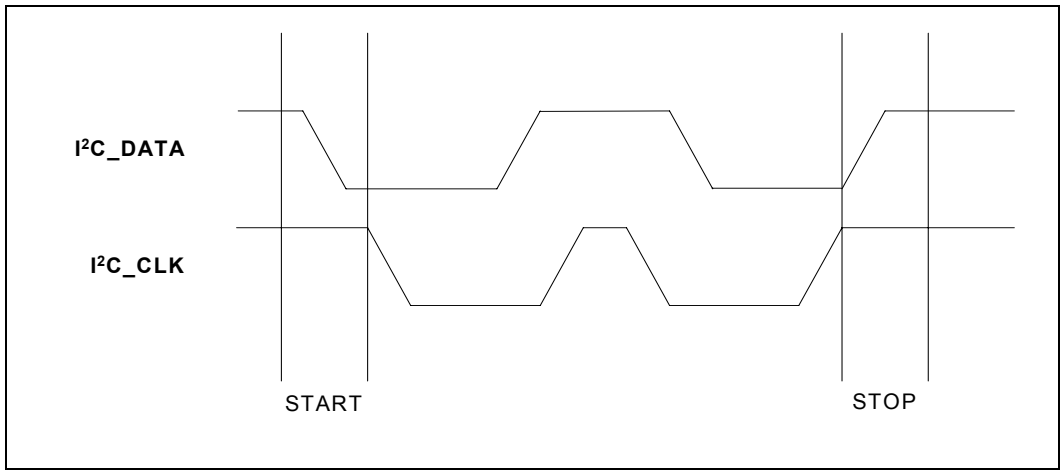
3.4.5.4.1 Start Condition

A High-to-Low transition of I²C_DATA, with I²C_CLK High, is a start condition that must precede any other command (see Figure 17).

3.4.5.4.2 Stop Condition

A Low-to-High transition of the I²C_DATA with I²C_CLK High is a stop condition. After a Read sequence, the stop command places the E²PROM in the GBIC in a standby power mode (see Figure 17).

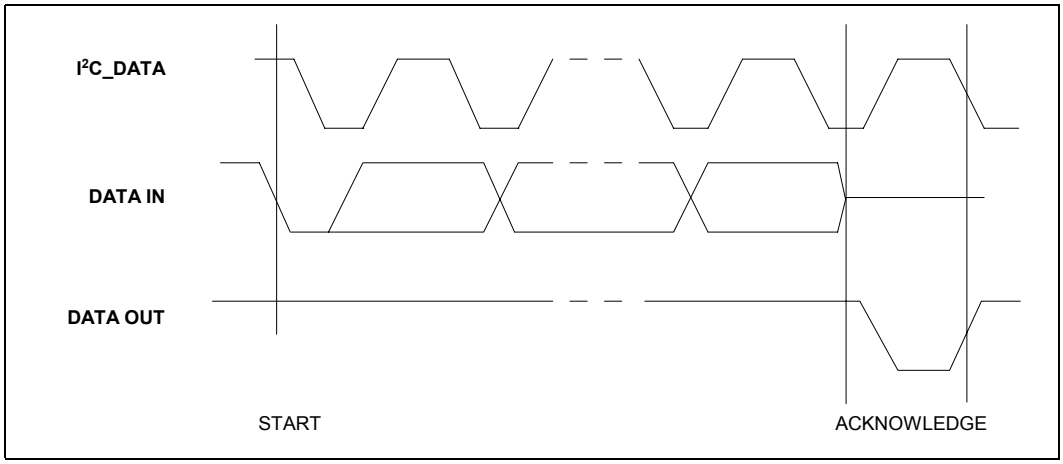
Figure 17. Start and Stop Definition Timing Diagram



3.4.5.4.3 Acknowledge

All addresses and data words are serially transmitted to and from the GBIC in 8-bit words. The GBIC E^{2}PROM sends a zero to acknowledge that it has received each word, which happens during the ninth clock cycle (see Figure 18).

Figure 18. Acknowledge Timing Diagram



3.4.5.4.4 Memory Reset

After an interruption in protocol, power loss, or system reset, any two-wire GBIC can be reset by following three steps:

1. Clock up to 9 cycles
2. Wait for I^{2}C_DATA High in each cycle while I^{2}C_CLK is High
3. Initiate a start condition

Memory reset on this device is defined as follows: Always add a stop condition following the start as there is no clean finish to end the reset of the memory with a start condition after completing steps one through three. This ensures a clean protocol termination if there is no more data to transfer at the end of the reset cycle.

3.4.5.4.5 Device Addressing

All E^{2}PROMs in GBIC devices require an 8-bit device address word following a start condition to enable the chip to read or write. The device address word consists of a mandatory one, zero sequence for the four most significant bits. This is common to all devices. The next 3 bits are the A2, A1 and A0 device address bits that are tied to zero in a GBIC module. The eighth bit of the device address is the Read/Write operation select bit. A Read operation is initiated if this bit is High and a Write operation is initiated if this bit is Low.

Upon comparison of the device address, the GBIC module outputs a zero. If a comparison is not made, the GBIC E^{2}PROM returns to a standby state.

When not accessing the GBIC E^{2}PROM, the device address or device ID is completely programmable for maximum flexibility.

3.4.5.4.6 Random Read Operation

A random Read requires a “dummy” Byte/Write sequence to load the data word address. The following describes how to achieve the “dummy” Write:

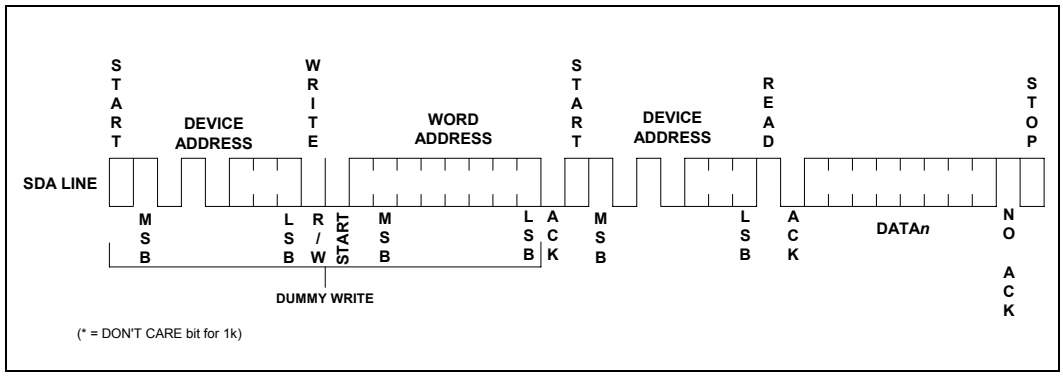
- The IXF1110 generates a start condition.
- The IXF1110 sends a device address word with the Read/Write bit cleared to Low, signaling a Write operation.
- The GBIC acknowledges receipt of the device address word.
- The IXF1110 sends the data word address, which is again acknowledged by the GBIC.
- The IXF1110 generates another start condition.

This completes the “dummy” Write and sets the GBIC E^2PROM pointers to the desired location.

The following describes how the IXF1110 initiates a current address Read:

- The IXF1110 sends a device address with the Read/Write bit set High
- The GBIC acknowledges the device address and serially clocks out the data word.
- The IXF1110 does not respond with a zero but generates a stop condition (see Figure 19).

Figure 19. Random Read



Timing diagrams and tables can be found in Section 5.0, “Test Specifications” on page 77.

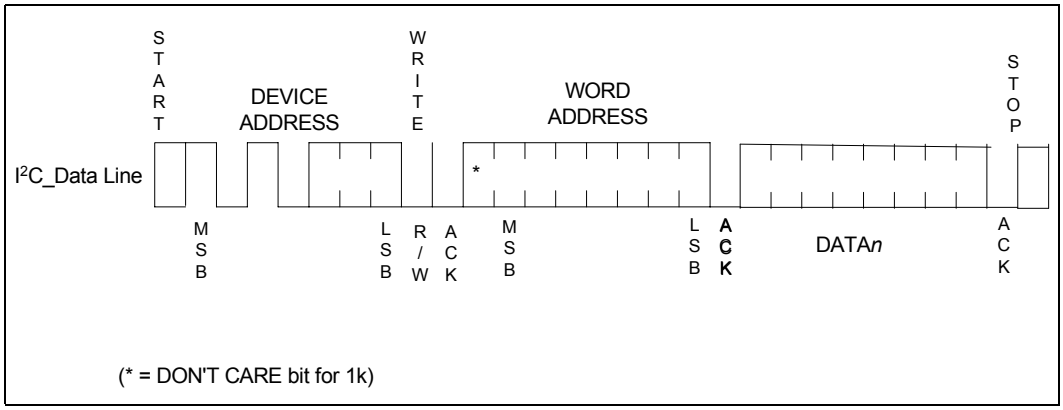
3.4.5.4.7 Byte Write Operation

The following describes how to achieve the byte write operation:

- The IXF1110 generates a start condition.
- The IXF1110 sends a device address word with the Read/Write bit cleared to Low, signaling a Write operation.
- The GBIC acknowledges receipt of the device address word.
- The IXF1110 sends the data word address.
- The GBIC acknowledges receipt of the data word address.
- The IXF1110 sends the data byte to be written.
- The GBIC acknowledges the data word.

- The IXF1110 generates a stop condition (see Figure 20).

Figure 20. Byte Write



3.4.5.5 AC Timing Characteristics

Table 35, "I2C AC Timing Characteristics" on page 90, Figure 39, "I2C Bus Timing Diagram" on page 90, and Figure 40, "I2C Write Cycle Diagram" on page 90 provide the AC timing characteristics of the GBIC interface.

3.5 LED Interface

3.5.1 Introduction

The IXF1110 uses a serial interface consisting of three signals to provide LED data to some form of external driver. This interface provides the data for 30 separate direct drive LEDs and allows three LEDs per MAC port.

There are two modes of operation, each with its own separate LED decode mapping. Modes of operation and LEDs are detailed in "Modes of Operation".

3.5.2 Modes of Operation

Mode selection is accomplished by using the LED_SEL_MODE bit. This bit is globally selected and controls the operation of all ports (see Table 68, "LED Control Register (Addr: 0x509)" on page 120).

There are two modes of operation:

Mode 0: (LED_SEL_MODE = 0 [Default]): This mode selects operations compatible with the SGS Thompson M5450 Led Display Driver Device. This device converts the serial data stream, output by the IXF1110, into 30 direct-drive LED outputs.

Mode 1: (LED_SEL_MODE = 1): This mode is used with standard TTL (74LS595) or HCMOS (74HC595) octal shift registers with latches, providing the most general and cost-effective implementation of the serial data stream conversion.

In addition to these physical modes of operation, there are two types of specific LED data decodes available. This option is a global selection and controls the operation of all ports (see Table 68, "LED Control Register (Addr: 0x509)" on page 120).

3.5.3 LED Interface Signal Description

The IXF1110 LED interface consists of three output signal pins that are 2.5 V CMOS level pads. Table 13 provides LED signal names, pin numbers and descriptions.

Table 13. LED Pin Descriptions

Pin Name	Pin #	Pin Description
LED_CLK	A20	LED_CLK: This signal is an output that provides a continuous clock synchronous to the serial data stream output on the LED_DATA pin. This clock has a maximum speed of 0.5 MHz. The behavior of this signal remains constant in all modes of operation.
LED_DATA	A19	LED_DATA: This signal provides the data, in various formats, as a serial bit stream. The data must be valid on the rising edge of the LED_CLK signal. In Mode 0, the data presented on this pin is TRUE (Logic 1 = High). In Mode 1, the data presented on this pin is INVERTED (Logic 1 = Low).
LED_LATCH	K18	LED_LATCH: This is an output pin and the signal is used only in Mode 1 as the Latch enable for the shift register chain. This signal is not used in Mode 0, and should be left unconnected.

3.5.4 Mode 0: Detailed Operation

Note: Please refer to the SGS Thompson M5450 datasheet for device-operation information.

The operation of the LED Interface in Mode 0 is based on a 36-bit counter loop. The data for each LED is placed in turn on the serial data line and clocked out by the LED_CLK. Figure 21 on page 61 shows the basic timing relationship and relative positioning in the data stream of each bit.

Figure 21 shows the 36 clocks that are output on the LED_CLK pin. The data changes on the falling edge of the clock and is valid for almost the entire clock cycle. This ensures that the data is valid during the rising edge of the LED_CLK, which is used to clock the data into the M5450 device.The actual data shown in Figure 21 consists of a chain of 36 bits only, 30 of which are valid LED DATA. The 36-bit data chain is built up as follows:

Figure 21. Mode 0 Timing Diagram

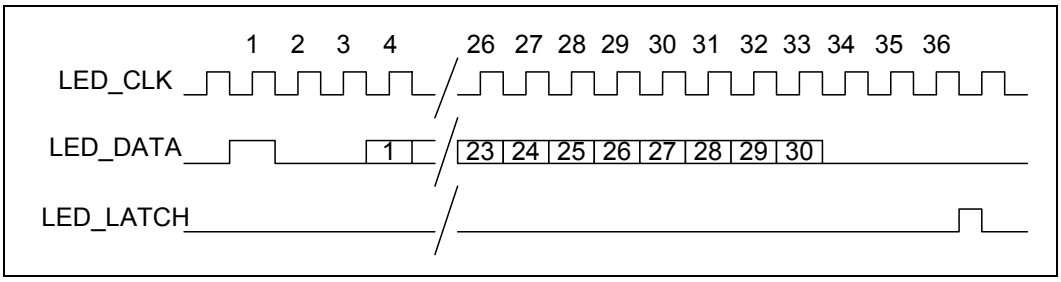


Table 14. Mode 0 Clock Cycle to Data Bit Relationship

LED_CLK CYCLE	LED_DATA NAME	LED_DATA DESCRIPTION
1	START BIT	This bit is used to synchronize the M5450 device to expect 35 bits of data to follow.
2:3	PAD BITS	These bits are used only as fillers in the data stream to extend the length from the actual 30 bit LED DATA to the required 36-bit frame length. These bits should always be a Logic 0.
4:33	LED DATA 1-30	These bits are the actual data transmitted to the M5450 device. The decode for each individual bit in each mode is defined in Table 13 on page 61. The data is TRUE. Logic 1(LED ON) = High
34:36	PAD BITS	These bits are used as fillers in the data stream to extend the length from the actual 30-bit LED DATA to the required 36-bit frame length. These bits should always be a Logic 0.

When implemented on a board with the M5450 device, the LED DATA bit 1 appears on output bit 3 of the M5450 and the LED DATA bit 2 appears on output bit 4, etc. This means that output bits 1, 2, 3, 34, and 35 will never have valid data and should not be used.

3.5.5 Mode 1: Detailed Operation

Note: Please refer to manufacturers' 74LS/HC595 datasheet for information on device operation.

The operation of the LED Interface in Mode 1 is again based on a 36-bit counter loop. The data for each LED is placed in turn on the serial data line and clocked out by the LED_CLK. Figure 22 on page 63 shows the basic timing relationship and relative positioning in the data stream of each bit.

Figure 22 shows the 36 clocks that are output on the LED_CLK pin. The data changes on the falling edge of the clock and is valid for almost the entire clock cycle. This ensures that the data is valid during the rising edge of the LED_CLK, which is used to clock the data into the Shift Register chain devices.

The LED_LATCH signal is required in Mode 1, and is used to latch the data shifted into the shift register chain into the output latches of the 74HC595 device. As seen in Figure 22, the LED_LATCH signal is active High during the Low period on the 36th LED_CLK cycle. This avoids any possibility of trying to latch data as it is shifting through the register.

When this operation mode is implemented on a board with a shift register chain containing three 74HC595 devices, the LED DATA bit 1 is output on Shift Register bit 1, and so on up the chain. Only Shift Register bits 31 and 32 do not contain valid data. The actual data shown in Figure 22 consists of a 36-bit chain, of which 30 bits are valid LED DATA. The 36-bit data chain is built up as follows:

Note: The LED_DATA signal is now inverted from the state in Mode 0.

Figure 22. Mode 1 Timing Diagram

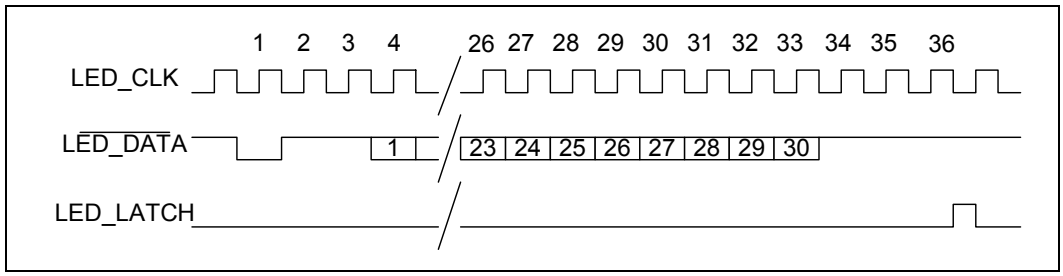


Table 15. Mode 1 Clock Cycle to Data Bit Relationship

LED_CLK CYCLE	LED_DATA NAME	LED_DATA DESCRIPTION
1	START BIT	This bit has no meaning in Mode 1 operation and is shifted out of the 32-stage shift register chain before the LED_LATCH signal is asserted.
2:3	PAD BITS	These bits have no meaning in Mode 1 operation and are shifted out of the 32-stage shift register chain before the LED_LATCH signal is asserted.
4:33	LED DATA 1-30	These bits are the actual data to be transmitted to the 32-stage shift register chain. The decode for each bit in each mode is defined in Table 15 on page 63. The data is INVERTED. Logic 1 (LED ON) = Low.
34:36	PAD BITS	These bits have no meaning in Mode 1 operation and are latched into positions 31 and 32 in the shift register chain. These bits are not considered as valid data and should be ignored. They should always be a Logic 0 = High.

3.5.6 Power-On, Reset, and Initialization

The LED interface is disabled at power-on or reset. The system software controller must enable the LED interface. The internal state machines and output pins are held in reset until the full IXF1110 device configuration is completed. This is done by setting the LED_ENABLE bit to a logic 1 (see Table 68, “LED Control Register (Addr: 0x509)” on page 120). The power-on default for this bit is Logic 0.

3.5.7 LED Data Decodes

Table 16 shows the data decode of the data for the IXF1110.

Table 16. LED Data Decodes

LED_DATA#	MACPORT #	IXF1110 Designation
1	0	Rx LED - Amber
2		Rx LED - Green
3		Tx LED - Green
4	1	Rx LED - Amber
5		Rx LED - Green
6		Tx LED - Green
7	2	Rx LED - Amber
8		Rx LED - Green
9		Tx LED - Green
10	3	Rx LED - Amber
11		Rx LED - Green
12		Tx LED - Green
13	4	Rx LED - Amber
14		Rx LED - Green
15		Tx LED - Green
16	5	Rx LED - Amber
17		Rx LED - Green
18		Tx LED - Green
19	6	Rx LED - Amber
20		Rx LED - Green
21		Tx LED - Green
22	7	Rx LED - Amber
23		Rx LED - Green
24		Tx LED - Green
25	8	Rx LED - Amber
26		Rx LED - Green
27		Tx LED - Green
28	9	Rx LED - Amber
29		Rx LED - Green
30		Tx LED - Green

3.5.7.1 LED Signaling Behavior

Operation in each mode for the decoded LED data in Table 16 is detailed in Table 17.

3.5.7.1.1 IXF1110 LED Behavior

Table 17. IXF1110 LED Behavior

Type	Status	Description
RxLED Amber	Off	Port has no link synchronization or remote fault error
	On	Port has a link synchronization error or no optical signal
	Blinking	Port has remote fault
RxLED Green	Off	Port is not enabled
	On	Port has link and is enabled
	Blinking	Port is receiving data
TxLED Green	Off	Port is not transmitting data
	Blinking	Port is transmitting data

3.6 CPU Interface

3.6.1 General Description

The CPU Interface block provides access to registers and statistics in the IXF1110. The interface is asynchronous externally and operates within the 125 MHz clock domain internally. The interface provides access to the following registers:

- MAC Control
- MAC RX Statistics
- MAC TX Statistics
- Global Status and Configuration
- RX Block
- TX Block
- SPI4-2 Block
- SerDes Block
- GBIC Block

3.6.2 Functional Description

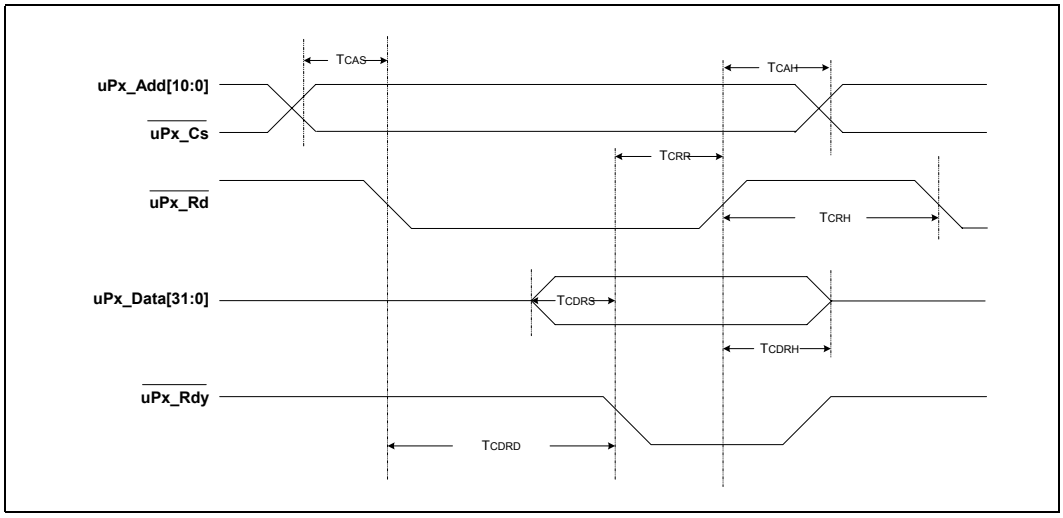
3.6.2.1 Read Access

Read access involves the following:

- Detect assertion of asynchronous Read control signal and latch address
- Generate internal Read strobe
- Drive valid data onto processor bus
- Assert asynchronous-ready signal for required length of time

Figure 23 provides the timing of the asynchronous interface for Read access.

Figure 23. Read Timing Diagram - Asynchronous Interface



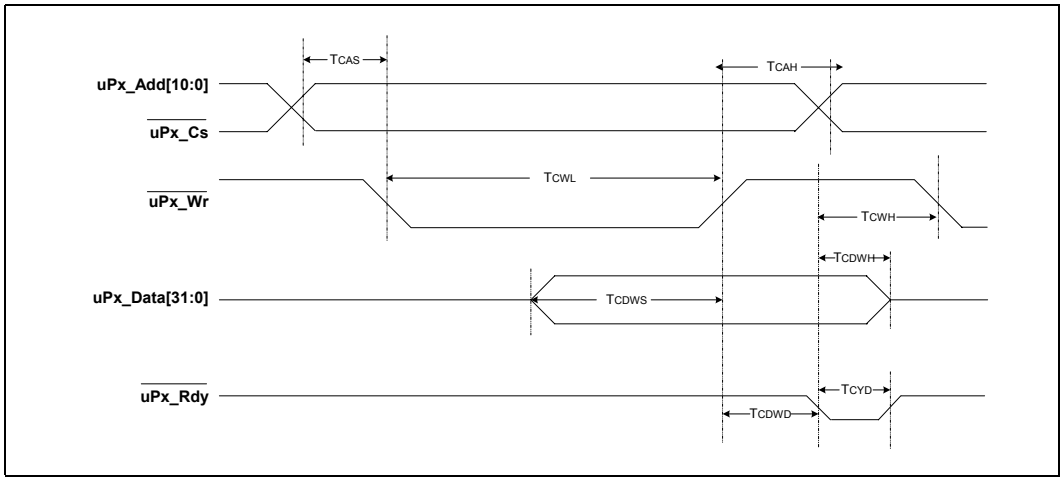
3.6.2.2 Write Access

The Write process involves the following:

- Detect assertion of asynchronous Write control signal and latch address
- Detect de-assertion of asynchronous Write control signal and latch data
- Generate internal Write strobe
- Assert asynchronous Ready signal for required length of time

Figure 24 illustrates the timing of the asynchronous interface for Write access.

Figure 24. Write Timing Diagram - Asynchronous Interface



3.6.3 Endian

The Endian of the CPU interface may be changed to allow connection of various CPUs to the IXF1110. The Endian selection is determined by setting the Endian bit in the CPU Interface Register (see Table 67 on page 120).

3.7 Clocks

The IXF1110 device has system interface reference clocks, SPI4-2 data path input and output clocks, a JTAG input clock, a GBIC output clock, and an LED output clock. This section details the unique clock source requirements.

3.7.1 System Interface Reference Clocks

There are two system interface clocks required by the IXF1110:

3.7.1.1 CLK125

The system interface clock, which supplies the clock to the majority of the internal circuitry, is the 125 MHz clock. The source of this clock must meet the following specifications:

- 2.5 V CMOS drive
- +/- 50 ppm
- Maximum duty cycle distortion 40/60

3.7.1.2 CLK50

The other system interface clock supplies the clock source to the SPI4-2 receive circuitry. The source of this clock must meet the following specifications:

- 2.5 V CMOS drive
- 1/8 frequency of the SPI4-2 data path clock (RDCLK+/-)
- Maximum duty cycle distortion 45/55
- Maximum peak-to-peak jitter (low and high frequency) of 125 pS
- Range = 40 Mhz to 50 MHz

3.7.2 SPI4-2 Receive and Transmit Data Path Clocks

The SPI4-2 data path clocks are compliant with the OIF 2000.88.4 Specification.

The IXF1110 has the following requirements on the transmit data path:

- 2.5 V LVDS drive
- Maximum duty cycle distortion 45/55
- Maximum peak-to-peak jitter (low and high frequency) of 125 pS
- Stable (frequency and level) when reset is removed or when sourced, whichever happens last

- TSCLK frequency is one-quarter TDCLK frequency

The IXF1110 meets the following specifications on the receive data path:

- 2.5 V LVDS drive
- Maximum duty cycle distortion 45/55
- Maximum peak-to-peak jitter (low and high frequency) of 125 pS
- Stable when sourced

3.7.3 JTAG Clock

The IXF1110 supports JTAG. The source of this clock must meet the following specifications:

- 2.5 V CMOS drive
- Maximum clock frequency 11 MHz
- Maximum duty cycle distortion 40/60

3.7.4 GBIC Clock

The IXF1110 device supports a single output GBIC clock to support all 10 GBIC interfaces. The IXF1110 meets the following specifications for this clock:

- 2.5 V CMOS drive
- Maximum clock frequency of 100 MHz

3.7.5 LED Clock

The IXF1110 supports a serial LED data stream. This interface implements a 2.5 V CMOS output clock with a maximum frequency of 720 kHz.

The IXF1110 supports a serial LED data stream. The IXF1110 meets the following specifications for this clock:

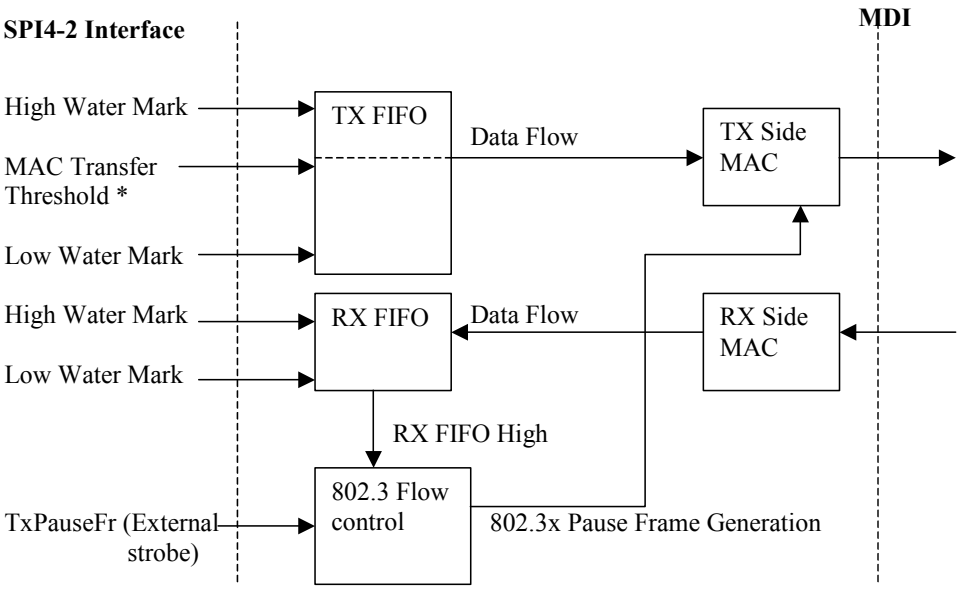
- 2.5 V CMOS drive
- Maximum frequency of 720 kHz
- Maximum duty cycle distortion: 50/50

4.0 Applications

4.1 TX and RX FIFO Operation

The Intel® IXF1110 packet buffering is comprised of individual port FIFOs and system-interface FIFOs. Figure 25 illustrates the interaction of these FIFOs.

Figure 25. Packet Buffering FIFO



1. Note: The MAC Transfer Threshold determines when the transmit data is transferred from the TX FIFO to the TX side of the MAC. Once the data has been sent from the TX FIFO to the MAC, it will be transmitted to the PHY and cannot be flow controlled from the link partner.

4.1.1 TX FIFO

The IXF1110 TX FIFOs are implemented with 4.5 KB for each channel. This provides enough space for at least one maximum size packet per-port storage and ensures that no under-run conditions occur, assuming that the sending device can supply data at the required data rate.

The MAC threshold parameter, which is user programmable, determines when data is transmitted out of the MAC. This parameter is configurable for specific block sizes and the user must ensure that an under-run does not occur. The threshold must be set to a value that exceeds the programmed MaxBurst1 parameter. This method of operation eliminates the possibility of under-run, except when the controlling switch device fails.

4.1.2 RX FIFO

The IXF1110 RX FIFOs are provisioned so that each port has its own 17.0 KB memory space. This is enough memory to ensure against an over-run on any channel while transferring normal Ethernet frame-size data.

The FIFOs can be configured to automatically generate Pause control frames to initiate the following:

- Halt the link partner when the High watermark is reached
- Restart the link partner when the data stored in the FIFO falls below the low watermark

4.2 Reset and Initialization

When powering up the IXF1110, the hardware reset signal ($\overline{\text{Sys\_Res}}$) should be held active Low for a minimum of 100 ns after all of the power rails have fully stabilized to their nominal values and the input clocks have reached their nominal frequency (TDCLK = 400 MHz, CLK125 = 125 MHz, and CLK50 = 50 MHz).

Note: In systems where the $\overline{\text{Sys\_Res}}$ pin is driven from a single board-wide reset signal, the switch or network processor only comes out of reset at the same time as the IXF1110, or possibly later. This means the TDCLK will not be stable when the $\overline{\text{Sys\_Res}}$ pin is released. A built-in feature in the IXF1110 reactivates the internal reset once TDCLK is applied. Ensure that the switch or network processor does not output TDCLK until it is stable and has reached its nominal operating frequency.

The IXF1110 extends this hardware reset internally to ensure synchronization of all internal blocks within the system. The internal reset is extended for a minimum of 4.11 ms after all clocks are stable.

The device is correctly initialized at this point and ready for use. Clocks start to appear at the relevant device ports and the SPI4-2 interface begins to source a training pattern on the receive side while waiting for a training pattern on the transmit side. The SPI4-2 interface synchronizes with the connected switch or network processor per the SPI4-2 Specification.

The CPU accesses can begin to configure the device for any existing user preferences desired. By default, all ports on the IXF1110 are enabled after power-up. The device is ready for use at this time if the default settings are to be used. Otherwise, access the required registers via the CPU interface and configure the control registers to the required settings.

4.3 Optical Module Connections to the IXF1110

4.3.1 SFP-to-IXF1110 Connection

The IXF1110 SerDes and GBIC interfaces allow system designers to connect the IXF1110 to various optical transceivers. When using Small Form Factor Pluggable (SFP) optical transceivers to connect to the IXF1110, all SerDes and GBIC status pins are used. Use Figure 26 and Table 18 to connect an SFP to the IXF1110.

Figure 26. SFP-to-IXF1110 Connection Diagram

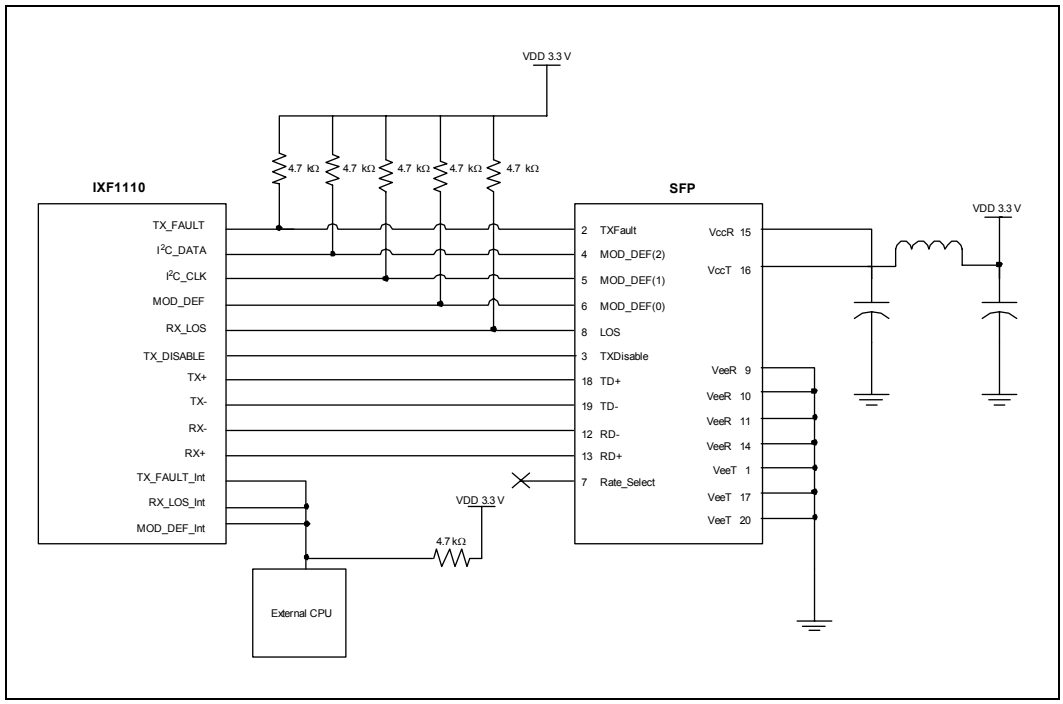


Table 18. SFP-to-IXF1110 Connection

SFP Pin #	SFP Pin Name	IXF1110 Pin # 0:9	IXF1110 Pin Name	Description
1	VeeT	NA	NA	Connect to ground.
2	TxFault	M24, V23, Y17, R15, W14, W11, W9, AC5, P8, L2	TX_FAULT_[0:9]	Use an external 4.7 kΩ pull-up resistor to 3.3 V.
3	TxDisable	K22, M22, AC22, U18, U14, AA18, U9, AA9, V7, L4	TX_DISABLE_[0:9]	SFP module has internal pull-up.
4	MOD_DEF (2)	G22, G23, J24, F22, E23, H24, G20, E22, G24, F24	I^2C_DATA_[0:9]	Use an external 4.7 kΩ pull-up resistor to 3.3 V.
5	MOD_DEF (1)	L19	I^2C_CLK	Use an external 4.7 kΩ pull-up resistor to 3.3 V.
6	MOD_DEF (0)	N24, Y21, AA16, M20, AC14, U11, T4, AB2, R7, L1	MOD_DEF_[0:9]	Use an external 4.7 kΩ pull-up resistor to 3.3 V.
7	Rate Select	NA	NA	Leave floating.
8	LOS	L22, V17, AD18, R12, AB15, V12, Y9, AC3, T2, P2	RX_LOS_[0:9]	Use an external 4.7 kΩ pull-up resistor to 3.3 V.
9	VeeR	NA	NA	Connect to ground.
10	VeeR	NA	NA	Connect to ground.
11	VeeR	NA	NA	Connect to ground.

Table 18. SFP-to-IXF1110 Connection (Continued)

SFP Pin #	SFP Pin Name	IXF1110 Pin # 0:9	IXF1110 Pin Name	Description
12	RD-	U22, U20, T24, V24, AB14, AD14, AC16, AD15, V4, Y5	RX-_[0:9]	The IXF1110 has a 100 Ω differential termination on the chip that requires it to be AC-coupled. AC-coupling is done inside the SFP module and is not required on the host board.
13	RD+	T22, T20, U24, W24, AB13, AD13, AB16, AD16, V5, Y6	RX+_[0:9]	
14	VeeR	NA	NA	Connect to ground.
15	VccR	NA	NA	Connect to filtered 3.3 V.
16	VccT	NA	NA	Connect to filtered 3.3 V.
17	VeeT	NA	NA	Connect to ground.
18	TD+	V20, Y19, V22, Y23, AB12, AD12, AB9, AD9, T3, T5	TX+_[0:9]	These pins are the differential transmitter inputs. They are AC-coupled differential lines with 100 Ω differential termination inside the SFP module. The AC-coupling is done inside the SFP module and is not required on the host board.
19	TD-	V21, Y20, W22, Y22, AB11, AD11, AC9, AD10, U3, U5	TX-_[0:9]	
20	VeeT	NA	NA	Connect to ground.
N/A	N/A	B11	TX_FAULT_Int	Connect to Interrupt Service Routine. Use an external 4.7 kΩ pull-up resistor to 3.3 V.
N/A	N/A	B14	RX_LOS_Int	Connect to Interrupt Service Routine. Use an external 4.7 kΩ pull-up resistor to 3.3 V.
N/A	N/A	G15	MOD_DEF_Int	Connect to Interrupt Service Routine. Use an external 4.7 kΩ pull-up resistor to 3.3 V.

4.3.2 SFF-to-IXF1110 Connection

Use Figure 27 and Table 19 to connect a Small Form Factor (SFF) optical transceiver to the IXF1110.

Figure 27. SFF-to-IXF1110 Connection Diagram

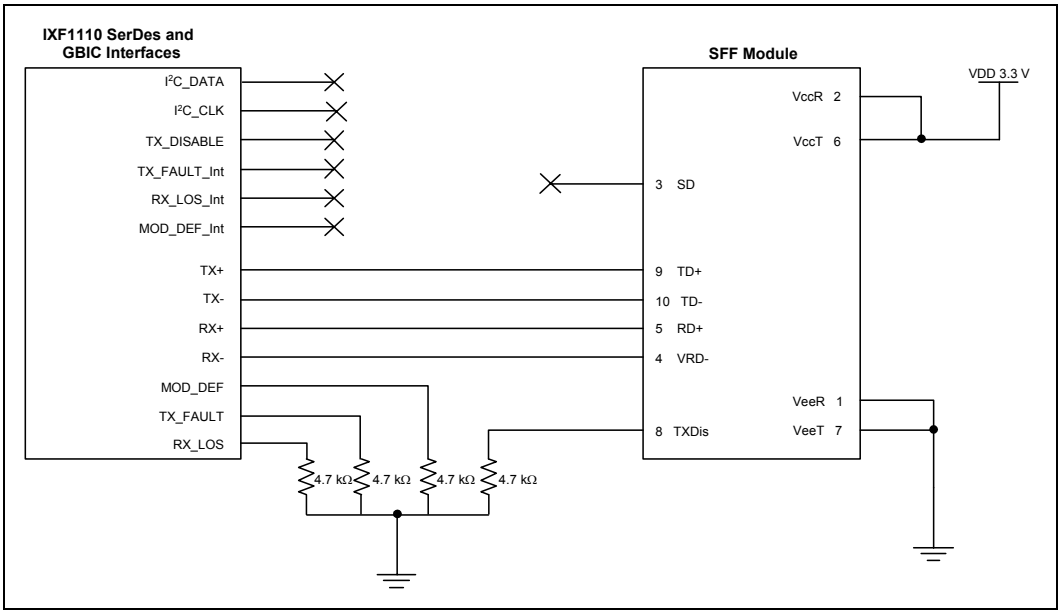


Table 19. SFF-to-IXF1110 Connection

SFF Pin #	SFF Pin Name	IXF1110 Pin # 0:9	IXF1110 Pin Name	Description
1	VeeT	NA	NA	Connect to ground.
2	Vccr	NA	NA	Connect to 3.3 V.
3	SD	L1, R7,AB2, T4, U11, AC14, M20, AA16, Y21, N24	MOD_DEF[0:9]	Need to invert SD or force the IXF1110 to be permanently enabled by connecting MOD_DEF[0:9] directly to ground.
4	RD-	Y5, V4, AD15, AC16, AD14, AB14, V24, T24, U20, U22	RX -_[0:9]	The IXF1110 has a 100 Ω differential termination on the chip and requires AC-coupling.
5	RD+	Y6, V5, AD16, AB16, AD13, AB13, W24, U24, T20, T22	RX +_[0:9]	
6	VCCT	NA	NA	Connect to 3.3 V.
7	VEET	NA	NA	Connect to ground.
8	TxDIS	L22, V17, AD18, R12, AB15, V12, Y9, AC3, T2, P2	TX_DISABLE[0:9]	Need to invert TX_DISABLE or force SFF to be permanently enabled by connecting TxDIS directly to ground.

Table 19. SFF-to-IXF1110 Connection (Continued)

SFF Pin #	SFF Pin Name	IXF1110 Pin # 0:9	IXF1110 Pin Name	Description
9	TD+	T5, T3, AD9, AB9, AD12, AB12, Y23, V22, Y19, V20	TX +_[0:9]	The SFF has a 100 Ω differential termination inside the module. The IXF1110 requires these to be AC-coupled.
10	TD-	U5, U3, AD10, AC9,AD11, AB11, Y22, W22, Y20, V21	TX -_[0:9]	
Various	MS	N/A	N/A	Chassis ground connection (may vary from manufacturer to manufacturer).
N/A	N/A	M24, V23, Y17, R15, W14, W11, W9, AC5, P8, L2	TX_FAULT[0:9]	Use external 4.7 kΩ pull-down to ground to ensure proper operation.
N/A	N/A	L22, V17, AD18, R12, AB15, V12, Y9, AC3, T2, P2	RX_LOS_[0:9]	Use external 4.7 kΩ pull-down to ground to ensure proper operation.
N/A	N/A	G22, G23, J24, F22, E23, H24, G20, E22, G24, F24	I^2C_DATA_[0:9]	Leave as no-connect.
N/A	N/A	L19	I^2C_CLK	Leave as no-connect.
N/A	N/A	B11	TX_FAULT_Int	Leave as no-connect.
N/A	N/A	B14	RX_LOS_Int	Leave as no-connect.
N/A	N/A	G15	MOD_DEF_Int	Leave as no-connect.

4.3.3 1 x 9-to-IXF1110 Connection

Use Figure 28 and Table 20 to connect a 1 x 9 optical transceiver to the IXF1110.

Figure 28. 1 x 9-to-IXF1110 Connection

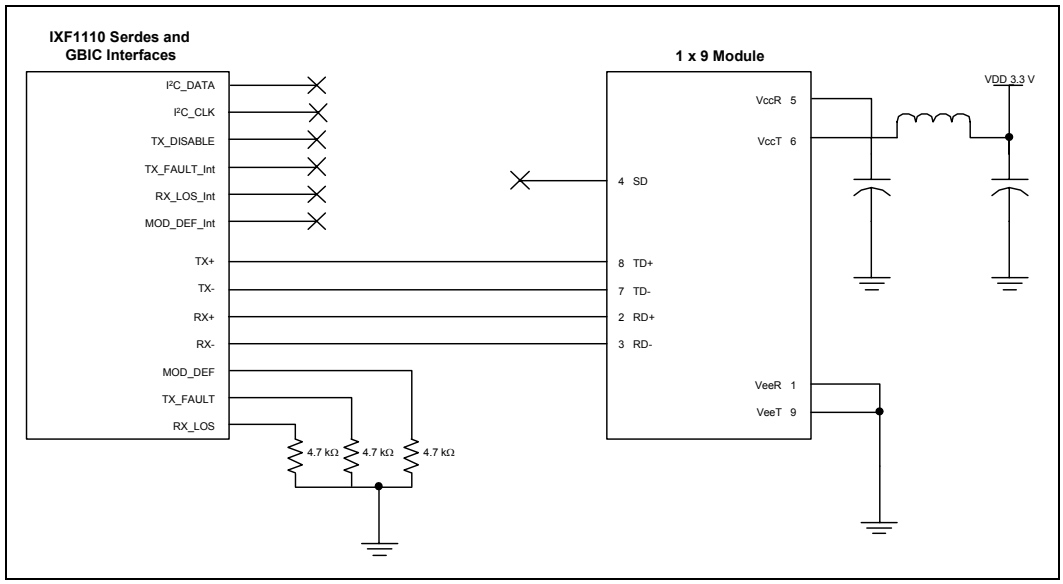


Table 20. 1 x 9-to-IXF1110 Connection

1 x 9 Pin #	1x9 Pin Name	IXF1110 Pin # 0:9	IXF1110 Pin Name	Description
1	VeeR	NA	NA	Connect to ground.
2	RD+	Y6, V5, AD16, AB16,AD13, AB13, W24, U24, T20, T22	RX +_[0:9]	The IXF1110 has a 100 Ω differential termination on the chip and requires AC-coupling.
3	RD-	Y5, V4, AD15, AC16, AD14, AB14, V24, T24, U20, U22	RX -_[0:9]	
4	SD	L1, R7, AB2, T4, U11, AC14, M20, AA16, Y21, N24	MOD_DEF[0:9]	Need to invert SD or force the IXF1110 to be permanently enabled by connecting MOD_DEF[0:9] directly to ground.
5	VccR	NA	NA	Connect to filtered 3.3 V.
6	VccT	NA	NA	Connect to filtered 3.3 V.
7	TD-	U5, U3, AD10, AC9, AD11, AB11, Y22, W22, Y20, V21	TX -_[0:9]	The IXF1110 requires a 100 Ω termination and for these lines to be AC-coupled.
8	TD+	T5, T3, AD9, AB9, AD12, AB12, Y23, V22, Y19, V20	TX +_[0:9]	
9	VeeT	NA	NA	Connect to ground.
N/A	N/A	L22, V17, AD18, R12, AB15, V12, Y9, AC3, T2, P2	TX_DISABLE[0:9]	Leave as no-connect.

Table 20. 1 x 9-to-IXF1110 Connection (Continued)

1 x 9 Pin #	1x9 Pin Name	IXF1110 Pin # 0:9	IXF1110 Pin Name	Description
N/A	N/A	M24, V23, Y17, R15, W14, W11, W9, AC5, P8, L2	TX_FAULT[0:9]	Use external 4.7 kΩ pull-down to ground to ensure proper operation.
N/A	N/A	L22, V17, AD18, R12, AB15, V12, Y9, AC3, T2, P2	RX_LOS_[0:9]	Use external 4.7 kΩ pull-down to ground to ensure proper operation.
N/A	N/A	G22, G23, J24, F22, E23, H24, G20, E22, G24, F24	I^2C_DATA_[0:9]	Leave as no-connect.
N/A	N/A	L19	I^2C_CLK	Leave as no-connect.
N/A	N/A	B11	TX_FAULT_Int	Leave as no-connect.
N/A	N/A	B14	RX_LOS_Int	Leave as no-connect.
N/A	N/A	G15	MOD_DEF_Int	Leave as no-connect.

5.0 Test Specifications

Table 21 through Table 34 on page 89 and Figure 29 on page 80 through Figure 38 on page 89 represent the target specifications of the following IXF1110 interfaces:

- CPU
- JTAG
- Transmit Pause Control
- GBIC
- Hardware Reset
- LED
- SerDes
- SPI4-2
- I^2C

Note: These specifications are not guaranteed and are subject to change without notice. Minimum and maximum values listed in Table 23 through Table 34 on page 89 apply over the recommended operating conditions specified in Table 21.

Table 21. Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
Supply Voltage		VDD	-0.3	2.4	Volts
		AVDD	-0.3	2.4	Volts
		VDD2	-0.3	3.0	Volts
		AVDD2	-0.3	3.0	Volts
Operating Temperature	Ambient	TOPA	-15	+85	°C
	Case	TOPC	–	+130	°C
Storage Temperature		TST	-65	+150	°C
Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.					

Table 22. Operating Conditions

Parameter		Symbol	Min	Typ[1]	Max	Units
Recommended Supply Voltage		VDD, AVDD	1.71	1.80	1.89	Volts
		VDD2, AVDD2	2.375	2.50	2.625	Volts
Operating Current	1000BASE-SX	IDD and AIDD	–	2.31	–	Amps
		IDD2 and AIDD2	–	0.310	–	Amps
Recommended Operating Temperature	Ambient	TOPA	0	–	70	°C
	Case with Heat Sink	TOPC-HS	0	–	119	°C
	Case without Heat Sink	TOPC-NHS	0	–	118	°C
Power Consumption	1000BASE-SX full-duplex TX and RX at 25 °C	P	–	4.9	–	Watts

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 23. 2.5 V LVTTL and CMOS I/O Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low Voltage	VIL	–	–	0.70	V	VCC = MIN
Input High Voltage	VIH	1.7	–	3.3	V	VCC = MIN
Output Low Voltage	VOL	–	–	0.40	V	VCC = Min, IOL = 3.9 mA
Output High Voltage	VOH	2.0	–	–	V	VCC = MIN, IOH = -2.9 mA
Output Leakage Current	IOZ	–	–	10	µA	VCC = MAX

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. 3.3 V CMOS tolerant.

Table 24. LVDS I/O Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Voltage Range	VI	-0.20	–	VddMax+ 0.20	V	–
Differential Input Voltage	|VID|	100	–	–	mV	@ 400 MHz
Input Common-Mode Current	ICM	–	–	–	µA	LVDS Input VOS = 1.2 V
Threshold Hysteresis	TH	25	–	–	mV	–
Differential Input Impedance	RIN	85	–	115	Ω	Typical 100 Ω
Output Low Voltage	VOL	0.95	–	–	V	–
Output High Voltage	VOH		–	1.51	V	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 24. LVDS I/O Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Differential Output Voltage	|VOD|	330	–	446	mV	–
Delta Differential Output Voltage (Complementary States)	Δ|VOD|	–	–	25	mV	–
Offset (Common-Mode) Voltage	VOS	1.12	–	1.3	V	–
Output Leakage Current	IOZ	–	–	10	µA	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 29. CPU Port Read Timing Diagram

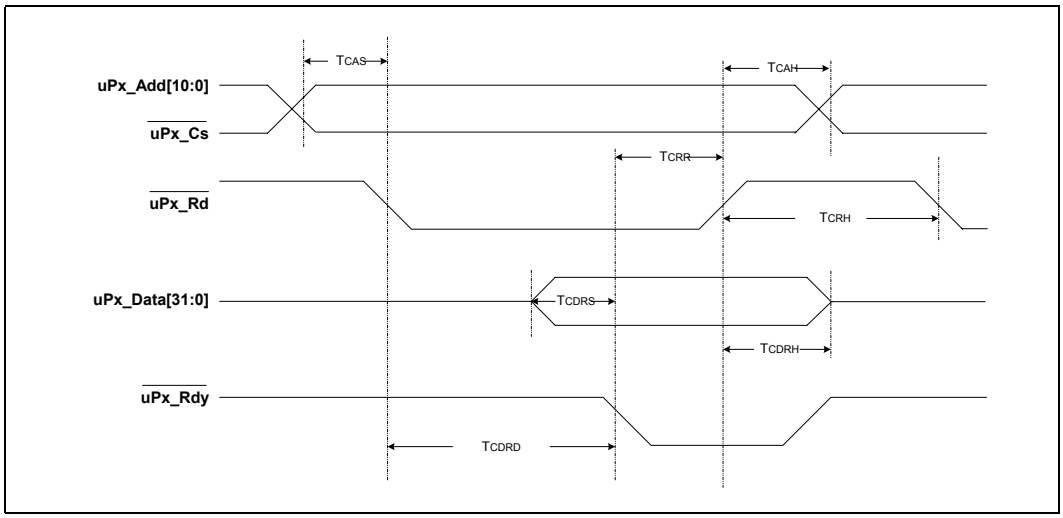


Figure 30. CPU Port Write Timing Diagram

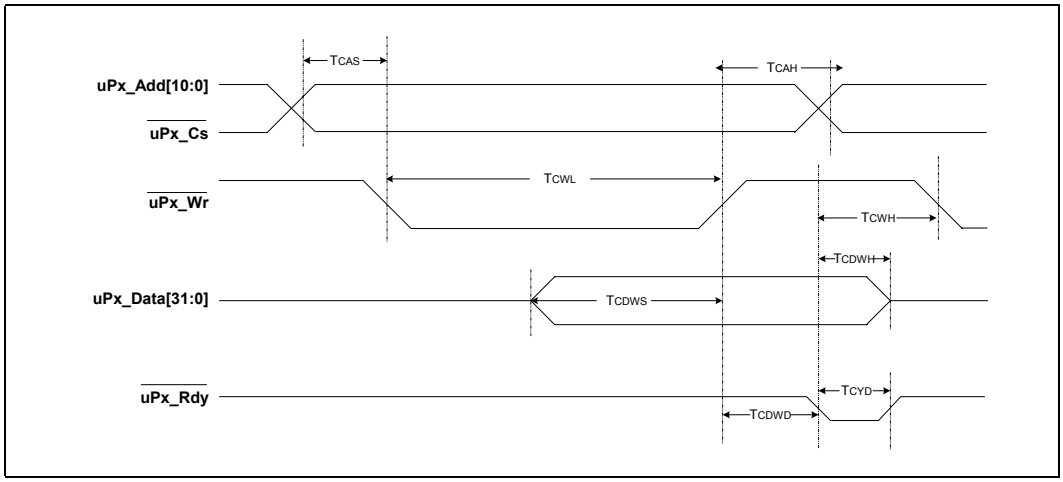


Table 25. CPU Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
uPx_Add[12:0], $\overline{\text{uPx\_Cs}}$ Setup Time	TCAS	10	–	–	ns	–
uPx_Add[12:0], $\overline{\text{uPx\_Cs}}$ Hold Time	TCAH	10	–	–	ns	–
$\overline{\text{uPx\_Rdy}}$ Assertion to $\overline{\text{uPx\_Rd}}$ De-assertion	TCRR	10	–	–	ns	–
$\overline{\text{uPx\_Rd}}$ High Width	TCRH	24 (3x cycle)	–	–	ns	–
uPx_Data[31:0] to $\overline{\text{uPx\_Rdy}}$ Setup Time	TCDRS	10	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 25. CPU Timing Parameters (Continued)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
uPx_Data[31:0] to $\overline{\text{uPx\_Rd}}$ Hold Time	TCDRH	8	–	32	ns	–
Read uPx_Data[31:0] Driving Delay	TCDRD	24	–	120	ns	–
$\overline{\text{uPx\_Wr}}$ Width	TCWL	40	–	–	ns	–
$\overline{\text{uPx\_Rdy}}$ to $\overline{\text{uPx\_Wr}}$ Hold Time	TCWH	16	–	–	ns	–
uPx_Data[31:0] to $\overline{\text{uPx\_Wr}}$ Setup Time	TCDWS	10	–	–	ns	–
$\overline{\text{uPx\_Rdy}}$ to uPx_Data[31:0] Hold Time	TCDWH	10	–	–	ns	–
uPx_Data[31:0] Latching Delay	TCDWD	8	–	32	ns	–
$\overline{\text{uPx\_Rdy}}$ Width in Write Cycle	TCYD	24	–	40	ns	–
Read $\overline{\text{uPx\_Rdy}}$ de-assertion to $\overline{\text{uPx\_Wr}}$ Assertion	TRTW	32	–	–	ns	–
Write $\overline{\text{uPx\_Rdy}}$ de-assertion to $\overline{\text{uPx\_Rd}}$ Assertion	TWTR	32	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 31. JTAG Timing Diagram

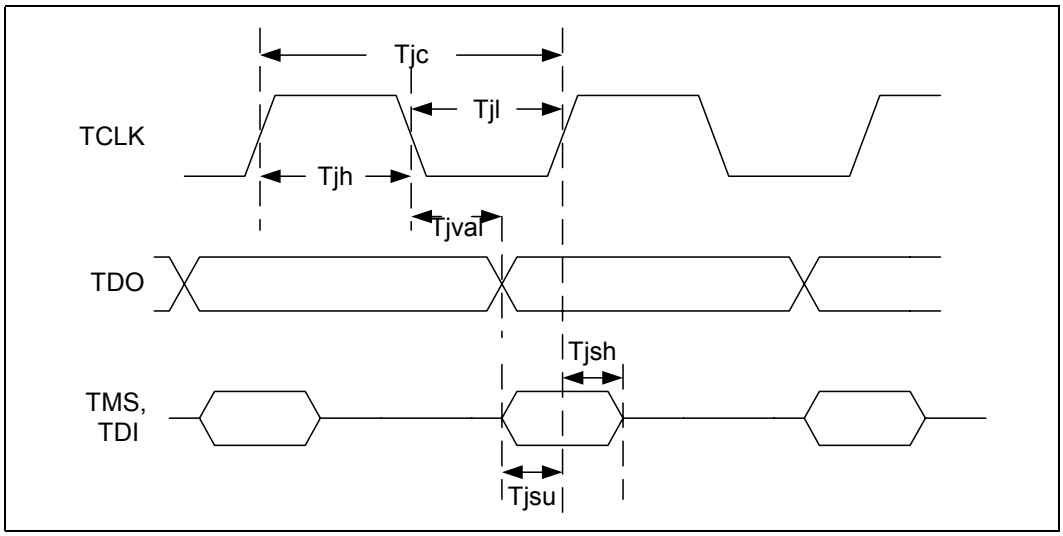


Table 26. JTAG Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
TCLK Cycle Time	T_{JC}	90	–	–	ns	–
TCLK High Time	T_{JH}	0.4 x T_{JC}	–	0.6 x T_{JC}	ns	–
TCLK Low Time	T_{JL}	0.4 x T_{JC}	–	0.6 x T_{JC}	ns	–
TCLK Falling Edge to TDO Valid	T_{JVAL}	–	–	25	ns	–
TMS/TDI Setup to TCLK	T_{JSU}	20	–	–	ns	–
TMS/TDI Hold from TCLK	T_{JSH}	5	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 32. Transmit Pause Control Interface Diagram

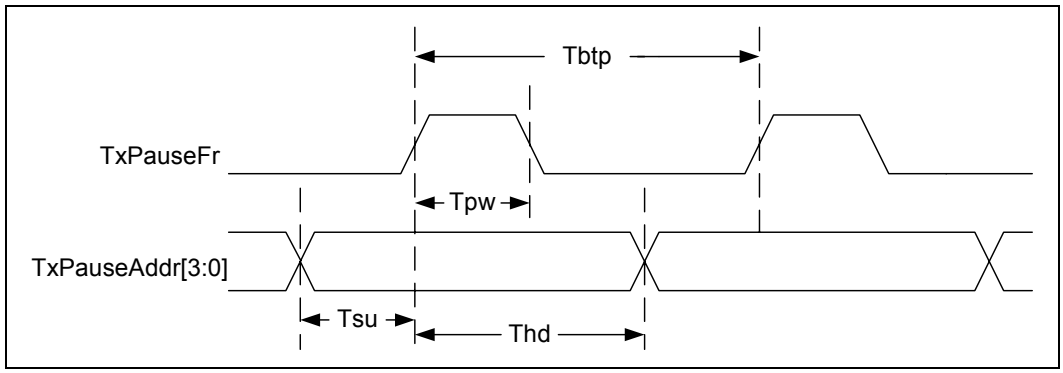


Table 27. Transmit Pause Control Interface Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
TxPauseFr Width	TPW	16	–	–	ns	–
TxPauseAddr[3:0] Setup to TxPauseFr	TSU	16	–	–	ns	–
TxPauseAddr[3:0] Hold from TxPauseFr	THD	32	–	–	ns	–
TxPauseFr Pulse to Pulse	TBTP	48	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 33. GBIC Interrupt Timing

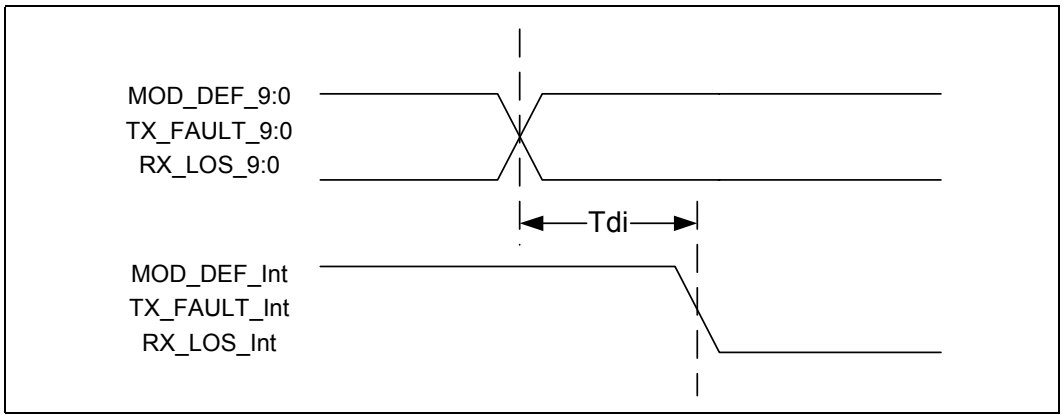


Table 28. GBIC Interrupt Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Change of state on MOD_DEF_9:0 or TX_FAULT_9:0 or RX_LOS_9:0 to assertion (active Low) on MOD_DEF_Int or TX_FAULT_Int or RX_LOS_Int	TDI	24	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 34. Hardware Reset Timing Diagram

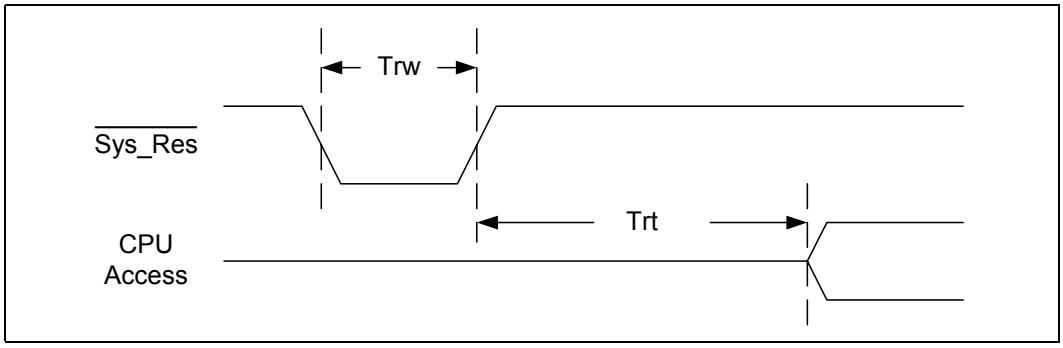


Table 29. Hardware Reset Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Reset Pulse Width	TRW	100	–	–	ns	–
Reset Recovery Time	TRT	4.11	–	–	µs	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 35. LED Timing Diagram

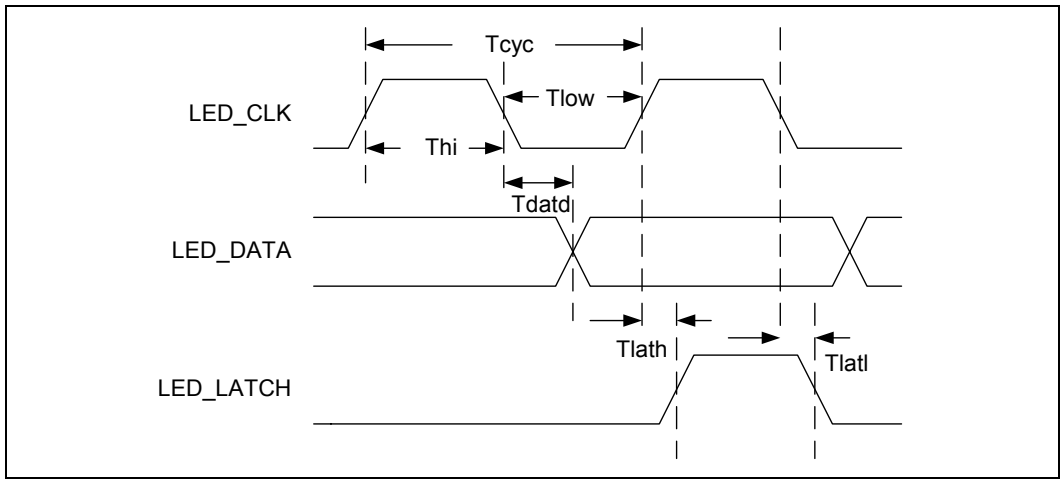


Table 30. LED Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions[2]
LED_CLK Cycle Time	TCYC	1.36	–	1.40	ms	–
LED_CLK High Time	THI	680	–	700	µs	50% duty cycle
LED_CLK Low Time	TLOW	680	–	700	µs	50% duty cycle
LED_CLK Falling Edge to LED_DATA Valid	TDATD	2	–	5	ns	–
LED_CLK Rising Edge to LED_LATCH Rising Edge	TLATH	690	–	700	µs	–
LED_CLK Falling Edge to LED_LATCH Falling Edge	TLATL	690	–	700	µs	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Flash Rate = 100 ms, LED Mode 1.

Table 31 specifies the transmit electrical specifications based on a recommended 1.8 V AVDD termination voltage and the required 50 Ω termination and Table 32 specifies the receiver electrical specifications based on a recommended 1.8 V AVDD termination voltage. Figure 36 illustrates the timing requirements for the IXF1110 transmit and receive SerDes signals.

Note: It is essential that both positive and negative drive levels at the receiver input maintain a minimum voltage of 0.8 V relative to ground to help ensure proper circuit operation.

Figure 36. SerDes Timing Diagram

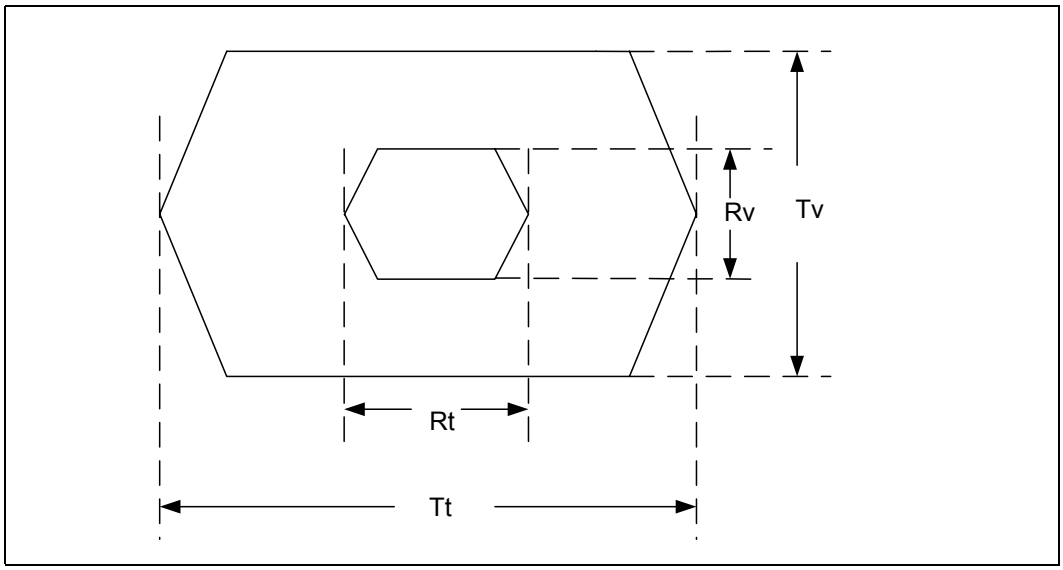


Table 31. Transmitter Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit differential signal level	T_V	600	770	1050	mVpp diff	AVDD terminated to 1.8 V; R_{LOAD} = 50 Ω;
Transmit Eye Width	T_T	800	–	–	pS	–
Differential signal rise/fall time	–	60	96	132	pS	R_{LOAD} = 50 Ω; 20% to 80% max
Differential Output Impedance	–	60	100	150	Ω diff	DC
Transmitter short circuit current	–	-100	–	100	mA	–
Transmitter Frequency	–	1.249875	1.25	1.250125	GHz	Reference Oscillator 125 MHz +/- 100 ppm
Total Transmitter output jitter	–			122	pS p-p	Total Jitter at BER 1E-12

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 32. Receiver Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Receiver differential voltage requirement at center of receive-eye	RV	200	–	–	mVp-p diff	–
Receive Eye Width	RT	280	–	–	pS	–
Receiver termination impedance	–	40	–	62.5	Ω	–
Signal detect level	–	125	–	400	mVp-p diff	–
Total Receiver jitter tolerance	–	–	–	600	pS p-p	Total Jitter at BER 1E-12

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 37. SPI4-2 Transmit FIFO Status Bus Timing Diagram

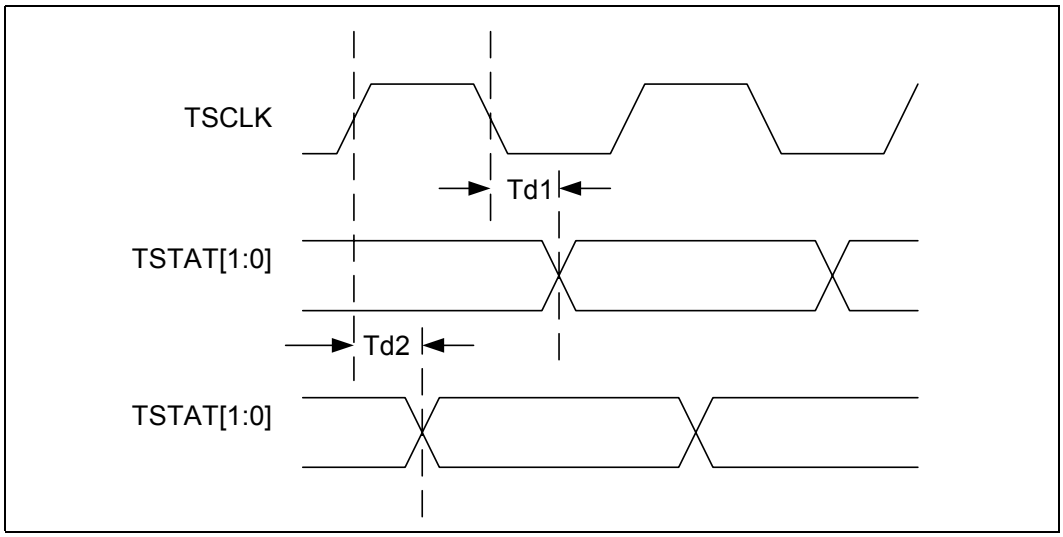


Table 33. SPI4-2 Transmit FIFO Status Bus Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
TSCLK Falling Edge to TSTAT[1:0] Valid (Active edge flipped to falling)	TD1	–	–	280	pS	–
TSCLK Rising Edge to TSTAT[1:0] Valid (Default operation)	TD2	–	–	280	pS	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 38. SPI4-2 Receive FIFO Status Bus Timing Diagram

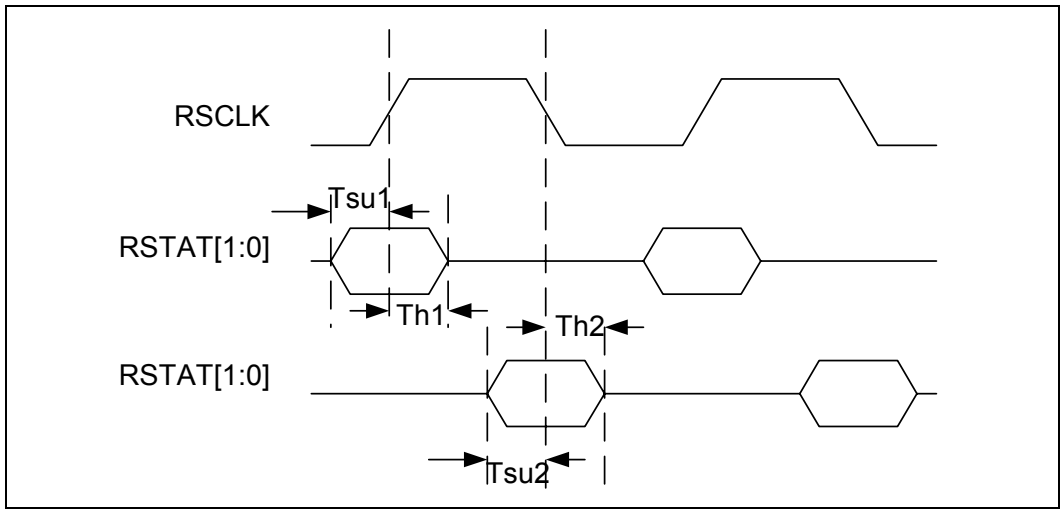


Table 34. SPI4-2 Receive FIFO Status Bus Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
RSTAT[1:0] Setup to RSCLK Rising Edge (Default operation)	T_{SU1}	2	–	–	ns	–
RSTAT[1:0] Hold From RSCLK Rising Edge (Default operation)	T_{H1}	0.5	–	–	ns	–
RSTAT[1:0] Setup to RSCLK Falling Edge (When active edge flipped to falling)	T_{SU2}	2	–	–	ns	–
RSTAT[1:0] Hold From RSCLK Falling Edge (When active edge flipped to falling)	T_{H2}	0.5	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 39. I²C Bus Timing Diagram

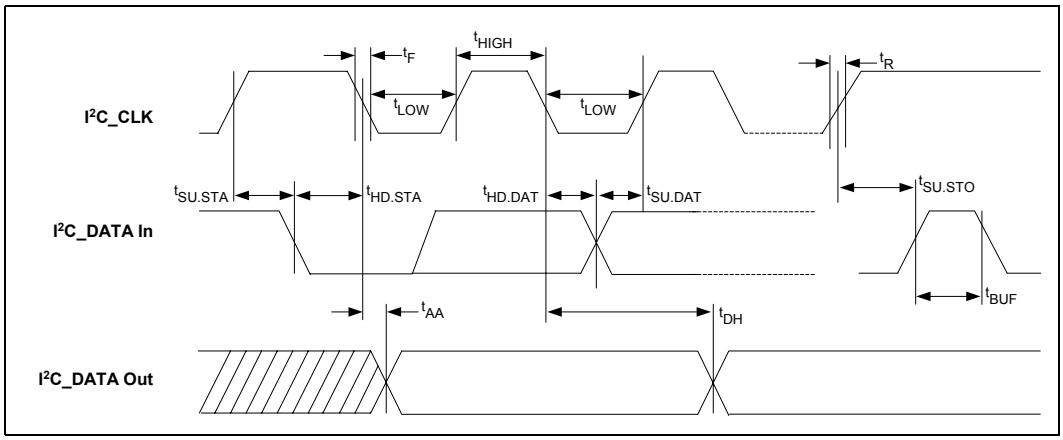


Figure 40. I²C Write Cycle Diagram

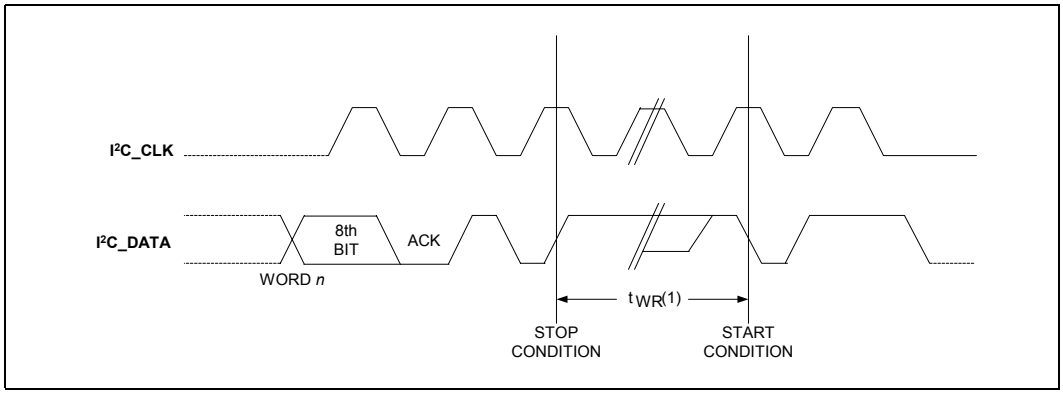


Table 35. I²C AC Timing Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Clock Frequency, SCL	f_{SCL}	–	–	100	kHz	–
Clock Pulse Width Low	t_{LOW}	4.7	–		µs	–
Clock Pulse Width High	t_{HIGH}	4.0	–		µs	–
Noise Suppression	t_I	–	–	100	ns	–
Clock Low to Data Valid Out	t_{AA}	0.1	–	4.5	µs	–
Time bus must be free before a new transmission starts	t_{BUF}	4.7	–	–	µs	–
Start Hold Time	$t_{HD.STA}$	4.0	–	–	µs	–
Start Setup Time	$t_{SU.STA}$	4.7	–	–	µs	–
Data In Hold Time	$t_{HD.DAT}$	0	–	–	µs	–
Data In Setup time	$t_{SU.DAT}$	200	–	–	ns	–
Inputs Rise Time	t_R	–	–	1.0	µs	–
Inputs Fall Time	t_F	–	–	300	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 35. I²C AC Timing Characteristics (Continued)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Stop Setup Time	$t_{SU.STO}$	4.7	–	–	µs	–
Data Out Hold Time	t_{DH}	100	–	–	ns	–
Write Cycle Time	t_{WR}	–	–	10	ms	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

6.0 Register Definitions

6.1 Introduction

This section provides information on the location and functionality of the control and status registers contained in the Intel® IXF1110.

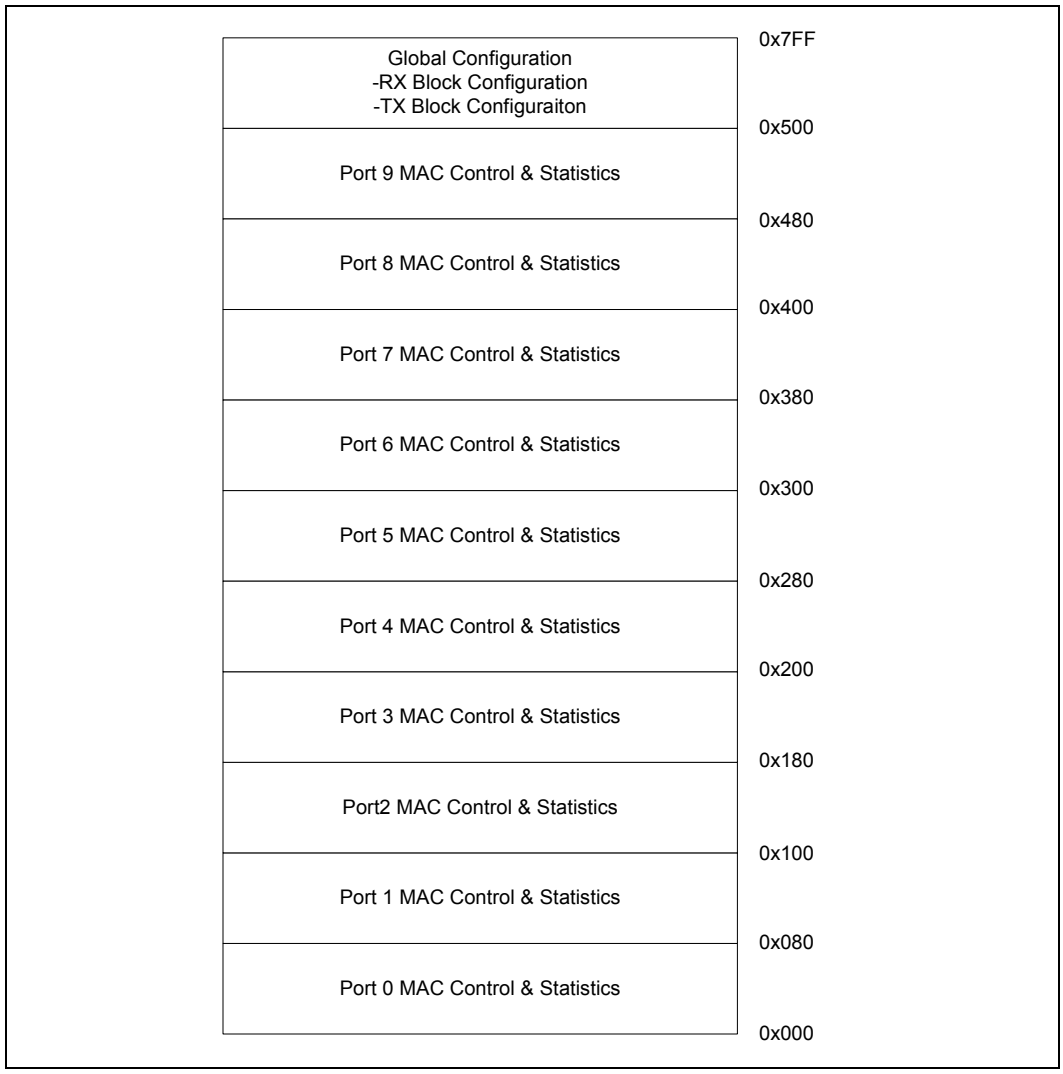
6.2 Document Structure

This document is structured to give a general overview of the register map and an in-depth description of each bit of a register in later sections.

6.3 Graphical Representation

Figure 41 represents an overview of the IXF1110 global control status registers that are used to configure or report on all ports.

Figure 41. Memory Overview Diagram

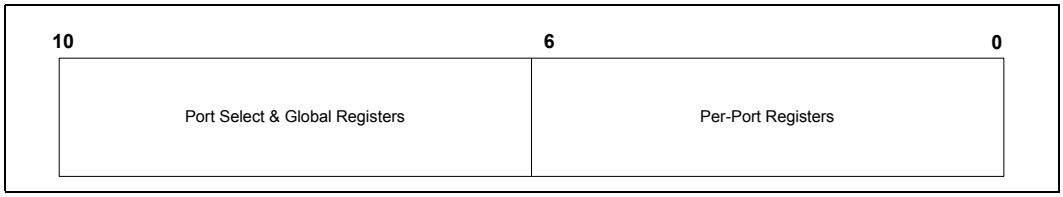


6.4 Per Port Registers

The following section covers all of the registers that are replicated in each of the 10 ports in the IXF1110. These registers perform an identical function in each port.

The address vector for the IXF1110 is 11 bits wide. This allows for 7 bits of port-specific access and a 4-bit vector to address each port and all global registers. The address format is shown in Figure 42.

Figure 42. Register Overview Diagram



6.5 Memory Map

Table 36 through Table 44 on page 101 provide the IXF1110 memory maps. A number of global control and status registers are used to configure or report on all ports, and some registers are replicated on a per-port basis.

Note: All registers in the IXF1110 are 32 bits.

Table 36. MAC Control Register Map

Register	Bit Size	Mode[1]	Ref Page	Offset
MAC Control Registers (Port Index + Offset)				
Station Address Low	32	R/W	102	0x00
Station Address High	32	R/W	102	0x01
Reserved	32	RO	–	0x02
FDFC Type	32	R/W	102	0x03
Reserved	32	RO	–	0x04
Reserved	32	RO	–	0x05
Reserved	32	RO	–	0X06
FC TX Timer Value	32	R/W	102	0x07
FDFC Address Low	32	R/W	103	0x08
FDFC Address High	32	R/W	103	0x09
Reserved	32	RO	–	0x0A
Reserved	32	RO	–	Ox0B
IPG Transmit Time	32	R/W	103	0x0C
Reserved	32	R/W	--	0x0D
Pause Threshold	32	R/W	103	0x0E
Max Frame Size	32	R/W	104	0x0F
Reserved	32	RO	–	0x10
Reserved	32	RO	–	0x11
FC Enable	32	R/W	104	0x12
Reserved	32	RO	–	0x13
Short Runts Threshold	32	R/W	104	0x14
Discard Unknown Control Frame	32	R/W	104	0x15
RX Config Word	32	R/W	105	0x16
TX Config Word	32	R/W	106	0x17
Diverse Config	32	R/W	106	0x18
RX Packet Filter Control	32	R/W	107	0x19
Port Multicast Address Low	32	R/W	109	0x1A
Port Multicast Address High	32	R/W	109	0x1B

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 37. MAC RX Statistics Register Map

Register	Bit Size	Mode[1]	Ref Page	Offset
MAC RX Statistics Registers (Port Index + Offset)				
RXOctetsTotalOK	32	RR	110	0x20
RXOctetsBAD	32	RR	110	0x21
RXUCPckts	32	RR	110	0x22
RXMCPkts	32	RR	110	0x23
RXBCPkts	32	RR	110	0x24
RXPkts64Octets	32	RR	110	0x25
RXPkts65to127Octets	32	RR	110	0x26
RXPkts128to255Octets	32	RR	110	0x27
RXPkts256to511Octets	32	RR	110	0x28
RXPkts512to1023Octets	32	RR	110	0x29
RXPkts1024to1518Octets	32	RR	110	0x2A
RXPkts1519toMaxOctets	32	RR	110	0x2B
RXFCSErrors	32	RR	110	0x2C
RXTagged	32	RR	110	0x2D
RXDataError	32	RR	110	0x2E
RXAlignErrors	32	RR	110	0x2F
RXLongErrors	32	RR	110	0x30
RXJabberErrors	32	RR	110	0x31
RXPauseMacControlCounter	32	RR	110	0x32
RXUnknownMacControlFrameCounter	32	RR	110	0x33
RXVeryLongErrors	32	RR	110	0x34
RXRuntErrors	32	RR	110	0x35
RXShortErrors	32	RR	110	0x36
RXCarrierExtendError	32	RR	110	0x37
RXSequenceErrors	32	RR	110	0x38
RXSymbolErrors	32	RR	110	0x39

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 38. MAC TX Statistics Register Map

Register	Bit Size	Mode[1]	Ref Page	Offset
MAX TX Statistics Registers (Port Index + Offset)				
TXOctetsTotalOK	32	RR	114	0x40
TXOctetsBad	32	RR	114	0x41
TXUCPkts	32	RR	114	0x42
TXMCPkts	32	RR	114	0x43
TXBCPkts	32	RR	114	0x44
TXPkts64Octets	32	RR	114	0x45
TXPkts65to127Octets	32	RR	114	0x46
TXPkts128to255Octets	32	RR	114	0x47
TXPkts256to511Octets	32	RR	114	0x48
TXPkts512to1023Octets	32	RR	114	0x49
TXPkts1024to1518Octets	32	RR	114	0x4A
TXPkts1519toMaxOctets	32	RR	114	0x4B
TXDeferred	32	RR	114	0x4C
TXTotalCollisions	32	RR	114	0x4D
TXSingleCollisions	32	RR	114	0x4E
TXMultipleCollisions	32	RR	114	0x4F
TXLateCollisions	32	RR	114	0x50
TXExcessiveCollisionErrors	32	RR	114	0x51
TXExcessiveDeferralErrors	32	RR	114	0x52
TXExcessiveLengthDrop	32	RR	114	0x53
TXUnderrun	32	RR	114	0x54
TXTagged	32	RR	114	0x55
TXCRCError	32	RR	114	0x56
TXPauseFrames	32	RR	114	0x57
TXFlowControlCollisionsSend	32	RR	114	0x58

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 39. Global Status and Configuration Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
Port Enable	32	R/W	118	0x500
Reserved	32	RO	–	0x501
Link LED Enable	32	R/W	119	0x502
Reserved	32	RO	–	0x503

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 39. Global Status and Configuration Register Map (Continued)

Register	Bit Size	Mode[1]	Ref Page	Address
Reserved	32	RO	–	0x504
Reserved	32	RO	–	0x505
Reserved	32	RO	–	0x506
Reserved	32	RO	–	0x507
CPU Interface	32	R/W	120	0x508
LED Control	32	R/W	120	0x509
LED Flash Rate	32	R/W	120	0x50A
LED Fault Disable	32	R/W	121	0x50B
JTAG ID	32	R/W	122	0x50C
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 40. RX Block Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
RX FIFO High Watermark Port 0	32	R/W	123	0x580
RX FIFO High Watermark Port 1	32	R/W	123	0x581
RX FIFO High Watermark Port 2	32	R/W	123	0x582
RX FIFO High Watermark Port 3	32	R/W	123	0x583
RX FIFO High Watermark Port 4	32	R/W	123	0x584
RX FIFO High Watermark Port 5	32	R/W	123	0x585
RX FIFO High Watermark Port 6	32	R/W	123	0x586
RX FIFO High Watermark Port 7	32	R/W	123	0x587
RX FIFO High Watermark Port 8	32	R/W	123	0x588
RX FIFO High Watermark Port 9	32	R/W	123	0x589
RX FIFO Low Watermark Port 0	32	R/W	124	0x58A
RX FIFO Low Watermark Port 1	32	R/W	124	0x58B
RX FIFO Low Watermark Port 2	32	R/W	124	0x58C
RX FIFO Low Watermark Port 3	32	R/W	124	0x58D
RX FIFO Low Watermark Port 4	32	R/W	124	0x58E
RX FIFO Low Watermark Port 5	32	R/W	124	0x58F
RX FIFO Low Watermark Port 6	32	R/W	124	0x590
RX FIFO Low Watermark Port 7	32	R/W	124	0x591
RX FIFO Low Watermark Port 8	32	R/W	124	0x592
RX FIFO Low Watermark Port 9	32	R/W	124	0x593
RX FIFO Number of Frames Removed on Port 0	32	RR	126	0x594
RX FIFO Number of Frames Removed on Port 1	32	RR	126	0x595
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 40. RX Block Register Map (Continued)

Register	Bit Size	Mode[1]	Ref Page	Address
RX FIFO Number of Frames Removed on Port 2	32	RR	126	0x596
RX FIFO Number of Frames Removed on Port 3	32	RR	126	0x597
RX FIFO Number of Frames Removed on Port 4	32	RR	126	0x598
RX FIFO Number of Frames Removed on Port 5	32	RR	126	0x599
RX FIFO Number of Frames Removed on Port 6	32	RR	126	0x59A
RXFIFO Number of Frames Removed on Port 7	32	RR	126	0x59B
RX FIFO Number of Frames Removed on Port 8	32	RR	126	0x59C
RX FIFO Number of Frames Removed on Port 9	32	RR	126	0x59D
Reserved	32	RO	–	0x59E
RX FIFO Errored Frames Drop Enable	32	R/W	128	0x59F
RX FIFO Overflow Event	32	RR	129	0x5A0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 41. TX Block Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
TX FIFO High Watermark Port 0	32	R/W	131	0x600
TX FIFO High Watermark Port 1	32	R/W	131	0x601
TX FIFO High Watermark Port 2	32	R/W	131	0x602
TX FIFO High Watermark Port 3	32	R/W	131	0x603
TX FIFO High Watermark Port 4	32	R/W	131	0x604
TX FIFO High Watermark Port 5	32	R/W	131	0x605
TX FIFO High Watermark Port 6	32	R/W	131	0x606
TX FIFO High Watermark Port 7	32	R/W	131	0x607
TX FIFO High Watermark Port 8	32	R/W	131	0x608
TX FIFO High Watermark Port 9	32	R/W	131	0x609
TX FIFO Low Watermark Port 0	32	R/W	131	0x60A
TX FIFO Low Watermark Port 1	32	R/W	132	0x60B
TX FIFO Low Watermark Port 2	32	R/W	132	0x60C
TX FIFO Low Watermark Port 3	32	R/W	132	0x60D
TX FIFO Low Watermark Port 4	32	R/W	132	0x60E
TX FIFO Low Watermark Port 5	32	R/W	132	0x60F
TX FIFO Low Watermark Port 6	32	R/W	132	0x610
TX FIFO Low Watermark Port 7	32	R/W	132	0x611
TX FIFO Low Watermark Port 8	32	R/W	132	0x612
TX FIFO Low Watermark Port 9	32	R/W	132	0x613

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 41. TX Block Register Map (Continued)

Register	Bit Size	Mode[1]	Ref Page	Address
TX FIFO MAC Transfer Threshold Port 0	32	R/W	134	0x614
TX FIFO MAC Transfer Threshold Port 1	32	R/W	134	0x615
TX FIFO MAC Transfer Threshold Port 2	32	R/W	134	0x616
TX FIFO MAC Transfer Threshold Port 3	32	R/W	134	0x617
TX FIFO MAC Transfer Threshold Port 4	32	R/W	134	0x618
TX FIFO MAC Transfer Threshold Port 5	32	R/W	134	0x619
TX FIFO MAC Transfer Threshold Port 6	32	R/W	134	0x61A
TX FIFO MAC Transfer Threshold Port 7	32	R/W	134	0x61B
TX FIFO MAC Transfer Threshold Port 8	32	R/W	134	0x61C
TX FIFO MAC Transfer Threshold Port 9	32	R/W	134	0x61D
TX FIFO Overflow Event	32	RR	137	0x61E
Reserved	32	RO	–	0x61F
Reserved	32	RO	–	0x620
TX FIFO Info Out of Sequence	32	RR	138	0x621
TX FIFO Number of Frames Removed on Port 0	32	RR	139	0x622
TX FIFO Number of Frames Removed on Port 1	32	RR	139	0x623
TX FIFO Number of Frames Removed on Port 2	32	RR	139	0x624
TX FIFO Number of Frames Removed on Port 3	32	RR	139	0x625
TX FIFO Number of Frames Removed on Port 4	32	RR	139	0x626
TX FIFO Number of Frames Removed on Port 5	32	RR	139	0x627
TX FIFO Number of Frames Removed on Port 6	32	RR	139	0x628
TX FIFO Number of Frames Removed on Port 7	32	RR	139	0x629
TX FIFO Number of Frames Removed on Port 8	32	RR	139	0x62A
TX FIFO Number of Frames Removed on Port 9	32	RR	139	0x62B
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 42. SPI4-2 Block Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
SPI4-2 Rx Burst Size	32	R/W	140	0x700
SPI4-2 Rx Training	32	R/W	140	0x701
SPI4-2 Calendar	32	R/W	141	0x702
SPI4-2 Tx Synchronization	32	R/W	142	0x703
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 43. SerDes Block Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
TX and RX AC/DC Coupling Selection	32	R/W	142	0x780
Reserved	32	RO	–	0x781
Reserved	32	RO	–	0x782
Reserved	32	RO	–	0x783
Reserved	32	RO	–	0x784
Reserved	32	RO	–	0x785
Reserved	32	RO	–	0x786
Tx and Rx Power-Down Ports 0-9	32	R/W	143	0x787
Reserved	32	RO	–	0x788
Reserved	32	RO	–	0x789
Reserved	32	RO	–	0x78A
Reserved	32	RO	–	0x78B
Reserved	32	RO	–	0x78C
Reserved	32	RO	–	0x78D
Reserved	32	RO	–	0x78E
Reserved	32	RO	–	0x78F
Reserved	32	RO	–	0x790
Reserved	32	RO	–	0x791
Reserved	32	RO	–	0x792
Rx Signal Detect Level Ports 0-9	32	RO	143	0x793
Reserved	32	RO	–	0x794
Reserved	32	RO	–	0x795
Reserved	32	RO	–	0x796
Reserved	32	RO	–	0x797
Reserved	32	RO	–	0x798

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 44. GBIC Block Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
GBIC Status Register Ports 0-9	32	RO	144	0x799
GBIC Control Register Ports 0-9	32	R/W	144	0x79A
I^2C Control Register Ports 0-9	32	R/W	146	0x79B
I^2C Data Register Ports 0-9	32	R/W	146	0x79C

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

6.5.1 MAC Control Registers

Table 45 through Table 62 on page 109 provide details on the control and status registers associated with each MAC port. The register address is '**Port_index + 0x****', where the port index is set at any value from 0x000 through 0x500. All registers are 32 bits.

Table 45. Station Address Register Low (Addr: Port_Index + 0x00)

Bit	Name	Description	Type[1]	Default
31:0	Station Address Low	Source MAC address bits 31-0. This address is inserted in the source address field when transmitting Pause frames, and is also used to compare against unicast Pause frames at the receiving side.	R/W	0x00000000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 46. Station Address Register High (Addr: Port_Index + 0x01)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	Station Address High	Source MAC address bits 47-32. This address is inserted in the source address field when transmitting Pause frames, and is also used to compare against unicast Pause frames at the receiving side.	R/W	
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 47. FDFC Type Register (Addr: Port_Index + 0x03)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	FDFC Type	Contains the value of the type field transmitted in an internally generated flow control (pause) frame. Internally generated flow control frames are generated via the external pause interface or when the RX FIFO exceeds its high watermark.	R/W	0x8808
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 48. FC TX Timer Value Register (Addr: Port_Index + 0x07)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	FC TX Timer Value	The pause length sent to the receiving station in 512 bit times	R/W	0x005E
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 49. FDFC Address Low Register (Addr: Port_Index + 0x08)

Bit	Name	Description	Type[1]	Default
31:0	FDFC Address Low	Contains the value of the lowest 32 bits of the destination address field transmitted in an internally generated flow control (pause) frame. Internally generated flow control frames are generated via the external pause interface or when the RX FIFO exceeds it high watermark.	R/W	0xC2000001
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 50. FDFC Address High Register (Addr: Port_Index + 0x09)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	FDFC Address High	Contains the value of the highest 16 bits of the destination address filed transmitted in an internally generated flow control (pause) frame. Internally generated flow control frames are generated via the external pause interface or when the RX FIFO exceeds it high watermark.	R/W	0x0180
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 51. IPG Transmit Time Register (Addr: Port_Index + 0x0C)

Bit	Name	Description	Type[1]	Default
31:10	Reserved	Reserved	RO	0x0000
9:0	IPG Transmit Time	IPG time for back-to-back transmissions (specified in multiples of 512 bit times) **Note:** The value specified in this register should be four less than desired.	R/W	0x0008
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 52. Pause Threshold Register (Addr: Port_Index + 0x0E)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	Pause Threshold	When a pause frame is sent, an internal timer checks when a new pause frame must be scheduled for transmission to keep the link partner in pause mode. The pause threshold value is the minimum time to send before the earlier pause frame is aged out (specified in multiples of 512 bit times).	R/W	0x002F
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 53. Max Frame Size Register (Addr: Port_Index + 0x0F)

Bit	Name	Description	Type[1]	Default
31:14	Reserved	Reserved	RO	0x0000
13:0	Max Frame Size	The maximum frame size the MAC can receive or transmit without activating any error counters, and without truncation. The maximum frame size is internally adjusted by +4 if VLAN is tagged.	R/W	0x05EE
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 54. FC Enable Register (Addr: Port_Index + 0x12)

Bit	Name	Description	Type[1]	Default
Register Description: Indicates flow control settings of the IXF1110.				0x00000007
31:2	Reserved	Reserved	RO	0x00000001
1	TX FD FC	1 = Enable TX FD Flow Control 0 = Disables	R/W	1
0	RX FD FC	1 = Enable RX FD Flow Control 0 = Disables	R/W	1
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 55. Short Runts Threshold Register (Addr: Port_Index + 0x14)

Bit	Name	Description	Type[1]	Default
31:5	Reserved	Reserved	RO	0x0000000
4:0	Short Runts Threshold	Holds the value in bytes, which applies to the threshold in determining between runts and short.	R/W	01000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 56. Discard Unknown Control Frame Register (Addr: Port_Index + 0x15)

Bit	Name	Description	Type[1]	Default
31:1	Reserved	Reserved	RO	0x00000000
0	Discard Unknown Control Frame	0 = Keep unknown control frames 1 = Discard unknown control frames.	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 57. RX Config Word Register (Addr: Port_Index + 0x16)

Bit	Name	Description	Type[1]	Default
Register Description: This register is used in the IXF1110 only for auto-negotiation. The contents of this register are the "config_reg" received from the link partner, as described in IEEE 802.3, Subclause 37.2.1.				0x00000000
31:22	Reserved	Reserved	RO	0
21	An_complete	Auto-negotiation complete. This bit remains cleared from the time auto-negotiation is reset until auto-negotiation reaches the "LINK_OK" state. It remains set until auto-negotiation is disabled or restarted. (This bit is only valid if auto-negotiation is enabled.)	RO	0
20	RX Sync	0 = Loss of synchronization 1 = Bit synchronization (bit remains Low until register is read)	RR	0
19	RX Config	0 = Receiving idle/data stream 1 = Receiving /C/ ordered sets	RO	
18	Config Changed	0 = RxConfigWord has changed since last read 1 = RxConfigWord has not changed since last read (This bit remains High until register is read)	RR	0
17	Invalid Word	0 = Have not received an invalid symbol 1 = Have received an invalid symbol (This bit remains High until register is read)	RR	0
16	Carrier Sense	0 = Device is not receiving idle characters (carrier sense is true). 1 = Device is receiving idle characters (carrier sense is false).	RO	0
15	Next Page	Next Page request	RO	0
14	Reserved	Reserved	RO	0
13:12	RemoteFault[1:0]	Remote fault definitions: 00 = No error, link okay 01 = Offline 10 = Link failure 11 = Auto-negotiation_Error	RO	00
11:9	Reserved	Reserved	RO	000
8	Asym Pause	Asym Pause (ability to send pause frames)	RO	0
7	Sym Pause	Syn Pause (ability to send and receive pause frames)	RO	0
6	Half Duplex	Half-duplex	RO	0
5	Full Duplex	Full-duplex	RO	0
4:0	Reserved	Reserved	RO	00000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 58. TX Config Word Register (Addr: Port_Index + 0x17)

Bit	Name	Description	Type[1]	Default
Register Description: This register is used in the IXF1110 for auto-negotiation only. The contents of this register are sent as the config_word.				0x000001A0
31:16	Reserved	Reserved	RO	0x0000
15	NextPage	Next Page request	R/W	0
14	Reserved	Reserved	RO	0
13:12[2]	Remote Fault [1:0]	Remote fault definitions: 00 = No error, link okay 01 = Offline 10 = Link failure 11 = Auto-negotiation_Error	R/W	00
11:9	Reserved	Reserved	RO	000
8	Asym Pause	Ability to send pause frames	R/W	1
7	Sym Pause	Ability to send and receive pause frames	R/W	1
6	Half Duplex	Half-duplex	R/W	0
5	Full Duplex	Full-duplex	R/W	1
4:0	Reserved	Reserved	RO	00000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. There is no way to automatically update the state of the Remote Fault bits for transmission. The state of these bits must be set by the system controller via the uP interface prior to enabling auto-negotiation.

Table 59. Diverse Config Register (Addr: Port_Index + 0x18)

Bit	Name	Description	Type[1]	Default
Register Description: This register contains various configuration bits for general use.				0x0000110D
31:16	Reserved	Reserved	RO	0x0000
31:17	Reserved	Reserved	RO	0x0000
16:9	Reserved	Reserved	RO	000100
8	Reserved	Reserved	RO	1
7	pad_enable	Enable padding of undersized packets	R/W	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 59. Diverse Config Register (Addr: Port_Index + 0x18) (Continued)

Bit	Name	Description	Type[1]	Default
6	crc_add	Enable automatic CRC appending	R/W	0
5	AN_enable	Auto-negotiation enable: 1 = Setting this bit to 1 puts the port in an Auto-Neogatiate mode and starts Auto-Negoation. 0 = Setting this bit to 0 disables auto-negotiation and puts the IXF1110 in forced mode. Note: Since default = 0, this bit must be changed to a 1 via the CPU to enable auto-negotiation. Auto-negotiation can be restarted by de-asserting this bit, then re-aserting.	R/W	0
4:0	Reserved	Reserved	RO	01101

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 60. RX Packet Filter Control Register (Addr: Port_Index + 0x19)

Bit	Name	Description	Type[1]	Default
Register Description: This register allows for specific packet types to be marked for filtering, and is used in conjunction with the RX FIFO Errored Frames Drop Enable Register				0x00000000
31:6	Reserved	Reserved	RO	0x000000
5	CRC Error Pass[2]	This bit enables a Global filter on frames with a CRC Error. When CRCErrorPASS = 0, all frames with a CRC Error are marked as bad. **Note:** When used in conjunction with the RX FIFO ErroredFrameDropEnable[9:0] Register (see Table 75 on page 128). This allows the frame to be dropped in the RX FIFO. Otherwise, the frame is sent across the SPI4-2 interface but marked as an EOP Abort frame. When CRCErrorPASS = 1, frames with a CRC Error are not marked as bad and are passed to the SPI4-2 interface for transfer as good frames, regardless of the state of the FrameDropEn[9:0] bits.	R/W	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. Jumbo frames (1519 - 9600 bytes), matching the filter conditions, which would cause the frame to be dropped by the RX FIFO, will not be dropped. Instead, jumbo frames that are marked to be dropped by the RX FIFO, based on the filter setting in this register, will still be sent across the SPI4-2 interface, but will be marked as an EOP abort frame. Thus, jumbo frames matching the filter conditions will not be counted in the RX FIFO Number of Frames Removed Register because they are not removed by the RX FIFO. Only standard packet sizes (64 - 1518 bytes) meeting the filter conditions set in this register will actually be dropped by the RX FIFO and counted in the RX FIFO Number of Frames Removed.
3. Frames are dropped only when the appropriate bits are set in the RX FIFO Errored Frame Drop Enable Register (Table 75 on page 128). When the appropriate bits are not set, the frames are sent across the SPI4-2 interface and marked as EOP abort frames.

Table 60. RX Packet Filter Control Register (Addr: Port_Index + 0x19) (Continued)

Bit	Name	Description	Type[1]	Default
4	Pause Frame Pass[2]	This bit enables a Global filter on Pause frames. When PauseFramePass = 0, all Pause frames are marked as bad. **Note:** When used in conjunction with the RX FIFO ErroredFrameDropEnable[9:0] Register (see Table 75 on page 128). This allows the frame to be dropped in the RX FIFO. Otherwise, the frame is sent across the SPI4-2 interface but marked as an EOP Abort frame. When PauseFramePass = 1, all Pause frames are not marked as bad and are passed to the SPI4-2 interface for transfer as good frames, regardless of the state of the FrameDropEn[9:0] bits.	R/W	0
3	VLAN Drop En[2]	This bit enables a Global filter on VLAN frames. When VLANDropEn = 0, all VLAN frames are passed to the SPI4-2 Interface. When VLANDropEn = 1, all VLAN frames are dropped.[3]	R/W	0
2	B/Cast Drop En[2]	This bit enables a Global filter on Broadcast frames. When B/CastDropEn = 0, all broadcast frames are passed to the SPI4-2 Interface. When B/CastDropEn = 1, all broadcast frames are dropped.[3]	R/W	0
1	M/Cast Match En[2]	This bit enables a filter on multicast frames. If this bit = 0, all multicast frames are good and are passed to the SPI4-2 Interface. If this bit = 1, only multicast frames with a destination address that matches the PortMulticastAddress is forwarded. All other multicast frames are dropped.[3]	R/W	0
0	U/Cast Match En[2]	This bit enables a filter on unicast frames. If this bit = 0, all unicast frames are good and are passed to the SPI4-2 interface. If this bit = 1, only unicast frames with a destination address that matches the Station Address is forwarded. All other unicast frames are dropped.[3]	R/W	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. Jumbo frames (1519 - 9600 bytes), matching the filter conditions, which would cause the frame to be dropped by the RX FIFO, will not be dropped. Instead, jumbo frames that are marked to be dropped by the RX FIFO, based on the filter setting in this register, will still be sent across the SPI4-2 interface, but will be marked as an EOP abort frame. Thus, jumbo frames matching the filter conditions will not be counted in the RX FIFO Number of Frames Removed Register because they are not removed by the RX FIFO. Only standard packet sizes (64 - 1518 bytes) meeting the filter conditions set in this register will actually be dropped by the RX FIFO and counted in the RX FIFO Number of Frames Removed.
3. Frames are dropped only when the appropriate bits are set in the RX FIFO Errored Frame Drop Enable Register (Table 75 on page 128). When the appropriate bits are not set, the frames are sent across the SPI4-2 interface and marked as EOP abort frames.

Table 61. Port Multicast Address Low Register (Addr: Port_Index + 0x1A)

Bit	Name	Description	Type[1]	Default
31:0	Port Multicast Address Low	This address is used to compare against multicast frames at the receiving side if multicast filtering is enabled. This register contains bits 31:0 of the address.	R/W	0x00000000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 62. Port Multicast Address High Register (Addr: Port_Index + 0x1B)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	Port Multicast Address High	This address is used to compare against multicast frames at the receiving side if Multicast filtering is enabled. This register contains bits 47:32 of the address.	R/W	0x0000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

6.5.2 MAC RX Statistics Register Overview

The MAC RX Statistics Registers contain the MAC receiver statistic counters and are cleared when read. The software polls these registers and accumulates values to ensure that the counters do not wrap. The 32-bit counters wrap after approximately 30 seconds.

Table 63 covers the MAC RX Statistics Registers for all 10 MAC ports. The address is identical to the port number.

Table 63. MAC RX Statistics Registers (Addr: Port_Index + 0x20 - Port_Index + 0x39)

Name	Description	Address	Type[1]	Default
RxOctetsTotalOK	Counts the bytes received in all legal frames, including all bytes from the destination MAC address to and including the CRC. The initial preamble and SFD bytes are not counted.	Port_Index + 0x20	RR	0x00000000
RxOctetsBAD[2]	Counts the bytes received in all bad frames of a size greater than or equal to 64 bytes. A bad frame is defined as a properly framed packet containing a CRC, alignment error, or code violation. The 64-byte value is measured from the destination address, up to and including CRC. The initial preamble and SFD are not included in this value. **Note:** This register does not increment the Bad Octet count on undersized receive packets.	Port_Index + 0x21	RR	0x00000000
RxUCPkts	The total number of unicast packets received (excluding bad packets) **Note:** This count includes non-pause control and VLAN packets, which are also counted in other counters. These packet types are counted twice. Take care when summing register counts for reporting MIB information.	Port_Index + 0x22	RR	0x00000000
RxMCPkts	The total number of multicast packets received (excluding bad packets) **Note:** This count includes pause control packets, which are also counted in the PauseMacControl-ReceivedCounter. These packet types are counted twice. Take care when summing register counts for reporting MIB information.	Port_Index + 0x23	RR	0x00000000
RxBCPkts	The total number of Broadcast packets received (excluding bad packets)	Port_Index + 0x24	RR	0x00000000
RxPkts64Octets	The total number of packets received (including bad packets) that were 64 octets in length. Incremented for tagged packets with a length of 64 bytes, including tag field	Port_Index + 0x25	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. When sending in large frames, the counters can only deal with certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*MaxFrameSize, dependent on where the MaxFrameSize variable is set. If MaxFrameSize sets greater than half of the available count in RxOctetsBad (2^14-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2^14-1. MaxFrameSize is determined by the settings in the "Max Frame Size Register (Addr: Port_Index + 0x0F)" on page 104.

Table 63. MAC RX Statistics Registers (Addr: Port_Index + 0x20 - Port_Index + 0x39)

Name	Description	Address	Type[1]	Default
RxPkts65to127 Octets	The total number of packets received (including bad packets) that were [65-127] octets in length. Incremented for tagged packets with a length of 65 - 127 bytes, including tag field	Port_Index + 0x26	RR	0x00000000
RxPkts128to255 Octets	The total number of packets received (including bad packets) that were [128-255] octets in length. Incremented for tagged packets with a length of 128-255 bytes, including tag field	Port_Index + 0x27	RR	0x00000000
RxPkts256to511 Octets	The total number of packets received (including bad packets) that were [256-511] octets in length. Incremented for tagged packets with a length of 256 - 511 bytes, including tag field	Port_Index + 0x28	RR	0x00000000
RxPkts512to1023 Octets	The total number of packets received (including bad packets) that were [512-1023] octets in length. Incremented for tagged packets with a length of 512 - 1023 bytes, including tag field	Port_Index + 0x29	RR	0x00000000
RxPkts1024to1518 Octets	The total number of packets received (including bad packets) that were [1024-1518] octets in length. Incremented for tagged packet with a length between 1024-1522, including the tag	Port_Index + 0x2A	RR	0x00000000
RxPkts1519toMax Octets	The total number of packets received (including bad packets) that were >1518 octets in length. Incremented for tagged packet with a length between 1523-max frame size, including the tag	Port_Index + 0x2B	RR	0x00000000
RxFCSErrors	Number of frames received with legal size, but with wrong CRC field (also called FCS field) **Note:** Legal size is 64 bytes through the value stored in the "Max Frame Size Register (Addr: Port_Index + 0x0F)" on page 104.	Port_Index + 0x2C	RR	0x00000000
RxTagged	Number of frames (including bad packets) with VLAN tag (Type field = 0x8100)	Port_Index + 0x2D	RR	0x00000000
RxDataError	Number of frames received with legal length, containing a code violation (signaled with RX_ERR on RGMII) **Note:** The IXF1110 does not support an RGMII interface; thus, this counter is not applicable to the IXF1110.	Port_Index + 0x2E	RR	0x00000000
RxAlignErrors	Frames with a legal frame size, but containing less than 8 additional bits. The CRC of the frame is wrong when the additional bits are stripped. If the CRC is OK, the frame is not counted, but treated as an OK frame.	Port_Index + 0x2F	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. When sending in large frames, the counters can only deal with certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*MaxFrameSize, dependent on where the MaxFrameSize variable is set. If MaxFrameSize sets greater than half of the available count in RxOctetsBad (2^14-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2^14-1. MaxFrameSize is determined by the settings in the "Max Frame Size Register (Addr: Port_Index + 0x0F)" on page 104.

Table 63. MAC RX Statistics Registers (Addr: Port_Index + 0x20 - Port_Index + 0x39)

Name	Description	Address	Type[1]	Default
RxLongErrors[2]	Frames bigger than the maximum allowed, with both OK CRC and the integral number of octets Default maximum allowed is 1518 bytes untagged and 1522 bytes tagged, but the value can be changed by a register Frames bigger than the larger of 2*MaxFrameSize and 50000 bits are not counted here, but counted in the VeryLongError counter.	Port_Index + 0x30	RR	0x00000000
RxJabberErrors	Frames bigger than the maximum allowed, with either a bad CRC or a non-integral number of octets. The default maximum allowed is 1518 bytes untagged and 1522 bytes tagged, but the value can be changed by a register. Frames bigger than the larger of 2*MaxFrameSize and 50000 bits are not counted here, but counted in the VeryLongError counter.	Port_Index + 0x31	RR	0x00000000
RxPauseMac ControlCounter	Number of Pause MAC control frames received	Port_Index + 0x32	RR	0x00000000
RxUnknownMac ControlFrame Counter	Number of MAC control frames received with an op code different from 0001 (Pause)	Port_Index + 0x33	RR	0x00000000
RxVeryLongErrors[2]	Frames bigger than the larger of 2*MaxFrameSize and 50000 bits	Port_Index + 0x34	RR	0x00000000
RxRuntErrors	The total number of packets received that are less than 64 octets in length, but longer than or equal to 96 bit times. **Note:** RxRuntErrors is not supported in the IXF1110. Any runt or short packets received are not counted in this register. **Note:** The “ShortRuntsThreshold” Register controls the byte count used to determine the difference between Runts and Shorts, and therefore controls which counter is incremented for a given frame size. This counter is only updated after receipt of two good frames.	Port_Index + 0x35	RR	0x00000000
RxShortErrors	The total number of packets received that are less than 96 bit times, which corresponds to a 4-byte frame with a well formed preamble and SFD. This counter indicates fragment sizes illegal in all modes, and is only fully updated after reception of a good frame following a fragment. **Note:** RxShortErrors is not supported in the IXF1110. Any runt or short packets received are not counted in this register.	Port_Index + 0x36	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. When sending in large frames, the counters can only deal with certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*MaxFrameSize, dependent on where the MaxFrameSize variable is set. If MaxFrameSize sets greater than half of the available count in RxOctetsBad (2^14-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2^14-1. MaxFrameSize is determined by the settings in the “Max Frame Size Register (Addr: Port_Index + 0x0F)” on page 104.

Table 63. MAC RX Statistics Registers (Addr: Port_Index + 0x20 - Port_Index + 0x39)

Name	Description	Address	Type[1]	Default
RxCarrierExtend Error	Gigabit half-duplex event only Note: N/A - half-duplex only	Port_Index + 0x37	RR	0x00000000
RxSequenceErrors	Records the number of sequencing errors that occur.	Port_Index + 0x38	RR	0x00000000
RxSymbolErrors	Records the number of symbol errors encountered.	Port_Index + 0x39	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. When sending in large frames, the counters can only deal with certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*MaxFrameSize, dependent on where the MaxFrameSize variable is set. If MaxFrameSize sets greater than half of the available count in RxOctetsBad (2^14-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2^14-1. MaxFrameSize is determined by the settings in the “Max Frame Size Register (Addr: Port_Index + 0x0F)” on page 104.

6.5.3 MAC TX Statistics Register Overview

The MAC TX Statistics Registers contain all the MAC transmit statistic counters and are cleared when read. The software must poll these registers to accumulate values and ensure that the counters do not wrap. The 32-bit counters wrap after approximately 30 seconds.

Table 64 covers the MAC TX Statistics Registers for all 10 MAC ports. The address is identical to the port number.

Table 64. MAC TX Statistics Registers (Addr: Port_Index + 0x40 - Port_Index + 0x58)

Name	Description	Address	Type[1]	Default
TXOctetsTotalOK	Counts the bytes transmitted in all legal frames. The count includes all bytes from the destination MAC address to and including the CRC. The initial preamble and SFD bytes are not counted.	Port_Index + 0x40	RR	0x00000000
TXOctetsBad	Counts the bytes transmitted in all bad frames. The count includes all bytes from the destination MAC address to and including the CRC. The initial preamble and SFD bytes are not counted. TX underrun counted: The count is expected to match the number of bytes actually transmitted before the frame is discarded. TX CRC error counted: All bytes not sent with success are counted by this counter	Port_Index + 0x41	RR	0x00000000
TXUCPkts	The total number of unicast packets transmitted (excluding bad packets)	Port_Index + 0x42	RR	0x00000000
TXMCPkts	The total number of multicast packets transmitted (excluding bad packets) **Note:** This count includes pause control packets which are also counted in the TxPauseFrames Counter. Thus, these types of packets are counted twice. Take care when summing register counts for reporting MIB information.	Port_Index + 0x43	RR	0x00000000
TXBCPkts	The total number of broadcast packets transmitted (excluding bad packets)	Port_Index + 0x44	RR	0x00000000
TXPkts64Octets	The total number of packets transmitted (including bad packets) that were 64 octets in length. Incremented for tagged packets with a length of 64 bytes, including tag field	Port_Index + 0x45	RR	0x00000000
TXPkts65to127Octets	The total number of packets transmitted (including bad packets) that were [65-127] octets in length. Incremented for tagged packets with a length of 65 - 127 bytes, including tag field	Port_Index + 0x46	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 64. MAC TX Statistics Registers (Addr: Port_Index + 0x40 - Port_Index + 0x58)

Name	Description	Address	Type[1]	Default
TXPkts128to255Octets	The total number of packets transmitted (including bad packets) that were [128-255] octets in length. Incremented for tagged packets with a length of 128 - 255 bytes, including tag field	Port_Index + 0x47	RR	0x00000000
TXPkts256to511Octets	The total number of packets transmitted (including bad packets) that were [256-511] octets in length. Incremented for tagged packets with a length of 256 - 511 bytes, including tag field	Port_Index + 0x48	RR	0x00000000
TXPkts512to1023Octets	The total number of packets transmitted (including bad packets) that were [512 - 1023] octets in length. Incremented for tagged packets with a length of 512 - 1023 bytes, including tag field	Port_Index + 0x49	RR	0x00000000
TXPkts1024to1518Octets	The total number of packets transmitted (including bad packets) that were [1024-1518] octets in length. Incremented for tagged packet with a length between 1024-1522, including the tag	Port_Index + 0x4A	RR	0x00000000
TXPkts1519toMaxOctets	The total number of packets transmitted (including bad packets) that were >1518 octets in length. Incremented for tagged packet with a length between 1523-max frame size, including the tag	Port_Index + 0x4B	RR	0x00000000
TXDeferred	Number of times the initial transmission attempt of a frame is postponed due to another frame already being transmitted on the Ethernet network. **Note**: N/A - half-duplex only	Port_Index + 0x4C	RR	0x00000000
TXTotalCollisions	Sum of all collision events **Note**: N/A - half-duplex only	Port_Index + 0x4D	RR	0x00000000
TXSingleCollisions	A count of successfully transmitted frames on a particular interface where the transmission is inhibited by exactly one collision. A frame that is counted by an instance of this object is also counted by the corresponding instance of either the UnicastPkts, MulticastPkts, or BroadcastPkts, and is not counted by the corresponding instance of the MultipleCollisionFrames object. **Note**: N/A - half-duplex only	Port_Index + 0x4E	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 64. MAC TX Statistics Registers (Addr: Port_Index + 0x40 - Port_Index + 0x58)

Name	Description	Address	Type[1]	Default
TXMultipleCollisions	A count of successfully transmitted frames on a particular interface for which transmission is inhibited by more than one collision. A frame that is counted by an instance of this object is also counted by the corresponding instance of either the UnicastPkts, MulticastPkts, or BroadcastPkts, and is not counted by the corresponding instance of the SingleCollisionFrames object. **Note**: N/A - half-duplex only	Port_Index + 0x4F	RR	0x00000000
TXLateCollisions	The number of times a collision is detected on a particular interface later than 512 bit-times into the transmission of a packet. Such frame are terminated and discarded. **Note**: N/A - half-duplex only	Port_Index + 0x50	RR	0x00000000
TXExcessiveCollisionErrors	A count of frames, which collides 16 times and is then discarded by the MAC. Not effecting xMultipleCollisions Note: N/A - half-duplex only	Port_Index + 0x51	RR	0x00000000
TXExcessiveDeferralErrors	Number of times frame transmission is postponed more than 2*MaxFrameSize due to another frame already being transmitted on the Ethernet network. This causes the MAC to discard the frame. **Note**: N/A - half-duplex only	Port_Index + 0x52	RR	0x00000000
TXExcessiveLengthDrop	Frame transmissions aborted by the MAC because the frame is longer than maximum frame size. These frames are truncated by the MAC when the maximum frame size violation is detected by the MAC.	Port_Index + 0x53	RR	0x00000000
TXUnderrun	Internal TX error which causes the MAC to end the transmission before the end of the frame because the MAC did not get the needed data in time for transmission. The frames are lost and a fragment or a CRC error is transmitted.	Port_Index + 0x54	RR	0x00000000
TXTagged	Number of OK frames with VLAN tag. (Type field = 0x8100).	Port_Index + 0x55	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 64. MAC TX Statistics Registers (Addr: Port_Index + 0x40 - Port_Index + 0x58)

Name	Description	Address	Type[1]	Default
TXCRCError	Number of frames transmitted with a legal size, but with the wrong CRC field (also called FCS field)	Port_Index + 0x56	RR	0x00000000
TXPauseFrames	Number of pause MAC frames transmitted	Port_Index + 0x57	RR	0x00000000
TXFlowControlCollisions Send	Collisions generated on purpose on incoming frames, to avoid reception of traffic, while the port is in half-duplex and has flow control enabled, and do not have sufficient memory to receive more frames. Note: Due to the internal counting technique, a last frame might have to be transmitted after last flow control collision send to get the correct statistic. **Note**: N/A - half-duplex only	Port_Index + 0x58	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

6.5.4 Global Status and Configuration Register Overview

Table 65 through Table 70 on page 121 provide an overview of the Global Control and Status Registers.

Table 65. Port Enable Register (Addr: 0x500)

Bit	Name	Description	Type[1]	Default
Register Description: A control register for each port in the IXF1110. Port ID = bit position in the register. To make a port active, the bit must be set High (for example, port 4 active implies register value = 0001.0000). Setting the bit to 0 disables the port. The default state for this register is for all 10 ports to be active.				0x000003FF
31:10	Reserved	Reserved	RO	0x00000
9	Port 9 Enable	Port 9 0 = Disable 1 = Enable	R/W	1
8	Port 8 Enable	Port 8 0 = Disable 1 = Enable	R/W	1
7	Port 7 Enable	Port 7 0 = Disable 1 = Enable	R/W	1
6	Port 6 Enable	Port 6 0 = Disable 1 = Enable	R/W	1
5	Port 5 Enable	Port 5 0 = Disable 1 = Enable	R/W	1
4	Port 4 Enable	Port 4 0 = Disable 1 = Enable	R/W	1
3	Port 3 Enable	Port 3 0 = Disable 1 = Enable	R/W	1
2	Port 2 Enable	Port 2 0 = Disable 1 = Enable	R/W	1
1	Port 1 Enable	Port 1 0 = Disable 1 = Enable	R/W	1
0	Port 0 Enable	Port 0 0 = Disable 1 = Enable	R/W	1

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. If a port is disabled mid-packet on the receive side in SerDes mode, the RX Stats will not update for that packet due to power-down of SerDes when the port is disabled.

Table 66. Link LED Enable Register (Addr: 0x502)

Bit	Name	Description	Type[1]	Default
Register Description: Per-port bit should be set upon detection of link to enable proper operation of the link LEDs.				0x00000000
31:10	Reserved	Reserved	RO	0x00000
9	Link LED Enable Port 9	Port 9 link 0 = No link 1 = Link	R/W	0
8	Link LED Enable Port 8	Port 8 link 0 = No link 1 = Link	R/W	0
7	Link LED Enable Port 7	Port 7 link 0 = No link 1 = Link	R/W	0
6	Link LED Enable Port 6	Port 6 link 0 = No link 1 = Link	R/W	0
5	Link LED Enable Port 5	Port 5 link 0 = No link 1 = Link	R/W	0
4	Link LED Enable Port 4	Port 4 link 0 = No link 1 = Link	R/W	0
3	Link LED Enable Port 3	Port 3 link 0 = No link 1 = Link	R/W	0
2	Link LED Enable Port 2	Port 2 link 0 = No link 1 = Link	R/W	0
1	Link LED Enable Port 1	Port 1 link 0 = No link 1 = Link	R/W	0
0	Link LED Enable Port 0	Port 0 link 0 = No link 1 = Link	R/W	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 67. CPU Interface Register (Addr: 0x508)

Bit	Name	Description	Type[1]	Default
Register Description: CPU interface Endian select. This register allows the user to select the Endian of the CPU interface to allow various different CPUs to be connected to the IXF1110.				0x00000000
31:1	Reserved	Reserved	RO	0x00000000
0	Endian	0 = Little Endian 1 = Big Endian	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 68. LED Control Register (Addr: 0x509)

Bit	Name	Description	Type[1]	Default
Register Description: Globally selects and enables the LED mode.				0x00000000
31-2	Reserved	Reserved	RO	0x00000000
1	LED Enable	0 = Disable LEDs 1 = Enable LEDs	R/W	0
0	LED_SEL_MODE	0 = Enable LED Mode 0 for use with SGS Thompson M5450 LED driver 1 = (Default) LED Mode 1 for use with Standard Octal Shift Register	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 69. LED Flash Rate Register (Addr: 0x50A)

Bit	Name	Description	Type[1]	Default
Register Description: Globally selects and enables the flash rate.				0x00000000
31:3	Reserved	Reserved	RO	0x00000000
2:0	LED Flash Rate	000 = 100 ms flash rate 001 = 200 ms flash rate 010 = 300 ms flash rate 011 = 400 ms flash rate 100 = 500 ms flash rate 101 = Reserved 110 = Reserved 111 = Reserved	R/W	000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 70. LED Fault Disable Register (Addr: 0x50B)

Bit	Name	Description	Type[1]	Default
Register Description: Per-port fault disable: Disables the LED flashing for local or remote faults				0x00000000
31:10	Reserved	Reserved	RO	0x000000
9	LED Fault Disable Port 9	Port 9 0 = Fault enabled 1 = Fault disabled	R/W	0
8	LED Fault Disable Port 8	Port 8 0 = Fault enabled 1 = Fault disabled	R/W	0
7	LED Fault Disable Port 7	Port 7 0 = Fault enabled 1 = Fault disabled	R/W	0
6	LED Fault Disable Port 6	Port 6 0 = Fault enabled 1 = Fault disabled	R/W	0
5	LED Fault Disable Port 5	Port 5 0 = Fault enabled 1 = Fault disabled	R/W	0
4	LED Fault Disable Port 4	Port 4 0 = Fault enabled 1 = Fault disabled	R/W	0
3	LED Fault Disable Port 3	Port 3 0 = Fault enabled 1 = Fault disabled	R/W	0
2	LED Fault Disable Port 2	Port 2 0 = Fault enabled 1 = Fault disabled	R/W	0
1	LED Fault Disable Port 1	Port 1 0 = Fault enabled 1 = Fault disabled	R/W	0
0	LED Fault Disable Port 0	Port 0 0 = Fault enabled 1 = Fault disabled	R/W	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 71. JTAG ID Revision Register (Addr: 0x50C)

Bit	Name	Description	Type	Default
Register Description: The value of this register follows the same scheme as the device identification register found in the IEEE 1149.1 specification. The upper 4 bits correspond to silicon stepping. The next 16 bits store a Part ID Number. The next 11 bits contain a JEDEC Manufacturer ID. Bit zero = 1 if the chip is the first in a stack. The encoding scheme used for the Product ID field is implementation dependent.				0x20456013
31:28	Version	Version	RO	0010
27:12	Part ID	Part ID	RO	0000010001010110
11:8	JEDEC Cont.	JEDEC Cont.	RO	0000
7:1	JEDEC ID	JEDEC ID	RO	0001001
0	Reserved	Reserved	RO	1
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

6.5.5 Global RX Block Register Overview

Table 72 through Table 76 on page 129 provide an overview of the RX Block Registers, which include the RX FIFO High and Low watermarks.

Table 72. RX FIFO High Watermark Ports 0 to 9 Registers (Addr: 0x580 - 0x589)

Name[2]	Description	Address	Type[1]	Default
RX FIFO High Watermark Port 0	High watermark for RX FIFO port 0. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x580	R/W	0x00000740
RX FIFO High Watermark Port 1	High watermark for RX FIFO port 1. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x581	R/W	0x00000740
RX FIFO High Watermark Port 2	High watermark for RX FIFO port 2. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x582	R/W	0x00000740
RX FIFO High Watermark Port 3	High watermark for RX FIFO port 3. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x583	R/W	0x00000740
RX FIFO High Watermark Port 4	High watermark for RX FIFO port 4. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x584	R/W	0x00000740
RX FIFO High Watermark Port 5	High watermark for RX FIFO port 5. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x585	R/W	0x00000740
RX FIFO High Watermark Port 6	High watermark for RX FIFO port 6. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x586	R/W	0x00000740

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all RX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:15 - Reserved and RO.
   Bits 14:0 - Described above.

Table 72. RX FIFO High Watermark Ports 0 to 9 Registers (Addr: 0x580 - 0x589) (Continued)

Name[2]	Description	Address	Type[1]	Default
RX FIFO High Watermark Port 7	High watermark for RX FIFO port 7. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x587	R/W	0x00000740
RX FIFO High Watermark Port 8	High watermark for RX FIFO port 8. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC	0x588	R/W	0x00000740
RX FIFO High Watermark Port 9	High watermark for RX FIFO port 9. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x589	R/W	0x00000740

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all RX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:15 - Reserved and RO.
   Bits 14:0 - Described above.

Table 73. RX FIFO Low Watermark Ports 0 to 9 Registers (Addr: 0x58A - 0x593)

Name[2]	Description	Address	Type[1]	Default
RX FIFO Low Watermark Port 0	Low watermark for RX FIFO port 0. The default value is 1840 bytes. When the port is in flow control, and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58A	R/W	0x00000730
RX FIFO Low Watermark Port 1	Low watermark for RX FIFO port 1. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58B	R/W	0x00000730
RX FIFO Low Watermark Port 2	Low watermark for RX FIFO port 2. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58C	R/W	0x00000730
RX FIFO Low Watermark Port 3	Low watermark for RX FIFO port 3. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58D	R/W	0x00000730
RX FIFO Low Watermark Port 4	Low watermark for RX FIFO port 4. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58E	R/W	0x00000730

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all RX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:15 - Reserved and RO.
   Bits 14:0 - Described above.

Table 73. RX FIFO Low Watermark Ports 0 to 9 Registers (Addr: 0x58A - 0x593) (Continued)

Name[2]	Description	Address	Type[1]	Default
RX FIFO Low Watermark Port 5	Low watermark for RX FIFO port 5. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58F	R/W	0x00000730
RX FIFO Low Watermark Port 6	Low watermark for RX FIFO port 6. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x590	R/W	0x00000730
RX FIFO Low Watermark Port 7	Low watermark for RX FIFO port 7. The default value is 1840 bytes.When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x591	R/W	0x00000730
RX FIFO Low Watermark Port 8	Low watermark for RX FIFO port 8. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x592	R/W	0x00000730
RX FIFO Low Watermark Port 9	Low watermark for RX FIFO port 9. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x593	R/W	0x00000730

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all RX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:15 - Reserved and RO.
   Bits 14:0 - Described above.

Table 74. RX FIFO Number of Frames Removed Ports 0 to 9 Registers (Addr: 0x594 - 0x59D)

Name[2]	Description	Address	Type[1]	Default
RX FIFO Number of Frames Removed on Port 0	This register counts all frames removed from the RX FIFO for port 0 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 75 on page 128) • Frames are greater than the MaxFrameSize (Table 53 on page 104)	0x594	RR	0x00000000
RX FIFO Number of Frames Removed on Port 1	This register counts all frames removed from the RX FIFO for port 1 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 75 on page 128) • Frames are greater than the MaxFrameSize (Table 53 on page 104)	0x595	RR	0x00000000
RX FIFO Number of Frames Removed on Port 2	This register counts all frames removed from the RX FIFO for port 2 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 75 on page 128) • Frames are greater than the MaxFrameSize (Table 53 on page 104)	0x596	RR	0x00000000
RX FIFO Number of Frames Removed on Port 3	This register counts all frames removed from the RX FIFO for port 3 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 75 on page 128) • Frames are greater than the MaxFrameSize (Table 53 on page 104)	0x597	RR	0x00000000
RX FIFO Number of Frames Removed on Port 4	This register counts all frames removed from the RX FIFO for port 4 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 75 on page 128) • Frames are greater than the MaxFrameSize (Table 53 on page 104)	0x598	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write.
2. For all Number of Frames Removed Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:22 - Reserved and RO.
   Bits 21:0 - Described above.

Table 74. RX FIFO Number of Frames Removed Ports 0 to 9 Registers (Addr: 0x594 - 0x59D)

Name[2]	Description	Address	Type[1]	Default
RX FIFO Number of Frames Removed on Port 5	This register counts all frames removed from the RX FIFO for port 5 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 75 on page 128) • Frames are greater than the MaxFrameSize (Table 53 on page 104)	0x599	RR	0x00000000
RX FIFO Number of Frames Removed on Port 6	This register counts all frames removed from the RX FIFO for port 6 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 75 on page 128) • Frames are greater than the MaxFrameSize (Table 53 on page 104)	0x59A	RR	0x00000000
RX FIFO Number of Frames Removed on Port 7	This register counts all frames removed from the RX FIFO for port 7 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 75 on page 128) • Frames are greater than the MaxFrameSize (Table 53 on page 104)	0x59B	RR	0x00000000
RX FIFO Number of Frames Removed on Port 8	This register counts all frames removed from the RX FIFO for port 8 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 75 on page 128) • Frames are greater than the MaxFrameSize (Table 53 on page 104)	0x59C	RR	0x00000000
RX FIFO Number of Frames Removed on Port 9	This register counts all frames removed from the RX FIFO for port 9 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 75 on page 128) • Frames are greater than the MaxFrameSize (Table 53 on page 104)	0x59D	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write.
2. For all Number of Frames Removed Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:22 - Reserved and RO.
   Bits 21:0 - Described above.

Table 75. RX FIFO Errored Frame Drop Enable Register (Addr: 0x59F)

Bit	Name	Description	Type[1]	Default
Register Description: This register is used in conjunction with the RX Packet Filter Control Register bits to select whether errored or filtered frames are to be dropped.				0x00000000
31:10	Reserved	Reserved	RO	0x000000
9	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the "RX Packet Filter Control Register (Addr: Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 9: 0 = Do not drop frames 1 = Drop frames	R/W	0
8	RX FIFO Errored Frame Drop Enable Port 8	These bits are used in conjunction with the "RX Packet Filter Control Register (Addr: Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 8: 0 = Do not drop frames 1 = Drop frames	R/W	0
7	RX FIFO Errored Frame Drop Enable Port 7	These bits are used in conjunction with the "RX Packet Filter Control Register (Addr: Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 7: 0 = Do not drop frames 1 = Drop frames	R/W	0
6	RX FIFO Errored Frame Drop Enable Port 6	These bits are used in conjunction with the "RX Packet Filter Control Register (Addr: Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 6: 0 = Do not drop frames 1 = Drop frames	R/W	0
5	RX FIFO Errored Frame Drop Enable Port 5	These bits are used in conjunction with the "RX Packet Filter Control Register (Addr: Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 5: 0 = Do not drop frames 1 = Drop frames	R/W	0
4	RX FIFO Errored Frame Drop Enable Port 4	These bits are used in conjunction with the "RX Packet Filter Control Register (Addr: Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 4: 0 = Do not drop frames 1 = Drop frames	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 75. RX FIFO Errored Frame Drop Enable Register (Addr: 0x59F) (Continued)

Bit	Name	Description	Type[1]	Default
3	RX FIFO Errored Frame Drop Enable Port 3	These bits are used in conjunction with the "RX Packet Filter Control Register (Addr: Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 3: 0 = Do not drop frames 1 = Drop frames	R/W	0
2	RX FIFO Errored Frame Drop Enable Port 2	These bits are used in conjunction with the "RX Packet Filter Control Register (Addr: Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 2: 0 = Do not drop frames 1 = Drop frames	R/W	0
1	RX FIFO Errored Frame Drop Enable Port 1	These bits are used in conjunction with the "RX Packet Filter Control Register (Addr: Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 1: 0 = Do not drop frames 1 = Drop frames	R/W	0
0	RX FIFO Errored Frame Drop Enable Port 0	These bits are used in conjunction with the "RX Packet Filter Control Register (Addr: Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 0: 0 = Do not drop frames 1 = Drop frames	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 76. RX FIFO Overflow Event Register (Addr: 0x5A0)

Bit	Name	Description	Type[1]	Default
Register Description: This register provides a status if a FIFO-full situation has occurred (for example, a FIFO overflow). The bit position equals the port number. This register is cleared on Read.				0x00000000
31:10	Reserved	Reserved	RO	0x000000
9	RX FIFO Overflow Event Port 9	Port 9 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
8	RX FIFO Overflow Event Port 8	Port 8 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
7	RX FIFO Overflow Event Port 7	Port 7 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 76. RX FIFO Overflow Event Register (Addr: 0x5A0) (Continued)

Bit	Name	Description	Type[1]	Default
6	RX FIFO Overflow Event Port 6	Port 6 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
5	RX FIFO Overflow Event Port 5	Port 5 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
4	RX FIFO Overflow Event Port 4	Port 4 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
3	RX FIFO Overflow Event Port 3	Port 3 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
2	RX FIFO Overflow Event Port 2	Port 2 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
1	RX FIFO Overflow Event Port 1	Port 1 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
0	RX FIFO Overflow Event Port 0	Port 0 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

6.5.6 TX Block Register Overview

Table 77 through Table 82 on page 139 provide an overview of the TX Block Registers, which include the TX FIFO High and Low Watermark.

Table 77. TX FIFO High Watermark Ports 0 to 9 (Addr: 0x600 - 0x609)

Name[2]	Description	Address	Type[1]	Default
TX FIFO High Watermark Port 0	High watermark for TX FIFO port 0. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x600	R/W	0x00000630
TX FIFO High Watermark Port 1	High watermark for TX FIFO port 1. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x601	R/W	0x00000630
TX FIFO High Watermark Port 2	High watermark for TX FIFO port 2. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x602	R/W	0x00000630
TX FIFO High Watermark Port 3	High watermark for TX FIFO port 3. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x603	R/W	0x00000630
TX FIFO High Watermark Port 4	High watermark for TX FIFO port 4. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x604	R/W	0x00000630
TX FIFO High Watermark Port 5	High watermark for TX FIFO port 5. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x605	R/W	0x00000630
TX FIFO High Watermark Port 6	High watermark for TX FIFO port 6. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x606	R/W	0x00000630

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all TX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and RO.
   Bits 12:0 - Described above.

Table 77. TX FIFO High Watermark Ports 0 to 9 (Addr: 0x600 - 0x609) (Continued)

Name[2]	Description	Address	Type[1]	Default
TX FIFO High Watermark Port 7	High watermark for TX FIFO port 7. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x607	R/W	0x00000630
TX FIFO High Watermark Port 8	High watermark for TX FIFO port 8. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x608	R/W	0x00000630
TX FIFO High Watermark Port 9	High watermark for TX FIFO port 9. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x609	R/W	0x00000630

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all TX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and RO.
   Bits 12:0 - Described above.

Table 78. TX FIFO Low Watermark Ports 0 to 9 (Addr: 0x60A - 0x613)

Name[2]	Description	Address	Type[1]	Default
TX FIFO Low Watermark Port 0	Low watermark for TX FIFO port 0. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60A	R/W	0x000001D0
TX FIFO Low Watermark Port 1	Low watermark for TX FIFO port 1. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60B	R/W	0x000001D0
TX FIFO Low Watermark Port 2	Low watermark for TX FIFO port 2. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60C	R/W	0x000001D0
TX FIFO Low Watermark Port 3	Low watermark for TX FIFO port 3. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60D	R/W	0x000001D0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all TX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and RO.
   Bits 12:0 - Described above.

Table 78. TX FIFO Low Watermark Ports 0 to 9 (Addr: 0x60A - 0x613) (Continued)

Name[2]	Description	Address	Type[1]	Default
TX FIFO Low Watermark Port 4	Low watermark for TX FIFO port 4. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60E	R/W	0x000001D0
TX FIFO Low Watermark Port 5	Low watermark for TX FIFO port 5. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60F	R/W	0x000001D0
TX FIFO Low Watermark Port 6	Low watermark for TX FIFO port 6. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x610	R/W	0x000001D0
TX FIFO Low Watermark Port 7	Low watermark for TX FIFO port 7. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x611	R/W	0x000001D0
TX FIFO Low Watermark Port 8	Low watermark for TX FIFO port 8. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x612	R/W	0x000001D0
TX FIFO Low Watermark Port 9	Low watermark for TX FIFO port 9. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x613	R/W	0x000001D0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all TX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and RO.
   Bits 12:0 - Described above.

Table 79. TX FIFO MAC Transfer Threshold Ports 0 to 9 (Addr: 0x614 - 0x61D)

Name[2]	Description[3]	Address	Type[1]	Default
TX FIFO MAC Transfer Threshold Port 0	Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, and the threshold is set in increments of 8-byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x614	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 1	Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, and the threshold is set in increments of 8-byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x615	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 2	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x616	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 3	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x617	R/W	0x00000100

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all MAC Transfer Threshold Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and RO.
   Bits 12:0 - Described above.
3. For proper operation of the IXF1110, the MAC transfer threshold must be set to greater than the MaxBurst1 on the SPI4-2.

Table 79. TX FIFO MAC Transfer Threshold Ports 0 to 9 (Addr: 0x614 - 0x61D) (Continued)

Name[2]	Description[3]	Address	Type[1]	Default
TX FIFO MAC Transfer Threshold Port 4	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x618	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 5	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x619	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 6	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x61A	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 7	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x61B	R/W	0x00000100

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all MAC Transfer Threshold Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and RO.
   Bits 12:0 - Described above.
3. For proper operation of the IXF1110, the MAC transfer threshold must be set to greater than the MaxBurst1 on the SPI4-2.

Table 79. TX FIFO MAC Transfer Threshold Ports 0 to 9 (Addr: 0x614 - 0x61D) (Continued)

Name[2]	Description[3]	Address	Type[1]	Default
TX FIFO MAC Transfer Threshold Port 8	Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x61C	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 9	Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x61D	R/W	0x00000100

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all MAC Transfer Threshold Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and RO.
   Bits 12:0 - Described above.
3. For proper operation of the IXF1110, the MAC transfer threshold must be set to greater than the MaxBurst1 on the SPI4-2.

Table 80. TX FIFO Overflow Event Register (Addr: 0x61E)

Bit	Name	Description	Type[1]	Default
Register Description: This register provides status that a FIFO- full situation has occurred (for example, a FIFO overflow). The bit position equals the port number. This register is cleared on Read.				0x00000000
31:10	Reserved	Reserved	RO	0x000000
9	TX FIFO Overflow Event Port 9	Port 9 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
8	TX FIFO Overflow Event Port 8	Port 8 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
7	TX FIFO Overflow Event Port 7	Port 7 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
6	TX FIFO Overflow Event Port 6	Port 6 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
5	TX FIFO Overflow Event Port 5	Port 5 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
4	TX FIFO Overflow Event Port 4	Port 4 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
3	TX FIFO Overflow Event Port 3	Port 3 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
2	TX FIFO Overflow Event Port 2	Port 2 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
1	TX FIFO Overflow Event Port 1	Port 1 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
0	TX FIFO Overflow Event Port 0	Port 0 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 81. TX FIFO Info Out-of-Sequence Register (Addr: 0x621)

Bit	Name	Description	Type[1]	Default
Register Description: This register signals when out-of-sequence data is detected in the TX FIFO. Events such as SOP followed by another SOP cause this bit to be set and remain so until read. This register is cleared on Read.				0x00000000
31:10	Reserved	Reserved	RO	0x000000
9	TX FIFO Info Out-of-Sequence Port 9	Port 9 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
8	TX FIFO Info Out-of-Sequence Port 8	Port 8 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
7	TX FIFO Info Out-of-Sequence Port 7	Port 7 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
6	TX FIFO Info Out-of-Sequence Port 6	Port 6 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
5	TX FIFO Info Out-of-Sequence Port 5	Port 5 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
4	TX FIFO Info Out-of-Sequence Port 4	Port 4 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
3	TX FIFO Info Out-of-Sequence Port 3	Port 3 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
2	TX FIFO Info Out-of-Sequence Port 2	Port 2 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
1	TX FIFO Info Out-of-Sequence Port 1	Port 1 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
0	TX FIFO Info Out-of-Sequence Port 0	Port 0 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 82. TX FIFO Number of Frames Removed Ports 0-9 (Addr: 0x622 - 0x62B)

Name	Description	Address	Type[1]	Default
TX FIFO Number of Frames Removed on Port 0	This register counts the number of frames removed on port 0 due to a TX FIFO overflow.	0x622	RR	0x00000000
TX FIFO Number of Frames Removed on Port 1	This register counts the number of frames removed on port 1 due to a TX FIFO overflow.	0x623	RR	0x00000000
TX FIFO Number of Frames Removed on Port 2	This register counts the number of frames removed on port 2 due to a TX FIFO overflow.	0x624	RR	0x00000000
TX FIFO Number of Frames Removed on Port 3	This register counts the number of frames removed on port 3 due to a TX FIFO overflow.	0x625	RR	0x00000000
TX FIFO Number of Frames Removed on Port 4	This register counts the number of frames removed on port 4 due to a TX FIFO overflow.	0x626	RR	0x00000000
TX FIFO Number of Frames Removed on Port 5	This register counts the number of frames removed on port 5 due to a TX FIFO overflow.	0x627	RR	0x00000000
TX FIFO Number of Frames Removed on Port 6	This register counts the number of frames removed on port 6 due to a TX FIFO overflow.	0x628	RR	0x00000000
TX FIFO Number of Frames Removed on Port 7	This register counts the number of frames removed on port 7 due to a TX FIFO overflow.	0x629	RR	0x00000000
TX FIFO Number of Frames Removed on Port 8	This register counts the number of frames removed on port 8 due to a TX FIFO overflow.	0x62A	RR	0x00000000
TX FIFO Number of Frames Removed on Port 9	This register counts the number of frames removed on port 9 due to a TX FIFO overflow.	0x62B	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

6.5.7 SPI4-2 Block Register Overview

Table 83 through Table 86 on page 142 provide an overview of the SPI4-2 Block Registers.

Table 83. SPI4-2 RX Burst Size Register (Addr: 0x700)

Bit	Name	Description	Type[1]	Default
Register Description: SPI4-2 RX interface start-up parameters for burst size.				0x00060002
31	idles	1 = Inserts four idle control words between each burst. (This occurs not only on an EOP, but also at the end of every MaxBurst1 or MaxBurst2.) 0 = Zero idle insertion between transfer bursts.	R/W	0x0
30:25	Reserved	Reserved	RO	0x00
24:16	MaxBurst1	Maximum number of 16-byte blocks that the FIFO in the receive path, external to IXF1110, can accept when the FIFO Status channel indicates STARVING.	R/W	0x006
15:9	Reserved	Reserved	RO	0x00
8:0	MaxBurst2	Maximum number of 16-byte blocks that the FIFO in the receive path, external to the IXF1110, can accept when the FIFO Status channel indicates HUNGRY.	R/W	0x002
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 84. SPI4-2 RX Training Register (Addr: 0x701)

Bit	Name	Description	Type[1]	Default
Register Description: SPI4-2 RX interface start-up parameters for training sequences				0x00000000
31:24	Reserved	Reserved	RO	0x00
23:16	REP_T	Number of repetitions of the data training sequence that must be scheduled every DATA_MAX_T cycles	R/W	0x00
15:0	DATA_MAX_T[2]	Maximum interval (in number of cycles) between scheduling of training sequences on receive data path interface An all zero value disables periodic training sequences.	R/W	0x0000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write 2. The value of DATA_MAX_T is the Most Significant 16 bits of a 24-bit counter value. The Least Significant 8 bits are always 0x00. This allows for a much larger DAT_MAX_T time-out period and provides a more than adequate granularity of selection.				

Table 85. SPI4-2 RX Calendar Register (Addr: 0x702)

Bit	Name	Description	Type[1]	Default Value
Register Description: SPI4-2 RX interface start-up parameters for FIFO status calendar operation.				0x00010300
31:30	RX Train Test Modes	00 = Normal mode. 01 = Do not enter training based on a repeating “11” pattern on RSTAT[1:0] 1x = Train continuously	R/W	0x0
29	RSCLK_invert	1 = The FIFO status is captured on the falling edge of RSCLK 0 = The FIFO status is captured on the rising edge of the RSCLK as per the SPI4-2 specification.	R/W	0
28	TSCLK_invert	1 = The FIFO status is launched on the falling edge of TSCLK 0 = The FIFO status is launched on the rising edge of the TSCLK as per the SPI4-2 specification.	R/W	0
27:21	Reserved	Reserved	RO	0x000
20	DIP2_Error	Set based on an incorrect RX DIP2 result. This bit is cleared upon a read	RR	0x0
19:16	DIP-2_Thr	Defines how many consecutive correct DIP-2s are required to disable sending of training sequences on the RX SPI4-2.	R/W	0x1
15:14	Reserved	Reserved	RO	0x0
13	RX SPI4 Sync	1 = RX SPI4 Out Of Training (RDAT = idles). 0 = RX SPI4 In Training (RDAT = training).	RO	0
12	TX SPI4 Sync	1 = The TX SPI4-2 has received the valid training patterns on TDAT and is now sending a 10 port Calendar on TSAT with valid FIFO information. 0 = TX SPI4-2 Calendar is in constant Framing.	RO	0
11:8	Loss_of_Sync	Loss-of-Sync is a parameter specifying the number of consecutive framing calendar cycles required to indicate a loss of synchronization and restart training sequences.	R/W	0x3
7:4	Reserved	Reserved	RO	0x0
3:0	CAL_M	Number of times FIFO status for ports 0 through 9 repeat between framing and DIP-2 cycles over the default value of 1.	R/W	0x0
1. R0 = Read Only; RR = Clear on Read; W = Write only; R/W = Read/Write				

Table 86. SPI4-2 TX Synchronization Register (Addr: 0x703)

Bit	Name	Description	Type[1]	Default
Register Description: SPI4-2 synchronization DIP-4 counters.				0x00000420
31:16	DIP4_Errors	DIP4_Errors is the total number of DIP4 errors detected since this register was last read.	RR	0x0000
15:8	DIP4_UnLock[2]	DIP-4_Unlock is a SPI4-2 parameter specifying the number of incorrect DIP4 fields to be detected to declare loss of synchronization and drive the TSTAT[1:0] bus with framing.	R/W	0x04
7:0	DIP4_Lock	Number of consecutive correct DIP4 results to achieve synchronization and end training	R/W	0x20

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. When Periodic Training is enabled, the actual count of DIP4 errors required to lose synchronization is 1 less than the programmed value in this register. Therefore, this value should always be programmed to be 1 more than the desired value and should never be programmed to either 0 or 1.

6.5.8 SerDes Register Overview

Table 87 through Table 89 on page 143 define the contents of the SerDes Register Block at base location 0x780 which contain the control and status for the ten SerDes interfaces on the IXF1110.

Table 87. TX and RX AC/DC Coupling Selection Register (Addr: 0x780)

Bit	Name	Description	Type[1]	Default
Register Description: Allows selection of AC or DC coupling on the output of each SerDes port (TX and RX are independent)				0x00000000
31:20	Reserved	Reserved	RO	0x000
19	RxACDC9	Selects line coupling mode, AC = 0, DC = 1	R/W	0
18	TxACDC9	Selects line coupling mode, AC = 0, DC = 1	R/W	0
17	RxACDC8	Selects line coupling mode, AC = 0, DC = 1	R/W	0
16	TxACDC8	Selects line coupling mode, AC = 0, DC = 1	R/W	0
15	RxACDC7	Selects line coupling mode, AC = 0, DC = 1	R/W	0
14	TxACDC7	Selects line coupling mode, AC = 0, DC = 1	R/W	0
13	RxACDC6	Selects line coupling mode, AC = 0, DC = 1	R/W	0
12	TxACDC6	Selects line coupling mode, AC = 0, DC = 1	R/W	0
11	RxACDC5	Selects line coupling mode, AC = 0, DC = 1	R/W	0
10	TxACDC5	Selects line coupling mode, AC = 0, DC = 1	R/W	0
9	RxACDC4	Selects line coupling mode, AC = 0, DC = 1	R/W	0
8	TxACDC4	Selects line coupling mode, AC = 0, DC = 1	R/W	0
7	RxACDC3	Selects line coupling mode, AC = 0, DC = 1	R/W	0
6	TxACDC3	Selects line coupling mode, AC = 0, DC = 1	R/W	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 87. TX and RX AC/DC Coupling Selection Register (Addr: 0x780) (Continued)

Bit	Name	Description	Type[1]	Default
5	RxACDC2	Selects line coupling mode, AC = 0, DC = 1	R/W	0
4	TxACDC2	Selects line coupling mode, AC = 0, DC = 1	R/W	0
3	RxACDC1	Selects line coupling mode, AC = 0, DC = 1	R/W	0
2	TxACDC1	Selects line coupling mode, AC = 0, DC = 1	R/W	0
1	RxACDC0	Selects line coupling mode, AC = 0, DC = 1	R/W	0
0	TxACDC0	Selects line coupling mode, AC = 0, DC = 1	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 88. Tx and Rx Power-Down Ports 0-9 Register (Addr: 0x787)

Bit	Name	Description	Type[1]	Default
Register Description: Tx and Rx power-down bits to allow per-port power-down of unused ports				0x00000000
31:20	Reserved	Reserved	RO	0x000
19:10	TPWRDWN[9:0]	Tx power-down for Ports 9-0 (1 = Power-down)	R/W	0000000000
9:0	RPWRDWN[9:0]	Rx Power-Down power-down for Ports 9-0 (1 = Power-down)	R/W	0000000000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 89. Rx Signal Detect Level Ports 0-9 Register (Addr: 0x793)

Bit	Name	Description	Type[1]	Default
Register Description: This register shows the status of the Rx input in relation to the level of the signal being received from the line, and is mainly used for debug and test purposes.				0x00000000
31:10	Reserved	Reserved	RO	0x000000
9	RX Signal Detect Port 9	Signal Detect for Port 9 0 = Noise 1 = Signal	RO	0
8	RX Signal Detect Port 8	Signal Detect for Port 8 0 = Noise 1 = Signal	RO	0
7	RX Signal Detect Port 7	Signal Detect for Port 7 0 = Noise 1 = Signal	RO	0
6	RX Signal Detect Port 6	Signal Detect for Port 6 0 = Noise 1 = Signal	RO	0
5	RX Signal Detect Port 5	Signal Detect for Port 5 0 = Noise 1 = Signal	RO	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 89. Rx Signal Detect Level Ports 0-9 Register (Addr: 0x793) (Continued)

Bit	Name	Description	Type[1]	Default
4	RX Signal Detect Port 4	Signal Detect for Port 4 0 = Noise 1 = Signal	RO	0
3	RX Signal Detect Port 3	Signal Detect for Port 3 0 = Noise 1 = Signal	RO	0
2	RX Signal Detect Port 2	Signal Detect for Port 2 0 = Noise 1 = Signal	RO	0
1	RX Signal Detect Port 1	Signal Detect for Port 1 0 = Noise 1 = Signal	RO	0
0	RX Signal Detect Port 0	Signal Detect for Port 0 0 = Noise 1 = Signal	RO	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

6.5.9 GBIC Block Register Overview

Table 90 through Table 93 provide an overview of the GBIC Block Registers. These registers provide a means to control and monitor the interface to the GBIC modules.

Table 90. GBIC Status Register Ports 0-9 (Addr: 0x799)

Bit	Name	Description	Type[1]	Default
Register Description: This register provides GBIC status information.				0x00000000
31:30	Reserved	Reserved	RO	00
29:20	RX_LOS_9:0	RX_LOS inputs for Ports 0-9	RO	0000000000
19:10	TX_FAULT_9:0	TX_FAULT inputs for Ports 0-9	RO	0000000000
9:0	MOD_DEF_9:0	MOD_DEF inputs for Ports 0-9	RO	0000000000
1. RO = Read Only; RR = Clear on Read; W = Write only; R/W = Read/Write				

Table 91. GBIC Control Register Ports 0-9 Register (Addr: 0x79A)

Bit	Name	Description	Type[1]	Default
Register Description: This register provides access to GBIC interrupt enables and TX_DISABLE status information.				0x00000000
31:13	Reserved	Reserved	RO	0000000000 000000000
12	RX_LOS_En	Enable for RX_LOS_Int operation (Enabled = 1)	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write only; R/W = Read/Write				

Table 91. GBIC Control Register Ports 0-9 Register (Addr: 0x79A)

Bit	Name	Description	Type[1]	Default
11	TX_FAULT_En	Enable for TX_FAULT_Int operation (Enabled = 1)	R/W	0
10	MOD_DEF_En	Enable for MOD_DEF_Int operation (Enabled = 1)	R/W	0
9:0	TX_DISABLE_9:0	TX_DISABLE outputs for Ports 0-9	R/W	0000000000
1. RO = Read Only; RR = Clear on Read; W = Write only; R/W = Read/Write				

Table 92. I²C Control Register Ports 9-0 Register (Addr: 0x79B)

Bit	Name	Description	Type[1]	Default
Register Description: This register controls I²C Reads and Writes.				0x00000000
31:29	Reserved	Reserved	RO	000
28	Port Address Error	Port Address Error is set to 1 when an access is requested to port address > 0x9.	RO	0
27	WP_Err	Write Protect error is set to 1 when a write access is requested to Device ID = 0xA and Register Address [10:8] = 0. This address combination is used solely for the read only GBIC.	RO	0
26	no_ack-err	This bit is set to 1 when a GBIC has failed to assert an acknowledge cycle. This signal should be used to validate the data being read. Data is only valid if this bit is equal to zero.	RO	0
25	I²CEnable	Enables device wide I²C Accesses (Enabled = 1)	R/W	0
24	I²C Start	I²C Start = 1 will initiate the I²C cycle. This bit is clear on read.	RR	0
23	Reserved	Reserved	RO	0
22	Write Complete	Write Complete is set to a 1 when the byte write cycle has completed.	RO	0
21	Reserved	Reserved	RO	0
20	Read Valid	Read Valid is set to a 1 when valid data is available in the DataRead7:0 field.	RO	0
19:16	Port Address Select 3:0	Address of the IXF1110 port to be accessed	R/W	0x0
15	Read/Write	1 = Read, 0 = Write.	R/W	1
14:11	Device ID	Most Significant 4 bits of Device ID/Address field.	R/W	0xA
10:0	Register Address	Bits 10:8 define least significant 3 bits of Device ID/ Address field. Bits 7:0 define the register address.	R/W	00000000000
1. RO = Read Only; RR = Clear on Read; W = Write only; R/W = Read/Write				

Table 93. I²C Data Register Ports 9-0 Register (Addr: 0x79C)

Bit	Name	Description	Type[1]	Default
Register Description: This register provides I²C Reads and Writes.				0x00000000
31:24	Reserved	Reserved	RO	0x00
23:16	Write Data	Write_Data contains the data to be written during the I²C byte write cycle.	R/W	0x00
15:8	Reserved	Reserved	RO	0x00
7:0	Read_Data	Read_Data contains the byte received during the last I²C Read Cycle.	RO	0x00
1. RO = Read Only; RR = Clear on Read; W = Write only; R/W = Read/Write				

7.0 Package Overview

CBGA packages are suited for applications requiring high I/O counts and high electrical performance. They are recommended for high-power applications, having high noise immunity requirements.

7.1 Features

- Flip chip die attach; surface mount second-level interconnect
- High electrical performance
- High I/O counts
- Area array I/O options
- Multiple power zone offering supports core and four additional voltages
- JEDEC-compliant package

7.2 Package Specifics for the IXF1110

The IXF1110 uses the following packaging (see Figure 43, “IXF1110 552-Ceramic Ball Grid Array (CBGA) Package Specification” on page 149):

- 552-ball CBGA
- Ball pitch of 1.0 mm
- Overall package dimensions of 25 mm x 25 mm

7.2.1 Markings

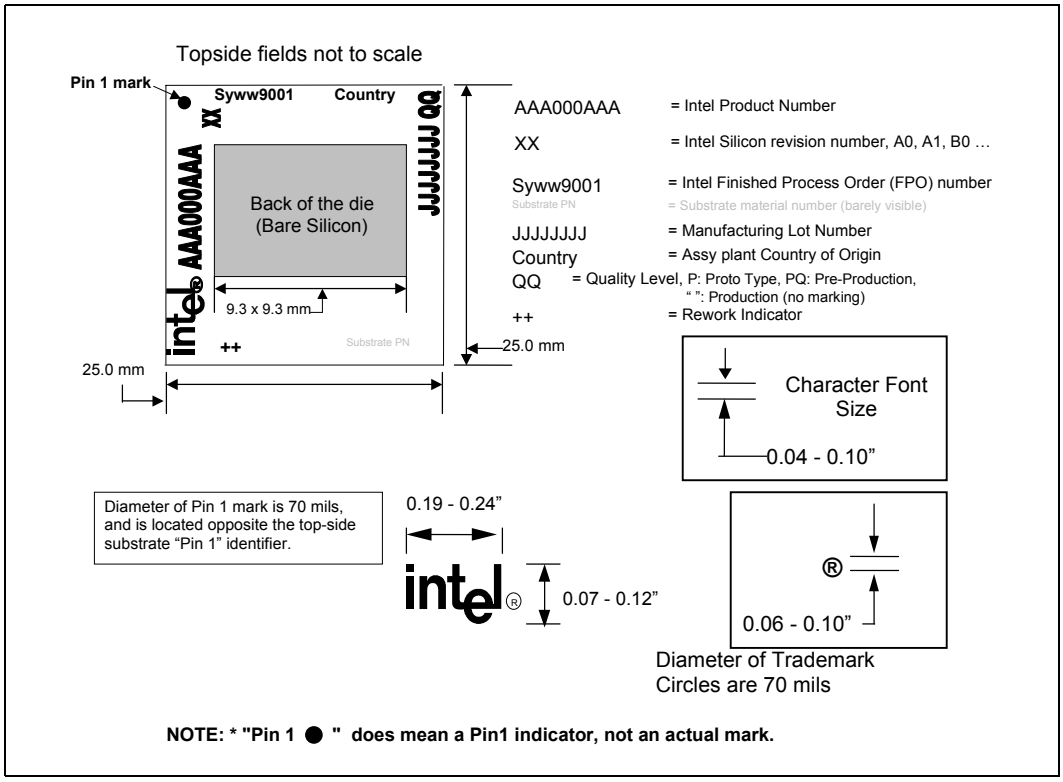
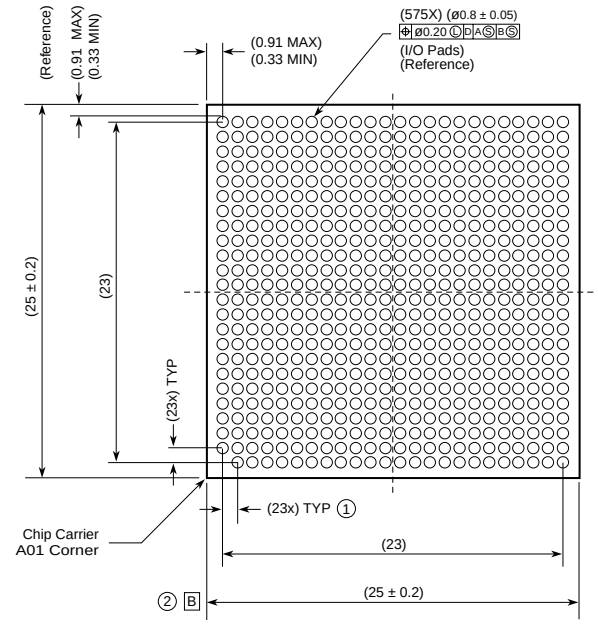
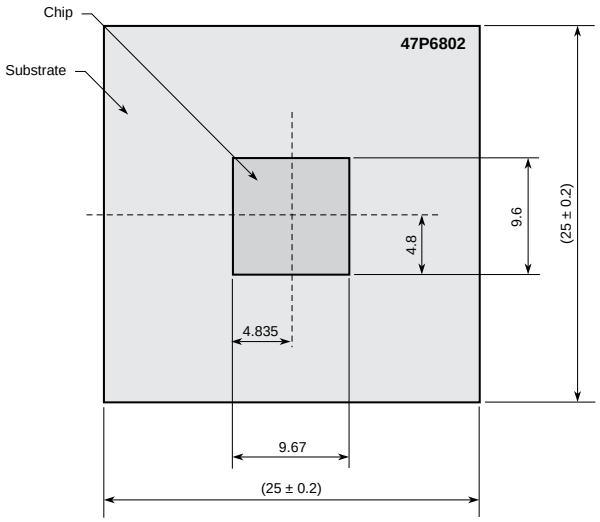


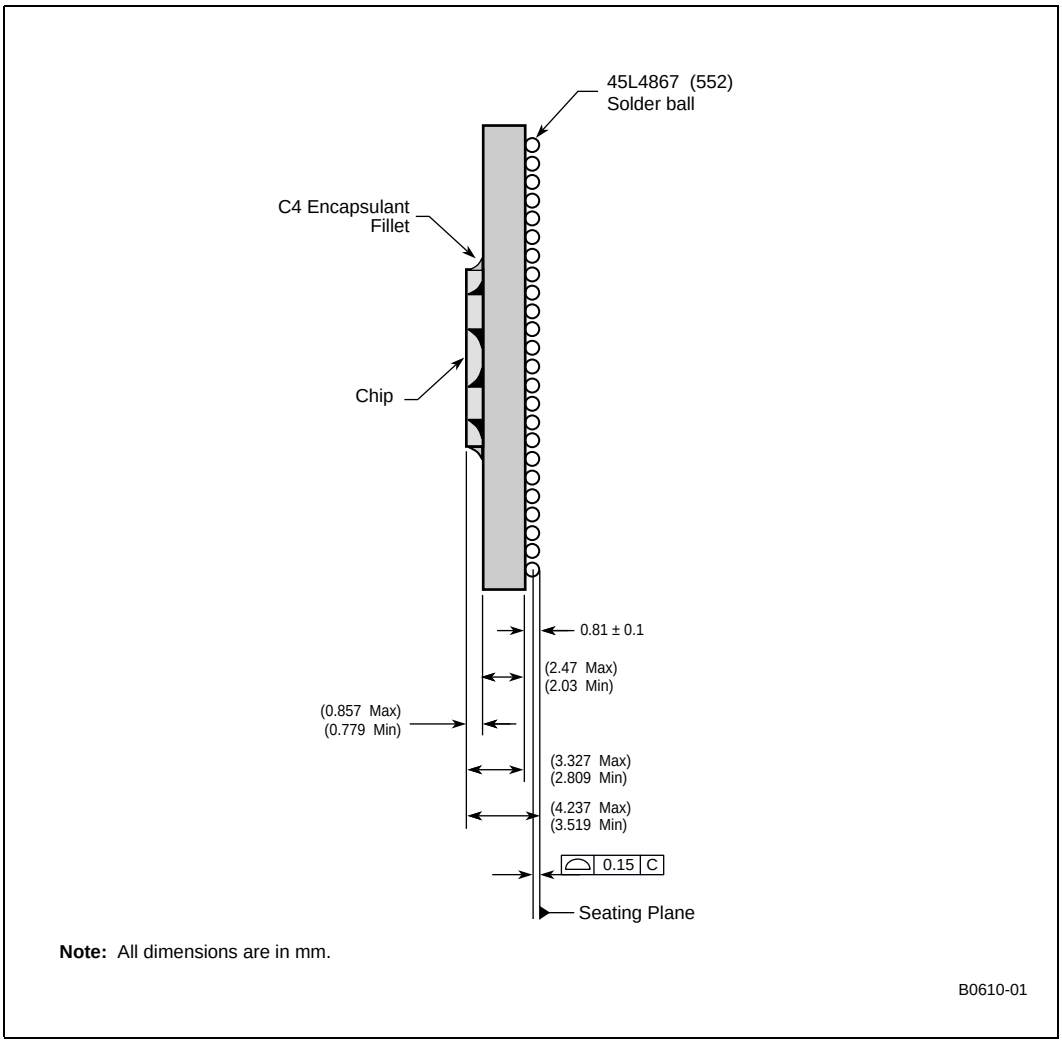
Figure 43. IXF1110 552-Ceramic Ball Grid Array (CBGA) Package Specification





Note: All dimensions are in mm.

Figure 44. IXF1110 CBGA Package Side View Diagram



8.0 Product Ordering Information

Table 94. Product Information

Number	Revision	Qualification	MM Number	Ship Media
HFIXF1110CC.A2 QE000	A2	Q	848598	Tray
HF1110CC.A2 SMPL QE000	A2	Q	849909	Tray

Figure 45. Ordering Information - Sample