CYRS1542AV18
CYRS1544AV18

72-Mbit QDR® II+ SRAM Two-Word Burst Architecture with RadStop™ Technology

Radiation Performance

Radiation Data

- Total Dose = 300 Krad
- Soft error rate (both Heavy Ion and proton)
  Heavy ions ≤ 1 × 10^{-10} upsets/bit-day with single error correction - double error detection error detection and correction (SEC-DED EDAC)
- Neutrons = 2.0 × 10^{14} N/cm^2
- Dose rate = 2.0 × 10^9 rad(Si)/sec
- Dose rate survivability (rad(Si)/sec) = 1.5 × 10^11 rad(Si)/sec
- Latch up immunity = 120 MeV.cm^2/mg (125 °C)

Prototyping Options

- Non qualified CYPT1542AV18 and CTPY1544AV18 devices with same functional and timing characteristics in a 165-ball Ceramic Column Grid Array (CCGA) package

Features

- Separate independent read and write data ports
  - Supports concurrent transactions
- 250-MHz clock for high bandwidth
- 2-word burst on all accesses
- Double data rate (DDR) interfaces on both read and write ports at 250 MHz (data transferred at 500 MHz)
- Two input clocks (K and $\overline{K}$) for precise DDR timing
  - SRAM uses rising edges only
- Echo clocks (CQ and $\overline{CQ}$) simplify data capture in high speed systems
- Single multiplexed address input bus latches address inputs for both read and write ports
- Separate port selects for depth expansion
- Synchronous internally self-timed writes
- QDR® II operates with 2.0 cycle read latency when delay lock loop (DLL) is enabled
- Available in × 18 and × 36 configurations
- Full data coherency, providing most current data
- Core V_{DD} = 1.8 V (±0.1 V); I/O V_{DDQ} = 1.4 V to V_{DD}
- Available in 165-ball CCGA (21 × 25 × 2.83 mm)
- HSTL inputs and variable drive HSTL output buffers
- JTAG 1149.1 compatible test access port
- DLL for accurate data placement

Configurations

CYRS1542AV18 – 4 M × 18

CYRS1544AV18 – 2 M × 36

Functional Description

The CYRS1542AV18 and CYRS1544AV18 are synchronous pipelined SRAMs, equipped with 1.8-V QDR II+ architecture with RadStop™ technology. Cypress's state-of-the-art RadStop Technology is radiation hardened through proprietary design and process hardening techniques.

The QDR II+ architecture has separate data inputs and data outputs to completely eliminate the need to turnaround the data bus that exists with common I/O devices. Access to each port is through a common address bus. Addresses for read and write addresses are latched on alternate rising edges of the input (K) clock. Accesses to the QDR II+ read and write ports are completely independent of one another. To maximize data throughput, both read and write ports are equipped with DDR interfaces. Each address location is associated with two 18-bit words (CYRS1542AV18), or 36-bit words (CYRS1544AV18) that burst sequentially into or out of the device. Because data can be transferred into and out of the device on every rising edge of both input clocks (K and $\overline{K}$), memory bandwidth is maximized while simplifying system design by eliminating bus turnarounds.

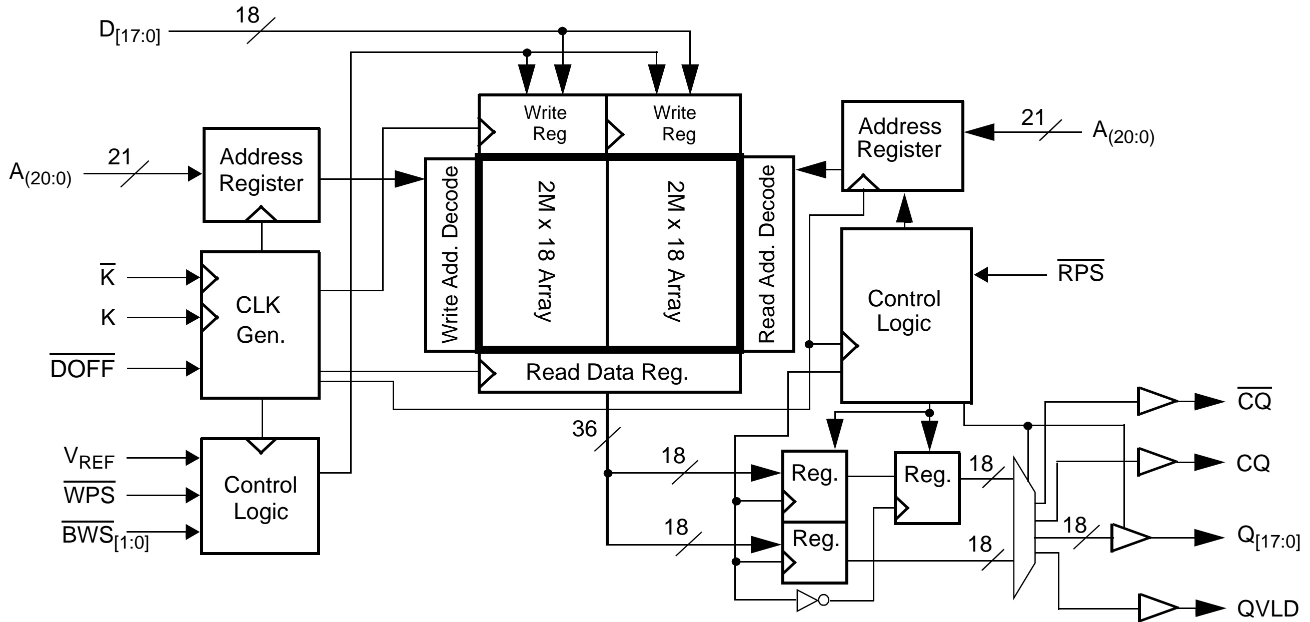
Depth expansion is accomplished with port selects, which enables each port to operate independently.

All synchronous inputs pass through input registers controlled by the K or $\overline{K}$ input clocks. All data outputs pass through output registers controlled by the K or $\overline{K}$ input clocks. Writes are conducted with on-chip synchronous self-timed write circuitry.

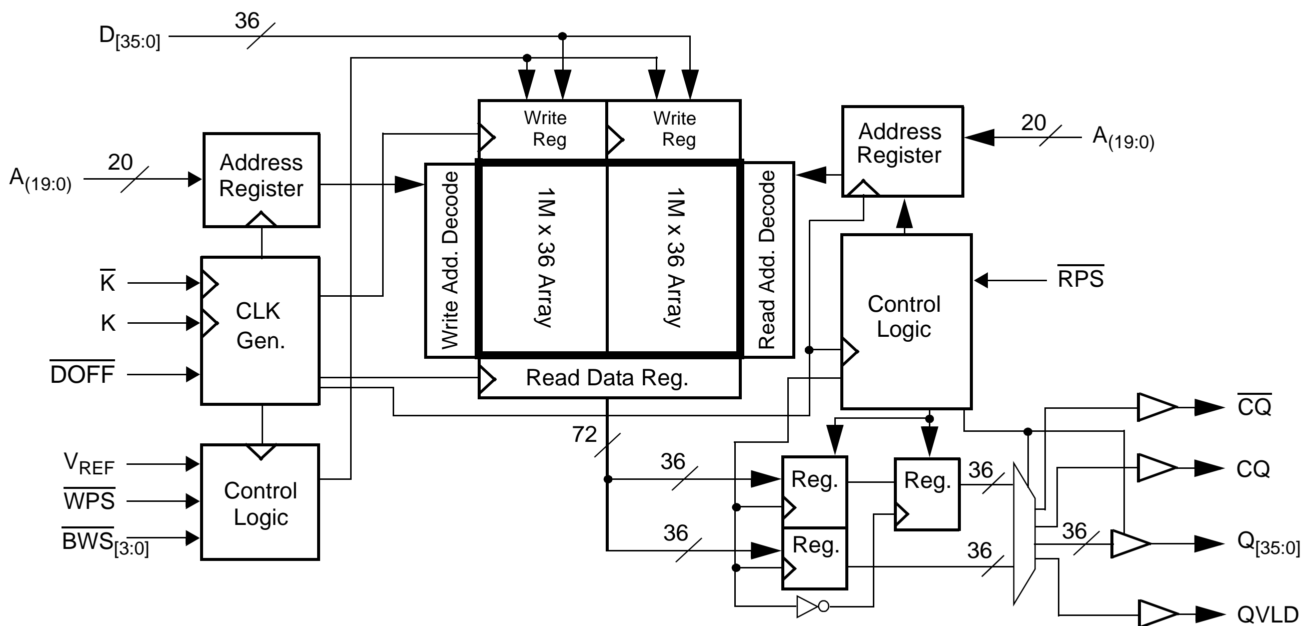
Selection Guide

Description		250 MHz	Unit
Maximum operating frequency		250	MHz
Maximum operating current (concurrent R/W)	× 18	1650	mA
	× 36	1650	

Logic Block Diagram – CYRS1542AV18



Logic Block Diagram – CYRS1544AV18



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Manufacturing Flow

Step	Screen	Method	Requirement
1	Wafer lot acceptance test	TM 5007	–
2	Internal visual	2010, Condition A	100%
3	Serialization		100%
4	Temperature cycling	1010, Condition C, 50 cycles minimum	100%
5 6	Constant acceleration	2001, YI orientation only Condition TBD (package in design)	100%
7	Particle impact noise detection (PIND)	2020 Condition A	100%
8	Radiographic (X-ray)	2012, one view (Y-1 orientation) only	
9	Pre burn in electrical parameters	In accordance with applicable Cypress specification	100%
10	Dynamic burn in	1015, Condition D 240 hours at 125 °C or 120 hours at 150 °C minimum	100%
11	Interim (post dynamic burn in) electricals	In accordance with applicable Cypress device specifications	100%
12	Static burn in	1015, Condition C, 72 hours at 150 °C or 144 hours at 125 °C minimum	100%
13	Interim (post static burn in) electricals	In accordance with applicable Cypress device specifications	100%
14	Percent defective allowable (PDA) calculation	5% overall, 3% functional parameters at 25 °C	All lots
15	Final electrical test a. Static tests (1) 25 °C (2) –55 °C and +125 °C b. Functional tests (1) 25 °C (2) –55 °C and +125 °C c. Switching test at 25 °C	In accordance with applicable Cypress device specifications 5005, Table I, Subgroup 1 5005, Table I, Subgroup 2, 3 5005, Table I, Subgroup 7 5005, Table I, Subgroup 8a, 8b 5005, Table I, Subgroup 9	100%
16	Seal (fine and gross leak test)	1014	100%
17	External visual	2009	100%
18	Wafer lot specific life test (Group C)	Mil-PRF 38535, Appendix B, section B.4.2.c	All wafer lots

Radiation Hardened Design

The single event latch up (SEL) immunity is improved by a radiation hardened design technique developed by Cypress called RadStop. This design mitigation technique allows the SEL performance to achieve radiation hard performance levels.

Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical single-bit upsets	25 °C	320	368	FIT/ Mb
LMBU	Logical multi-bit upsets	25 °C	0	0.01	FIT/ Mb
SEL	Single event latch up	85 °C	0	0.1	FIT/ Dev

* *No LMBU or SEL events occurred during testing*; this column represents a statistical χ^2, 95% confidence limit calculation. For more details refer to application note AN54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates"

Pin Configuration

Pin configurations for CYRS1542AV18 and CYRS1544AV18.[1]

Figure 1. 165-ball CCGA pinout

CYRS1542AV18 (4 M × 18)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/144M	A	$\overline{WPS}$	$\overline{BWS_1}$	$\overline{K}$	NC/288M	$\overline{RPS}$	A	A	CQ
B	NC	Q9	D9	A	NC	K	$\overline{BWS_0}$	A	NC	NC	Q8
C	NC	NC	D10	V_{SS}	A	A	A	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	A	A	A	V_{SS}	NC	NC	D1
P	NC	NC	Q17	A	A	QVLD	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

CYRS1544AV18 (2 M × 36)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/288M	A	$\overline{WPS}$	$\overline{BWS_2}$	$\overline{K}$	$\overline{BWS_1}$	$\overline{RPS}$	A	NC/144M	CQ
B	Q27	Q18	D18	A	$\overline{BWS_3}$	K	$\overline{BWS_0}$	A	D17	Q17	Q8
C	D27	Q28	D19	V_{SS}	A	A	A	V_{SS}	D16	Q7	D8
D	D28	D20	Q19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q16	D15	D7
E	Q29	D29	Q20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	Q15	D6	Q6
F	Q30	Q21	D21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D14	Q14	Q5
G	D30	D22	Q22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q13	D13	D5
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	D31	Q31	D23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D12	Q4	D4
K	Q32	D32	Q23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q12	D3	Q3
L	Q33	Q24	D24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	D11	Q11	Q2
M	D33	Q34	D25	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D10	Q1	D2
N	D34	D26	Q25	V_{SS}	A	A	A	V_{SS}	Q10	D9	D1
P	Q35	D35	Q26	A	A	QVLD	A	A	Q9	D0	Q0
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

Note

1. NC/144M and NC/288M are not connected to the die and can be tied to any voltage level.

Pin Definitions

Pin Name	I/O	Pin Description
$D_{[x:0]}$	Input-Synchronous	**Data input signals**. Sampled on the rising edge of K and $\overline{K}$ clocks during valid write operations. CYRS1542AV18 – $D_{[17:0]}$ CYRS1544AV18 – $D_{[35:0]}$
$\overline{WPS}$	Input-Synchronous	**Write port select – Active LOW**. Sampled on the rising edge of the K clock. When asserted active, a write operation is initiated. Deasserting deselects the write port. Deselecting the write port ignores $D_{[x:0]}$.
$\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$	Input-Synchronous	**Byte write select (BWS) 0, 1, 2, and 3 – Active LOW**. Sampled on the rising edge of the K and $\overline{K}$ clocks during write operations. Used to select which byte is written into the device during the current portion of the write operations. Bytes not written remain unaltered. CYRS1542AV18 – $\overline{BWS_0}$ controls $D_{[8:0]}$ and $\overline{BWS_1}$ controls $D_{[17:9]}$. CYRS1544AV18 – $\overline{BWS_0}$ controls $D_{[8:0]}$, $\overline{BWS_1}$ controls $D_{[17:9]}$, $\overline{BWS_2}$ controls $D_{[26:18]}$ and $\overline{BWS_3}$ controls $D_{[35:27]}$. All the BWS are sampled on the same edge as the data. Deselecting a BWS ignores the corresponding byte of data and it is not written into the device.
A	Input-Synchronous	**Address inputs**. Sampled on the rising edge of the K (read address) and $\overline{K}$ (write address) clocks during active read and write operations. These address inputs are multiplexed for both read and write operations. Internally, the device is organized as 4 M × 18 (2 arrays each of 2 M × 18) for CYRS1542AV18, and 2 M × 36 (2 arrays each of 1 M × 36) for CYRS1544AV18. Therefore, only 21 address inputs are needed to access the entire memory array of CYRS1542AV18, and 20 address inputs for CYRS1544AV18. These inputs are ignored when the appropriate port is deselected.
$Q_{[x:0]}$	Output-Synchronous	**Data output signals**. These pins drive out the requested data during a read operation. Valid data is driven out on the rising edge of the K and $\overline{K}$ clock. When the read port is deselected, $Q_{[x:0]}$ are automatically tristated. CYRS1542AV18 – $Q_{[17:0]}$ CYRS1544AV18 – $Q_{[35:0]}$
$\overline{RPS}$	Input-Synchronous	**Read port select – Active LOW**. Sampled on the rising edge of positive input clock (K). When active, a read operation is initiated. Deasserting deselects the read port. When deselected, the pending access is allowed to complete and the output drivers are automatically tristated following the next rising edge of the K clock. Each read access consists of a burst of four sequential transfers.
QVLD	Valid Output Indicator	**Valid output indicator**. The Q Valid indicates valid output data. QVLD is edge aligned with CQ and $\overline{CQ}$.
K	Input Clock	**Positive input clock input**. The rising edge of K is used to capture synchronous inputs to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode. All accesses are initiated on the rising edge of K.
$\overline{K}$	Input Clock	**Negative input clock input**. $\overline{K}$ is used to capture synchronous inputs being presented to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode.
CQ	Echo Clock	**CQ referenced with respect to C**. This is a free running clock and is synchronized to the input clock K. The timing for the echo clocks is shown in Switching Characteristics on page 25.
$\overline{CQ}$	Echo Clock	**$\overline{CQ}$ referenced with respect to $\overline{C}$**. This is a free running clock and is synchronized to the input clock $\overline{K}$. The timing for the echo clocks is shown in the Switching Characteristics on page 25.
ZQ	Input	**Output impedance matching input**. This input is used to tune the device outputs to the system data bus impedance. CQ, $\overline{CQ}$, and $Q_{[x:0]}$ output impedance are set to 0.2 × RQ, where RQ is a resistor connected between ZQ and ground. Alternatively, connect this pin directly to V_{DDQ}, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.
$\overline{DOFF}$	Input	**DLL turn off – Active LOW**. Connecting this pin to ground turns off the DLL inside the device. The timing in the operation with the DLL turned off differs from those listed in this data sheet. For normal operation, connect this pin to a pull up through a 10 kΩ or less pull up resistor. The device behaves in QDR I mode when the DLL is turned off. In this mode, the device can be operated at a frequency of up to 167 MHz with QDR I timing.
TDO	Output	**Test data out (TDO) Pin for JTAG**.

Pin Definitions (continued)

Pin Name	I/O	Pin Description
TCK	Input	**Test clock (TCK) Pin for JTAG**.
TDI	Input	**Test data in (TDI) Pin for JTAG**.
TMS	Input	**Test mode select (TMS) Pin for JTAG**.
NC	N/A	**Not connected to the die**. Can be tied to any voltage level.
NC/144M	Input	**Not connected to the die**. Can be tied to any voltage level.
NC/288M	Input	**Not connected to the die**. Can be tied to any voltage level.
V_{REF}	Input-Reference	**Reference voltage input**. Static input used to set the reference level for HSTL inputs, outputs, and AC measurement points.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**.
V_{SS}	Ground	**Ground for the device**.
V_{DDQ}	Power Supply	**Power supply inputs for the outputs of the device**.

Functional Overview

The CYRS1542AV18, and CYRS1544AV18 are synchronous pipelined burst SRAMs with a read port and a write port. The read port is dedicated to read operations and the write port is dedicated to write operations. Data flows into the SRAM through the write port and flows out through the read port. These devices multiplex the address inputs to minimize the number of address pins required. By having separate read and write ports, the QDR II+ completely eliminates the need to turnaround the data bus and avoids any possible data contention, thereby simplifying system design. Each access consists of two 18-bit data transfers in the case of CYRS1542AV18, and two 36-bit data transfers in the case of CYRS1544AV18 in one clock cycle.

This device operates with a read latency of two cycles when $\overline{DOFF}$ pin is tied HIGH. When $\overline{DOFF}$ pin is set LOW or connected to V_{SS} then the device behaves in QDR I mode with a read latency of one clock cycle.

Accesses for both ports are initiated on the rising edge of the positive input clock (K). All synchronous input timing is referenced from the rising edge of the input clocks (K and $\overline{K}$) and all output timing is referenced to the output clocks (K and $\overline{K}$).

All synchronous data inputs ($D_{[x:0]}$) pass through input registers controlled by the input clocks (K and $\overline{K}$). All synchronous data outputs ($Q_{[x:0]}$) pass through output registers controlled by the rising edge of the output clocks (K and $\overline{K}$).

All synchronous control ($\overline{RPS}$, $\overline{WPS}$, $\overline{BWS}_{[x:0]}$) inputs pass through input registers controlled by the rising edge of the input clocks (K and $\overline{K}$).

CYRS1542AV18 is described below. The same basic descriptions also apply to CYRS1544AV18.

Read Operations

The CYRS1542AV18 is organized internally as two arrays of 2 M × 18. Accesses are completed in a burst of two sequential 18-bit data words. Read operations are initiated by asserting $\overline{RPS}$ active at the rising edge of the positive input clock (K). The address is latched on the rising edge of the K clock. The address presented to the address inputs is stored in the read address register. Following the next two K clock rise, the corresponding lowest order 18-bit word of data is driven onto the $Q_{[17:0]}$ using K as the output timing reference. On the subsequent rising edge of $\overline{K}$, the next 18-bit data word is drive onto the $Q_{[17:0]}$. The requested data is valid 0.45 ns from the rising edge of the output clock (K and $\overline{K}$).

When the read port is deselected, the CYRS1542AV18 first completes the pending read transactions. Synchronous internal circuitry automatically tri-states the outputs following the next rising edge of the positive input clock (K). This allows for a seamless transition between devices without the insertion of wait states in a depth expanded memory.

Write Operations

Write operations are initiated by asserting $\overline{WPS}$ active at the rising edge of the positive input clock (K). On the same K clock rise the data presented to $D_{[17:0]}$ is latched and stored into the lower 18-bit write data register, provided $\overline{BWS}_{[1:0]}$ are both asserted active. On the subsequent rising edge of the negative input clock ($\overline{K}$), the address is latched and the information presented to $D_{[17:0]}$ is also stored into the write data register, provided $\overline{BWS}_{[1:0]}$ are both asserted active. The 36 bits of data are then written into the memory array at the specified location.

When deselected, the write port ignores all inputs after the pending write operations are complete.

Byte Write Operations

Byte write operations are supported by the CYRS1542AV18. A write operation is initiated as described in the Write Operations section. The bytes that are written are determined by $\overline{BWS}_0$ and $\overline{BWS}_1$, which are sampled with each set of 18-bit data words. Asserting the appropriate BWS input during the data portion of a write latches the data being presented and writes it into the device. Deasserting the byte write select input during the data portion of a write enables the data stored in the device for that byte to remain unaltered. This feature can be used to simplify read, modify, or write operations to a byte write operation.

Concurrent Transactions

The read and write ports on the CYRS1542AV18 operate independently of one another. As each port latches the address inputs on different clock edges, you can read or write to any location, regardless of the transaction on the other port. You can start reads and writes in the same clock cycle. If the ports access the same location at the same time, the SRAM delivers the most recent information associated with the specified address location. This includes forwarding data from a write cycle that was initiated on the previous K clock rise.

Depth Expansion

The CYRS1542AV18 has a port select input for each port. This allows for easy depth expansion. Both port selects are sampled on the rising edge of the positive input clock only (K). Each port select input can deselect the specified port. Deselecting one port does not affect the other port. All pending transactions (read and write) are completed before the device is deselected.

Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to enable the SRAM to adjust its output driver impedance. The value of RQ must be 5 × the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a tolerance of ±15% is between 175 Ω and 350 Ω, with V_{DDQ} = 1.5 V. The output impedance is adjusted every 1024 cycles upon power-up to account for drifts in supply voltage and temperature.

Echo Clocks

Echo clocks are provided on the QDR II+ to simplify data capture on high speed systems. Two echo clocks are generated by the QDRII+. CQ is referenced with respect to K and CQb is referenced with respect to K. These are free-running clocks and are synchronized to the input clock of the QDR II+. The timing for the echo clocks is shown in Switching Characteristics on page 25.

Valid Data Indicator (QVLD)

QVLD is provided on the QDR II+ to simplify data capture on high speed systems. The QVLD is generated by the QDR II+ device along with data output. This signal is also edge-aligned with the echo clock and follows the timing of any data pin. This signal is asserted half a cycle before valid data arrives.

DLL

These chips use a DLL that is designed to function between 120 MHz and the specified maximum clock frequency. During power-up, when the DOFF is tied HIGH, the DLL is locked after 10240 cycles of stable clock. The DLL can also be reset by slowing or stopping the input clocks K and K for a minimum of 30 ns. The DLL may be disabled by applying ground to the DOFF pin. When the DLL is turned off, the device behaves in QDR I mode (with one cycle latency and a longer access time). For information refer to the application note AN5062, DLL Considerations in QDRII/DDRII.

Qualification and Screening

The 90-nm RadStop technology was qualified by Cypress after meeting the criteria of the General Manufacturing Standards. The test flow includes screening units with the defined flow (Class V) and the appropriate periodic or lot conformance testing (Groups B, C, D, and E). Both the 90-nm process and the SRAM products are subject to period or lot-based technology conformance inspection (TCI) and quality conformance inspection (QCI) tests, respectively. Cypress offers both prototyping models and flight units of these product configurations.

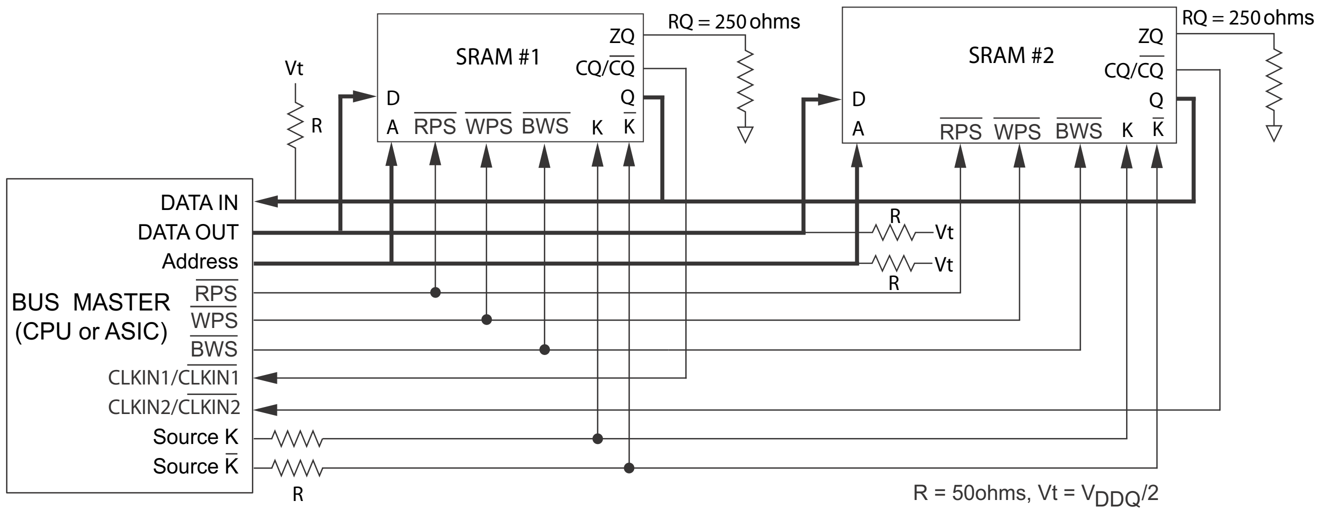
Table 1. Qualification Tests

Group A	General electrical tests
Group B	Mechanical - Dimensions, bond strength, solvents, die shear, solderability, lead Integrity, seal, and acceleration
Group C	Life tests - 1000 hours at 125 °C or equivalent
Group D	Package related mechanical tests - shock, vibration, accel, salt, seal, lead finish adhesion, lid torque, thermal shock, and moisture resistance
Group E	Radiation tests

Application Example

Figure 2 shows two QDR II+ used in an application.

Figure 2. Application Example



Truth Table

CYRS1542AV18 and CYRS1544AV18 [2, 3, 4, 5, 6, 7]

Operation	K	$\overline{RPS}$	$\overline{WPS}$	DQ	DQ
Write cycle: Load address on the rising edge of $\overline{K}$; input write data on K and $\overline{K}$ rising edges.	L–H	X	L	D(A) at K(t)↑	D(A + 1) at $\overline{K}$(t)↑
Read cycle:(2.0 cycle Latency) Load address on the rising edge of K; wait two cycles; read data on $\overline{K}$ and K rising edges.	L–H	L	X	Q(A) at K(t + 2)↑	Q(A + 1) at $\overline{K}$(t + 2)↑
NOP: No operation	L–H	H	H	D = X Q = High Z	D = X Q = High Z
Standby: Clock stopped	Stopped	X	X	Previous state	Previous state

Write Cycle Descriptions

CYRS1542AV18 [2, 8]

$\overline{BWS_0}$	$\overline{BWS_1}$	K	$\overline{K}$	Comments
L	L	L–H	–	During the data portion of a write sequence: Both bytes ($D_{[17:0]}$) are written into the device.
L	L	–	L–H	During the data portion of a write sequence: Both bytes ($D_{[17:0]}$) are written into the device.
L	H	L–H	–	During the data portion of a write sequence: Only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
L	H	–	L–H	During the data portion of a write sequence: Only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
H	L	L–H	–	During the data portion of a write sequence: Only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered.
H	L	–	L–H	During the data portion of a write sequence: Only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered.
H	H	L–H	–	No data is written into the devices during this portion of a write operation.
H	H	–	L–H	No data is written into the devices during this portion of a write operation.

Notes
2. X = "Don't Care," H = Logic HIGH, L = Logic LOW, ↑represents rising edge.
3. Device powers up deselected with the outputs in a tristate condition.
4. "A" represents address location latched by the devices when transaction was initiated. A + 0, A + 1 represents the internal address sequence in the burst.
5. "t" represents the cycle at which a Read/Write operation is started. t + 1, and t + 2 are the first, and second clock cycles respectively succeeding the "t" clock cycle.
6. Data inputs are registered at K and $\overline{K}$ rising edges. Data outputs are delivered on K and $\overline{K}$ rising edges.
7. It is recommended that K = $\overline{K}$ = HIGH when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
8. Is based on a write cycle that was initiated in accordance with the Write Cycle Descriptions table. $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$ and $\overline{BWS_2}$ can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved.

Write Cycle Descriptions

CYRS1544AV18 [9, 10]

$\overline{BWS_0}$	$\overline{BWS_1}$	$\overline{BWS_2}$	$\overline{BWS_3}$	K	$\overline{K}$	Comments
L	L	L	L	L–H	–	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	L	L	L	–	L–H	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	H	H	H	L–H	–	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
L	H	H	H	–	L–H	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
H	L	H	H	L–H	–	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	L	H	H	–	L–H	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	H	L	H	L–H	–	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	L	H	–	L–H	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	H	L	L–H	–	During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	L	–	L–H	During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	H	L–H	–	No data is written into the device during this portion of a write operation.
H	H	H	H	–	L–H	No data is written into the device during this portion of a write operation.

Notes

9. X = "Don't Care," H = Logic HIGH, L = Logic LOW, ↑represents rising edge.
10. Is based on a write cycle that was initiated in accordance with the Write Cycle Descriptions table. $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$ and $\overline{BWS_2}$ can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved

IEEE 1149.1 Serial Boundary Scan (JTAG)

These SRAMs incorporate a serial boundary scan Test Access Port (TAP) in the FBGA package. This part is fully compliant with IEEE Standard #1149.1-2001. The TAP operates using JEDEC standard 1.8 V I/O logic levels.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternatively be connected to V_{DD} through a pull up resistor. TDO must be left unconnected. Upon power up, the device comes up in a reset state, which does not interfere with the operation of the device.

Test Access Port

Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram on page 15. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

Test Data Out (TDO)

The TDO output pin is used to serially clock data out from the registers. The output is active, depending upon the current state of the TAP state machine (see Instruction Codes on page 19). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This reset does not affect the operation of the SRAM and can be performed while the SRAM is operating. At power up, the TAP is reset internally to ensure that TDO comes up in a high Z state.

TAP Registers

Registers are connected between the TDI and TDO pins to scan the data in and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins, as shown in TAP Controller Block Diagram on page 16. At power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This enables shifting of data through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all of the input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the RAM input and output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the input and output ring.

The Boundary Scan Order on page 20 shows the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in Identification Register Definitions on page 19.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in Instruction Codes on page 19. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in this section in detail.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction after it is shifted in, the TAP controller must be moved into the Update-IR state.

IDCODE

The IDCODE instruction loads a vendor specific, 32-bit code into the instruction register. It also places the instruction register between the TDI and TDO pins and shifts the IDCODE out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register at power up or whenever the TAP controller is supplied a Test-Logic-Reset state.

SAMPLE Z

The SAMPLE Z instruction connects the boundary scan register between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a high Z state until the next command is supplied during the Update IR state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is an 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the input and output pins is captured in the boundary scan register.

You must be aware that the TAP controller clock only operates at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the K and $\overline{K}$ captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD places an initial data pattern at the latched parallel outputs of the boundary scan register cells before the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required, that is, while the data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST

The EXTEST instruction drives the preloaded data out through the system output pins. This instruction also connects the boundary scan register for serial access between the TDI and TDO in the Shift-DR controller state.

EXTEST OUTPUT BUS TRISTATE

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tristate mode.

The boundary scan register has a special bit located at bit #108. When this scan cell, called the “extest output bus tristate,” is latched into the preload register during the Update-DR state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a high Z condition.

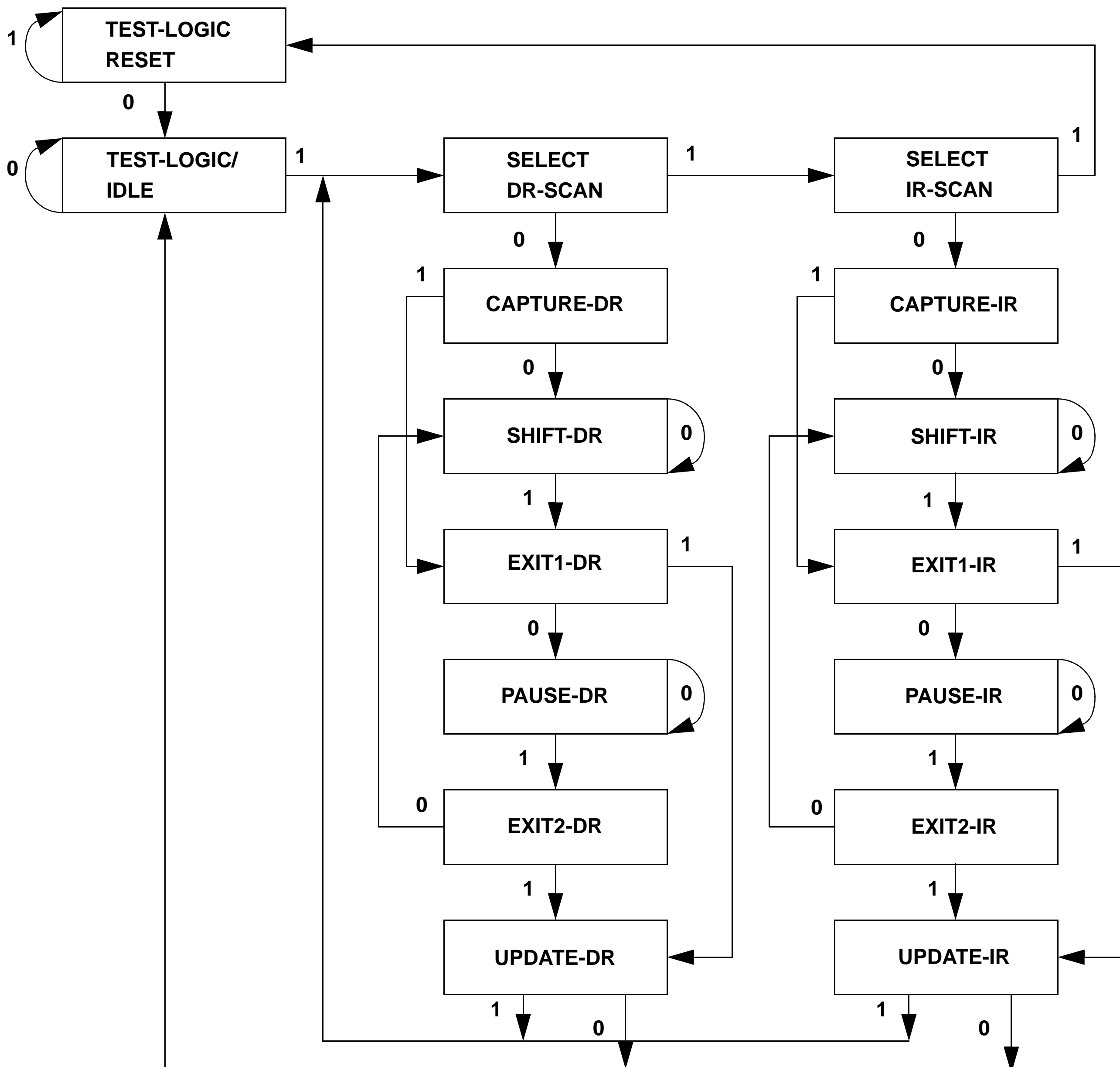
This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the Shift-DR state. During Update-DR, the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is preset LOW to enable the output when the device is powered up, and also when the TAP controller is in the Test Logic Reset state.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram

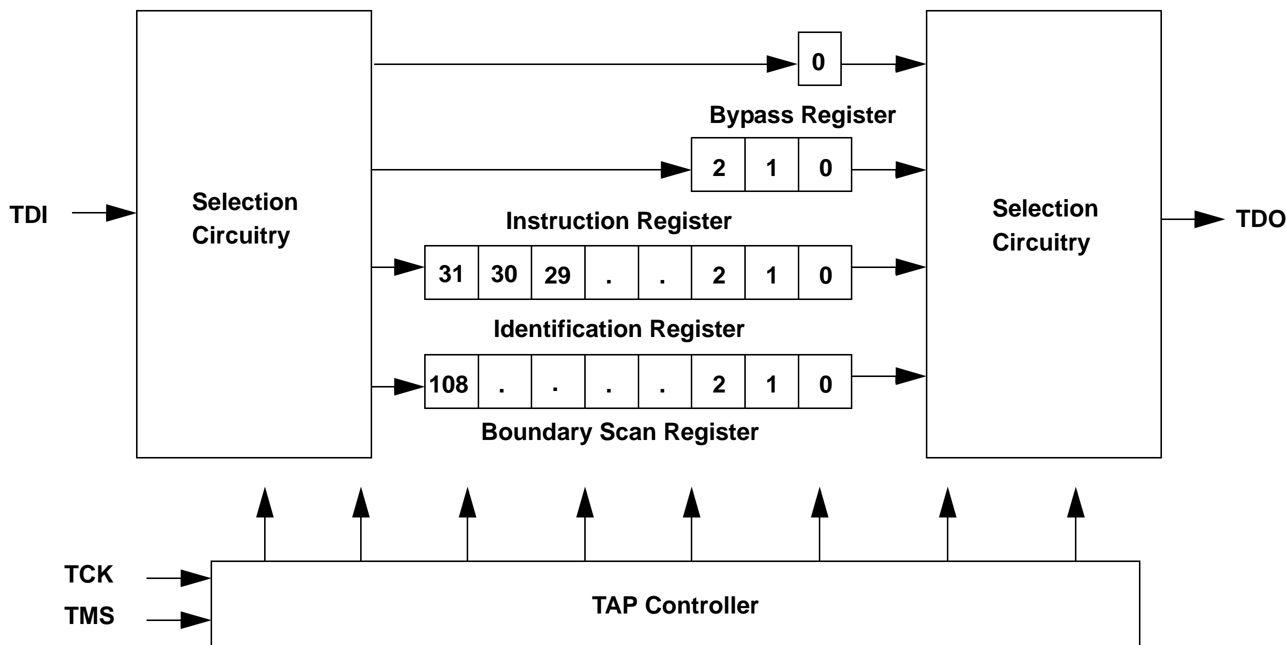
The state diagram for the TAP controller follows.[11]



Note

11. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Electrical Characteristics

Over the Operating Range

Parameter [12, 13, 14]	Description	Test Conditions	Min	Max	Unit
V_{OH1}	Output high voltage	I_{OH} = –2.0 mA	1.4	–	V
V_{OH2}	Output high voltage	I_{OH} = –100 µA	1.6	–	V
V_{OL1}	Output low voltage	I_{OL} = 2.0 mA	–	0.4	V
V_{OL2}	Output low voltage	I_{OL} = 100 µA	–	0.2	V
V_{IH}	Input high voltage		0.65 × V_{DD}	V_{DD} + 0.3	V
V_{IL}	Input low voltage		–0.3	0.35 × V_{DD}	V
I_X	Input and output load current	GND ≤ V_I ≤ V_{DD}	–5	5	µA

Notes
12. These characteristics pertain to the TAP inputs (TMS, TCK, TDI and TDO). Parallel load levels are specified in Electrical Characteristics on page 22.
13. Overshoot: $V_{IH(AC)} < V_{DDQ} + 0.85$ V (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL(AC)} > -1.5$ V (Pulse width less than $t_{CYC}/2$).
14. All Voltage referenced to ground.

TAP AC Switching Characteristics

Over the Operating Range

Parameter [15, 16]	Description	Min	Max	Unit
t_{TCYC}	TCK clock cycle time	50	–	ns
t_{TF}	TCK clock frequency	–	20	MHz
t_{TH}	TCK clock HIGH	20	–	ns
t_{TL}	TCK clock LOW	20	–	ns
Setup Times				
t_{TMSS}	TMS setup to TCK clock rise	5	–	ns
t_{TDIS}	TDI setup to TCK clock rise	5	–	ns
t_{CS}	Capture setup to TCK rise	5	–	ns
Hold Times				
t_{TMSH}	TMS hold after TCK clock rise	5	–	ns
t_{TDIH}	TDI hold after clock rise	5	–	ns
t_{CH}	Capture hold after clock rise	5	–	ns
Output Times				
t_{TDOV}	TCK clock LOW to TDO valid	–	10	ns
t_{TDOX}	TCK clock LOW to TDO invalid	0	–	ns

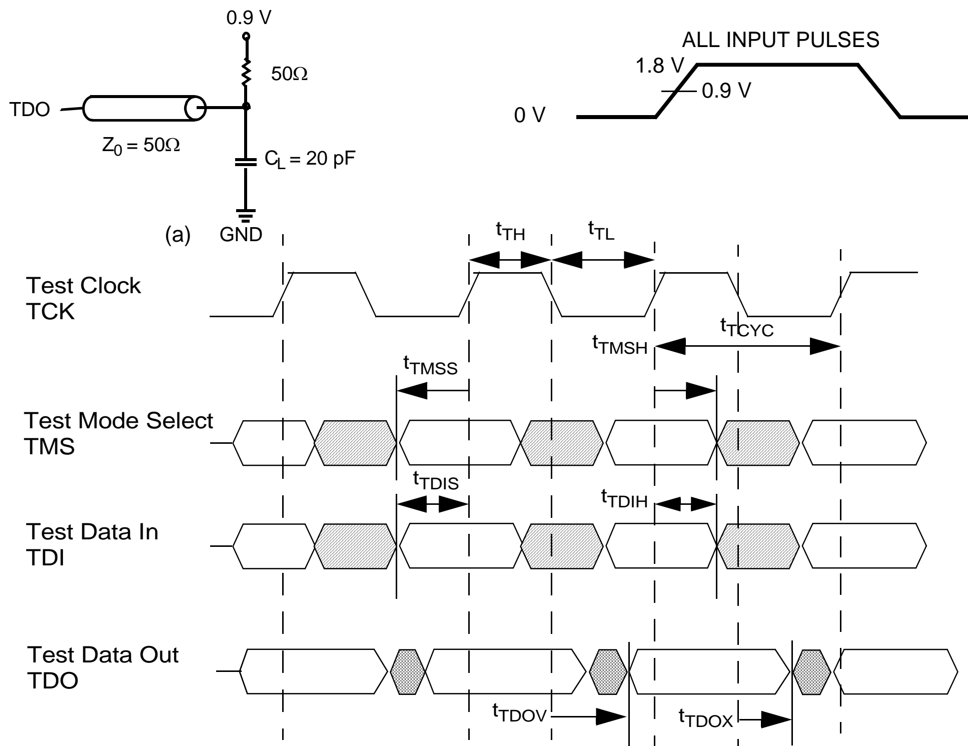
Notes

15. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
16. Test conditions are specified using the load in TAP AC Test Conditions. t_R/t_F = 1 ns.

TAP Timing and Test Conditions

Figure 3 shows the TAP timing and test conditions. [17]

Figure 3. TAP Timing and Test Conditions



Note
17. Test conditions are specified using the load in TAP AC Test Conditions. t_R/t_F = 1 ns.

Identification Register Definitions

Instruction Field	Value		Description
	CYRS1542AV18	CYRS1544AV18	
Revision number (31:29)	000	000	Version number.
Cypress device ID (28:12)	11010010100010100	11010010100100100	Defines the type of SRAM.
Cypress JEDEC ID (11:1)	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID register presence (0)	1	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	109

Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the input and output ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the input and output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a high Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the input and output contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

Boundary Scan Order

Bit #	Bump ID
0	6R
1	6P
2	6N
3	7P
4	7N
5	7R
6	8R
7	8P
8	9R
9	11P
10	10P
11	10N
12	9P
13	10M
14	11N
15	9M
16	9N
17	11L
18	11M
19	9L
20	10L
21	11K
22	10K
23	9J
24	9K
25	10J
26	11J
27	11H

Bit #	Bump ID
28	10G
29	9G
30	11F
31	11G
32	9F
33	10F
34	11E
35	10E
36	10D
37	9E
38	10C
39	11D
40	9C
41	9D
42	11B
43	11C
44	9B
45	10B
46	11A
47	10A
48	9A
49	8B
50	7C
51	6C
52	8A
53	7A
54	7B
55	6B

Bit #	Bump ID
56	6A
57	5B
58	5A
59	4A
60	5C
61	4B
62	3A
63	2A
64	1A
65	2B
66	3B
67	1C
68	1B
69	3D
70	3C
71	1D
72	2C
73	3E
74	2D
75	2E
76	1E
77	2F
78	3F
79	1G
80	1F
81	3G
82	2G
83	1H

Bit #	Bump ID
84	1J
85	2J
86	3K
87	3J
88	2K
89	1K
90	2L
91	3L
92	1M
93	1L
94	3N
95	3M
96	1N
97	2M
98	3P
99	2N
100	2P
101	1P
102	3R
103	4R
104	4P
105	5P
106	5N
107	5R
108	Internal

Power Up Sequence in QDR II+ SRAM

QDR II+ SRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

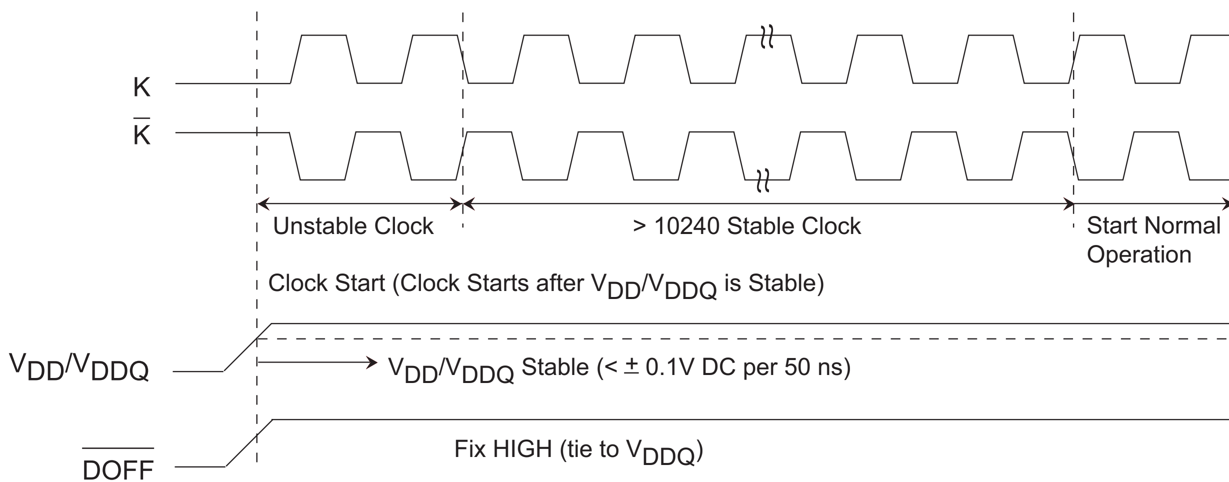
Power Up Sequence

- Apply power and drive $\overline{DOFF}$ either HIGH or LOW (All other inputs can be HIGH or LOW).
  - Apply V_{DD} before V_{DDQ}.
  - Apply V_{DDQ} before V_{REF} or at the same time as V_{REF}.
  - Drive $\overline{DOFF}$ HIGH.
- Provide stable $\overline{DOFF}$ (HIGH), power and clock (K, $\overline{K}$) for 10240 cycles to lock the DLL.

DLL Constraints

- DLL uses K clock as its synchronizing input. The input must have low phase jitter, which is specified as $t_{KC\ Var}$.
- The DLL functions at frequencies down to 120 MHz.
- If the input clock is unstable and the DLL is enabled, then the DLL may lock onto an incorrect frequency, causing unstable SRAM behavior. To avoid this, provide 10240 cycles stable clock to relock to the desired clock frequency.

Figure 4. Power Up Waveforms



Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Case temperature under power .... –55 °C to +125 °C

Junction temperature under power .... –55 °C to +150°C

Supply voltage on V_{DD} relative to GND ....–0.5 V to +2.9 V

Supply voltage on V_{DDQ} relative to GND ...... –0.5 V to +V_{DD}

DC applied to outputs in high Z ....–0.5 V to V_{DDQ} + 0.5 V

DC input voltage [18] ....–0.5 V to V_{DD} + 0.5 V

Current into outputs (LOW) .... 20 mA

Static discharge voltage
(MIL-STD-883, M. 3015) ....> 2001 V

Latch up current ....> 200 mA

Operating Range

Range	Case Temperature (T_c)	V_{DD}[19]	V_{DDQ}[19]
Military	–55 °C to +125 °C	1.8 ± 0.1 V	1.4 V to V_{DD}

Electrical Characteristics

Over the Operating Range

DC Electrical Characteristics

Over the Operating Range

Parameter[20]	Description	Test Conditions			Min	Typ	Max	Unit
V_{DD}	Power supply voltage				1.7	1.8	1.9	V
V_{DDQ}	I/O supply voltage				1.4	1.5	V_{DD}	V
V_{OH}	Output high voltage	Note 21			$V_{DDQ}/2 – 0.12$	–	$V_{DDQ}/2 + 0.12$	V
V_{OL}	Output low voltage	Note 22			$V_{DDQ}/2 – 0.12$	–	$V_{DDQ}/2 + 0.12$	V
$V_{OH(LOW)}$	Output high voltage	I_{OH} = –0.1 mA, nominal impedance			V_{DDQ} – 0.2	–	V_{DDQ}	V
$V_{OL(LOW)}$	Output low voltage	I_{OL} = 0.1 mA, nominal impedance			V_{SS}	–	0.2	V
V_{IH}	Input high voltage				V_{REF} + 0.1	–	V_{DDQ} + 0.3	V
V_{IL}	Input low voltage				–0.3	–	V_{REF} – 0.1	V
I_X	Input leakage current	GND ≤ V_I ≤ V_{DDQ}			–20	–	20	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ $V_{DDQ,}$ output disabled			–20	–	20	µA
V_{REF}	Input reference voltage [23]	Typical value = 0.75 V			0.68	0.75	0.95	V
I_{DD} [24]	V_{DD} operating supply	V_{DD} = Max, I_{OUT} = 0 mA, T_J=125 °C, f = f_{MAX} = 1/t_{CYC}	250 MHz	(× 18)	–	–	1650	mA
				(× 36)	–	–	1650	
			200 MHz	(× 18)	–	–	1410	mA
				(× 36)	–	–	1410	
I_{SB1}	Automatic power down current	Max V_{DD}, Both ports deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX} = 1/t_{CYC}, T_J = 125 °C, Inputs static	250 MHz	(× 18)	–	–	600	mA
				(× 36)	–	–	550	
			200 MHz	(× 18)	–	–	600	mA
				(× 36)	–	–	550	

Notes

18. Overshoot: $V_{IH(AC)} < V_{DDQ}$ + 0.85 V (Pulse width less than t_{CYC}/2), Undershoot: $V_{IL(AC)}$ > –1.5 V (Pulse width less than t_{CYC}/2).
19. Power up: Assumes a linear ramp from 0 V to $V_{DD(min)}$ within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \le V_{DD}$.
20. All Voltage referenced to ground.
21. Output are impedance controlled. I_{OH} = –(V_{DDQ}/2)/(RQ/5) for values of 175 Ω ≤ RQ ≤ 350 Ω.
22. Output are impedance controlled. I_{OL} = (V_{DDQ}/2)/(RQ/5) for values of 175 Ω ≤ RQ ≤ 350 Ω.
23. $V_{REF(min)}$ = 0.68 V or 0.46 V_{DDQ}, whichever is larger, $V_{REF(max)}$ = 0.95 V or 0.54 V_{DDQ}, whichever is smaller.
24. The operation current is calculated with concurrent read and write cycles.

AC Electrical Characteristics

Over the Operating Range

Parameter [25, 26]	Description	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input high voltage		V_{REF} + 0.2	–	–	V
V_{IL}	Input low voltage		–	–	V_{REF} – 0.2	V

Radiation Performance

Parameter	Test Conditions	Limits	Unit
Total dose	T_A = 25 °C, V_{DD} = V_{DDQ} = 1.8 V	300 Krad	Rads(Si) Co60
Soft error rate	T_A = 25 °C to 125 °C, V_{DD} = V_{DDQ} = 1.8 V with EDAC	$1.0 \times 10^{\wedge-10}$	Upsets/bit-day
Transient dose rate upset	Pulse width (FWHM) = 50 ns, X-Ray, T_C = 25 °C, V_{DD} = V_{DDQ} = 1.8 V	2.0×10^9	Rads(Si)/s
Neutron fluence	1 MeV equivalent energy, Unbiased T_A = 25 °C	2e14	N/cm^2
Latch up immunity	T_A = 125 °C, V_{DD} = V_{DDQ} = 1.9 V	110	MeVcm^2/mg

Capacitance

Parameter [27]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 1.8 V, V_{DDQ} = 1.5 V	10	pF
C_{CLK}	Clock input capacitance		10	pF
C_O	Output capacitance		10	pF

Thermal Resistance

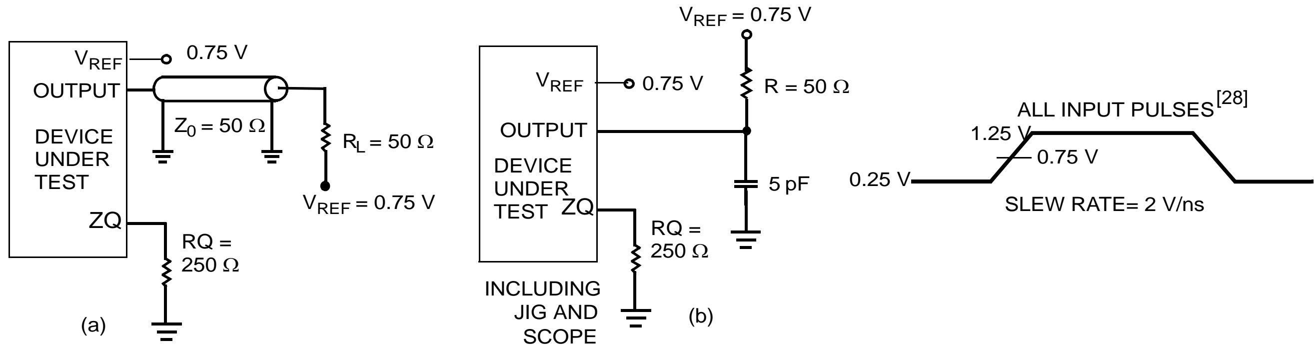
Parameter [27]	Description	Test Conditions	165-ball CCGA Package	Unit
Θ_{JC}	Thermal resistance (Junction to case)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	8.9	°C/W

Notes

25. Overshoot: $V_{IH(AC)} < V_{DDQ}$ + 0.85 V (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL(AC)} > -1.5$ V (Pulse width less than $t_{CYC}/2$).
26. Power up: Assumes a linear ramp from 0 V to $V_{DD(min)}$ within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.
27. Tested initially and after any design or process change that may affect these parameters.

AC Test Loads and Waveforms

Figure 5. AC Test Loads and Waveforms



Note

28. Unless otherwise noted, test conditions are based on signal transition time of 2 V/ns, timing reference levels of 0.75 V, Vref = 0.75 V, RQ = 250 Ω, V_{DDQ} = 1.5 V, input pulse levels of 0.25 V to 1.25 V, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in (a) of Figure 5.

Switching Characteristics

Over the Operating Range

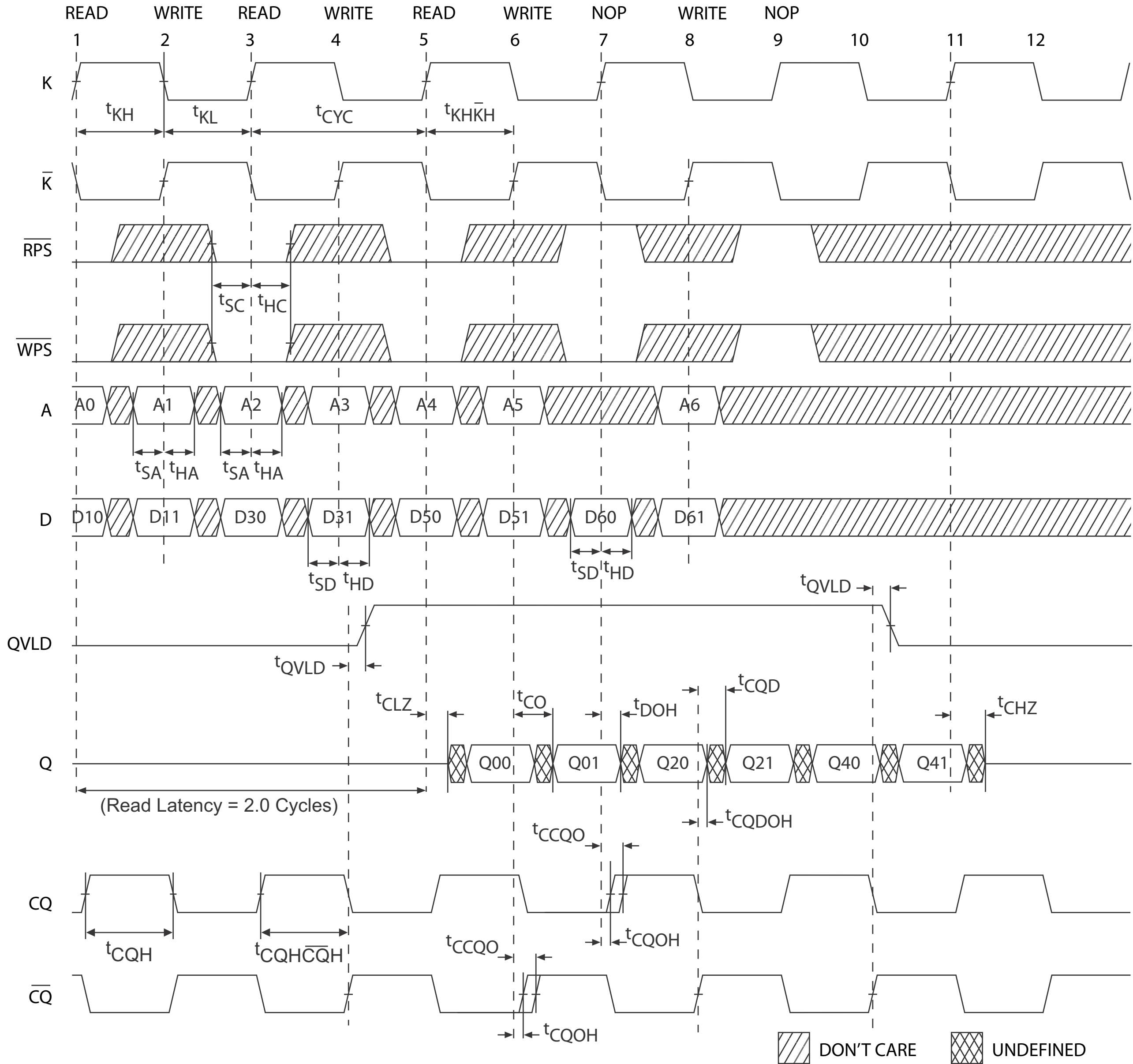
Parameters [29, 30]		Description	250 MHz		200 MHz		Unit
Cypress Parameter	Consortium Parameter		Min	Max	Min	Max	
t_{POWER}		V_{DD}(typical) to the first access [31]	1	–	1	–	ms
t_{CYC}	t_{KHKH}	K clock cycle time	4.0	8.4	5.0	8.4	ns
t_{KH}	t_{KHKL}	Input clock (K/$\overline{K}$) HIGH	1.6	–	2.0	–	ns
t_{KL}	t_{KLKH}	Input clock (K/$\overline{K}$) LOW	1.6	–	2.0	–	ns
$t_{KH\overline{K}H}$	$t_{KH\overline{K}H}$	K clock rise to $\overline{K}$ clock rise (rising edge to rising edge)	1.8	–	2.2	–	ns
Setup Times							
t_{SA}	t_{AVKH}	Address setup to K clock rise	0.5	–	0.6	–	ns
t_{SC}	t_{IVKH}	Control setup to K clock rise ($\overline{RPS}$, $\overline{WPS}$)	0.5	–	0.6	–	ns
t_{SCDDR}	t_{IVKH}	DDR control setup to clock (K/$\overline{K}$) rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.5	–	0.6	–	ns
t_{SD}	t_{DVKH}	$D_{[X:0]}$ setup to clock (K/$\overline{K}$) rise	0.5	–	0.6	–	ns
Hold Times							
t_{HA}	t_{KHAX}	Address hold after K clock rise	0.5	–	0.5	–	ns
t_{HC}	t_{KHIX}	Control hold after K clock rise ($\overline{RPS}$, $\overline{WPS}$)	0.5	–	0.5	–	ns
t_{HCDDR}	t_{KHIX}	DDR control hold after clock (K/$\overline{K}$) rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.5	–	0.5	–	ns
t_{HD}	t_{KHDX}	$D_{[X:0]}$ hold after clock (K/$\overline{K}$) rise	0.5	–	0.5	–	ns
Output Times							
t_{CO}	t_{CHQV}	K/$\overline{K}$ clock rise to data valid	–	0.7	–	0.7	ns
t_{DOH}	t_{CHQX}	Data output hold after output K/$\overline{K}$ clock rise (Active to active)	–0.7	–	–0.7	–	ns
t_{CCQO}	t_{CHCQV}	K/$\overline{K}$ clock rise to echo clock valid	–	0.7	–	0.7	ns
t_{CQOH}	t_{CHCQX}	Echo clock hold after C/$\overline{C}$ clock rise	–0.7	–	–0.7	–	ns
t_{CQD}	t_{CQHQV}	Echo clock high to data valid	–	0.50	–	0.50	ns
t_{CQDOH}	t_{CQHQX}	Echo clock high to data invalid	–0.30	–	–0.35	–	ns
t_{CQH}	t_{CQHCQL}	Output clock (CQ/$\overline{CQ}$) HIGH [32]	1.55	–	1.95	–	ns
$t_{CQH\overline{CQ}H}$	$t_{CQH\overline{CQ}H}$	CQ clock rise to $\overline{CQ}$ clock rise (rising edge to rising edge) [32]	1.55	–	1.95	–	ns
t_{CHZ}	t_{CHQZ}	Clock (K/$\overline{K}$) rise to high Z (active to high Z) [33, 34]	–	0.45	–	0.45	ns
t_{CLZ}	t_{CHQX1}	Clock (K/$\overline{K}$) rise to low Z [33, 34]	–0.45	–	–0.45	–	ns
t_{QVLD}	$t_{CQHQVLD}$	Echo Clock High to QVLD Valid [35]	–0.5	0.5	–0.5	0.5	ns
DLL Timing							
$t_{KC\ Var}$	$t_{KC\ Var}$	Clock phase jitter	–	0.20	–	0.20	ns
$t_{KC\ lock}$	$t_{KC\ lock}$	DLL lock time (K)	10240	–	10240	–	Cycles
$t_{KC\ Reset}$	$t_{KC\ Reset}$	K static to DLL reset	30	–	30	–	ns

Notes

29. Unless otherwise noted, test conditions are based on signal transition time of 2 V/ns, timing reference levels of 0.75 V, Vref = 0.75 V, RQ = 250 Ω, V_{DDQ} = 1.5 V, input pulse levels of 0.25 V to 1.25 V, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in (a) of Figure 5 on page 24.
30. When a part with a maximum frequency above 167 MHz is operating at a lower clock frequency, it requires the input timings of the frequency range in which it is being operated and outputs data with the output timings of that frequency range.
31. This part has a voltage regulator internally; t_{POWER} is the time that the power must be supplied above $V_{DD(minimum)}$ initially before initiating a read or write operation.
32. These parameters are extrapolated from the input timing parameters ($t_{KH\overline{K}H}$ – 250 ps, where 250 ps is the internal jitter. An input jitter of 200 ps ($t_{KC\ Var}$) is already included in the $t_{KH\overline{K}H}$). These parameters are only guaranteed by design and are not tested in production.
33. t_{CHZ}, t_{CLZ}, are specified with a load capacitance of 5 pF as in part (b) of Figure 5 on page 24. Transition is measured ± 100 mV from steady state voltage.
34. At any voltage and temperature t_{CHZ} is less than t_{CLZ} and t_{CHZ} less than t_{CO}.
35. t_{QVLD} Spec is applicable for both rising and falling edges of QVLD signal.

Switching Waveforms

Figure 6. Read/Write/Deselect Sequence [36, 37, 38]



Notes

36. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, that is, A0 + 1.
37. Outputs are disabled (high Z) one clock cycle after a NOP.
38. In this example, if address A0 = A1, then data Q00 = D10 and Q01 = D11. Write data is forwarded immediately as read results. This note applies to Figure 6.

Ordering Information

The following table contains only the parts that are currently available. If you do not see what you are looking for (× 18 option), contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products

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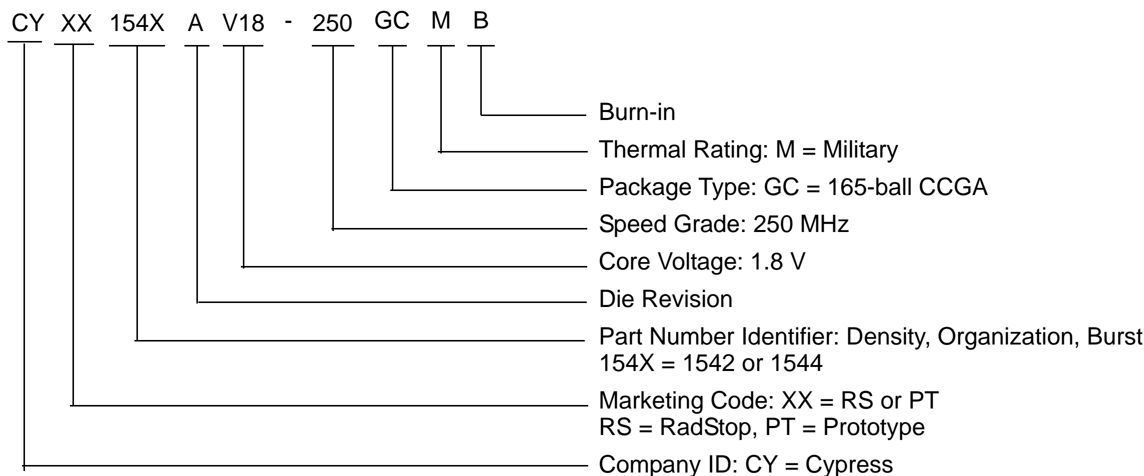
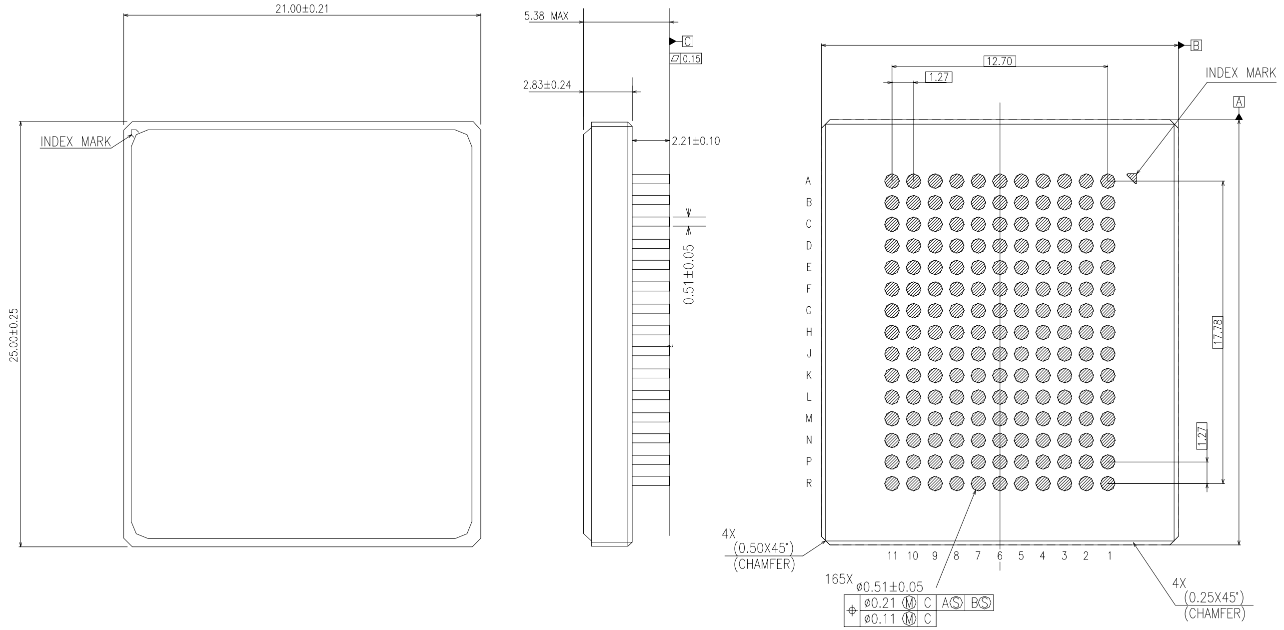
Speed (MHz)	Ordering Code	Description	Package Diagram	Package Type	Operating Range
250	CYRS1542AV18-250GCMB	72M QDR II+, × 18, Burst of 2	001-58969	165-ball CCGA (21 × 25 × 2.83 mm)	Military
250	CYRS1544AV18-250GCMB	72M QDR II+, × 36, Burst of 2	001-58969	165-ball CCGA (21 × 25 × 2.83 mm)	Military
250	CYPT1542AV18-250GCMB	72M QDR II+, × 18, Burst of 2, Prototype	001-58969	165-ball CCGA (21 × 25 × 2.83 mm)	Military
250	CYPT1544AV18-250GCMB	72M QDR II+, × 36, Burst of 2, Prototype	001-58969	165-ball CCGA (21 × 25 × 2.83 mm)	Military
250	5962F1120101QXA	72M QDR II+, × 18, Burst of 2, DLAM Part	001-58969	165-ball CCGA (21 × 25 × 2.83 mm)	Military
250	5962F1120201QXA	72M QDR II+, × 36, Burst of 2, DLAM Part	001-58969	165-ball CCGA (21 × 25 × 2.83 mm)	Military

Ordering Code Definitions



Package Diagram

Figure 7. 165-ball Ceramic Column Grid Array (CCGA) (21 × 25 mm) Package Outline, 001-58969



NOTES:

1. PACKAGE WEIGHT : 16g (estimate)
2. JEDEC REFERENCE : MO-158 VAR BE-1

001-58969 *C

Acronyms

Acronym	Description
BWS	byte write select
CCGA	ceramic column grid array
DED	double error detection
DLL	delay lock loop
DDR	double data rate
DSCC	defense supply center columbus
EDAC	error detection and correction
HSTL	high speed transceiver logic
I/O	input/output
JTAG	Joint Test Action Group
LSB	least significant bit
LSBU	logical single-bit upsets
LMBU	logical multi-bit upsets
MSB	most significant bit
PDA	percent defect allowable
PIND	particle impact noise detection
PDA	percent defective allowable
QDR	quad data rate
RPS	read port select
SEC	single error correction
SEL	single event latch up
SRAM	static random access memory
TAP	test access port
TCK	test clock
TDI	test data in
TDO	test data out
TMS	test mode select
WPS	write port select

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Krad	kiloradian
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
N/cm^2	Neutron particles fluence per cm^2 area
ns	nanosecond
nm	nanometer
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
Rads(Si)	unit of absorbed radiation energy from ionizing radiation per kg of material. (1 rad(Si)) = 10 mGy = 10 – 2 J/kg
V	volt
W	watt

Glossary

Total Dose	Permanent device damage due to ions over device life
Heavy Ion	Instantaneous device latch up due to single ion
LET	Linear energy transfer (measured in $MeVcm^2$)
Krad	Unit of measurement to determine device life in radiation environments.
Neutron	Permanent device damage due to energetic neutrons or protons
Prompt Dose	Data loss of permanent device damage due to X-rays and gamma rays < 20 ns
165-ball Ceramic Column Grid Array	Hermetic ceramic 165-column package. Columns attached by Six Sigma
RadStop Technology	Cypress's patented Rad Hard design methodology
DLAM	Defense Logistics Agency Land and Maritime
LSBU	Logical Single Bit Upset. Single bits in a single correction word are in error.
LMBU	Logical Multi Bit Upset. Multiple bits in a single correction word are in error
Group A	General electrical testing
Group B	Mechanical - Dimensions, bond strength, solvents, die shear, solderability, lead integrity, seal, acceleration
Group C	Life test - 1000 hours at 125 °C
Group D	Package related mechanical tests - shock, vibration, Accel, salt, seal, lead finish adhesion, lid torque, thermal shock, moisture resistance
Group E	Radiation testing

Document History Page

Document Title: CYRS1542AV18/CYRS1544AV18, 72-Mbit QDR® II+ SRAM Two-Word Burst Architecture with RadStop™ Technology Document Number: 001-60006				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	2940931	05/31/2010	HRP	New data sheet.
*A	3016545	08/26/2010	HRP	Changed part numbers from CYRS1512AV18/CYRS1514AV18 to reflect change to QDR II+ die. Updated Switching Characteristics (Updated minimum and maximum values for Setup Time, Hold Time parameters, and updated minimum and maximum values for t_{CO} parameter under Output Time parameter). Updated Ordering Information (Added 200-MHz part numbers (CYRS1542AV18-250GCMB, CYRS1544AV18-250GCMB for Burst 2 mode). Updated Package Diagram. Added Units of Measure.
*B	3281455	06/13/2011	HRP	Changed status from Advanced to Final. Updated Configurations (corrected typo). Updated Selection Guide. Updated DC Electrical Characteristics (maximum current limit values for the parameters I_{DD} and I_{SB1} based on device characterization). Updated Radiation Performance (Limits of Radiation Data based on RHA qualification. Updated Thermal Resistance. Updated Switching Characteristics (Minimum and Maximum timing values for the parameters t_{co}, t_{DOH}, t_{CCQO}, t_{CQOH} based on device characterization). Updated Ordering Information (Removed × 18 option from ordering table). Updated Package Diagram. Changed DLL lockup cycles from 2048 to 10240 throughout document. Updated in new template.
*C	3471321	12/21/2011	HRP	Updated Identification Register Definitions (Replaced the value of Cypress device ID (28:12) from 11010011010010100 to 11010010100010100 for CYRS1542AV18 and replaced the value of Cypress device ID (28:12) from 11010011010100100 to 11010010100100100 for CYRS1544AV18).
*D	3524961	02/14/2012	HRP	Updated Prototyping Options under Radiation Performance. (Added two devices). Updated Application Example. Updated Truth Table. Updated Maximum Ratings. Updated Radiation Performance. Updated Capacitance. Updated Thermal Resistance. Updated Switching Characteristics. Updated Ordering Information (Removed 200 MHz speed part CYRS1544AV18-200GCMB).
*E	3537277	02/29/2012	HRP	Updated Radiation Data under Radiation Performance. Updated Ordering Information (Removed the part number CYRS1544AV18-250GCMB and added the part numbers CYRS1543AV18-250GCMB, CYRS1545AV18-250GCMB, CYPT1543AV18-250GCMB, CYPT1545AV18-250GCMB, 5962F1120201VXA and 5962F1120202VXA).
*F	3580538	04/12/2012	HRP	Updated Ordering Information (Updated part numbers).
*G	3617759	05/15/2012	HRP	Updated Radiation Performance (Updated Prototyping Options). Updated Ordering Information (Added part 5962F1120101VXA). Updated Glossary.

Document History Page (continued)

Document Title: CYRS1542AV18/CYRS1544AV18, 72-Mbit QDR® II+ SRAM Two-Word Burst Architecture with RadStop™ Technology Document Number: 001-60006				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
*H	3640834	06/08/2012	HRP	Updated Radiation Performance (Updated Prototyping Options). Renamed the section Class V Flow as Manufacturing Flow. Updated Glossary.
*I	3857750	01/04/2013	HRP	Updated Ordering Information (Updated part numbers).

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