MCS7705

USB with IEEE-1284 Port

Features

- Single 5-V Operation
- Full compliance with the USB V1.1 Specification
- Supports external EEprom for device configuration
- Low Power
- Multi-mode compatible controller (SPP, PS2, EPP, ECP)
- Fast data rates up to 1.5 Mbytes/s
- 16 Byte FIFO
- Microsoft Compatible
- Software programmable mode selects
- On chip oscillator
- 48-pin SSOP package

Applications

- Portable backup units
- Printer Server
- Monitoring equipment
- Add on I/O interface
- Printer interface

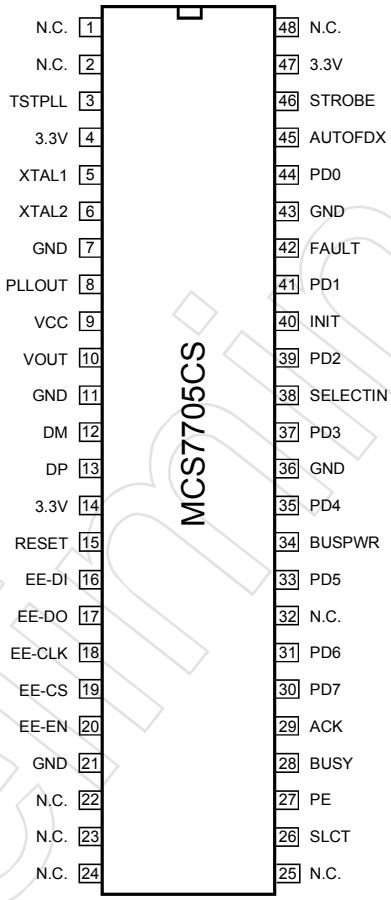
General Description

The MCS7705 is an IEEE-1284 compatible high performance parallel port with USB 1.1 interface. MCS7705 fully supports the existing Centronics printer interface as well as PS/2, EPP, and ECP modes. The MCS7705 contains all the necessary logic to communicate with host computer using USB bus. USB bulk-type data is adopted for maximum data transfer. The MCS7705 is ideally suited for PC/MAC applications, such as high speed parallel port. The MCS7705 is available in 48-Pin SSOP package. It is fabricated in an advanced in sub-micron CMOS process to achieve low drain power and high speed requirements.

Ordering Information

Commercial Grade		
MCS7705CS	48-SSOP	0° C to +70° C

48-Pin SSOP Package



Pin Name	48	Type	Description
TSTPLL	3	I	Test mode (active low, internal pull-up) input. When this pin is tied to GND, the internal PLL is by passed and external 48MHz clock is used as reference clock.
XTAL1	5	I	Crystal oscillator input or External clock input pin (6 MHz). This signal input is used in conjunction with XTAL2 to form a feedback circuit for the internal timing. Two external capacitors (10pF) connected from each side of the XTAL1 and XTAL2 to GND is required to form a crystal oscillator circuit.
XTAL2	6	O	Crystal oscillator output. See XTAL1 description.
PLLOUT	8	O	Internal 48MHz PLL clock output. This pin is active when TEST pin is tied to GND.
VCC	9	Pwr	5-V Voltage regulator supply input.
VOUT	10	Pwr	3.3-V Voltage regulator output.
DM	12	I/O	Root USB port differential data minus.
DP	13	I/O	Root USB port differential data plus.
RESET	15	I	System reset (active low). Resets all internal register, sequencers, and signals to a consistent state.
EE-DI	16	I	External EE-Prom data input.
EE-DO	17	O	External EE-Prom data output.
EE-CLK	18	O	External EE-Prom clock.
EE-CS	19	O	External EE-Prom chip select (active high). After power on reset, MCS7705 reads the EE-Prom and loads the read-only configuration registers sequentially from the first 64 bytes in the EE-Prom.
EE-EN	20	I	Enable/Disable external EEprom (active high, internal pull-up). External EEprom can be disabled when this pin is tied to GND or pulled low. When external EEprom is disabled, the default values for MCS7705 will be loaded into the configuration register.
SLCT	26	I	Peripheral/printer selected (internal pull-up). This pin is set to high by peripheral/printer when it is selected.
PE	27	I	Paper empty (internal pull-up). This pin is set to high by peripheral/printer when printer paper is empty.

Pin Name	48	Type	Description
nBUSY	28	I	Peripheral/printer busy (internal pull-up). This pin is set to high by peripheral/ printer, when printer or peripheral is not ready to accept data.
nACK	29	I	Peripheral/printer data acknowledge (internal pull-up). This pin is set to low by peripheral/printer to indicate a successful data transfer has taken place.
BUSPWR	34	I	Power source Indicator (active high, internal pull-up). BUSPWR is an active high input that indicates whether the downstream ports source their power from the USB cable or a local power supply. For the self-powered mode, this pin should be pulled low.
nSLCTIN	38	I/O	Peripheral/printer select (open-drain, active low). Selects the peripheral/printer when it is set to low.
nINIT	40	I/O	Initialize the Peripheral/printer (open drain, active low). When set to low, Peripheral/printer starts it's initialization routine.
nFAULT	42	I	Peripheral/printer data error (internal pull-up). This pin is set to low by peripheral/printer during error condition.
nAUTOFDX	45	I/O	Peripheral/printer auto feed (open-drain, active low). Continuous autofed paper is selected when this pin is set to low.
nSTROBE	46	I/O	Peripheral/printer data strobe (open drain, active low). On the rising edge of the nSTROBE, data is latched into printer port.
PD7-PD0	30,31 33,35 37,39 41,44	I/O	Peripheral/printer data ports.
GND	7,11,21, 36,43	Pwr	Power and signal ground.
3.3V	4,14,47	Pwr	Device Supply input. All 3.3V signals should be connected to VOUT pin.

Printer Registers Table

D2 D1 D0	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
0 0 0	DPR	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
0 0 1	DSR	nBUSY	nACK	PE	SLCT	FAULT	INT state	“0”	EPP TIMEOUT
0 1 0	DCR	“0”	“0”	DIR	INTA	nSLCTIN	INIT	nAUTOFD	nSTROBE
0 1 1	EPP Address	ADD-7	ADD-6	ADD-5	ADD-4	ADD-3	ADD-2	ADD-1	ADD-0
1 0 0	EPP data	DAT-7	DAT-6	DAT-5	DAT-4	DAT-3	DAT-2	DAT-1	DAT-0
1 0 1	EPP data	DAT-15	DAT-14	DAT-13	DAT-12	DAT-11	DAT-10	DAT-9	DAT-8
1 1 0	EPP data	DAT-23	DAT-22	DAT-21	DAT-20	DAT-19	DAT-18	DAT-17	DAT-16
1 1 1	EPP data	DAT-31	DAT-30	DAT-29	DAT-28	DAT-27	DAT-26	DAT-25	DAT-24
0 0 0	C-FIFO	CDAT-7	CDAT-6	CDAT-5	CDAT-4	CDAT-3	CDAT-2	CDAT-1	CDAT-0
0 0 0	CONF-A	“1”	“0”	“0”	“1”	“0”	“1”	“0”	“0”
0 0 1	CONF-B	“0”	INT Pin	“0”	“0”	“0”	“0”	“0”	“0”
0 1 0	ECR	MODE select			ErrIntrEn enable	“0”	Service Int	FIFO full	FIFO empty

Data Register
Data register is cleared at initialization by RESET. During a write operation, the Data register latches the contents of the data bus. The contents of this register are buffered and output onto the PD7-PD0 ports.

Device Status Register
The contents of this register are latched for the duration of the read cycle. The bits of the Status Port are defined as follows.

DSR Bit-0:
0 = Normal.
1 = 10μ s timeout (EPP mode only). Cleared by writing 1 into DSR register or consecutive reads (after the first read) always returns “0”.

DSR Bit-1:
Not used, set to “0”.

DSR Bit-2:
0 = nACK input pin is at low state (USB Interrupt follows the nACK pin), when SPP mode is selected. Normal (no interrupt) when PS/2 mode is selected.
1 = Normal (no interrupt). In standard mode operation, USB Interrupt is active (interrupt is generated on the rising edge of the nACK). It is cleared when DSR is read.

DSR Bit-3:
0 = Printer reports error condition.
1 = Normal operation.

DSR Bit-4:
0 = Printer is off line.
1 = Printer is on line.

DSR Bit-5:
0 = Normal operation
1 = Paper End/Empty is detected

DSR Bit-6:
0 = State of the nACK pin (ACK = low).
1 = State of the nACK pin (ACK = high).

DSR Bit-7:
0 = nBUSY pin is high, printer is not ready to take data.
1 = nBUSY pin is low, printer is read to take data.

Device Control Register

DCR Bit-0
0 = Sets the nSTROBE pin to high.
1 = Sets the nSTROBE pin to low. PD7-PD0 data are latched into printer

DCR Bit-1:
0 = Sets the nAUTOFD pin to high. Printer generates auto line feed after each line is printed.
1 = Sets the nAUTOFD pin to low. No auto feed function.

DCR Bit-2:
0 = Sets the INIT pin to high.
1 = Sets the INIT pin to low. Peripheral/printer starts it’s initialization routine.

DCR Bit-3:
0 = Sets the nSLCTIN pin to high. Selects the printer.
1 = Sets the nSLCTIN pin to low. Printer is not selected.

DCR Bit-4:
0 = Disables Printer interrupt function. nACK pin has no effect on the INT pin.
1 = Enables Printer interrupt function. The INT follows the nACK input pin during standard mode, latches high on the rising edge of the nACK, when PS/2 mode is selected.

DCR Bit-5:
0 = PD7-PD0 pins are out put mode.
1 = PD7-PD0 pins are input mode.

DCR Bits 7-6:
Not used, set to “0”.

Config: -A Register

Configuration A register (read only). Reading this register returns 10010100. Writing to this register has no effect and the data is ignored.

Config: -B Register

Configuration B register. This register allows software to control the selecting of interrupts. A read-write implementation implies a "software-configurable" device. Reading this register, returns the configured interrupt, and interrupt pin state. If a value is not set to 000 (the jumper-default) then it is assumed that the value in the register is correct and software will use the default interrupt.

Config-B Bit-7:
Not used, set to "0".

Config-B Bit-6:
0 = Configured printer interrupt pin is low.
1 = Configured printer interrupt pin is high.

Config-B Bit 7-0:
Interrupt pin select register.

Extended Control Register (ECR)

This register controls the mode selection and DMA operation.

Bit-7	Bit-6	Bit-5	Operating Mode
0	0	0	SPP
0	0	1	PS/2
0	1	0	PPF (FIFO mode)
0	1	1	ECP
1	0	0	EPP
1	0	1	Not used
1	1	0	FIFO test
1	1	1	Config A/B enable

Mode changes.

After hardware reset, PS/2 mode is selected as default mode. It is required to select mode 000 or 001 between any other mode configuration.

Mode "000"
SPP/Centronics/Compatible Mode
Forward direction only. The direction bit is forced to "0" and PD7-PD0 are set to output direction. The MCS7705 is under software controlled. This mode defines the protocol used by most PC's to transfer data to a printer. It is commonly called the "Centronics" mode and is the method utilized with the standard parallel port. Data is placed on the PD7-PD0 port's, the printer status is checked via DSR register. If no error condition is flagged and printer is not Busy, software toggles the nSTROBE pin to latch the PD7-PD0 data into printer. This operating cycle continues when printer/peripheral issues data acknowledge signal (pulls the ACK and nBUSY pin).

Nibble Mode

The Nibble mode is the most common way to get reverse channel data from a printer or peripheral. This mode is usually combined with the Centronics mode or a proprietary forward channel mode to create a Bi-directional channel. In this mode printer status bits are used as Nibble bits.

Bits order for Nibble mode.

PINS	DATA Bits
nBUSY	Bit-7
PE	Bit-6
SLCT	Bit-5
nFAULT	Bit-4
nBUSY	Bit-3
PE	Bit-2
SLCT	Bit-1
nFAULT	Bit-0

Mode “001”
PS/2, Byte Mode
The Byte mode protocol is used to transfer bi-directional data via PD7-PD0 ports without FIFO utilization. The direction of the port is controlled with DIR bit in DCR register. PS/2-Byte use SPP protocol for data transfer.

DCR Bit-5:
0 = PD7-PD0 pins are out put mode.
1 = PD7-PD0 pins are input mode.

Mode “010”
FIFO output Mode
In this mode, bytes written to the FIFO are transmitted automatically using the SPP/Centronics standard protocol.

Mode “011”
Extended Capability Port “ECP” Mode
The ECP provides an advanced mode for communication with printer or peripherals. Like EPP protocol, ECP provides 16 byte FIFO for a high performance bi-directional communication path between the host adapter and the peripheral. The ECP protocol provides the following cycle types in both the forward and reverse direction.

- Data cycle
- Command cycles
  - Run-Length counts (RLE)
  - Channel address

The RLE feature enables real time data compression that can achieve compression ratios up to 64:1. This is particularly useful for printers and peripherals that are transferring large raster images that have large strings of identical data. In order for the RLE mode to be enabled, both the host and peripheral must support it.
Channel addressing is intended to address multiple logical devices within single physical device like Modem/FAX/Printer in one physical package.

Mode “100”
Enhanced Parallel Port “EPP” Mode
In EPP mode, nSLCTIN (address strobe) and nAUTOFD (data strobe) are automatically generated while nSTROBE indicates a write or read cycle. Additional I/O addresses are defined for data and address access and when these locations are used, handshaking is performed automatically by MCS7705.

Mode “110”
FIFO test Mode
In this mode, the FIFO can be written and read in any direction, but no data will be transmitted on the PD7-PD0 ports. Whoever, data in the FIFO may be displayed on the PD7-PD0 ports.

ECR Bit-4:
Error Interrupt Enable.
0 = Enable nFAULT interrupt. nFAULT pin is used as source of interrupt.
1 = Disable nFAULT interrupt (nACK is used as source of interrupt).

ECR Bit-3:
0 = normal operating mode.

ECR Bit-2:
1 = Disables service interrupt.
0 = Enables one of the following 3 cases of interrupts. One of the 3 service interrupts has occurred, Service interrupt bit will be set to a “1” by hardware. Writing this bit to a “1” will not cause an interrupt.

Port Direction (DCR Bit-5 = 0), this bit will be set to “1” whenever there are Write Interrupt threshold (4 characters) or more bytes free in the FIFO. The MCS7705 generates interrupt when this condition is occurred and Service Interrupt is cleared to “0”.

Port Direction (DCR Bit-5 = 1), this bit will be set to “1” whenever there are Read Interrupt threshold (12 characters) or more bytes to be read from the FIFO. The MCS7705 generates interrupt when this condition is occurred and Service Interrupt is cleared to “0”.

ECR Bit-1:
0 = One or more empty location in FIFO is available.
1 = FIFO full.

ECR Bit-0:
0 = One or more data in FIFO.
1 = FIFO empty.

Master rest conditions

Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
DPR	X	X	X	X	X	X	X	X
DSR	0	1	1	1	1	0	0	0
DCR	0	0	0	0	0	0	0	0
EPP	0	0	0	0	0	0	0	0
C-FIFO	0	0	0	0	0	0	0	0
CONF-A	1	0	0	1	0	1	0	0
CONF-B	0	X	0	0	0	0	0	0
ECR	0	0	0	0	0	0	0	1

Absolute Maximum Ratings

Supply Range	7 Volts
Voltage at any pin	GND – 0.3 to VCC +0.3
Operating Temperature	-45° C to 90° C
Storage Temperature	-65° C to 150° C
Package Dissipation	500 mW
ESD	±2000 Volts
Latch up	220 mA

DC Electrical Specification

T = 0° C to 70° C (-40° C to +85° C for industrial "E" grade parts), VCC = 5V ±10% unless otherwise specified.

Symbol	Parameter	5-V Min	5-V Max	Unit	Condition
Vil	Input Low voltage	-0.3	0.8	V	
Vih	Input High voltage	2.0		V	
Vt-	Schmitt trigger negative going threshold voltage	1.10		V	
Vt+	Schmitt trigger positive going threshold voltage	1.87		V	
Vol	Output low voltage		0.4	V	Iol=4 mA
Voh	Output high voltage	3.5		C	Ioh=4 mA
Iil	Input low current		±1	µA	
Iih	Input high current		±1	µA	
Ioz	Three state leakage current		±10	µA	
Cin	Input capacitance	3	5	pF	
Cout	Output capacitance	3	5	pF	
Icc	Operating current		50	mA	No load

Revision	Notes	Date
1.0	-	11/01

Notes: