Motor Driver IC Series for Tape Record Systems

2 in 1 Motor Driver For VTRs

BD6903EFV, BD6904FP

● Description

The BD6903EFV and BD6904FP single chip 3-phase full-wave motor drivers integrate soft switching for low noise sensorless driving as well as a PG amplifier that enables PG/FG output, making them ideal for use in cylinder motors and loading motors in non-portable Video Tape Recorders (VTRs).

● Features
  1) Cylinder motor driver
  2) Sensorless 3-phase full-wave soft switching drive system
  3) DMOS output
  4) Built-in startup circuit
  5) Built-in PG amp
  6) 3-value common PG/FG output
  7) Loading motor driver
  8) Three mode output (forward, reverse, brake), depending on control logic input
  9) DMOS output
  10) Built-in Thermal Shut-Down (TSD) circuit

● Applications
  VTRs

● Product Line

Parameter		BD6903EFV	BD6904FP
Power Supply Voltage	Control block (VCC)	4.5～5.5V	4.5～5.5V
	Control block (VG)	VM+3～19V	VM+2～19V
	Output block (VM)	9～13.5V	9～14V
Maximum Output Current (cylinder)		800mA	800mA
(loading)		1000mA	800mA
Current Limit Voltage		No	295mV
Reversible Operation Mode		Forward rotation, reverse rotation, brake	Forward rotation, reverse rotation, stop, brake
Number of Reversible Control Input Pins		1pin	2pins
Package		HTSSOP-B20	HSOP-25

● Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	BD6903EFV Limit	BD6904FP Limit	Unit
Applied Voltage	VCC	7	7	V
Applied Voltage	VM	15	15	V
Applied Voltage	VG	20	20	V
Power Dissipation	Pd	1000 *1	1450 *2	mW
Operating Temperature Range	Topr	-20～+75	-20～+75	℃
Storage Temperature Range	Tstg	-55～+150	-55～+150	℃
Maximum Output Current (cylinder block)	Iomax1	800 *3	800 *3	mA
Maximum Output Current (loading block)	Iomax2	1000 *3	800 *3	mA
Junction Temperature	Tjmax	+150	+150	℃

*1 Reduced by 8.0 mW/℃ over 25°C when mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm).

*2 Reduced by 11.6 mW/℃ over 25°C when mounted on a glass epoxy board (90 mm × 90 mm × 1.6 mm).

*3 Must not exceed Pd or ASO.

● Operating Conditions

Parameter	Symbol	BD6903EFV Limit	BD6904FP Limit	Unit
Operating Power Supply Voltage Range	VCC	4.5～5.5	4.5～5.5	V
Operating Power Supply Voltage Range	VM	9～13.5	9～14	V
Operating Power Supply Voltage Range	VG	VM+3～19	VM+2～19	V
UIN, VIN, WIN In-phase Input Voltage Range	VBEMFD	0～VM	-	V
COM Input In-phase Voltage Range	VCOMD	-	0～VM-2.5	V
PG amp In-phase Input Voltage Range	VPD	1.5～3.0	1.5～3.7	V

● Electrical Characteristics

BD6903EFV

(Unless otherwise specified, Ta=25℃, VCC=5V, VM =12V, VG=17V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
<Overall>						
VCC Total Supply Current	ICC	-	9.2	14.2	mA	
VM Total Supply Current 1	IM1	-	1.4	2.8	mA	LIN=H or L
VM Total Supply Current 2	IM2	-	1.4	2.8	mA	LIN=M
<Output>						
High-side Output Saturation Voltage	VOH	-	0.4	0.8	V	Io=-400mA
Low-side Output Saturation Voltage	VOL	-	0.3	0.6	V	Io=400mA
<Torque Reference>						
EC Input Bias Current	IEC	-	0.5	2	μA	
Torque Reference Start Voltage	VECR	2.35	2.5	2.65	V	
Torque Reference I/O Gain	Gio	0.72	0.99	1.28	A/V	EC=2.6V-2.7V Gain output (HLM) RRNF = 0.5Ω
<Soft Switch>						
CT1, CT2 Charge Current	ICTD	-50	-35	-25	μA	
CT1, CT2 Discharge Current	ICTI	27	40	56	μA	
High CT1, CT2 Clamp Voltage	VCTH	4.4	4.7	-	V	
Low CT1, CT2 Clamp Voltage	VCTL	0.8	1.0	1.3	V	
<Startup Control Logic>						
CST Charge Current	ICSTH	-20	-14	-6	μA	
CST Discharge Current	ICSTI	2	6	10	μA	
High CST Clamp Voltage	VCSTH	2.4	2.8	3.3	V	
Low CST Clamp Voltage	VCSTL	0.8	1.0	1.3	V	
<PG Amp>						
Input Bias Current	IPG-	-	0.1	0.25	μA	PG-=GND
DC Bias Current	VPG	2.25	2.6	2.75	V	PG-=PGOUT
Voltage Gain 1	AV1	17.5	18.8	-	dB	f=1kHz
High Output Voltage	VOHP	3.4	3.75		V	IOH=-1mA
Low Output Voltage	VOLP	-	1.2	1.6	V	IOL=1mA
<HYS Amp>						
Hysteresis Width	VHYSP	-75	-100	-125	mV	
<PFG Pin>						
High Output Voltage	VPFGP	4.5	-	-	V	IO=-10μA
Middle Output Voltage	VPFGM	2.25	-	2.75	V	IO=±10μA
Low Output Voltage	VPFGL	-	-	0.5	V	IO=10μA
<Loading>						
High-level LIN Input	VLINH	3.5	-	-	V	Loading: Forward rotation
Middle-level LIN Input	VLINM	2.35	-	2.65	V	Loading: Brake
Low-level LIN Input	VLINL	-	-	1.5	V	Loading: Reverse rotation
LIN bias Voltage	VLINB	2.35	2.5	2.65	V	
Output Saturation Voltage	VCE	-	0.3	0.6	V	IO=200mA, total of output transistor high-side and low-side voltage

※Source currents are treated as negative while sinking currents are treated as positive.

◎This product is not designed to be resistant against radiation.

● Electrical Characteristics

BD6904FP

(Unless otherwise specified, Ta=25℃, VCC=5V, VM1=VM2 =12V, VG=17V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
<Overall>						
VCC Total Supply Current	ICC	-	9	13	mA	
<Output I>						
High-side Output Saturation Voltage	VOH	-	0.4	0.7	V	Io=-300mA
Low-side Output Saturation Voltage	VOL	-	0.55	0.55	V	Io=300mA
<BEMF Comparator I>						
BEMF Comparator Hysteresis Width+	VHYSB+	+24	+36	+48	mV	
BEMF Comparator Hysteresis Width-	VHYSB-	-59	-43	-27	mV	
<Torque Reference I>						
Torque Reference Start Voltage	VECR	2.35	2.5	2.65	V	
Torque Reference I/O Gain	Gio	0.80	1.05	1.33	A/V	EC=2.3V-2.2V Gain output (HLM) RRNF = 0.68 Ω
Current Limit Voltage	VCL	239	295	345	mV	RRNF=0.68Ω
<Soft Switch >						
CT1, CT2 Charge Current	ICTD	-53	-39	-25	μA	
CT1, CT2 Discharge Current	ICTI	29	45	61	μA	
High CT1, CT2 Clamp Voltage	VCTH	3.4	3.8	4.2	V	
Low CT1, CT2 Clamp Voltage	VCTL	0.85	1.05	1.25	V	
<Startup Control Logic >						
CST Charge Current	ICSTH	-20	-14	-8	μA	
CST Discharge Current	ICSTI	2	5.5	9	μA	
High CST Clamp Voltage	VCSTH	2.4	2.8	3.2	V	
Low CST Clamp Voltage	VCSTL	0.8	1.0	1.2	V	
CST OFF Voltage	VCSTO	3.6	3.8	4.0	V	
<PG Amp >						
Input Bias Current	IPG-	-	1	3	μA	PG-=2.5V
Input Offset Voltage	VIOP	-8	-	+8	mV	
DC Bias Current	VPG	2.25	2.5	2.75	V	PG-=PGOUT
Voltage Gain 1	AV1	50	71	-	dB	f=1kHz
High Output Voltage	VOHP	3.4	3.75	-	V	IOH=-1mA
Low Output Voltage	VOLP	-	1.2	1.6	V	IOL=1mA
<PFG Pin >						
PG Detection Level	VPGTH	VBP-0.075	VBP-0.1	VBP-0.125	V	
High Output Voltage	VPFGP	3.5	-	-	V	IO=-30μA
Middle Output Voltage	VPFGM	2.1	-	2.9	V	IO=±10μA
Low Output Voltage	VPFGL	-	-	0.9	V	IO=30μA
<Loading >						
High-level FIN Input	VFINH	3.5	-	-	V	
High-level RIN Input	VRINM	3.5	-	-	V	
Low-level FIN Input	VFINL	-	-	1.5	V	
Low-level RIN Input	VRINL	-	-	1.5	V	
Output Saturation Voltage	VCE	-	0.3	0.6	V	IO=200mA, total of output transistor high-side and low-side voltage

※Source currents are treated as negative while sink currents are treated as positive.

◎This product is not designed to be resistant against radiation.

● Reference Data

BD6903EFV
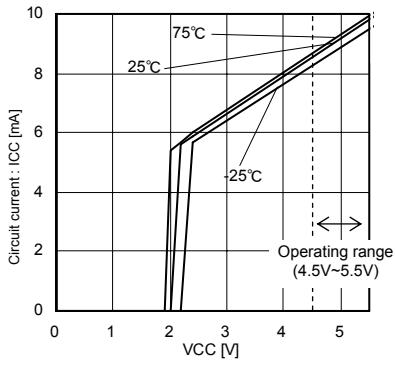
Fig.1 Total Supply Current
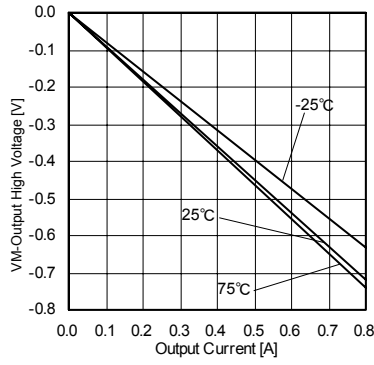(All blocks in operation)

Fig.2 Drum Output High-Side
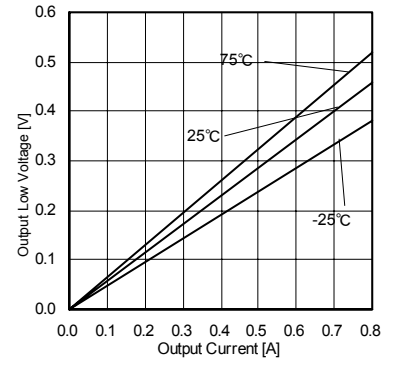Saturation Voltage

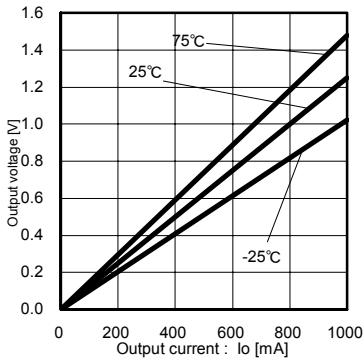Fig.3 Drum Output Low-Side
Saturation Voltage

Fig.4 Loading Output Saturation Voltage
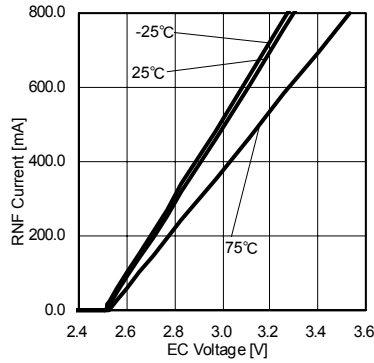(Total of high-side and low-side voltages)

Fig.5 Torque Reference Gain (RNF = 0.5 Ω)
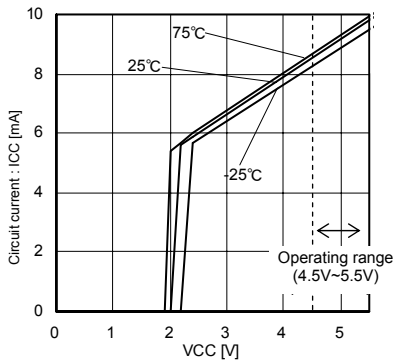
BD6904FP
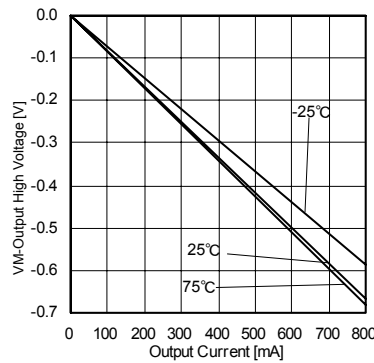

Fig.6 Total Supply Current
(All blocks in operation)

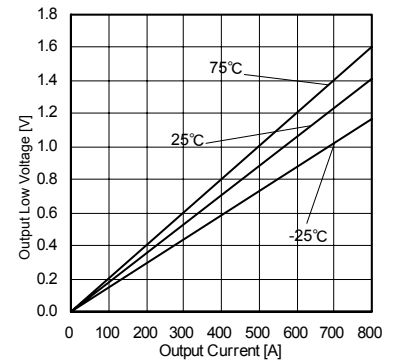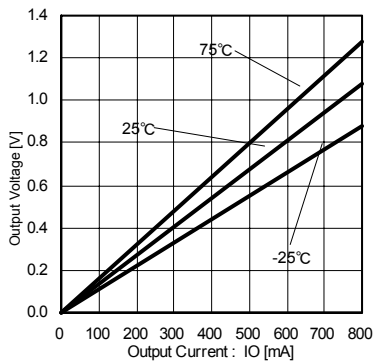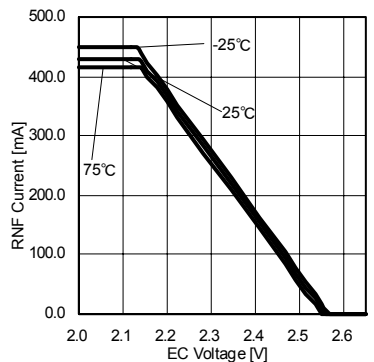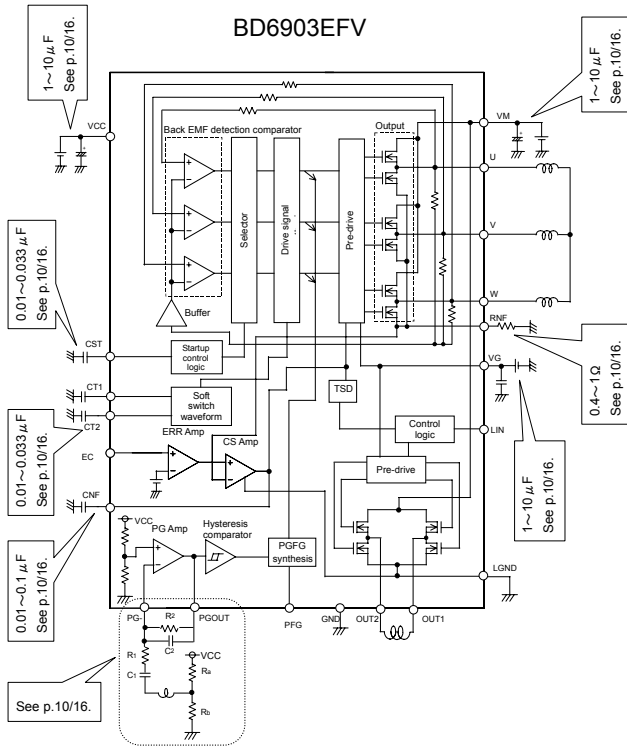Fig.7 Drum Output High-Side
Saturation Voltage

Fig.8 Drum Output Low-Side
Saturation Voltage

Fig.9 Loading Output Saturation Voltage
(Total of high-side and low-side voltages)

Fig.10 Torque Reference Gain and Current Limit
(RNF = 0.68 Ω)

● Block Diagram

BD6903EFV

Fig.11

Pin No.	Pin name	Function
1	GND	Signal GND pin
2	LIN	Loading block logic input pin
3	EC	Torque reference control input
4	CT1	Cylinder block slope capacitor connection pin
5	CT2	Cylinder block slope capacitor connection pin
6	CST	Cylinder block startup oscillation capacitor connection pin
7	CNF	Cylinder block phase compensation capacitor connection pin
8	PGOUT	Cylinder block PGAMP output pin
9	PG-	Cylinder block PG- input pin
10	VCC	VCC pin
11	W	Cylinder block motor output pin
12	V	Cylinder block motor output pin
13	RNF	Cylinder block motor GND pin (current detection resistor connection)
14	U	Cylinder block motor output pin
15	VG	DMOS VG power supply pin
16	VM	Cylinder and loading block motor power supply pin
17	OUT1	Loading block motor output pin
18	OUT2	Loading block motor output pin
19	LGND	Loading block motor GND pin
20	PFG	PG/FG synthesis output pin

BD6904FP
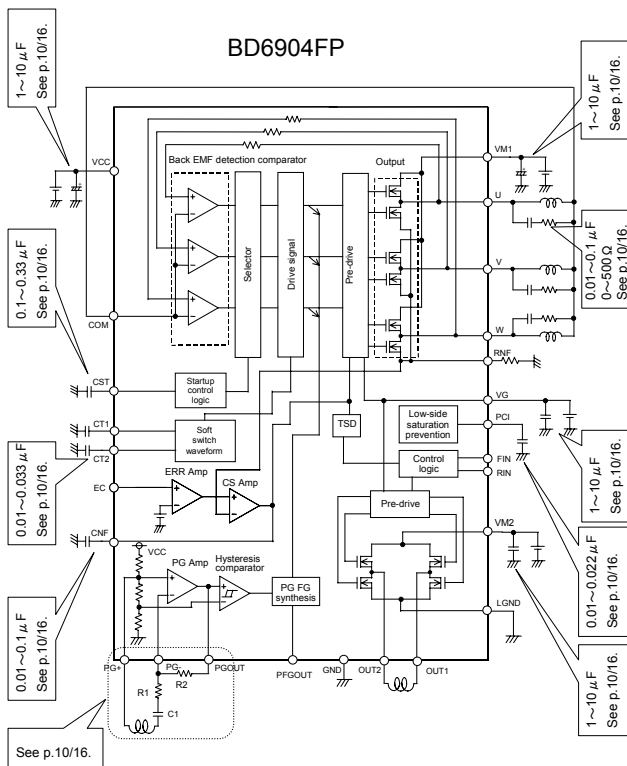
Fig.12

Pin No.	Pin name	Function
1	VM2	Loading block motor power supply pin
2	OUT1	Loading block motor output pin
3	LGND	Loading block motor GND pin
4	OUT2	Loading block motor output pin
5	FIN	Loading block logic input pin
6	RIN	Loading block logic input pin
7	VG	DMOS VG power supply pin
8	GND	Signal GND pin
9	CST	Cylinder block startup oscillation capacitor connection pin
10	CT1	Cylinder block slope capacitor connection pin
11	CT2	Cylinder block slope capacitor connection pin
12	PCI	Cylinder block phase compensation capacitor connection pin
13	CNF	Cylinder block phase compensation capacitor connection pin
14	EC	Torque reference control input pin
15	PG+	Cylinder block PG+ input pin
16	PG-	Cylinder block PG− input pin
17	PGOUT	Cylinder block PGAMP output pin
18	PFG	PG/FG synthesis output pin
19	VCC	Signal Vcc pin
20	COM	Cylinder block motor coil midpoint connection pin
21	VM1	Cylinder block motor power supply pin
22	U	Cylinder block motor output pin
23	V	Cylinder block motor output pin
24	RNF	Cylinder block motor GND pin (current detection resistor connection)
25	W	Cylinder block motor output pin

● Block Operation

○ Cylinder motor driver block

△ Output phase selection operation (See Figs.13 and 14 on P.9/16.)

1) Back EMF detection comparator

The back EMF Detection Comparator compares the motor output voltage and the motor midpoint potential to detect the position of the rotor (magnet) with respect to the stator (coil).

For the BD6904FP, the motor's midpoint potential should be connected directly to the COM pin, while for the BD6903EFV, the midpoint of the resistor connected internally to the output is used as a proxy indicator of the motor's midpoint potential.

2) Selector

The Selector selects either the internally synthesized 3-phase startup signal (startup mode) or back EMF detection comparator output (back EMF mode) based on the state of the SEL. It then outputs the selected signal to the next block. The SEL signal monitors the FG output and makes changes depending on whether the motor is rotating or not.

3) Drive signal synthesis

The signals used in position detection are passed through the MASK signal to eliminate any noise pulses caused by the motor's counter-electromotive voltage. These signals are then synthesized to create a signal (the FG signal) that switches between High and Low every 60° (electrical angle). After the position detection signals have been subject to noise elimination, their phase is delayed 30° (electrical angle) using the phase shift signal (COMPA). The signals are then synthesized with the SLOPE signal to create trapezoidal waveform signals that drive the High-side and Low-side value of each of the U, V, and W-phase components.

4) Soft switch waveform

Triangular waveforms are generated by charging and discharging the capacitors connected to the CT1 and CT2 pins out of phase (CT2 is discharged while CT1 is charged) using the FG signal. The MASK signal, the phase shift signal (COMPA), and the SLOPE signal are then created from these triangular waveforms.

5) Pre-drive

The pre-drive amplifies the U, V, and W-phase high-side and low-side drive trapezoidal waveform signals in proportion to the CS amp output signal. The voltage applied to the VG pin must be sufficiently higher than the VM voltage (BD6904FP: VM + 2 V or higher, BD6903EFV: VM + 3 V or higher) in order to lower the ON-resistance of the output's high-side power transistor.

6) Output

The signals from the pre-driver are current-amplified and used to drive the motors.

7) Startup control logic

The charge/discharge cycle is repeated by connecting a capacitor to the CST pin. When the motor is stopped, the CST pin is discharged after being charged until it reaches the high CST clamp voltage (2.8V typ.). It charges again after reaching the low CST clamp voltage (1.0V typ.). This charge/discharge interval acts to generate a rectangular waveform, which becomes the SEL signal. In addition to being input to the selector, the SEL signal is used to generate the drive signal during startup.

After its rising edge is divided, the SEL signal is synthesized and output as the drive signal during startup. When the SEL signal is high, the selector selects the drive signal during startup to force the motor to rotate, generating the counter-electromotive voltage required for sensorless operation (synchronization mode). Once the motor starts rotating and the FG signal's rising edge is detected before the D.CST pin voltage reaches the high CST clamp voltage, the CST pin begins to discharge in synchronization with the FG signal's rising edge. It then continues to repeat the cycle, beginning to charge again when the low CST clamp voltage is reached and discharging at the FG signal's rising edge. Once sustained rotation is achieved, the SEL signal will always be low because discharge occurs before the CST pin voltage reaches the high CST clamp voltage, causing the selector to select the back EMF comparator output signal to continue sensorless drive (back EMF mode).

△ Output current control operation

1) CS Amp.

The RNF pin is connected to the CS amp's negative input, causing a value (obtained by converting the output current to a voltage) to be input when a resistor with a small resistance value is connected between the RNF and GND pins. The CS amp outputs a control signal to the pre-driver so that the positive input voltage and negative input voltage remain equal, causing a current, obtained by dividing the positive input voltage by the RNF resistance value, to flow to the motor. Because this behavior comprises a negative feedback loop, a phase-compensation capacitor must be connected to the CNF pin to prevent oscillation.

2) ERR Amp.

The ERR amp reduces the differential between the voltage input to the EC pin and the internal reference voltage by a fixed factor and outputs it to create the CS amp's positive input voltage.

3) Low-side saturation prevention (BD6904FP only)

The IC continuously monitors the voltage differential between the output pins and the RNF pin and controls the pins so that their voltage differential stays above an internally set level (so that the output transistors do not become saturated). This control allows the IC to maintain the constant motor rotation by preventing distortion of the output current due to variations in the current's amplification factor caused by transistor saturation. Because the low-side saturation prevention circuit comprises a negative feedback loop circuit, a phase-compensation capacitor must be connected to the PCI pin to prevent oscillation.

△ PG/FB waveform output operation (See Fig.15 on P.9/16.)

    1) PG amp, Hysteresis comparator

        The PG amp amplifies the minute voltage generated by the motor's rotation in the external PG coil. The amp gain is determined by external resistors. The + input is biased through an internal reference. The hysteresis comparator converts the PG amp output waveform to a noiseless rectangular waveform (the PG signal).

    2) PG/FG synthesis

        The PG/FG synthesis circuit synthesizes the PG signal described above with the FG signal created by the drive signal synthesis circuit to output 3 values (high, middle, or low) to the PFG pin. The FG signal uses the low to middle output voltage, while the PG signal uses the middle to high output voltage.

○ Reversible Motor Driver

    1) Control logic

        The BD6903EFV controls the output state based on 3-value signal that inputted to the LIN pin (Pin 2).

        The BD6604FP controls the output state based on 2-value signal that inputted to the FIN pin (Pin 5) and RIN pin (Pin6).

        The driver must be placed in open or brake mode whenever switching between forward and reverse operation.

        For more information concerning the I/O logic, refer to the following table.

○ TSD

        The TSD, or Thermal Shut-Down circuit, turns OFF all driver output when the chip temperature Tj reaches approximately 170°C (typ, BD6903EFV) or approximately 175°C (typ, BD6904FP). The circuit resets after approximately 20°C (typ, BD6903EFV) or 25°C (typ, BD6904EP) of hysteresis.

● Loading Block I/O Logic Table

BD6903EFV

LIN	OUT1	OUT2	MODE
H	H	L	Forward rotation
M	L	L	Short brake
L	L	H	Reverse rotation

When no voltage is applied to V_{CC}, the loading block output and cylinder block output are open.

BD6904FP

FIN	RIN	OUT1	OUT2	MODE
H	L	H	L	Forward rotation
L	H	L	H	Reverse rotation
H	H	L	L	Short brake
L	L	OPEN	OPEN	Standby

When no voltage is applied to V_{CC}, the loading block output and cylinder block output are open.

● Timing Chart

Block waveforms during back EMF mode operation
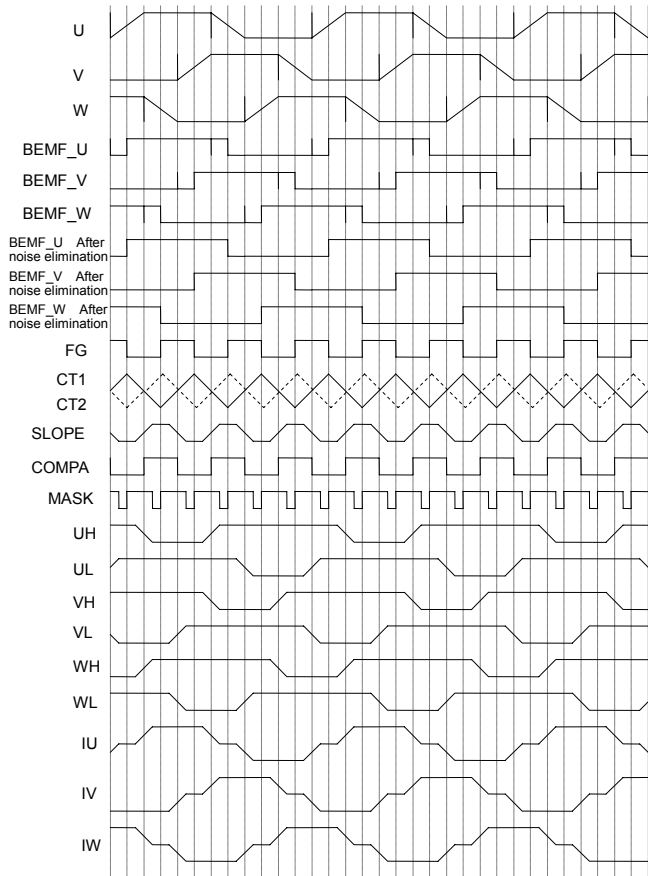
Fig.13

Startup waveforms
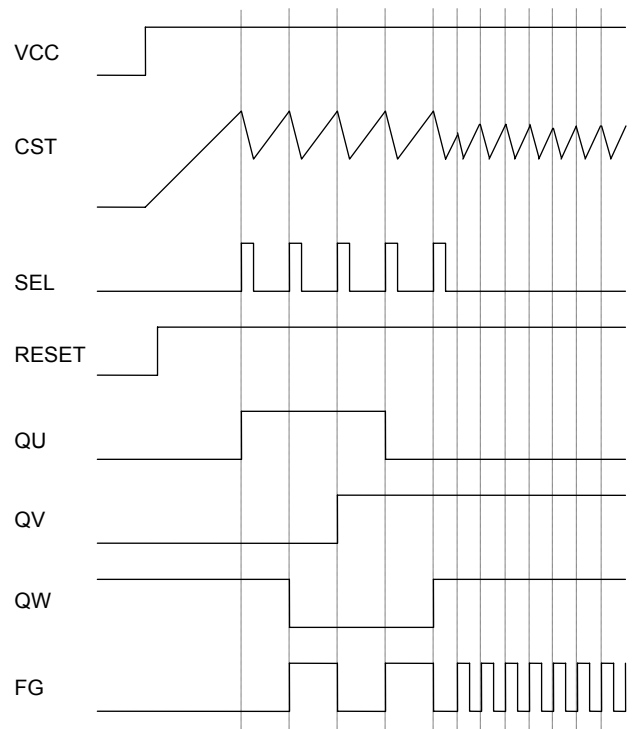
Fig.14

PG/FG synthesis
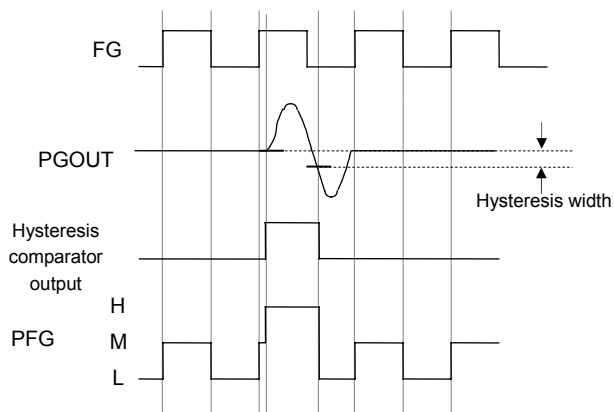
Fig.15

●Selecting Application Components

1) CST pin

The CST pin outputs a triangular waveform when a capacitor is connected between the CST and GND pins. The synchronized signal period and back EMF signal detection time varies with the connected capacitance value. Select the optimum value that produces the shortest startup time for the motor being used.

For most sensorless motors, a value between 0.1μF and 0.33μF is ideal.

2) CT1, CT2 pins

The CT1 and CT2 pins output triangular waveforms when capacitors are connected between the CT1 and GND pins and the CT2 and GND pins. These triangular waveforms are synchronized to the FG signal's high and low changes to create a repeating charge/discharge cycle. The triangular waveforms output by the CT1 and CT2 pins are anti-phase relative to one another.

CT1 and CT2 are reached to VCTL (low CT1, CT2 clamp voltage - see pgs. 3 and 4) to enable large discharge currents. Both the MASK signal, which is used to reject the noise pulse caused by the motor's back EMF, and the SLOPE signal, used to apply a gradient when the output current changes, are generated from the CT1 and CT2 triangular waveforms.

The amount of phase shift occurring from the rotor position detection comparator to the output voltage varies with the capacitance value connected to the CT1 and CT2 pins, as does the MASK signal time width. The gradient applied when the output current changes also varies accordingly. Connect the same capacitance value to both the CT1 and CT2 pins. The optimum value should be selected according to the motor being used so that there are no problems with motor rotation, output voltage, etc.

For most sensorless motors, a value from 0.01μF to 0.033μF is ideal.

3) CNF pin

The CNF pin serves as the CS amp output. The connection of a capacitor between it and the GND pin enables phase compensation. The capacitance value should be selected based on the servo constant, and proper motor operation should be confirmed. When the capacitance is too high, the I/O response deteriorates, while when too low, the output becomes easy to oscillate.

A value between 0.01μF and 0.1μF is ideal.

4) RNF pin

Connecting a resistor between the RNF and GND pins allows the detection of the current value flowing to output.

The output current IO is determined using the following equation, where RNF denotes the resistance connected between the RNF and GND pins, and VEC denotes the voltage applied to the EC pin.

$IO=(VEC-VECR)\cdot Gio\cdot 0.5/RNF$ (A) : BD6903EFV

$IO=(VECR-VEC)\cdot Gio\cdot 0.68/RNF$ (A) : BD6904FP

(VECR: torque reference start voltage, Gio: torque reference I/O gain – see P. 3/16, P. 4/16)

The BD6904FP incorporates a built-in current limiting circuit. The current limit current IOMAX is determined by the following equation:

$IOMAX=VCL/RNF$ (A)

(VCL: Current limit voltage - see P. 4/16)

For the BD6903EFV, a value from 0.4Ω to 1Ω (typical value: 0.5Ω) is recommended.

For the BD6904FP, a value from 0.45Ω to 1Ω (typical value: 0.68Ω) is recommended.

5) Motor output U, V, and W pins (applies to BD6904FP)

When there is a large amount of output voltage noise, reduce the noise by connecting a capacitor and resistor in series between each output pin and the COM pin. Determine the appropriate constants based on the motor. Use of non-optimum values may result in startup failures or uneven rotation.

If the motor operates properly without the capacitor and resistor, there is no need to add them.

The optimum capacitance and resistance values are from 0.01μF to 0.1μF and 0Ω to 500Ω, respectively.

6) PG amp gain setting resistance and filter capacitance

The PG amp gain GPG is determined by the ratio of R1 to R2 as described in the following equation:

$GPG=20logR2/R1$ (dB)

Set the gain from the input signal level so that the PGOUT amplitude is large enough compared to the hysteresis comparator's hysteresis level (BD6903EFV: VHYSP - see p. 3/16, BD6904FP: VPGTH - see P. 3/16) and so that the high and low output voltages (VOHP, VOLP: see P. 3/16) are not clamped.

R1 and C1 form a high-pass filter, while R2 and C2 form a low-pass filter, with the respective cutoff frequencies f_{HPF} and f_{LPF} determined by the following equation:

$f_{HPF}=1/2\pi R1C1$, $f_{LPF}=1/2\pi R2C2$

Select a value for which the main PG signal is not attenuated by the motor but for which unnecessary noise is attenuated.

7) PG coil bias resistance (applies to BD6903EFV), PG+ pin (applies to BD6904FP)

A DC bias is applied to the PG coil due to the PG coil's bias resistance. Set Ra = Rb to enable common mode rejection for the PG amp's positive input and VCC fluctuations. Select resistance values such that the current flowing to Ra and Rb is small and not prone to other types of interference.

If the PG+ pin is affected by noise, connect a capacitor between the PG+ pin and the GND pin.

The optimum resistance and capacitance values are from $10k\Omega$ to $100k\Omega$ and 0.01μF to 0.33μF, respectively.

8) VCC, VM, VG pins

Select a capacitance value that can sufficiently suppress high-frequency noise.

A value between 1μF and 10μF is ideal.

● Board layout precautions

   1. V_{CC} (BD6903EFV: Pin 10, BD6904FP: Pin 19) and VG pins (BD6903EFV: Pin 15, BD6904FP: Pin 7)

      Internal circuits other than output transistors operate on the V_{CC} and VG power supplies. The introduction of noise from an external source on these power supply lines may cause the IC to malfunction. Patterns should be laid out so that they are not affected by noise.

   2. GND pin (BD6903EFV: Pin 1, BD6904FP: Pin 8)

      Use the thickest wiring possible for ground.

   3. Power output pin (BD6903EFV: Pins 11, 12, 14, 17, and 18; BD6904FP: Pins 2, 4, 22, 23, and 25)

      Power loss may occur due to wiring resistance. Therefore, the IC should be placed close to the motor and connected using the shortest, thickest wiring possible.

   4. Motor GND pin (BD6903EFV: Pins 13 and 19, BD6904FP: Pins 3 and 24)

      Use the thickest wiring possible to prevent resistance contribution from the wiring. Connect the pin to the application ground using a separate line.

   5. COM pin (applies to BD6904FP: Pin 20)

      Use caution as noise input to the IC's internal back EMF detection comparator will cause the IC to malfunction.

   6. CT1, CT2 pins (BD6903EFV: Pins 4 and 5, BD6904FP: Pins 10, and 11)

      Use wiring of the same length and place the 2 capacitors close to the pins to ensure that they have the same charging/discharging characteristics.

   7. PG amp (BD6903EFV: Pins 8 and 9, BD6904FP: Pins 15,16 and 17)

      Noise will cause the IC to malfunction. Position the PG coil, external capacitors, and external resistors as close as possible to their respective pins.

   8. Island (applies to BD6903EFV)

      Connect the island to the GND pin using a separate line made of the thickest wiring possible.

● Power Dissipation Reduction

      The power dissipation (all loss) of the IC shows the power consumption of the IC when the ambient temperature is at room temperature (Ta = 25°C). The IC will generate heat when the IC consumes power, causing the temperature of the IC chip to be higher than the ambient temperature. The power consumption of the IC is limited. The power dissipation is determined by the thermal resistance (heat dissipation characteristics) of the package and the permissible temperature (i.e. absolute maximum rating of the junction temperature) of the IC chip in the package.

      Heat generated as a result of power consumption is radiated from the mold resin or lead frame of the package. A parameter that hampers the thermal radiation performance is called thermal resistance and expressed by θ j-a [°C/W]. The IC temperature in the package can be determined from the thermal resistance. Fig.16 depicts a thermal resistance package model.

      The thermal resistance θ j-a, ambient temperature Ta, junction temperature Tj, and power consumption P are obtained from the following equation.

$$\theta ja = (Tj - Ta) / P \quad [°C/W] \quad \cdots\cdots\cdots (I)$$

      The heat mitigation curve (derating curve) in Figs. 38 and 39 shows the permissible power consumption of the IC at ambient temperature. The possible power consumption of the IC decreases with increases in ambient temperature. This slope is determined by the thermal resistance θ ja.

      The thermal resistance θ ja depends on a variety of conditions, such as the chip size, power consumption, package ambient temperature, mounting conditions, and wind velocity. The derating curve depicts the reference values measured under specific conditions.

      For the BD6903EFV, the power dissipation is derated by 8.0 mW/°C over 25°C when mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm).

      For the BD6904FP, it is reduced by 11.6 mW/°C over 25°C when mounted on a glass epoxy board (90 mm × 90 mm × 1.6 mm).

$$\theta ja = (Tj\text{-}Ta) / P \quad [°C/W]$$

Ambient temperature Ta[°C]

Package surface temperature Ta[°C]

Chip surface temperature Tj[°C]
Power consumption P[W]
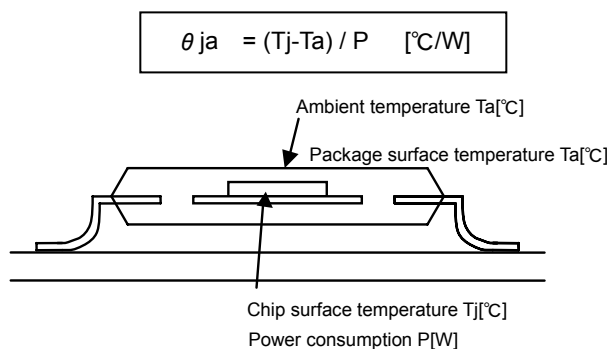
Fig.16 Thermal Resistance

● Heat Loss

    1) Heat generation mechanism

        With the BD6903EFV and BD6904EP, heat generation requires special attention during startup. Heat generation is significantly affected by the output current IO × the high-side and low-side loss voltage, as illustrated in Equation (1) below. The load on the IC is further increased when used with motors with low impedances,.
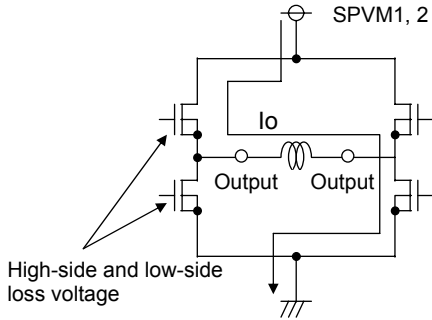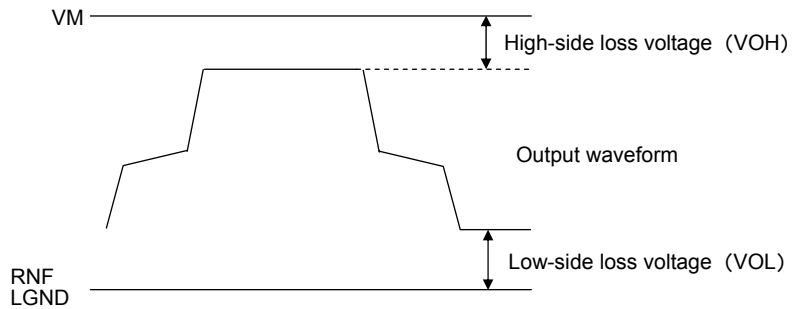

Fig.17 Motor Output Circuit Diagram

Fig.18 Output Waveform

        The IC's power consumption P is expressed by Equation (1).

$$P = VCC \times ICC + D.IO \times D.VLOSS + L.IO \times L.VLOSS \qquad (1)$$

(D.IO×D.VLOSS : cylinder block power consumption, L.IO×L.VLOSS : loading block power consumption)

        Consider Equation (1) as well as the package power (Pd) and ambient temperature (Ta) during operation and confirm that the IC's chip temperature Tj does not exceed 150°C.

        The chip will cease to function as a semiconductor when Tj exceeds 150°C, and problems such as parasitic behavior and leaks will occur. Continued use of the chip under these conditions will result in IC deterioration and damage. Therefore, the junction temperature must not exceed Tjmax=150℃ under any circumstances.

    2) Measuring the chip temperature

        The chip temperature can be determined by the following measurements.

Internal Equivalent Circuit

Sink a Constant-current of 100 µA.
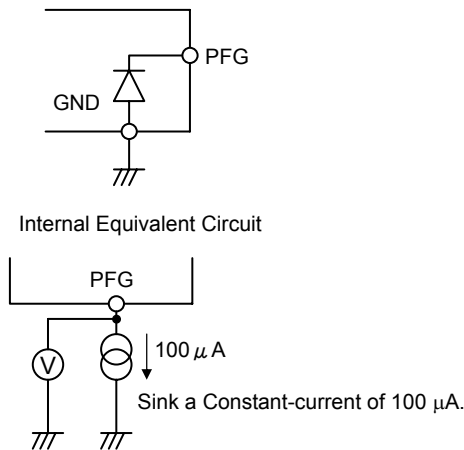
Fig.19

When not using the PFG output pin, the chip temperature can be estimated using the internal diode's temperature characteristics.

When calculating the chip temperature X under a given set of conditions:

Potential a (mV) at Tj = 25°C
Potential b (mV) at Tj = X°C

For example, if the value -2(mV/°C) is used for the diode's temperature characteristics, the chip temperature is given by:

$$\frac{b - a \ [mV]}{2 \ [mV \ / \ °C]} + 25 = X(°C)$$

    If an accurate chip temperature is required, the temperature characteristics of all of the IC's internal diodes must be taken into account.

● I/O Equivalent Circuit Diagrams

1) Loading block logic input pin
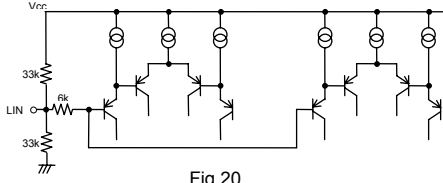
BD6903EFV

BD6904FP

Fig.20
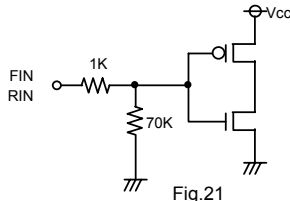
Fig.21

2) Torque reference control input pin
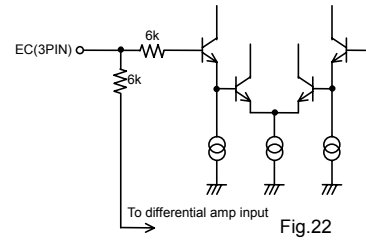
Fig.22

3) Slope capacitor connection pin
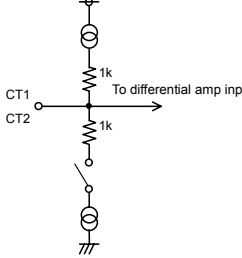
BD6903EFV

Fig.23

BD6904FP
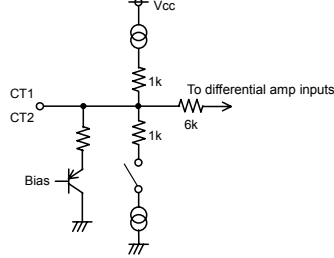
Fig.24

4) Startup oscillation capacitor connection pin
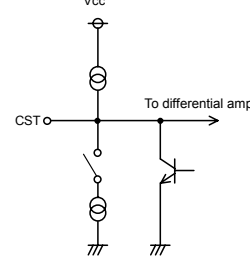
BD6903EFV

Fig.25

BD6904FP
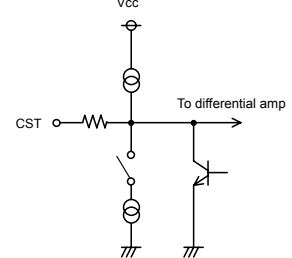
Fig.26

5) Capacitor connection pin for phase compensation

BD6903EFV
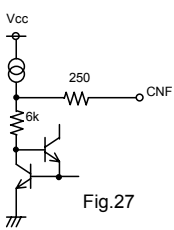
Fig.27

BD6904FP
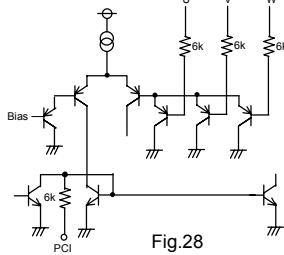
Fig.28

6) PGOUT output, PG input

BD6903EFV
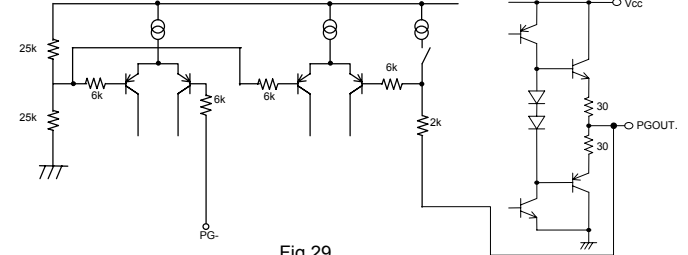
Fig.29

BD6904FP
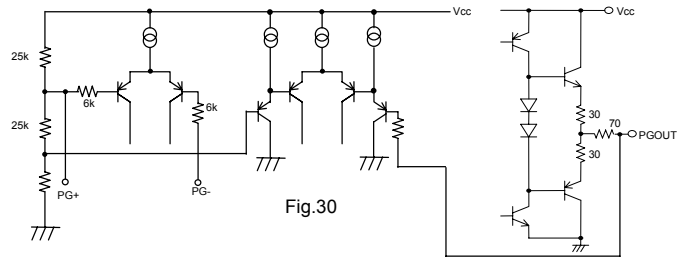
Fig.30

7) Cylinder block motor output

U, V, W, RNF
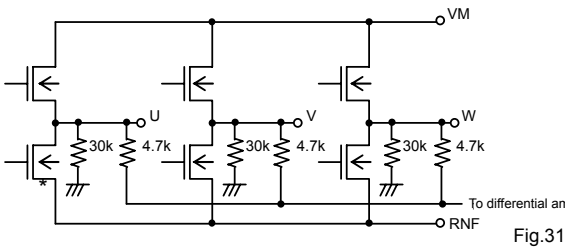
Fig.31
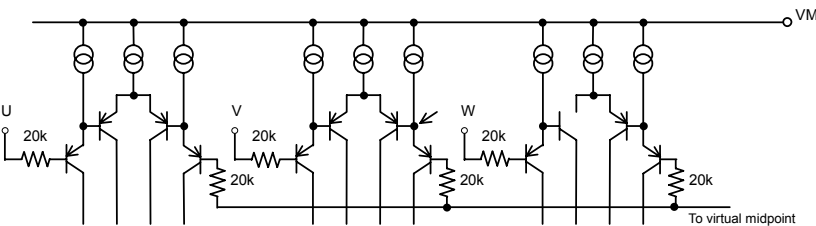
Fig.32

8) Loading block motor output

OUT1 ,OUT2, LGND
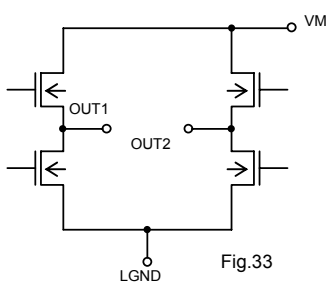
Fig.33

9) PG/FG synthesis output
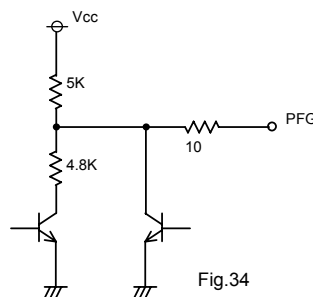
Fig.34

10) DMOS VG power supply

Fig.35

13/16
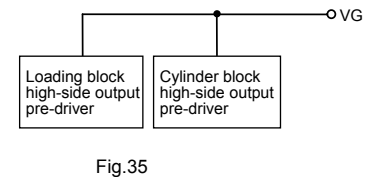
● Operation Notes

(1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

(2) Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

(3) Power supply lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, note that capacitance characteristic values are reduced at low temperatures.

(4) GND voltage

The potential of GND pin must be minimum potential in all operating conditions.

(5) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(6) Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

(7) Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

(8) ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

(9) Thermal shutdown circuit

The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

	TSD on temperature [°C] (Typ.)	Hysteresis temperature [°C] (Typ.)
BD6903EFV	170	20
BD6904FP	175	25

(10) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

(11) Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated.

P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.
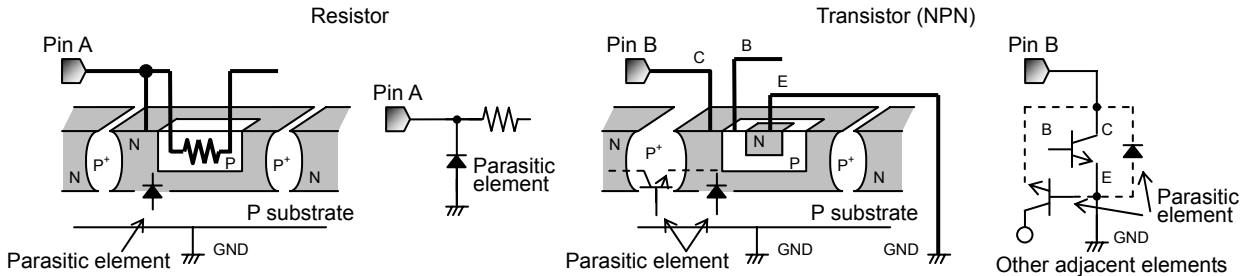
Fig. 36 Example of IC structure

(12) Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

(13) Power supply activation sequence

The power supplies should be turned ON in a specific order: VM → VG → VCC. Likewise, they should be turned OFF in a particular order: VCC → VG → VM. The position of VG and VM in the order can be switched without causing a problem. However, if VCC is activated before VM and VG have been turned ON, the loading block logic input pin (BD6903EFV: Pin 2, BD6904FP: Pins 5 and 6) must be OPEN and the torque reference control input pins (BD6903EFV: Pin 3, BD6904FP: Pin 14) set to 0V. Also, when VM and VG are turned OFF before VCC, the loading block logic input pin (BD6903EFV: Pin 2, BD6904FP: Pins 5 and 6) must be OPEN.

When turning the power supplies ON/OFF without regard to the orders described above, it is recommended that the loading block logic input pin (BD6903EFV: Pin 2, BD6904FP: Pins 5 and 6) be OPEN and the torque reference control input pins (BD6903EFV: Pin 3, BD6904FP: Pin be set to 0V.

● Power Dissipation Reduction

BD6903EFV
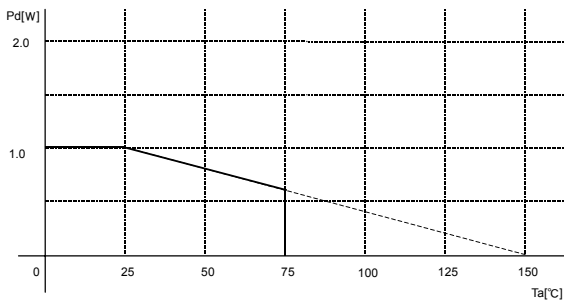
BD6904FP

∗ Reduced by 8.0 mW/°C over 25°C when mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm).

Fig.37
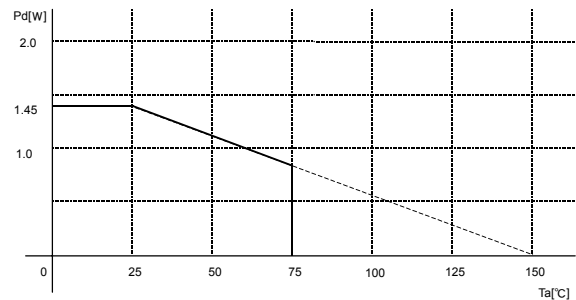
∗ Reduced by 11.6 mW/°C over 25°C when mounted on a glass epoxy board (90 mm × 90 mm × 1.6 mm)

Fig.38

● Part Number Explanation

• Please verify and specify the entire part number when ordering.

| B | D | 6 | 9 | 0 | 3 | E | F | V | – | E | 2 |

Part Number
• BD6903EFV
• BD6904FP

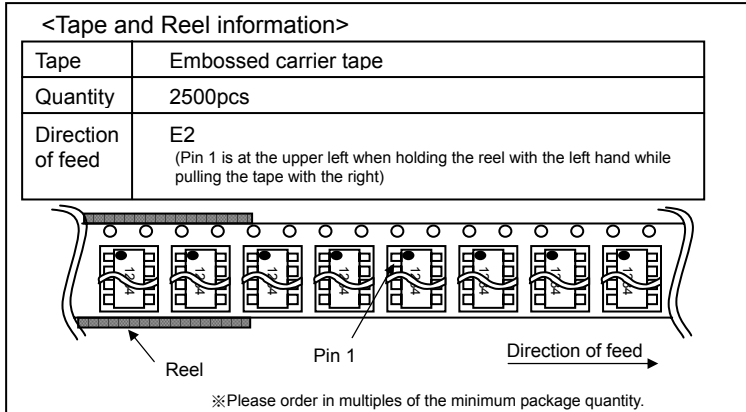**Package type**
• EFV : HTSSOP-B20
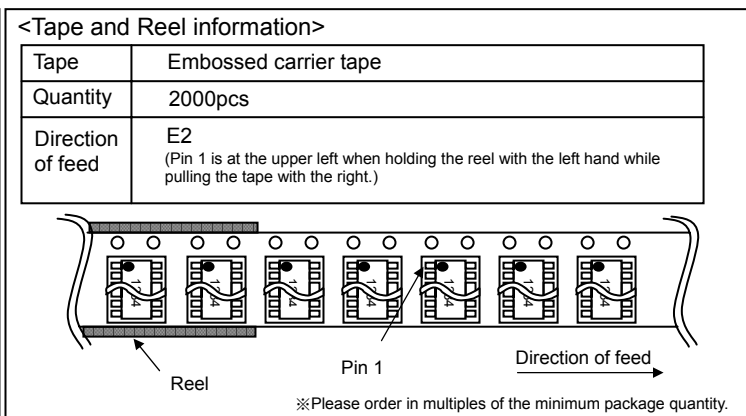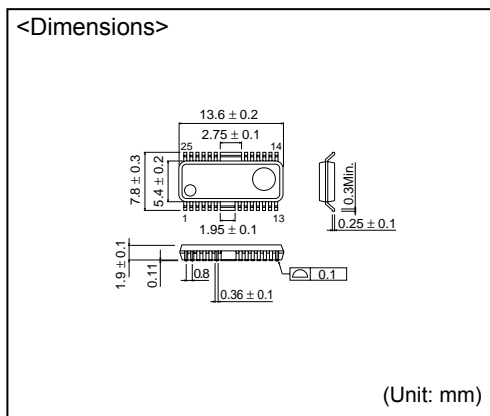• FM : HSOP25

E1: Reel-wound embossed taping,
    Pin 1 at front
E2: Reel-wound embossed taping,
    Pin 1 at back

HTSSOP-B20

<Dimensions>

6.5 ± 0.1
6.4 ± 0.2
4.4 ± 0.1
0.5 ± 0.15
1.0 ± 0.2
0.325
0.17 −0.05
20   11
1   10
S
1.0Max.
0.85 ± 0.05
0.08 ± 0.05
0.65   0.2 −0.03
0.08 S

(Unit: mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (Pin 1 is at the upper left when holding the reel with the left hand while pulling the tape with the right)

Reel   Pin 1   Direction of feed

※Please order in multiples of the minimum package quantity.

HSOP25

<Dimensions>

13.6 ± 0.2
2.75 ± 0.1
7.8 ± 0.3
5.4 ± 0.2
0.3Min.
25   14
1   13
1.95 ± 0.1
0.25 ± 0.1
1.9 ± 0.1
0.11
0.8
0.36 ± 0.1
0.1

(Unit: mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (Pin 1 is at the upper left when holding the reel with the left hand while pulling the tape with the right.)

Reel   Pin 1   Direction of feed

※Please order in multiples of the minimum package quantity.

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