

# DATA SHEET



## **SAA56xx**

Enhanced TV microcontrollers with  
On-Screen Display (OSD)

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**Enhanced TV microcontrollers with  
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**SAA56xx**

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## Enhanced TV microcontrollers with On-Screen Display (OSD)

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### 1 FEATURES

- Single-chip higher frequency microcontroller with integrated On-Screen Display (OSD)
- Versions available with integrated Data Capture
- Both active HIGH and active LOW reset pins
- OTP memory for both Program ROM and character sets
- In-System Programming (ISP) option for the embedded OTP memories using IEEE1149 (JTAG: Joint Test Action Group) interface
- Single power supply: 3.0 to 3.6 V
- 5 V tolerant digital inputs and I/O
- 32 I/O ports via individual addressable controls
- Larger Character ROM, up to 1020 characters of 12 × 10 pixels
- Smoothing capability on sized characters
- Programmable I/O for push-pull, open-drain and quasi-bidirectional and high-impedance
- Two port lines with 8 mA sink (at <0.4 V) capability, for direct drive of LED
- Single crystal oscillator for microcontroller, OSD and Data Capture
- Power reduction modes: Idle, Standby and Power-down
- Byte level I<sup>2</sup>C-bus up to 400 kHz dual port I/O
- 64 Dynamically Redefinable Characters for OSDs
- Increased special graphic characters allowing four colours per character
- Selectable character height 9, 10, 13 and 16 TV lines
- Pin compatibility throughout family
- Operating temperature: -20 to +70 °C.



### 2 GENERAL DESCRIPTION

The SAA56xx family of microcontrollers are a derivative of the Philips industry-standard 80C51 microcontroller and are intended for use as the central control mechanism in a television receiver. They provide control functions for the television system, OSD and incorporate an integrated Data Capture and display function for either Teletext or Closed Caption.

Additional features over the SAA55xx family have been included, e.g. 100/120 Hz (2H/2V only) display timing modes, two page operation (50/60 Hz mode for 16:9, 4:3), higher frequency microcontroller, increased character storage, more 80C51 peripherals and a larger Display memory. For CC operation, only a 50/60 Hz display option is available.

As with the rest of the SAA55xx family, the Data Capture hardware can decode and display both 525-line and 625-line World System Teletext (WST), Closed Caption information, Video Programming System (VPS) Information and Wide Screen Signalling (WSS) information. The same display hardware is used for Teletext, Closed Caption and On-Screen Display, which means that the display features available give greater flexibility to differentiate the TV set.

The family of devices offers a range of memory variants with Program ROM sizes of 128-kbyte and 192-kbyte, also up to 14 kbytes of RAM.

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### 3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>					
$V_{DDX}$	any supply voltage ( $V_{DD}$ to $V_{SS}$ )	3.0	3.3	3.6	V
$I_{DDP}$	periphery supply current	1.0	–	–	mA
$I_{DDC}$	core supply current	–	15.0	18.0	mA
$I_{DD(id)}$	Idle mode supply current	–	4.6	6.0	mA
$I_{DD(pd)}$	Power-down mode supply current	–	0.76	1.0	mA
$I_{DDA}$	analog supply current	–	45.0	48.0	mA
$I_{DDA(id)}$	Idle mode analog supply current	–	0.87	1.0	mA
$I_{DDA(pd)}$	Power-down mode analog supply current	–	0.45	0.7	mA
$f_{xtal}$	crystal frequency	–	12.0	–	MHz
$T_{amb}$	operating ambient temperature	–20	–	+70	°C
$T_{stg}$	storage temperature	–55	–	+125	°C

### 4 ORDERING INFORMATION

TYPE NUMBER <sup>(1)</sup>	PACKAGE			ROM	DATA RAM	DATA CAPTURE
	NAME	DESCRIPTION	VERSION			
SAA5667HL/nnnn	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1	192-kbyte	2-kbyte <sup>(2)</sup>	text and line 21
SAA5665HL/nnnn				128-kbyte		text and line 21
SAA5647HL/nnnn				192-kbyte		line 21 only
SAA5645HL/nnnn				128-kbyte		line 21 only

#### Notes

- 'nnnn' is a four digit number uniquely referencing the microcontroller program mask.
- Extendible to 8-kbyte in external SRAM application, see Fig.8.

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## 5 BLOCK DIAGRAM

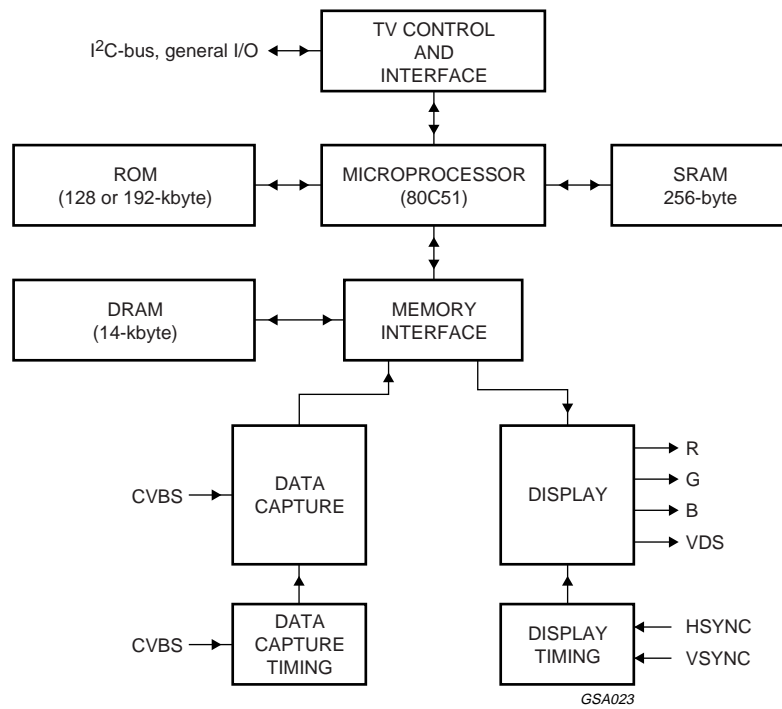


Fig.1 Block diagram (top level architecture).

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### 6 PINNING INFORMATION

#### 6.1 Pinning

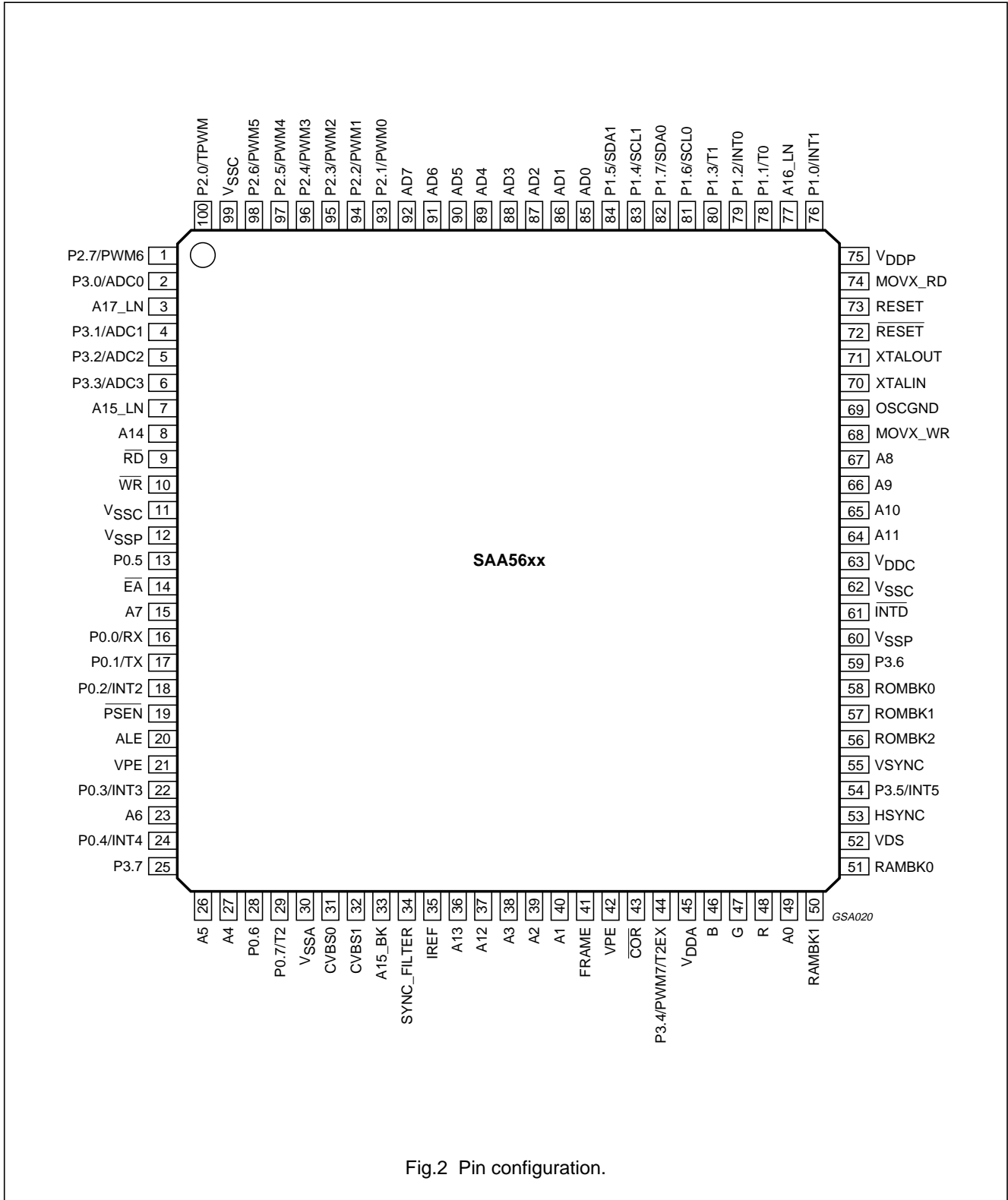


Fig.2 Pin configuration.

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### 6.2 Pin description

**Table 1** LQFP100 package

SYMBOL	PIN	TYPE	DESCRIPTION
P2.0/TPWM	100	I/O	<b>Port 2.</b> 8-bit programmable bidirectional port with alternative functions. P2.0/TPWM is the output for the 14-bit high precision PWM; P2.1/PWM0 to P2.7/PWM6 are the outputs for the 6-bit PWMs 0 to 6.
P2.1/PWM0	93	I/O	
P2.2/PWM1	94	I/O	
P2.3/PWM2	95	I/O	
P2.4/PWM3	96	I/O	
P2.5/PWM4	97	I/O	
P2.6/PWM5	98	I/O	
P2.7/PWM6	1	I/O	
P3.0/ADC0	2	I/O	<b>Port 3.</b> 8-bit programmable bidirectional port with alternative functions. P3.0/ADC0 to P3.3/ADC3 are the inputs for the software ADC facility and P3.4/PWM7 is the output for the 6-bit PWM7; P3.4/PWM7/T2EX is the output for the 6-bit PWM7 or the Timer 2 control; P3.5/INT5 is the external Interrupt 5; P3.6 and P3.7 have no alternative functions.
P3.1/ADC1	4	I/O	
P3.2/ADC2	5	I/O	
P3.3/ADC3	6	I/O	
P3.4/PWM7/T2EX	44	I/O	
P3.5/INT5	54	I/O	
P3.6	59	I/O	
P3.7	25	I/O	
V <sub>SSC</sub>	11, 62, 99	–	core ground
P0.0/RX	16	I/O	<b>Port 0.</b> 8-bit programmable bidirectional port (with alternative functions). P0.0/RX and P0.1/TX are respectively the serial transmit and receive lines for the UART; P0.2/INT2 to P0.4/INT4 are the external interrupts 2 to 4; P0.5 and P0.6 have no alternative functions and have 8 mA current sinking capability for direct drive of LEDs.
P0.1/TX	17	I/O	
P0.2/INT2	18	I/O	
P0.3/INT3	22	I/O	
P0.4/INT4	24	I/O	
P0.5	13	I/O	
P0.6	28	I/O	
P0.7/T2	29	I/O	
V <sub>SSA</sub>	30	–	analog ground
CVBS0	31	I	2 composite video input selectable via SFR; a positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor
CVBS1	32	I	
SYNC_FILTER	34	I/O	CVBS sync filter input; this pin should be connected to V <sub>SSA</sub> via a 100 nF capacitor.
IREF	35	I	Reference current input for analog circuits, connected to V <sub>SSA</sub> via a 24 kΩ resistor.
FRAME	41	O	De-interlace output synchronized with the VSYNC pulse to produce a non-interlaced display by adjustment of the vertical deflection circuits.
VPE	21, 42	I	OTP programming voltage
COR	43	O	Open-drain, active LOW output which allows selective contrast reduction of the TV picture to enhance a mixed mode display.
V <sub>DDA</sub>	45	–	+3.3 V analog power supply
B	46	O	pixel rate output of the BLUE colour information

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SYMBOL	PIN	TYPE	DESCRIPTION
G	47	O	pixel rate output of the GREEN colour information
R	48	O	pixel rate output of the RED colour information
VDS	52	O	video/data switch push-pull output for dot rate fast blanking
HSYNC	53	I	Schmitt triggered input for a TTL-level version of the horizontal sync pulse; the polarity of this pulse is programmable by register bit TXT1.H POLARITY.
VSYSN	55	I	Schmitt triggered input for a TTL-level version of the vertical sync pulse; the polarity of this pulse is programmable by register bit TXT1.V POLARITY.
V <sub>SSP</sub>	12, 60	–	periphery ground
V <sub>DDC</sub>	63	–	+3.3 V core power supply
OSCGND	69	–	crystal oscillator ground
XTALIN	70	I	12 MHz crystal oscillator input
XTALOUT	71	O	12 MHz crystal oscillator output
$\overline{\text{RESET}}$	72	I	If the reset input is LOW for at least 24 crystal oscillator periods while the oscillator is running, the device is reset (internal pull-up).
RESET	73	I	If the reset input is HIGH for at least 24 crystal oscillator periods while the oscillator is running, the device is reset. This pin should be connected to V <sub>DDC</sub> via a capacitor if an active HIGH reset is required (internal pull-down).
V <sub>DDP</sub>	75	–	+3.3 V periphery power supply
P1.0/INT1	76	I/O	<b>Port 1.</b> 8-bit programmable bidirectional port with alternative functions. P1.0/INT1 is external interrupt 1 which can be triggered on the rising and falling edge of the pulse; P1.1/T0 is Timer/counter 0; P1.2/INT0 is external interrupt 0; P1.3/T1 is Timer/counter 1; P1.6/SCL0 is the serial clock input for the I <sup>2</sup> C-bus; P1.7/SDA0 is the serial data port for the I <sup>2</sup> C-bus; P1.4/SCL1 is the serial clock input for the I <sup>2</sup> C-bus; P1.5/SDA1 is the serial data port for the I <sup>2</sup> C-bus.
P1.1/T0	78	I/O	
P1.2/INT0	79	I/O	
P1.3/T1	80	I/O	
P1.6/SCL0	81	I/O	
P1.7/SDA0	82	I/O	
P1.4/SCL1	83	I/O	
P1.5/SDA1	84	I/O	
$\overline{\text{RD}}$	9	O	read control signal to external data memory
$\overline{\text{WR}}$	10	O	write control signal to external data memory
$\overline{\text{EA}}$	14	I	Control signal used to select external (LOW) or internal (HIGH) program memory (internal pull-up).
PSEN	19	O	enable signal for external program memory
ALE	20	O	external latch enable signal; active HIGH
AD0 to AD7	85 to 92	I/O	address lines A0 to A7 multiplexed with data lines D0 to D7.
A0 to A7	49, 40, 39, 38, 27, 26, 23, 15	O	address lines A0 to A7
A8 to A14	67 to 64, 37, 36, 8	O	address lines A8 to A14
A15_LN to A17_LN	7, 77, 3	O	address lines A15 to A17; note 1
MOVX_WR	68	O	MOVX Write for Hitex 80C51 emulation (internal MOVX Write instruction)
MOVX_RD	74	O	MOVX Read for Hitex 80C51 emulation (internal MOVX Read instruction)



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SYMBOL	PIN	TYPE	DESCRIPTION
A15_BK	33	O	address line A15 when using ROMBK outputs for external program ROM access
ROMBK0 to ROMBK2	58 to 56	O	ROMBK SFR selection bits for external program ROM access >64 kbytes
RAMBK0 to RAMBK1	51, 50	O	RAMBK SFR selection bits for external program SRAM data storage >64 kbytes. Use A0 to A14 and A15_BK as lower address bits.
INTD	61	I	interrupt disable for emulation (internal pull-up)

### Note

1. A15\_LN, A16\_LN and A17\_LN form a linear address space and may be used as an alternative to A15\_BK (pin 33) and ROMBK2 to ROMBK0 (pins 56, 57 and 58) for external program ROM access.

## 7 MICROCONTROLLER

The functionality of the microcontroller used in this device is described here with reference to the industry standard 80C51 microcontroller. A full description of its functionality can be found in "*Handbook IC20 80C51-Based 8-bit Microcontrollers*".

### 7.1 Microcontroller features

- 80C51 microcontroller core standard instruction set and timing
- 0.5  $\mu$ s machine cycle
- Maximum 192K  $\times$  8-bit Program ROM
- Maximum of 14K  $\times$  8-bit data and display RAM
- 15-level interrupt controller with individual enable/disable and two level priority
- Up to six external interrupts with programmable detection characteristics
- Three 16-bit Timer/counter registers
- Watchdog Timer
- Auxiliary RAM page pointer
- 16-bit Data pointer
- Idle, Standby and Power-down modes
- 32 general I/O lines
- Eight 6-bit Pulse Width Modulator (PWM) outputs for control of TV analog signals
- One 14-bit PWM for Voltage Synthesis Tuner (VST) control
- 8-bit Analog-to-Digital Converter (ADC) with four multiplexed inputs
- Two high current outputs for directly driving LEDs etc.
- I<sup>2</sup>C-bus byte level interface with dual ports

- UART for asynchronous serial communication
- External ROM and SRAM compatibility.

## 8 MEMORY ORGANISATION

The device has the capability of a maximum of 192-kbyte Program ROM and 14-kbyte Data RAM internally.

### 8.1 ROM bank switching

The 128-kbyte Program ROM variant is arranged in four banks of 32 kbytes. One of the 32-kbyte banks is common and is always addressable. The other three banks (Bank 0, Bank 1 and Bank 2) can be selected with SFR ROMBK bits <2:0> (see Table 2 and Fig. 3).

The 192-kbyte Program ROM variant is arranged in six banks of 32 kbytes. One of the 32-kbyte banks is common and is always addressable. The other five banks (Bank 0, Bank 1, Bank 2, Bank 3 and Bank 4) can be selected with SFR ROMBK bits <2:0> (see Table 2 and Fig. 3).

**Table 2** ROM bank selection

ROMBK2	ROMBK1	ROMBK0	0 to 32-kbyte	32 to 64-kbyte
0	0	0	common	Bank 0
0	0	1	common	Bank 1
0	1	0	common	Bank 2
0	1	1	common	Bank 3
1	0	0	common	Bank 4
1	0	1	reserved	reserved
1	1	0	reserved	reserved
1	1	1	reserved	reserved

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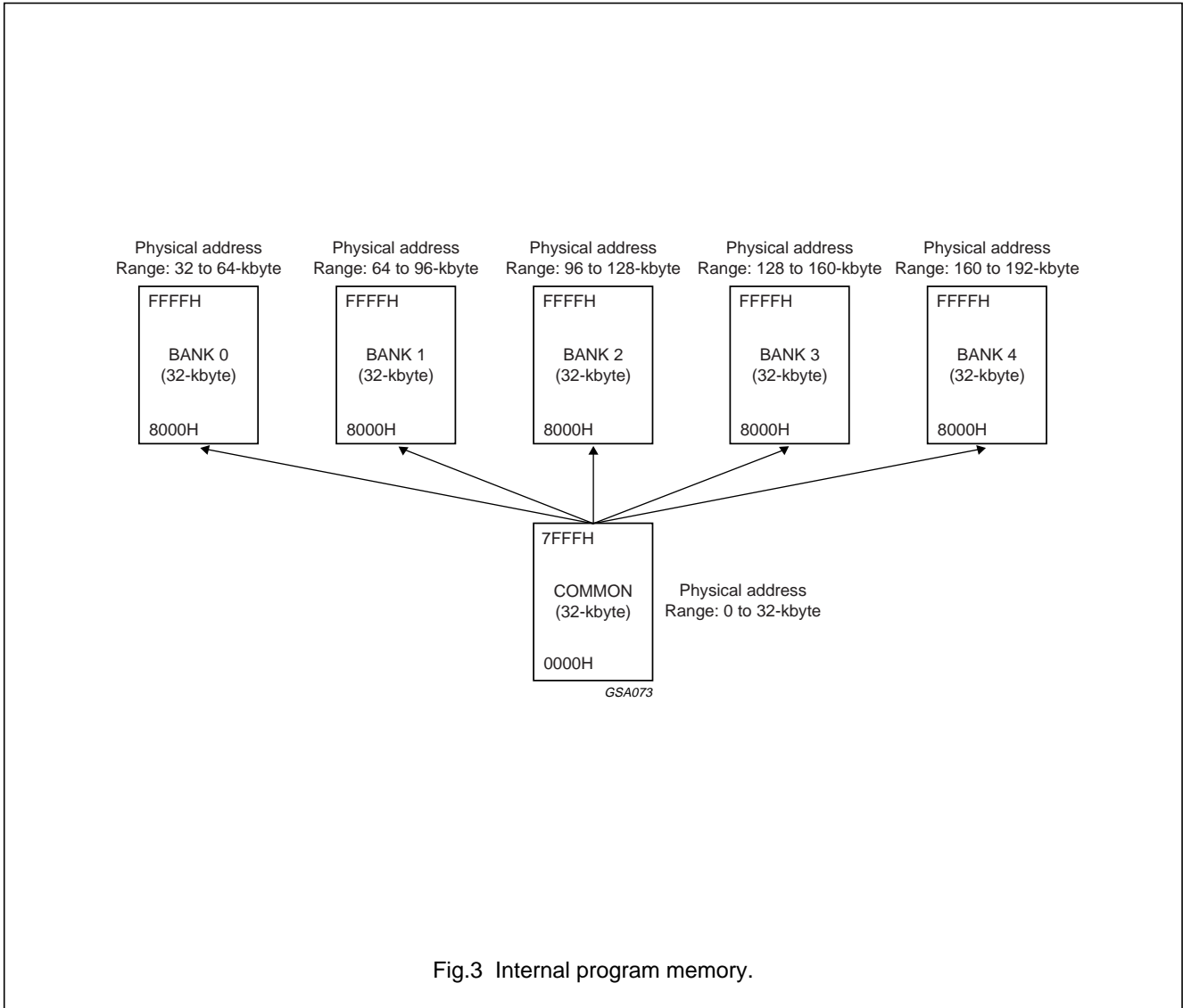


Fig.3 Internal program memory.

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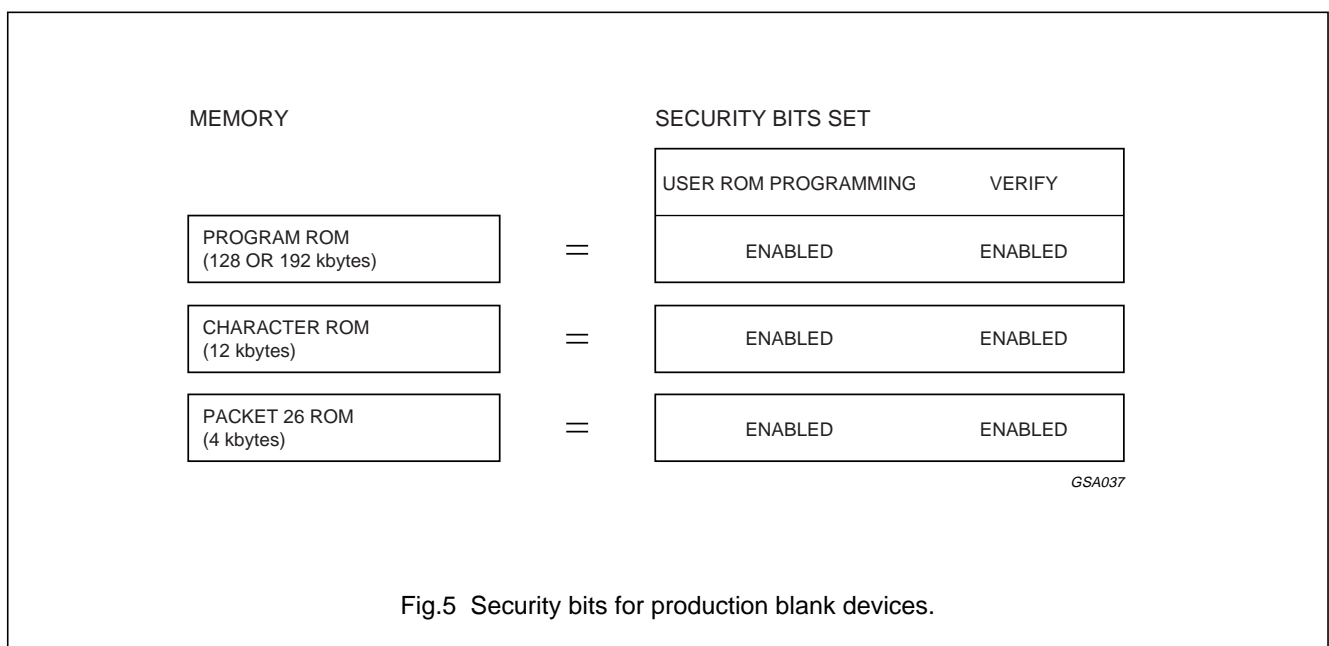
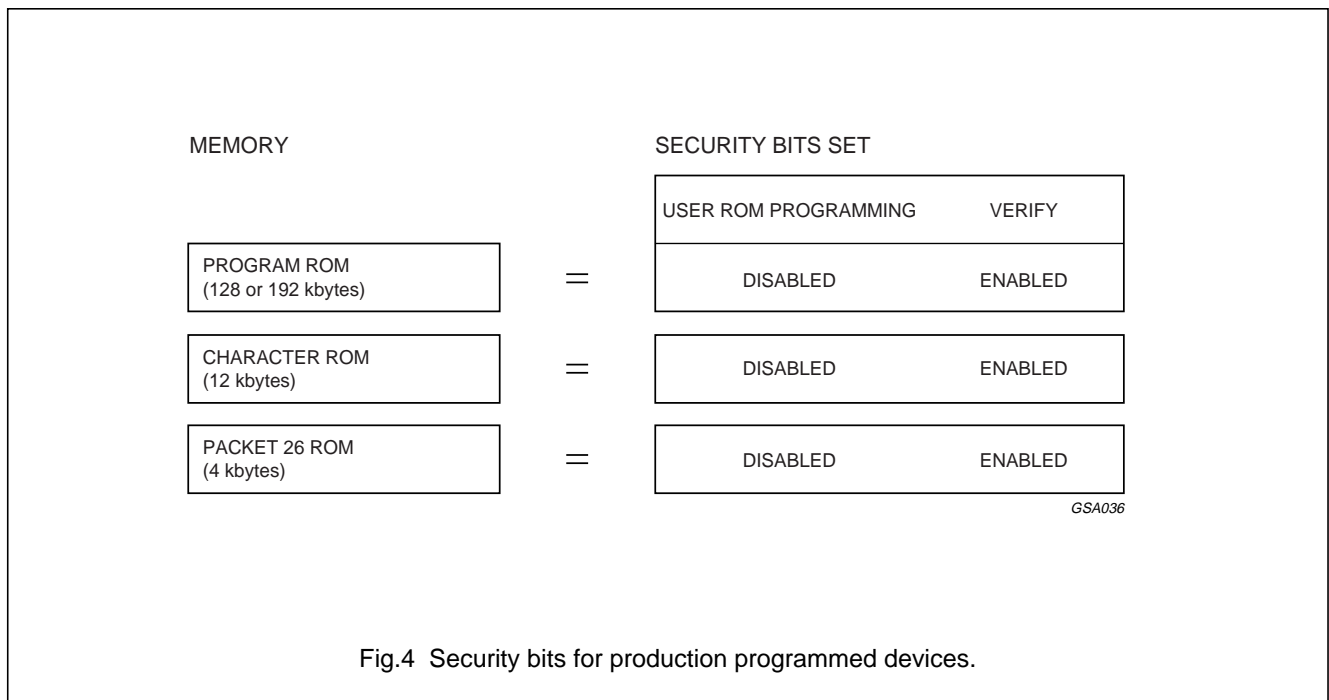
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### 8.2 ROM protection and verification

SAA56xx devices have a set of security bits allied with each section of the device, i.e. Program ROM, Character ROM and Packet 26 ROM. The security bits are used to prevent the ROM from being overwritten once programmed, and also the contents being verified once programmed.

The security bits can be programmed once only and **cannot** be erased.

The SAA56xx security bits are set as shown in Fig.4 for production programmed devices and are set as shown in Fig.5 for production blank devices.



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### 8.3 RAM organisation

Figure 6 shows the internal Data RAM is organised into two areas: Data memory and the Special Function Registers (SFRs).

### 8.4 Data memory

The Data memory (see Fig.6) is 256 × 8 bits and occupies address range 00H to FFH when using indirect addressing and 00H to 7FH when using direct addressing. The SFRs occupy the address range 80H to FFH and are accessible using direct addressing only.

The lower 128 bytes of Data memory are mapped as shown in Fig.7. The lowest 32 bytes are grouped into four banks of eight registers selectable via SFR PSW bits <4:3> (RS1/RS0; see Table 3), the next 16 bytes above the register banks form a block of bit addressable memory space.

The upper 128 bytes are not allocated for any special area or functions.

**Table 3** Bank selection

RS1	RS0	BANK
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 3

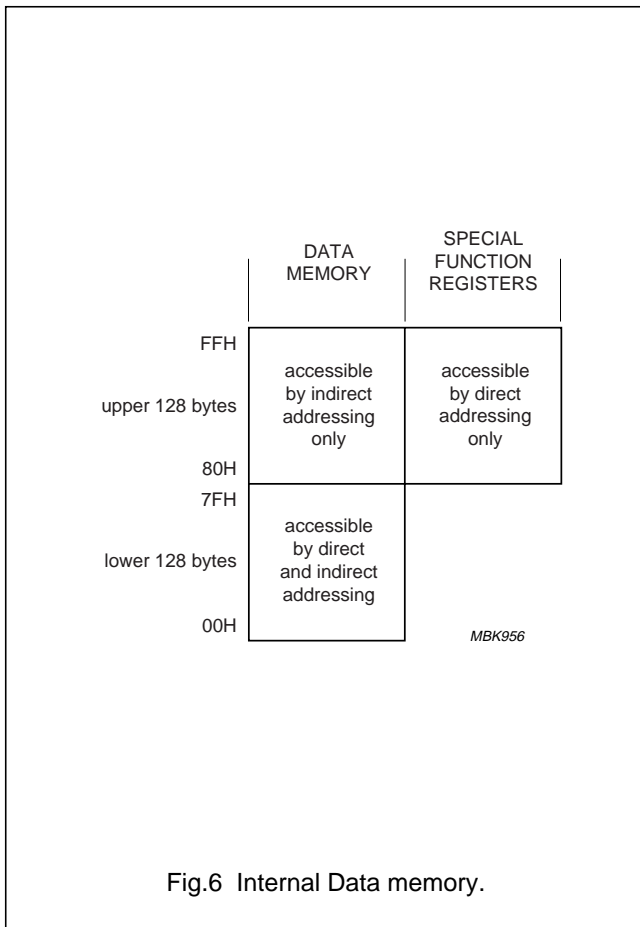


Fig.6 Internal Data memory.

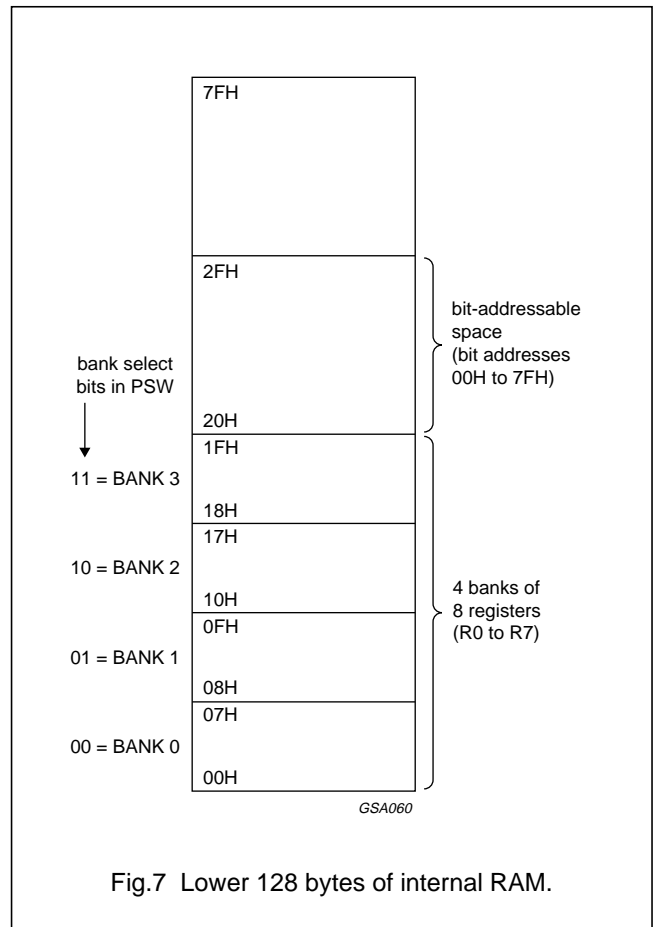


Fig.7 Lower 128 bytes of internal RAM.

## 8.5 SFR memory

The Special Function Register (SFR) space is used for port latches, timer, peripheral control, acquisition control and display control, etc. These registers can only be accessed by direct addressing. Sixteen of the addresses in the SFR space are both bit and byte addressable. The bit addressable SFRs are those whose address ends in 0H or 8H. Table 4 only presents the additional SFRs of the SAA56xx family over the SAA55xx family of devices. This SFR map table must therefore be read in conjunction with the SAA55xx SFR map table.

A description of the new SFR bits is shown in Table 5, which presents the SFRs in alphabetical order.

**Table 4** SFR memory map

ADD	R/W	NAME	7	6	5	4	3	2	1	0	RESET
80H	R/W	P0	P07	P06	P05	P04	P03	P02	P01	P00	FFH
81H	R/W	SP	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	07H
82H	R/W	DPL	DPL7	DPL6	DPL5	DPL4	DPL3	DPL2	DPL1	DPL0	00H
83H	R/W	DPH	DPH7	DPH6	DPH5	DPH4	DPH3	DPH2	DPH1	DPH0	00H
84H	R/W	IEN1	EX5	EX4	EX3	EX2	EUTX	EURX	EUART	ET2	00H
85H	R/W	IP1	PX5	PX4	PX3	PX2	PUTX	PURX	PUART	PT2	00H
86H	R/W	EXTINT	EX5CFG1	EX5CFG0	EX4CFG1	EX4CFG0	EX3CFG1	EX3CFG0	EX2CFG1	EX2CFG0	00H
87H	R/W	PCON	SMOD	ARD	RFI	WLE	GF1	GF0	PD	IDL	00H
88H	R/W	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
89H	R/W	TMOD	GATE	C/ $\bar{T}$	M1	M0	GATE	C/ $\bar{T}$	M1	M0	00H
8AH	R/W	TL0	TL07	TL06	TL05	TL04	TL03	TL02	TL01	TL00	00H
8BH	R/W	TL1	TL17	TL16	TL15	TL14	TL13	TL12	TL11	TL10	00H
8CH	R/W	TH0	TH07	TH06	TH05	TH04	TH03	TH02	TH01	TH00	00H
8DH	R/W	TH1	TH17	TH16	TH15	TH14	TH13	TH12	TH11	TH10	00H
90H	R/W	P1	P17	P16	P15	P14	P13	P12	P11	P10	FFH
91H	R/W	GPR1	GPR17	GPR16	GPR15	GPR14	GPR13	GPR12	GPR11	GPR10	00H
92H	R/W	GPR2	GPR27	GPR26	GPR25	GPR24	GPR23	GPR22	GPR21	GPR20	00H
93H	R/W	GPR3	GPR37	GPR36	GPR35	GPR34	GPR33	GPR32	GPR31	GPR30	00H
94H	R/W	GPR4	GPR47	GPR46	GPR45	GPR44	GPR43	GPR42	GPR41	GPR40	00H
95H	R/W	GPR5	GPR57	GPR56	GPR55	GPR54	GPR53	GPR52	GPR51	GPR50	00H
96H	R/W	P0CFGA	P0CFGA7	P0CFGA6	P0CFGA5	P0CFGA4	P0CFGA3	P0CFGA2	P0CFGA1	P0CFGA0	FFH
97H	R/W	P0CFGB	P0CFGB7	P0CFGB6	P0CFGB5	P0CFGB4	P0CFGB3	P0CFGB2	P0CFGB1	P0CFGB0	00H
98H	R/W	SADB	0	0	0	DC_COMP	SAD3	SAD2	SAD1	SAD0	00H
99H	R/W	S0CON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00H
9AH	R/W	S0BUF	S0BUF	S0BUF6	S0BUF5	S0BUF4	S0BUF3	S0BUF2	S0BUF1	S0BUF0	00H

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ADD	R/W	NAME	7	6	5	4	3	2	1	0	RESET
9CH	R/W	GPR6	GPR67	GPR66	GPR65	GPR64	GPR63	GPR62	GPR61	GPR60	00H
9DH	R/W	GPR7	GPR77	GPR76	GPR75	GPR74	GPR73	GPR72	GPR71	GPR70	00H
9EH	R/W	P1CFGA	P1CFGA7	P1CFGA6	P1CFGA5	P1CFGA4	P1CFGA3	P1CFGA2	P1CFGA1	P1CFGA0	FFH
9FH	R/W	P1CFGB	P1CFGB7	P1CFGB6	P1CFGB5	P1CFGB4	P1CFGB3	P1CFGB2	P1CFGB1	P1CFGB0	00H
A0H	R/W	P2	P27	P26	P25	P24	P23	P22	P21	P20	FFH
A1H	R	TXT31	–	–	–	–	GPF11	GPF10	GPF9	GPF8	00H
A2H	R	TXT32	9FE11	9FF11	9FF10	9FF9	9FF8	9FF7	9FF6	9FF5	00H
A3H	R	TXT33	BFE7	BFE6	BFE5	BFE4	BFE3	BFE2	BFE1	BFE0	00H
A4H	R	TXT34	–	–	–	–	BFE11	BFE10	BFE9	BFE8	00H
A5H	R/W	GPR8	GPR87	GPR86	GPR85	GPR84	GPR83	GPR82	GPR81	GPR80	00H
A6H	R/W	P2CFGA	P2CFGA7	P2CFGA6	P2CFGA5	P2CFGA4	P2CFGA3	P2CFGA2	P2CFGA1	P2CFGA0	FFH
A7H	R/W	P2CFGB	P2CFGB7	P2CFGB6	P2CFGB5	P2CFGB4	P2CFGB3	P2CFGB2	P2CFGB1	P2CFGB0	00H
A8H	R/W	IEN0	EA	EBUSY	ES2	ECC	ET1	EX1	ET0	EX0	00H
A9H	R/W	TXT23	NOT B 3	NOT B 2	NOT B 1	NOT B 0	EAST/WEST B	DRCS B ENABLE	BS B1	BS B0	00H
AAH	R/W	TXT24	BKGND OUT B	BKGND IN B	CORB OUT B	CORB IN B	TEXT OUT B	TEXT IN B	PICTURE ON OUT B	PICTURE ON IN B	00H
ABH	R/W	TXT25	BKGND OUT B	BKGND IN B	CORB OUT B	CORB IN B	TEXT OUT B	TEXT IN B	PICTURE ON OUT B	PICTURE ON IN B	00H
ACH	R/W	TXT26	EXTENDED DRCS	TRANS B	C MESH ENABLE B	B MESH ENABLE B	SHADOW ENABLE B	BOX ON 24 B	BOX ON 1 B to 23 B	BOX ON 0 B	00H
ADH	R/W	TXT28	MULTI PAGE	CC_TXT B	ACTIVE PAGE	DISPLAY BANK B	PAGE B3	PAGE B2	PAGE B1	PAGE B0	00H
B0H	R/W	P3	1	1	1	P34	P33	P32	P31	P30	FFH
B1H	R/W	TXT27	–	–	–	–	–	SCRB2	SCRB1	SCRB0	00H
B2H	R/W	TXT18	NOT3	NOT2	NOT1	NOT0	0	0	BS1	BS0	00H
B3H	R/W	TXT19	TEN	TC2	TC1	TC0	0	0	TS1	TS0	00H
B4H	R/W	TXT20	DRCS ENABLE	OSD PLANES	EXTENDED SPECIAL GRAPHICS	CHAR SELECT ENABLE	OSD LANG ENABLE	OSD LAN2	OSD LAN1	OSD LAN0	00H
B5H	R/W	TXT21	DISP LINES1	DISP LINES0	CHAR SIZE1	CHAR SIZE0	I <sup>2</sup> C PORT 1	CC ON	I <sup>2</sup> C PORT 0	CC/TXT	02H
B6H	R	TXT22	GPF7	GPF6	GPF5	GPF4	GPF3	GPF2	GPF1	GPFO	XXH

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ADD	R/W	NAME	7	6	5	4	3	2	1	0	RESET
B7H	R/W	CCLIN	0	0	0	CS4	CS3	CS2	CS1	CS0	15H
B8H	R/W	IP	0	PBUSY	PES2	PCC	PT1	PX1	PT0	PX0	00H
B9H	R/W	TXT17	0	FORCE ACQ1	FORCE ACQ0	FORCE DISP1	FORCE DISP0	SCREEN COL2	SCREEN COL1	SCREEN COL0	00H
BAH	R	WSS1	0	0	0	WSS<3:0> ERROR	WSS3	WSS2	WSS1	WSS0	00H
BBH	R	WSS2	0	0	0	WSS<7:4> ERROR	WSS7	WSS6	WSS5	WSS4	00H
BCH	R	WSS3	WSS<13:11> ERROR	WSS13	WSS12	WSS11	WSS<10:8> ERROR	WSS10	WSS9	WSS8	00H
BDH	R/W	GPR9	GPR97	GPR96	GPR95	GPR94	GPR93	GPR92	GPR91	GPR90	00H
BEH	R/W	P3CFGA	P3CFGA7	P3CFGA6	P3CFGA5	P3CFGA4	P3CFGA3	P3CFGA2	P3CFGA1	P3CFGA0	FFH
BFH	R/W	P3CFGB	P3CFGB7	P3CFGB6	P3CFGB5	P3CFGB4	P3CFGB3	P3CFGB2	P3CFGB1	P3CFGB0	00H
C0H	R/W	TXT0	X24 POSN	DISPLAY X24	AUTO FRAME	DISABLE HEADER ROLL	DISPLAY STATUS ROW ONLY	DISABLE FRAME	VPS ON	INV ON	00H
C1H	R/W	TXT1	EXT PKT OFF	8-BIT	ACQ OFF	X26 OFF	FULL FIELD	FIELD POLARITY	H POLARITY	V POLARITY	00H
C2H	R/W	TXT2	ACQ BANK	REQ3	REQ2	REQ1	REQ0	SC2	SC1	SC0	00H
C3H	W	TXT3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0	00H
C4H	R/W	TXT4	OSD BANK ENABLE	QUAD WIDTH ENABLE	EAST/WEST	DISABLE DOUBLE HEIGHT	B MESH ENABLE	C MESH ENABLE	TRANS ENABLE	SHADOW ENABLE	00H
C5H	R/W	TXT5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PICTURE ON OUT	PICTURE ON IN	03H
C6H	R/W	TXT6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PICTURE ON OUT	PICTURE ON IN	03H
C7H	R/W	TXT7	STATUS ROW TOP	CURSOR ON	REVEAL	BOTTOM/TOP	DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	00H
C8H	R/W	TXT8	(reserved) 0	FLICKER STOP ON	(reserved) 0	DISABLE SPANISH	PKT 26 RECEIVED	WSS RECEIVED	WSS ON	CVBS1/ CVBS0	00H
C9H	R/W	TXT9	CURSOR FREEZE	CLEAR MEMORY	A0	R4	R3	R2	R1	R0	00H
CAH	R/W	TXT10	0	0	C5	C4	C3	C2	C1	C0	00H
CBH	R/W	TXT11	D7	D6	D5	D4	D3	D2	D1	D0	00H

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ADD	R/W	NAME	7	6	5	4	3	2	1	0	RESET
CCH	R	TXT12	525/625 SYNC	SPANISH	ROM VER3	ROM VER2	ROM VER1	ROM VER0	1	VIDEO SIGNAL QUALITY	XXXX XX1X
CDH	R/W	TXT14	0	0	0	DISPLAY BANK	PAGE3	PAGE2	PAGE1	PAGE0	00H
CEH	R/W	TXT15	0	0	0	MICRO BANK	BLOCK3	BLOCK2	BLOCK1	BLOCK0	00H
CFH	R/W	CCBASE	CCBASE7	CCBASE6	CCBASE5	CCBASE4	CCBASE3	CCBASE2	CCBASE1	CCBASE0	20H
D0H	R/W	PSW	C	AC	F0	RS1	RS0	OV	–	P	00H
D1H	R/W	GPR10	GPR107	GPR106	GPR105	GPR104	GPR103	GPR102	GPR101	GPR100	00H
D2H	R/W	TDACL	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0	00H
D3H	R/W	TDACH	TPWE	1	TD13	TD12	TD11	TD10	TD9	TD8	40H
D4H	R/W	PWM7	PW7E	1	PW7V5	PW7V4	PW7V3	PW7V2	PW7V1	PW7V0	40H
D5H	R/W	PWM0	PW0E	1	PW0V5	PW0V4	PW0V3	PW0V2	PW0V1	PW0V0	40H
D6H	R/W	PWM1	PW1E	1	PW1V5	PW1V4	PW1V3	PW1V2	PW1V1	PW1V0	40H
D7H	R	CCDAT1	CCD17	CCD16	CCD15	CCD14	CCD13	CCD12	CCD11	CCD10	00H
D8H	R/W	S1CON	CR2	ENSI	STA	STO	SI	AA	CR1	CR0	00H
D9H	R	S1STA	STAT4	STAT3	STAT2	STAT1	STAT0	0	0	0	F8H
DAH	R/W	S1DAT	DAT7	DAT6	DAT5	DAT4	DAT3	DAT2	DAT1	DAT0	00H
DBH	R/W	S1ADR	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	GC	00H
DCH	R/W	PWM3	PW3E	1	PW3V5	PW3V4	PW3V3	PW3V2	PW3V1	PW3V0	40H
DDH	R/W	PWM4	PW4E	1	PW4V5	PW4V4	PW4V3	PW4V2	PW4V1	PW4V0	40H
DEH	R/W	PWM5	PW5E	1	PW5V5	PW5V4	PW5V3	PW5V2	PW5V1	PW5V0	40H
DFH	R/W	PWM6	PW6E	1	PW6V5	PW6V4	PW6V3	PW6V2	PW6V1	PW6V0	40H
E0H	R/W	ACC	ACC7	ACC6	ACC5	ACC4	ACC3	ACC2	ACC1	ACC0	00H
E1H	R/W	TXT29	TEN B	TS B1	TS B0	OSD PLANES B	OSD LANG ENABLE B	OSD LAN B2	OSD LAN B1	OSD LAN B0	00H
E2H	R/W	TXT30	TC B2	TC B1	TC B0	reserved	reserved	reserved	reserved	reserved	00H
E3H	R/W	GPR11	GPR117	GPR116	GPR115	GPR114	GPR113	GPR112	GPR111	GPR110	00H
E4H	R/W	PWM2	PW2E	1	PW2V5	PW2V4	PW2V3	PW2V2	PW2V1	PW2V0	40H
E5H	R/W	GPR12	GPR127	GPR126	GPR125	GPR124	GPR123	GPR122	GPR121	GPR120	00H
E6H	R/W	GPR13	GPR137	GPR136	GPR135	GPR134	GPR133	GPR132	GPR131	GPR130	00H
E7H	R	CCDAT2	CCD27	CCD26	CCD25	CCD24	CCD23	CCD22	CCD21	CCD20	00H



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ADD	R/W	NAME	7	6	5	4	3	2	1	0	RESET
E8H	R/W	SAD	VHI	CH1	CH0	ST	SAD7	SAD6	SAD5	SAD4	00H
E9H	R/W	GPR14	GPR147	GPR146	GPR145	GPR144	GPR143	GPR142	GPR141	GPR140	00H
EAH	R/W	GPR15	GPR157	GPR156	GPR155	GPR154	GPR153	GPR152	GPR151	GPR150	00H
EBH	R/W	GPR16	GPR167	GPR166	GPR165	GPR164	GPR163	GPR162	GPR161	GPR160	00H
ECH	R/W	GPR17	GPR177	GPR176	GPR175	GPR174	GPR173	GPR172	GPR171	GPR170	00H
EDH	R/W	GPR18	GPR187	GPR186	GPR185	GPR184	GPR183	GPR182	GPR181	GPR180	00H
EEH	R/W	TXT35	PKT1-247	PKT1-246	PKT1-245	PKT1-244	PKT1-243	PKT1-242	PKT1-241	PKT1-240	00H
EFH	R/W	TXT36	–	–	–	–	–	–	PKT1-249	PKT1-248	00H
F0H	R/W	B	B7	B6	B5	B4	B3	B2	B1	B0	00H
F1H	R/W	T2CON	TF2	EXF2	RCLK0	TCLK0	EXEN2	TR2	C/T2	CP/RL2	00H
F2H	R/W	T2MOD	–	–	–	–	–	T2RD	T2OE	DCEN	00H
F3H	R/W	RCAP2L	RCAP2L7	RCAP2L6	RCAP2L5	RCAP2L4	RCAP2L3	RCAP2L2	RCAP2L1	RCAP2L0	00H
F4H	R/W	RCAP2H	RCAP2H7	RCAP2H6	RCAP2H5	RCAP2H4	RCAP2H3	RCAP2H2	RCAP2H1	RCAP2H0	00H
F5H	R/W	TL2	TL27	TL26	TL25	TL24	TL23	TL22	TL21	TL20	00H
F6H	R/W	TH2	TH27	TH26	TH25	TH24	TH23	TH22	TH1	TH20	00H
F8H	R/W	TXT13	VPS RECEIVED	PAGE CLEARING	525 DISPLAY	525 TEXT	625 TEXT	PKT 8/30	FASTEXT	0	XXXX XXX0
F9H	R/W	GPR19	GPR197	GPR196	GPR195	GPR194	GPR193	GPR192	GPR191	GPR190	00H
FAH	R/W	XRAMP	XRAMP7	XRAMP6	XRAMP5	XRAMP4	XRAMP3	XRAMP2	XRAMP1	XRAMP0	00H
FBH	R/W	ROMBK	STANDBY	IIC_LUT1	IIC_LUT0	RAMBK1	RAMBK0	ROMBK2	ROMBK1	ROMBK0	00H
FCH	R/W	GPR20	GPR207	GPR206	GPR205	GPR204	GPR203	GPR202	GPR201	GPR200	00H
FDH	R	TEST	TEST7	TEST6	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0	00H
FEH	W	WDTKEY	WKEY7	WKEY6	WKEY5	WKEY4	WKEY3	WKEY2	WKEY1	WKEY0	00H
FFH	R/W	WDT	WDV7	WDV6	WDV5	WDV4	WDV3	WDV2	WDV1	WDV0	00H

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**Table 5** SFR bit description

<b>BITS</b>	<b>FUNCTION</b>
<b>Accumulator (ACC)</b>	
ACC7 to ACC0	accumulator value
<b>B Register (B)</b>	
B7 to B0	B register value
<b>CC Base Pointer (CCBASE)</b>	
CCBASE7 to CCBASE0	Closed Caption display base pointer
<b>CC data byte 1 (CCDAT1)</b>	
CCD17 to CCD10	Closed Caption first data byte
<b>CC data byte 2 (CCDAT2)</b>	
CCD26 to CCD20	Closed Caption second data byte
<b>CC line (CCLIN)</b>	
CS4 to CS0	Closed Caption slice line using 525-line number
<b>Data Pointer High byte (DPH)</b>	
DPH7 to DPH0	data pointer high byte, used with DPL to address auxiliary memory
<b>Data Pointer Low byte (DPL)</b>	
DPL7 to DPL0	data pointer low byte, used with DPH to address auxiliary memory
<b>External Interrupt (EXTINT) (n = 2 to 5)</b>	
EXnCFG<1:0> = 00	active LOW interrupt
EXnCFG<1:0> = 01	rising edge interrupt
EXnCFG<1:0> = 10	falling edge interrupt
EXnCFG<1:0> = 11	both rising and falling edge interrupt
<b>General Purpose Registers (GPR1 to GPR20) (n = 1 to 21)</b>	
GPRn<7:0>	general purpose read/write registers available for use by the embedded software
<b>Interrupt Enable Register 0 (IEN0)</b>	
EA	disable all interrupts (logic 0), or use individual interrupt enable bits (logic 1)
EBUSY	enable BUSY interrupt
ES2	enable I <sup>2</sup> C-bus interrupt
ECC	enable Closed Caption interrupt
ET1	enable Timer 1 interrupt
EX1	enable external interrupt 1
ET0	enable Timer 0 interrupt
EX0	enable external interrupt 0

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BITS	FUNCTION
<b>Interrupt Enable Register 1 (IEN1)</b>	
EX5	enable external interrupt 5
EX4	enable external interrupt 4
EX3	enable external interrupt 3
EX2	enable external interrupt 2
EUTX	enable UART transmitter interrupt
EURX	enable UART receiver interrupt
EUART	enable UART transmitter/receiver interrupt
ET2	enable Timer 2 interrupt
<b>Interrupt Priority Register 0 (IP)</b>	
PBUSY	priority EBUSY interrupt
PES2	priority ES2 interrupt
PCC	priority ECC interrupt
PT1	priority Timer 1 interrupt
PX1	priority external interrupt 1
PT0	priority Timer 0 interrupt
PX0	priority external interrupt 0
<b>Interrupt Priority Register 1 (IP1)</b>	
PX5	priority external interrupt 5
PX4	priority external interrupt 4
PX3	priority external interrupt 3
PX2	priority external interrupt 2
PUTX	priority UART transmitter interrupt
PURX	priority UART receiver interrupt
PUART	priority UART transmitter/receiver interrupt
PT2	priority Timer 2 interrupt
<b>Port 0 (P0)</b>	
P07 to P00	Port 0 I/O register connected to external pins
<b>Port 1 (P1)</b>	
P17 to P10	Port 1 I/O register connected to external pins
<b>Port 2 (P2)</b>	
P27 to P20	Port 2 I/O register connected to external pins
<b>Port 3 (P3)</b>	
P34 to P30	Port 3 I/O register connected to external pins

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BITS	FUNCTION
<b>Port 0 Configuration A (P0CFGA) and Port 0 Configuration B (P0CFGB)</b>	
P0CFGA<7:0> and P0CFGB<7:0>	<p>These two registers are used to configure Port 0 lines. For example, the configuration of Port 0 pin 3 is controlled by setting bit 3 in both P0CFGA and P0CFGB. P0CFGB&lt;x&gt;/P0CFGA&lt;x&gt;:</p> <ul style="list-style-type: none"> <li>00 = P0.x in Mode 0 (open-drain)</li> <li>01 = P0.x in Mode 1 (quasi-bidirectional)</li> <li>10 = P0.x in Mode 2 (high-impedance)</li> <li>11 = P0.x in Mode 3 (push-pull)</li> </ul>
<b>Port 1 Configuration A (P1CFGA) and Port 1 Configuration B (P1CFGB)</b>	
P1CFGA<7:0> and P1CFGB<7:0>	<p>These two registers are used to configure Port 1 lines. For example, the configuration of Port 1 pin 3 is controlled by setting bit 3 in both P1CFGA and P1CFGB. P1CFGB&lt;x&gt;/P1CFGA&lt;x&gt;:</p> <ul style="list-style-type: none"> <li>00 = P1.x in Mode 0 (open-drain)</li> <li>01 = P1.x in Mode 1 (quasi-bidirectional)</li> <li>10 = P1.x in Mode 2 (high-impedance)</li> <li>11 = P1.x in Mode 3 (push-pull)</li> </ul>
<b>Port 2 Configuration A (P2CFGA) and Port 2 Configuration B (P2CFGB)</b>	
P2CFGA<7:0> and P2CFGB<7:0>	<p>These two registers are used to configure Port 2 lines. For example, the configuration of Port 2 pin 3 is controlled by setting bit 3 in both P2CFGA and P2CFGB. P2CFGB&lt;x&gt;/P2CFGA&lt;x&gt;:</p> <ul style="list-style-type: none"> <li>00 = P2.x in Mode 0 (open-drain)</li> <li>01 = P2.x in Mode 1 (quasi-bidirectional)</li> <li>10 = P2.x in Mode 2 (high-impedance)</li> <li>11 = P2.x in Mode 3 (push-pull)</li> </ul>
<b>Port 3 Configuration A (P3CFGA) and Port 3 Configuration B (P3CFGB)</b>	
P3CFGA<7:0> and P3CFGB<7:0>	<p>These two registers are used to configure Port 3 lines. For example, the configuration of Port 3 pin 3 is controlled by setting bit 3 in both P3CFGA and P3CFGB. P3CFGB&lt;x&gt;/P3CFGA&lt;x&gt;:</p> <ul style="list-style-type: none"> <li>00 = P3.x in Mode 0 (open-drain)</li> <li>01 = P3.x in Mode 1 (quasi-bidirectional)</li> <li>10 = P3.x in Mode 2 (high-impedance)</li> <li>11 = P3.x in Mode 3 (push-pull)</li> </ul>
<b>Power Control Register (PCON)</b>	
SMOD	UART baud rate double control
ARD	auxiliary RAM disable, all MOVX instructions access the external data memory
RFI	disable ALE during internal access to reduce radio frequency Interference
WLE	Watchdog Timer enable
GF1	general purpose flag
GF0	general purpose flag
PD	Power-down activation bit
IDL	Idle mode activation bit

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BITS	FUNCTION
<b>Program Status Word (PSW)</b>	
C	carry bit
AC	auxiliary carry bit
F0	flag 0
RS1 to RS0	register bank selector bits RS<1:0>: 00 = Bank 0 (00H to 07H) 01 = Bank 1 (08H to 0FH) 10 = Bank 2 (10H to 17H) 11 = Bank 3 (18H to 1FH)
OV	overflow flag
P	parity bit
<b>Pulse Width Modulator 0 Control Register (PWM0)</b>	
PW0E	activate this PWM and take control of respective port pin (logic 1)
PW0V5 to PW0V0	pulse width modulator high time
<b>Pulse Width Modulator 1 Control Register (PWM1)</b>	
PW1E	activate this PWM (logic 1)
PW1V5 to PW1V0	pulse width modulator high time
<b>Pulse Width Modulator 2 Control Register (PWM2)</b>	
PW2E	activate this PWM (logic 1)
PW2V5 to PW2V0	pulse width modulator high time
<b>Pulse Width Modulator 3 Control Register (PWM3)</b>	
PW3E	activate this PWM (logic 1)
PW3V5 to PW3V0	pulse width modulator high time
<b>Pulse Width Modulator 4 Control Register (PWM4)</b>	
PW4E	activate this PWM (logic 1)
PW4V5 to PW4V0	pulse width modulator high time
<b>Pulse Width Modulator 5 Control Register (PWM5)</b>	
PW5E	activate this PWM (logic 1)
PW5V5 to PW5V0	pulse width modulator high time
<b>Pulse Width Modulator 6 Control Register (PWM6)</b>	
PW6E	activate this PWM (logic 1)
PW6V5 to PW6V0	pulse width modulator high time
<b>Pulse Width Modulator 7 Control Register (PWM7)</b>	
PW7E	activate this PWM (logic 1)
PW7V5 to PW7V0	pulse width modulator high time
<b>Timer 2 Reload Capture High Byte (RCAP2H)</b>	
RCAP2H7 to RCAP2H0	Timer 2 capture/reload high byte

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BITS	FUNCTION
<b>Timer 2 Reload Capture Low Byte (RCAP2L)</b>	
RCAP2L7 to RCAP2L0	Timer 2 capture/reload low byte
<b>ROM Bank (ROMBK)</b>	
STANDBY	standby activation bit
IIC_LUT1 to IIC_LUT0	I <sup>2</sup> C-bus lookup table selection; IIC_LUT<1:0>: 00 = P8xC558 normal mode 01 = P8xC558 fast mode 10 = P8xC558 slow mode 11 = reserved
RAMBK1 to RAMBK0	RAM Bank selection bits RAMBK<1:0>: 00 = Bank 0 (0 to 64 kbytes) 01 = Bank 1 (64 to 128 kbytes) 10 = Bank 2 (128 to 192 kbytes) 11 = Bank 3 (192 to 256 kbytes)
ROMBK2 to ROMBK0	ROM Bank selection bits ROMBK<2:0>: 000 = Bank 0 (32 to 64 kbytes) 001 = Bank 1 (64 to 96 kbytes) 010 = Bank 2 (96 to 128 kbytes) 011 = Bank 3 (128 to 160 kbytes) 100 = Bank 4 (160 to 192 kbytes) 101 to 111 = reserved
<b>UART Buffer (S0BUF)</b>	
S0BUF7 to S0BUF0	UART data buffer
<b>UART Control Register (S0CON)</b>	
SM0 to SM1	UART mode selection bits SM<0:1>: 00, Mode 0, Shift Register 01, Mode 2, 9-bit UART 10, Mode 1, 8-bit UART (variable baud rate) 11, Mode 3, 9-bit UART (variable baud rate)
SM2	Enables the multiprocessor communication feature in Modes 2 and 3. In Mode 2 or 3, if SM2 is set, then RI will not be activated, RB8 and S0BUF will not be loaded if the received 9 <sup>th</sup> data bit is logic 0. In Mode 1, if SM2 is set, then RI will not be activated, RB8 and S0BUF will not be loaded if no valid stop bit was received. In Mode 0, SM2 has no influence.
REN	Enables serial reception. Set by software to enable reception. Cleared by software to disable reception.
TB8	Is the 9 <sup>th</sup> data bit that will be transmitted in Modes 2 and 3. Set or cleared by software as desired.
RB8	In Modes 2 and 3, RB8 is the 9 <sup>th</sup> data bit that was received. In Mode 1, if SM2 is logic 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used. Loading of RB8 in Modes 1, 2 and 3 depends on SM2.

## Enhanced TV microcontrollers with On-Screen Display (OSD)

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BITS	FUNCTION
TI	Is the transmit interrupt flag. Set by hardware at the end of the 8 <sup>th</sup> bit time in Mode 0, or at the beginning of the stop bit in the other modes. Must be cleared by software.
RI	Is the receive interrupt flag. Set by hardware at the end of the 8 <sup>th</sup> bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.
<b>I<sup>2</sup>C-bus Slave Address Register (S1ADR)</b>	
ADR6 to ADR0	I <sup>2</sup> C-bus slave address to which the device will respond
GC	enable I <sup>2</sup> C-bus general call address (logic 1)
<b>I<sup>2</sup>C-bus Control Register (S1CON)</b>	
CR2 to CR0	clock rate bits; CR<2:0>: (for nominal mode) 000 = 200 kHz bit rate 001 = 7.5 kHz bit rate 010 = 300 kHz bit rate 011 = 400 kHz bit rate 100 = 50 kHz bit rate 101 = 3.75 kHz bit rate 110 = 75 kHz bit rate 111 = 100 kHz bit rate
ENSI	enable I <sup>2</sup> C-bus interface (logic 1)
STA	<b>START flag.</b> When this bit is set in slave mode, the hardware checks the I <sup>2</sup> C-bus and generates a START condition if the bus is free or after the bus becomes free. If the device operates in master mode, it will generate a repeated START condition.
STO	<b>STOP flag.</b> If this bit is set in a master mode, a STOP condition is generated. A STOP condition detected on the I <sup>2</sup> C-bus clears this bit. This bit may also be set in slave mode, to recover from an error condition. In this case, no STOP condition is generated to the I <sup>2</sup> C-bus, but the hardware releases the SDA and SCL lines and switches to the not selected receiver mode. The STOP flag is cleared by the hardware.
SI	<b>Serial Interrupt flag.</b> This flag is set and an interrupt request is generated, after any of the following events occur: <ul style="list-style-type: none"> <li>• A START condition is generated in master mode</li> <li>• The own slave address has been received during AA = 1</li> <li>• The general call address has been received while S1ADR.GC and AA = 1</li> <li>• A data byte has been received or transmitted in master mode (even if arbitration is lost)</li> <li>• A data byte has been received or transmitted as selected slave</li> <li>• A STOP or START condition is received as selected slave receiver or transmitter. While the SI flag is set, SCL remains LOW and the serial transfer is suspended. SI must be reset by software.</li> </ul>

## Enhanced TV microcontrollers with On-Screen Display (OSD)

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BITS	FUNCTION
AA	<p><b>Assert Acknowledge flag.</b> When this bit is set, an acknowledge is returned after any one of the following conditions:</p> <ul style="list-style-type: none"> <li>• Own slave address is received</li> <li>• General call address is received (S1ADR.GC = 1)</li> <li>• A data byte is received, while the device is programmed to be a master receiver</li> <li>• A data byte is received, while the device is selected slave receiver.</li> </ul> <p>When the bit is reset, no acknowledge is returned. Consequently, no interrupt is requested when the own address or general call address is received.</p>
<b>I<sup>2</sup>C-bus Data Register (S1DAT)</b>	
DAT7 to DAT0	I <sup>2</sup> C-bus data
<b>I<sup>2</sup>C-bus Status Register (S1STA)</b>	
STAT4 to STAT0	I <sup>2</sup> C-bus interface status
<b>Software ADC Register (SAD)</b>	
VHI	analog input voltage greater than DAC voltage (logic 1)
CH1 to CH0	ADC input channel select bits; CH<1:0>: 00 = ADC3 01 = ADC0 10 = ADC1 11 = ADC2
ST <sup>(1)</sup>	initiate voltage comparison between ADC input channel and SAD value
SAD7 to SAD4	4 MSBs of DAC input word
<b>Software ADC Control Register (SADB)</b>	
DC_COMP	enable DC comparator mode (logic 1)
SAD3 to SAD0	4 LSBs of SAD value
<b>Stack Pointer (SP)</b>	
SP7 to SP0	stack pointer value
<b>Timer/counter Control Register (TCON)</b>	
TF1	<b>Timer 1 overflow flag.</b> Set by hardware on Timer/counter overflow. Cleared by hardware when processor vectors to interrupt routine.
TR1	<b>Timer 1 run control bit.</b> Set/cleared by software to turn Timer/counter on/off.
TF0	<b>Timer 0 overflow flag.</b> Set by hardware on Timer/counter overflow. Cleared by hardware when processor vectors to interrupt routine.
TR0	<b>Timer 0 run control bit.</b> Set/cleared by software to turn Timer/counter on/off.
IE1	<b>Interrupt 1 edge flag.</b> Both edges generate flag. Set by hardware when external interrupt edge detected. Cleared by hardware when interrupt processed.
IT1	<b>Interrupt 1 type control bit.</b> Set/cleared by software to specify edge/low level triggered external interrupts.
IE0	<b>Interrupt 0 Edge I flag.</b> Set by hardware when external interrupt edge detected. Cleared by hardware when interrupt processed.
IT0	<b>Interrupt 0 type flag.</b> Set/cleared by software to specify falling edge/low level triggered external interrupts.



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BITS	FUNCTION
<b>Timer/counter2 Control Register (T2CON)</b>	
TF2	<b>Timer 2 overflow flag.</b> Cleared by software. TF2 will not be set when either baud rate generation mode or clock out mode.
EXF2	<b>Timer 2 External Flag.</b> Set on a negative transition on T2EX and EXEN2 = 1. In Auto-reload mode it is toggled on an under or overflow. Cleared by software.
RCLK0	<b>Receive clock 0 flag.</b> When set, causes the UART to use Timer 2 overflow pulses. RCLK0 = 0 causes Timer 1 overflow pulses to be used.
TCLK0	<b>Transmit clock 0 flag.</b> When set, causes the UART to use Timer 2 overflow pulses. TCLK0 = 0 causes Timer 1 overflow pulses to be used.
EXEN2	<b>Timer 2 external enable flag.</b> When set, allows a capture or reload to occur, together with an interrupt, as a result of a negative transition on input T2EX if in capture mode or Auto-reload mode with DCEN reset. If in Auto-reload mode and DCEN is set, this bit has no influence. In the other modes, EXF2 is set and an interrupt is generated on a HIGH-to-LOW transition on T2EX pin. In all modes, EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	<b>START/STOP control bit.</b> A logic 1 starts Timer 2.
$C/\overline{T2}$	<b>Counter Timer selection bit.</b> A logic 1 selects the counter for Timer 2.
$CP/\overline{RL2}$	<b>Capture/Reload flag.</b> Selection of mode capture or reload.
<b>14-bit PWM MSB Register (TDACH)</b>	
TPWE	activate this 14-bit PWM (logic 1)
TD13 to TD8	6 MSBs of 14-bit number to be output by the 14-bit PWM
<b>14-bit PWM LSB Register (TDACL)</b>	
TD7 to TD0	8 LSBs of 14-bit number to be output by the 14-bit PWM
<b>Timer 0 High byte (TH0)</b>	
TH07 to TH00	8 MSBs of Timer 0 16-bit counter
<b>Timer 1 High byte (TH1)</b>	
TH17 to TH10	8 MSBs of Timer 1 16-bit counter
<b>Timer 2 High byte (TH2)</b>	
TH27 to TH20	8 MSBs of Timer 2 16-bit counter
<b>Timer 0 Low byte (TL0)</b>	
TL07 to TL00	8 LSBs of Timer 0 16-bit counter
<b>Timer 1 Low byte (TL1)</b>	
TL17 to TL10	8 LSBs of Timer 1 16-bit counter
<b>Timer 2 Low byte (TL2)</b>	
TL27 to TL20	8 LSBs of Timer 2 16-bit counter

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BITS	FUNCTION
<b>Timer/counter Mode Control (TMOD)</b>	
GATE	gating control Timer/counter 1
C/T	Counter/Timer 1 selector
M1 to M0	mode control bits Timer/counter 1; M<1:0>: 00 = 8-bit Timer or 8-bit Counter with divide-by-32 prescaler 01 = 16-bit time interval or event Counter 10 = 8-bit time interval or event Counter with automatic reload upon overflow; reload value stored in TH1 11 = stopped
GATE	gating control Timer/counter 0
C/T	Counter/Timer 0 selector
M1 to M0	mode control bits Timer/counter 0; M<1:0>: 00 = 8-bit timer or 8-bit counter with divide-by-32 prescaler 01 = 16-bit time interval or event Counter 10 = 8-bit time interval or event Counter with automatic reload upon overflow; reload value stored in TH0 11 = one 8-bit time interval or event Counter and one 8-bit time interval Counter
<b>Timer 2 Mode Control (T2MOD)</b>	
T2RD	<b>Timer 2 Read flag.</b> This bit is set by hardware if following TL2 read and before TH2 read, TH2 is incremented. It is reset on the trailing edge of next TL2 read.
T2OE	<b>Timer 2 output enable bit.</b> When set, pin T2 is configured as a clock output.
DCEN	<b>Down count enable flag.</b> When set, this allows Timer 2 to be configured as an up/down Counter.
<b>Text Register 0 (TXT0)</b>	
X24 POSN	store packet 24 in extension packet memory (logic 0) or page memory (logic 1)
DISPLAY X24	display X24 from page memory (logic 0) or extension packet memory (logic 1)
AUTO FRAME	FRAME output switched off automatically if any video displayed (logic 1)
DISABLE HEADER ROLL	disable writing of rolling headers and time into memory (logic 1)
DISPLAY STATUS ROW ONLY	display row 24 only (logic 1)
DISABLE FRAME	FRAME output always LOW (logic 1)
VPS ON	enable capture of VPS data (logic 1)
INV ON	enable capture of inventory page in block 8 (logic 1)
<b>Text Register 1 (TXT1)</b>	
EXT PKT OFF	disable acquisition of extension packets (logic 1)
8-BIT	disable checking of packets 0 to 24 written into memory (logic 1)
ACQ OFF	disable writing of data into Display memory (logic 1)
X26 OFF	disable automatic processing of X/26 data (logic 1)
FULL FIELD	acquire data on any TV line (logic 1)
FIELD POLARITY	VSYNC pulse in second half of line during even field (logic 1)
H POLARITY	HSYNC reference edge is negative going (logic 1)

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<b>BITS</b>	<b>FUNCTION</b>
V POLARITY	VSYNC reference edge is negative going (logic 1)
<b>Text Register 2 (TXT2)</b>	
ACQ BANK	select acquisition Bank 1 (logic 1)
REQ3 to REQ0	page request
SC2 to SC0	start column of page request
<b>Text Register 3 (TXT3)</b>	
PRD4 to PRD0	page request data
<b>Text Register 4 (TXT4)</b>	
OSD BANK ENABLE	alternate OSD location available via graphic attribute, additional 32 locations (logic 1)
QUAD WIDTH ENABLE	enable display of quadruple width characters (logic 1)
EAST/WEST $\bar{}$	eastern language selection of character codes A0H to FFH (logic 1)
DISABLE DOUBLE HEIGHT	disable normal decoding of double height characters (logic 1)
B MESH ENABLE	enable meshing of black background (logic 1)
C MESH ENABLE	enable meshing of coloured background (logic 1)
TRANS ENABLE	display black background as video (logic 1)
SHADOW ENABLE	display shadow/fringe (default SE black) (logic 1)
<b>Text Register 5 (TXT5)</b>	
BKGND OUT	background colour displayed outside Teletext boxes (logic 1)
BKGND IN	background colour displayed inside Teletext boxes (logic 1)
COR OUT	COR active outside Teletext and OSD boxes (logic 1)
COR IN	COR active inside Teletext and OSD boxes (logic 1)
TEXT OUT	TEXT displayed outside Teletext boxes (logic 1)
TEXT IN	TEXT displayed inside Teletext boxes (logic 1)
PICTURE ON OUT	VIDEO displayed outside Teletext boxes (logic 1)
PICTURE ON IN	VIDEO displayed inside Teletext boxes (logic 1)
<b>Text Register 6 (TXT6)</b>	
BKGND OUT	background colour displayed outside Teletext boxes (logic 1)
BKGND IN	background colour displayed inside Teletext boxes (logic 1)
COR OUT	COR active outside Teletext and OSD boxes (logic 1)
COR IN	COR active inside Teletext and OSD boxes (logic 1)
TEXT OUT	TEXT displayed outside Teletext boxes (logic 1)
TEXT IN	TEXT displayed inside Teletext boxes (logic 1)
PICTURE ON OUT	VIDEO displayed outside Teletext boxes (logic 1)
PICTURE ON IN	VIDEO displayed inside Teletext boxes (logic 1)

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BITS	FUNCTION
<b>Text Register 7 (TXT7)</b>	
STATUS ROW TOP	Display memory row 24 information above Teletext page (on display row 0) (logic 1)
CURSOR ON	display cursor at position given by TXT9 and TXT10 (logic 1)
REVEAL	display characters in area with conceal attribute set (logic 1)
BOTTOM/ $\overline{\text{TOP}}$	Display memory rows 12 to 23 when DOUBLE HEIGHT height bit is set (logic 1)
DOUBLE HEIGHT	display each character as twice normal height (logic 1)
BOX ON 24	enable display of Teletext boxes in memory row 24 (logic 1)
BOX ON 1 to 23	enable display of Teletext boxes in memory row 1 to 23 (logic 1)
BOX ON 0	enable display of Teletext boxes in memory row 0 (logic 1)
<b>Text Register 8 (TXT8)</b>	
$\overline{\text{FLICKER STOP ON}}$	disable 'Flicker Stopper' circuit (logic 1)
DISABLE SPANISH	disable special treatment of Spanish packet 26 characters (logic 1)
PKT 26 RECEIVED <sup>(2)</sup>	packet 26 data has been processed (logic 1)
WSS RECEIVED <sup>(2)</sup>	WSS data has been processed (logic 1)
WSS ON	enable acquisition of WSS data (logic 1)
CVBS1/ $\overline{\text{CVBS0}}$	select CVBS1 as source for device (logic 1)
<b>Text Register 9 (TXT9)</b>	
CURSOR FREEZE	lock cursor at current position (logic 1)
CLEAR MEMORY <sup>(1)</sup>	clear memory block pointed to by TXT15 (logic 1)
A0	access extension packet memory (logic 1)
R4 to R0 <sup>(3)</sup>	current memory ROW value
<b>Text Register 10 (TXT10)</b>	
C5 to C0 <sup>(4)</sup>	current memory COLUMN value
<b>Text Register 11 (TXT11)</b>	
D7 to D0	data value written or read from memory location defined by TXT9, TXT10 and TXT15
<b>Text Register 12 (TXT12)</b>	
525/ $\overline{625}$ SYNC	525-line CVBS signal is being received (logic 1)
SPANISH	Spanish character set present (logic 1)
ROM VER3 to ROM VER0	mask programmable identification for character set
VIDEO SIGNAL QUALITY	acquisition can be synchronized to CVBS (logic 1)
<b>Text Register 13 (TXT13)</b>	
VPS RECEIVED	VPS data (logic 1)
PAGE CLEARING	software or power-on page clear in progress (logic 1)
525 DISPLAY	525-line synchronisation for display (logic 1)
525 TEXT	525-line WST being received (logic 1)
625 TEXT	625-line WST being received (logic 1)
PKT 8/30	packet 8/30/x(625) or packet 4/30/x(525) data detected (logic 1)

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BITS	FUNCTION
FASTEXT	packet x/27 data detected (logic 1)
<b>Text Register 14 (TXT14)</b>	
DISPLAY BANK	upper bank for display selected (logic 1)
PAGE3 to PAGE0	current display page
<b>Text Register 15 (TXT15)</b>	
MICRO BANK	upper bank for micro selected (logic 1)
BLOCK3 to BLOCK0	current micro block to be accessed by TXT9, TXT10 and TXT11
<b>Text Register 17 (TXT17)</b>	
FORCE ACQ1 to FORCE ACQ0	FORCE ACQ<1:0>: 00 = automatic selection 01 = force 525 timing, force 525 Teletext standard 10 = force 625 timing, force 625 Teletext standard 11 = force 625 timing, force 525 Teletext standard
FORCE DISP1 to FORCE DISP0	FORCE DISP<1:0>: 00 = automatic selection 01 = force display to 525 mode (9 lines per row) 10 = force display to 625 mode (10 lines per row) 11 = not valid (default to 625)
SCREEN COL2 to SCREEN COLO	Defines colour to be displayed instead of TV picture and black background; these bits <2:0> are equivalent to the RGB components. SCREEN COL<2:0>: 000 = transparent 001 = CLUT entry 9 010 = CLUT entry 10 011 = CLUT entry 11 100 = CLUT entry 12 101 = CLUT entry 13 110 = CLUT entry 14 111 = CLUT entry 15
<b>Text Register 18 (TXT18)</b>	
NOT3 to NOT0	National Option Table selection, maximum of 31 when used with EAST/WEST bit
BS1 to BS0	basic character set selection
<b>Text Register 19 (TXT19)</b>	
TEN	enable twist character set (logic 1)
TC2 to TC0	language control bits (C12/C13/C14) that has twisted character set
TS1 to TS0	twist character set selection

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BITS	FUNCTION
<b>Text Register 20 (TXT20)</b>	
DRCS ENABLE	re-map column 8/9 to DRCS (or column 8/9/A/C if extended DRCS is enabled) TXT and CC modes (logic 1)
OSD PLANES	character code columns 8/9 (or column 8/9/A/C if extended DRCS is enabled) defined as double plane characters (special graphics characters) (logic 1)
EXTENDED SPECIAL GRAPHICS	extended Special Graphics enabled, user definable range for special graphics characters, in CC mode only (logic 1)
CHAR SELECT ENABLE	enables character set selection in CC display mode (logic 1)
OSD LANG ENABLE	enable use of OSD LAN<2:0> to define language option for display, instead of C12/C13/C14
OSD LAN2 to OSD LAN0	alternative C12/C13/C14 bits for use with OSD menus
<b>Text Register 21 (TXT21)</b>	
DISP LINES1 to DISP LINES0	the number of display lines per character row; DISP LINES<1:0>: 00 = 10 lines per character (defaults to 9 lines in 525 mode) 01 = 13 lines per character 10 = 16 lines per character 11 = reserved
CHAR SIZE1 to CHAR SIZE0	character matrix size bits; CHAR SIZE<1:0>: 00 = 10 lines per character (matrix 12 × 10) 01 = 13 lines per character (matrix 12 × 13) 10 = 16 lines per character (matrix 12 × 16) 11 = reserved
I <sup>2</sup> C Port 1	enable I <sup>2</sup> C-bus Port 1 selection (P1.5/SDA1 and P1.4/SCL1) (logic 1)
CCON	Closed Caption acquisition on (logic 1)
I <sup>2</sup> C Port 0	enable I <sup>2</sup> C-bus Port 0 selection (P1.7/SDA0 and P1.6/SCL0) (logic 1)
CC/TXT	display configured for CC mode (logic 1)
<b>Text Register 22 (TXT22)</b>	
GPF7 to GPF6	reserved
GPF5 to GPF4 and GPF2 to GPF0	general purpose register, bits defined by mask programmable bits (Character ROM address 09FEH)
GPF3	PWM0, PWM1, PWM2 and PWM3 output on Port 3.0 to Port 3.3 respectively (logic 0) PWM0, PWM1, PWM2 and PWM3 output on Port 2.1 to Port 2.4 respectively (logic 1)
<b>Text Register 23 (TXT23)</b>	
NOT B3 to NOT B0	National Option Table selection for Page B, maximum of 32 when used with EAST/WEST B bit
EAST/WEST B	eastern language selection of character codes A0H to FFH for Page B (logic 1)
DRCS B ENABLE	normal OSD characters used on Page B (logic 0) re-map column 8/9 to DRCS (TXT and CC modes) on Page B (logic 1)
BS B1 to BS B0	basic character set selection for Page B

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BITS	FUNCTION
<b>Text Register 24 (TXT24)</b>	
BKGND OUT B	background colour displayed outside Teletext boxes (Teletext page) (logic 1)
BKGND IN B	background colour displayed inside Teletext boxes (Teletext page) (logic 1)
COR OUT B	COR active outside Teletext and OSD boxes (Teletext page) (logic 1)
COR IN B	COR active inside Teletext and OSD boxes (Teletext page) (logic 1)
TEXT OUT B	TEXT displayed outside Teletext boxes (Teletext page) (logic 1)
TEXT IN B	TEXT displayed inside Teletext boxes (Teletext page) (logic 1)
PICTURE ON OUT B	VIDEO displayed outside Teletext boxes (Teletext page) (logic 1)
PICTURE ON IN B	VIDEO displayed inside Teletext boxes (Teletext page) (logic 1)
<b>Text Register 25 (TXT25)</b>	
BKGND OUT B	background colour displayed outside Teletext boxes (Sub-Title/Newsflash page) (logic 1)
BKGND IN B	background colour displayed inside Teletext boxes (Sub-Title/Newsflash page) (logic 1)
COR OUT B	COR active outside Teletext and OSD boxes (Sub-Title/Newsflash page) (logic 1)
COR IN B	COR active inside Teletext and OSD boxes (Sub-Title/Newsflash page) (logic 1)
TEXT OUT B	TEXT displayed outside Teletext boxes (Sub-Title/Newsflash page) (logic 1)
TEXT IN B	TEXT displayed inside Teletext boxes (Sub-Title/Newsflash page) (logic 1)
PICTURE ON OUT B	VIDEO displayed outside Teletext boxes (Sub-Title/Newsflash page) (logic 1)
PICTURE ON IN B	VIDEO displayed inside Teletext boxes (Sub-Title/Newsflash page) (logic 1)
<b>Text Register 26 (TXT26)</b>	
EXTENDED DRCS	columns 8/9/A/C mapped to DRCS when DRCS characters enabled (allowing 64 DRCS characters) (logic 1); default (logic 0) only columns 8/9 mapped to DRCS when DRCS characters enabled (allowing 32 DRCS characters)
TRANS ENABLE B	display black background as video on Page B (logic 1)
C MESH ENABLE B	enable meshing of coloured background on Page B (logic 1)
B MESH ENABLE B	enable meshing of black background on Page B (logic 1)
SHADOW ENABLE B	disable display of shadow/fringing on Page B (logic 0) display shadow/ fringe (default SE black) on Page B (logic 1)
BOX ON 24 B	enable display of Teletext boxes in memory row 24 of Page B (logic 1)
BOX ON 1 B to 23 B	enable display of Teletext boxes in memory row 1 to 23 of Page B (logic 1)
BOX ON 0 B	enable display of Teletext boxes in memory row 0 of Page B (logic 1)

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BITS	FUNCTION
<b>Text Register 27 (TXT27)</b>	
SCRB2 to SCRB0	Defines colour to be displayed instead of TV picture and black background for Page B; these bits are equivalent to the RGB components. SCRB<2:0>: 000 = transparent 001 = CLUT entry 9 010 = CLUT entry 10 011 = CLUT entry 11 100 = CLUT entry 12 101 = CLUT entry 13 110 = CLUT entry 14 111 = CLUT entry 15
<b>Text Register 28 (TXT28)</b>	
MULTI-PAGE	conventional internal memory storage of acquisition data (logic 0) enables multi-page acquisition operation for software controlled storage of acquired data in external SRAM (logic 1)
CC/TXT B	display Page B configured for CC mode (logic 1)
ACTIVE PAGE	display Page B active during two page mode (logic 1)
DISPLAY BANK B	select upper bank for display Page B (logic 1)
PAGE B3 to PAGE B0	current display page for Page B
<b>Text Register 29 (TXT29)</b>	
TEN B	disable twist function for Page B (logic 0) enable twist character set for Page B (logic 1)
TS B1 to TS B0	twist character set selection for Page B
OSD PLANES B	character code columns 8 and 9 defined as single plane characters for display Page B (logic 0) character code columns 8 and 9 defined as double plane characters (special graphics characters) for display Page B (logic 1)
OSD LANG ENABLE B	enable use of OSD LAN B<2:0> to define language option for display, instead of C12/C13/C14 for display Page B
OSD LAN B2 to OSD LAN B0	alternative C12/C13/C14 bits for use with OSD menus for display Page B
<b>Text Register 30 (TXT30)</b>	
TC B2 to TC B0	language control bits (C12/C13/C14) that has twist character set for Page B
BOTTOM/TOP B	Display memory rows 0 to 11 when double height bit is set on display Page B (logic 0) Display memory rows 12 to 23 when double height bit is set on display Page B (logic 1)
DOUBLE HEIGHT B	display each character as twice normal height on display Page B (logic 1)
STATUS ROW TOP B	Display memory row 24 information below Teletext page (on display row 24) on display Page B (logic 0). Display memory row 24 information above Teletext page (on display row 0) on display Page B (logic 1).



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<b>BITS</b>	<b>FUNCTION</b>
DISPLAY X24 B	display row 24 from basic page memory on display Page B (logic 0) display row 24 from appropriate location in extension memory on display Page B (logic 1)
DISPLAY STATUS ROW ONLY B	display only row 24 on display Page B (logic 1)
<b>Text Register 31 (TXT31)</b>	
GPF11 to GPF10	general purpose register, bits defined by mask programmable location (Character ROM address 09FEH)
GPF9 to GPF8	00 = reserved 01 = 80C51 configured for 12 MHz operation 10 = reserved 11 = reserved
<b>Text Register 32 (TXT32)</b>	
9FE11	reserved
9FF11 to 9FF5	mask programmable bits available for UOC configuration (Character ROM address 09FFH)
<b>Text Register 33 (TXT33)</b>	
BFE7 to BFE0	mask programmable bits available for UOC configuration (Character ROM address 0BFEH)
<b>Text Register 34 (TXT34)</b>	
BFE11 to BFE8	mask programmable bits available for UOC configuration (Character ROM address 0BFEH)
<b>Text Register 35 (TXT35)</b>	
PKT1-24<7:0>	Teletext Packets 1-24 received for blocks 7 to 0, set by hardware and cleared by software. Teletext Packets 1-24 received after a header in any one Vertical Blanking Interval (VBI) (logic 1)
<b>Text Register 36 (TXT36)</b>	
PKT1-24<9:8>	Teletext Packets 1-24 received for blocks 9 to 8, set by hardware and cleared by software. Teletext Packets 1-24 received after a header in any one VBI (logic 1)
<b>Watchdog Timer (WDT)</b>	
WDV7 to WDV0	Watchdog Timer period
<b>Watchdog Timer Key (WDTKEY)</b>	
WKEY7 to WKEY0 <sup>(5)</sup>	Watchdog Timer key
<b>Wide Screen Signalling 1 (WSS1)</b>	
WSS<3:0> ERROR	error in WSS<3:0> (logic 1)
WSS3 to WSS0	signalling bits to define aspect ratio (group 1)

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BITS	FUNCTION
<b>Wide Screen Signalling 2 (WSS2)</b>	
WSS<7:4> ERROR	error in WSS<7:4> (logic 1)
WSS7 to WSS4	signalling bits to define enhanced services (group 2)
<b>Wide Screen Signalling 3 (WSS3)</b>	
WSS<13:11> ERROR	error in WSS<13:11> (logic 1)
WSS13 to WSS11	signalling bits to define reserved elements (group 4)
WSS<10:8> ERROR	error in WSS<10:8> (logic 1)
WSS10 to WSS8	signalling bits to define subtitles (group 3)
<b>External RAM Pointer (XRAMP)</b>	
XRAMP7 to XRAMP0	Upper address byte for MOVX RAM space in direct addressing. To use with one of the R0 to R7 registers to provide the lower address byte.

### Notes

1. This flag is set by software and reset by hardware.
2. This flag is set by hardware and must be reset by software.
3. Valid range TXT Mode 0 to 24.
4. Valid range TXT Mode 0 to 39.
5. Must be set to 55H to disable Watchdog Timer when active.

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### 8.6 Character set feature bits

Features available on the SAA56xx devices are reflected in a specific area of the Character ROM. These sections of the Character ROM are mapped to two Special Function Registers: TXT22 and TXT12. Character ROM address 09FEH is mapped to SFR TXT22, as shown in Table 6 and described in Table 7. Character ROM address 09FFH is mapped to SFR TXT12, as shown in Table 8 and described in Table 9.

**Table 6** Character ROM - TXT22 mapping

MAPPED ITEMS	11	10	9	8	7	6	5	4	3	2	1	0
Character ROM; address 09FEH	X	X	X	X	X	X	X	X	U	X	X	X
Mapped to TXT22	–	–	–	–	7	6	5	4	3	2	1	0

U = Used, X = Reserved

**Table 7** Description of Character ROM address 09FEH bits

BIT	FUNCTION
0 to 2	reserved
3	1 = PWM0, PWM1, PWM2 and PWM3 output routed to Port 2.1 to Port 2.4 respectively 0 = PWM0, PWM1, PWM2 and PWM3 output routed to Port 3.0 to Port 3.3 respectively
4 to 11	reserved

**Table 8** Character ROM - TXT12 mapping

MAPPED ITEMS	11	10	9	8	7	6	5	4	3	2	1	0
Character ROM; address 09FFH	X	X	X	X	X	X	X	U	X	X	X	X
Mapped to TXT12	–	–	–	–	–	–	–	6	5	4	3	2

U = Used, X = Reserved

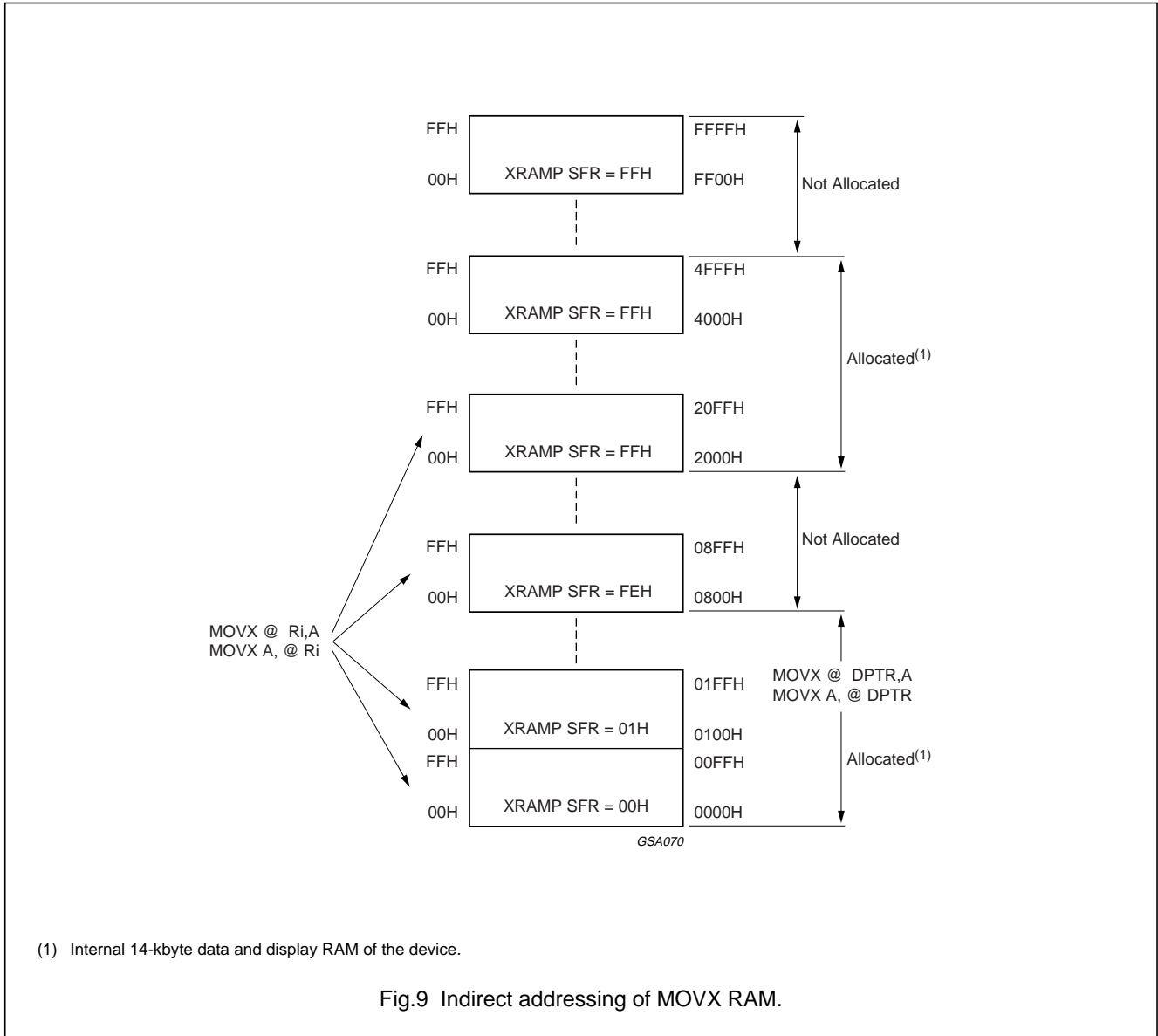
**Table 9** Description of Character ROM address 09FFH bits

BIT	FUNCTION
4	1 = Spanish character set present 0 = no Spanish character set present
0 to 3, 5 to 11	reserved



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**9 POWER-ON RESET**

Two reset inputs are present on the device, the RESET pin being active HIGH and  $\overline{\text{RESET}}$  pin being active LOW. Only one of these inputs need be connected in the system as they are ORed internally to the device and each pin has the necessary pull-down (for RESET) and pull-up (for  $\overline{\text{RESET}}$ ) resistors at the pad.

An automatic reset can be obtained when  $V_{DD}$  is switched on by connecting the RESET pin to  $V_{DDP}$  through a 10  $\mu\text{F}$  capacitor, providing the  $V_{DD}$  rise time does not exceed 1 ms, and the oscillator start-up time does not exceed 10 ms.

Alternatively, a capacitor connected to  $V_{SSP}$  with a suitable pull-up to  $V_{DDP}$ , (e.g. 10  $\mu\text{F}$  capacitor; 16 k $\Omega$  resistor) can be connected to the  $\overline{\text{RESET}}$  pin.

To ensure correct initialisation, the  $\overline{\text{RESET}}/\overline{\text{RESET}}$  pin must be held HIGH/LOW long enough for the oscillator to settle following power-up, usually a few milliseconds (application specific, typically 10 ms). Once the oscillator is stable, a further 24 crystal clocks are required to generate the reset. Once the above reset condition has been detected, an internal reset signal is triggered (which remains active for 2048 clock cycles).

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### 10 POWER SAVING MODES OF OPERATION

Three power saving modes are incorporated in the SAA56xx device: Standby, Idle and Power-down. When utilizing one of these modes, power to the device ( $V_{DDP}$ ,  $V_{DDC}$  and  $V_{DDA}$ ) should be maintained, since power saving is achieved by clock gating on a section-by-section basis.

#### 10.1 Standby mode

During Standby mode, the Acquisition and Display sections of the device are disabled. The following functions remain active:

- 80C51 CPU Core
- Memory interface
- I<sup>2</sup>C-bus interface
- Timer/counters
- Watchdog Timer
- UART, SAD, PWMs.

To enter Standby mode, the STANDBY bit in the ROMBK register must be set. Once in Standby, the crystal oscillator continues to run, but the internal clocks to Acquisition and Display are gated out. However, the clocks to the 80C51 CPU Core, Memory Interface, I<sup>2</sup>C-bus, UART, Timer/counters, Watchdog Timer and Pulse Width Modulators are maintained. Since the output values on RGB and VDS are maintained, the display output must be disabled before entering this mode.

The Standby mode may be used in conjunction with both Idle and Power-down modes. Hence, prior to entering either Idle or Power-down, the STANDBY bit may be set, thus allowing wake-up of the 80C51 CPU core without fully waking the entire device. (This enables detection of a Remote Control source in a power saving mode.)

#### 10.2 Idle mode

During Idle mode, Acquisition, Display and the CPU sections of the device are disabled. The following functions remain active:

- Memory interface
- I<sup>2</sup>C-bus interface
- Timer/counters
- Watchdog Timer
- UART, SAD, PWMs.

To enter Idle mode, bit IDL in the PCON register must be set. The Watchdog Timer must be disabled prior to entering Idle to prevent the device being reset.

Once in Idle mode, the crystal oscillator continues to run, but the internal clock to the CPU, Acquisition and Display are gated out. However, the clocks to the Memory Interface, I<sup>2</sup>C-bus, Timer/counters, Watchdog Timer and Pulse Width Modulators are maintained. The CPU state is frozen along with the status of all SFRs. Internal RAM contents are maintained, as are the device output pin values. Since the output values on RGB and VDS are maintained, the Display output must be disabled before entering this mode.

There are three methods available to recover from Idle:

- Assertion of an enabled interrupt will cause bit IDL to be cleared by hardware, thus terminating Idle mode. The interrupt is serviced and, following the instruction RETI, the next instruction to be executed will be the one after the instruction that put the device into Idle mode.
- A second method of exiting Idle is via an interrupt generated by the SAD DC Compare circuit. When the SAA56xx is configured in this mode, detection of an analog threshold at the input to the SAD may be used to trigger wake-up of the device i.e. TV Front Panel Key-press. As above, the interrupt is serviced, and following the instruction RETI, the next instruction to be executed will be the one following the instruction that put the device into Idle.
- The third method of terminating Idle mode is with an external hardware reset. Since the oscillator is running, the hardware reset need only be active for 24 crystal clocks at 12 MHz to complete the reset operation. Reset defines all SFRs and Display memory to a pre-defined state, but maintains all other RAM values. Code execution commences with the Program Counter set to '0000'.

#### 10.3 Power-down mode

In Power-down mode, the crystal oscillator is stopped. The contents of all SFRs and Data memory are maintained, however, the contents of the Auxiliary/Display memory are lost. The port pins maintain the values defined by their associated SFRs. Since the output values on RGB and VDS are maintained, the Display output must be made inactive before entering Power-down mode.

The Power-down mode is activated by setting bit PD in the PCON register. It is advisable to disable the Watchdog Timer prior to entering Power-down. Recovery from Power-down takes several milliseconds as the oscillator must be given time to stabilize.

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There are three methods of exiting Power-down:

- External interrupt. Since the clock is stopped, an external interrupt needs to be set level sensitive prior to entering Power-down. The interrupt is serviced and, following the instruction RETI, the next instruction to be executed will be the one after the instruction that put the device into Power-down mode.
- Interrupt generated by the SAD DC Compare circuit. When SAA56xx is configured in this mode, detection of a certain analog threshold at the input to the SAD may be used to trigger wake-up of the device, i.e. TV Front Panel Key-press. As above, the interrupt is serviced and, following the instruction RETI, the next instruction to be executed will be the one following the instruction that put the device into Power-down.
- External hardware reset. This reset defines all SFRs and Display memory, but maintains all other RAM values. Code execution commences with the Program Counter set to '0000'.

### 11 I/O FACILITY

The SAA56xx devices have 32 I/O lines, each of which can be individually addressed, or form four parallel 8-bit addressable ports: Port 0, Port 1, Port 2 and Port 3.

I<sup>2</sup>C-bus ports (P1.4, P1.5, P1.6 and P1.7) can only be configured as open-drain.

#### 11.1 Port type

All individual ports can be programmed to function in one of four modes, the mode is defined by two associated Port Configuration Registers: PnCFGA and PnCFGB (where n = port number 0, 1, 2 or 3). The modes available are open-drain, quasi-bidirectional, high-impedance and push-pull.

##### 11.1.1 OPEN-DRAIN (TTL, 5 V TOLERANT)

The open-drain mode can be used for bidirectional operation of a port and requires an external pull-up resistor. The pull-up voltage has a maximum value of 5.5 V, to allow connection of the device into a 5 V environment.

##### 11.1.2 QUASI-BIDIRECTIONAL (CMOS, 3V3 TOLERANT)

The quasi-bidirectional mode is a combination of open-drain and push-pull. It requires an external pull-up resistor to V<sub>DDP</sub> (normally 3.3 V).

When a LOW-to-HIGH signal transition is output from the device, the pad is put into push-pull mode for one clock cycle (166 ns) after which the pad goes into open-drain mode. This mode is used to speed up the edges of signal transitions. This is the default mode of operation of the pads after reset.

##### 11.1.3 HIGH-IMPEDANCE (TTL, 5 V TOLERANT)

The high-impedance mode can be used for input only operation of the port. When using this configuration, the two output transistors are turned off.

##### 11.1.4 PUSH-PULL (CMOS, 3V3 TOLERANT)

The push-pull mode can be used for output only. In this mode, the signal is driven to either 0 V or V<sub>DDP</sub>, which is nominally 3.3 V.

## 12 INTERRUPT SYSTEM

The device has 15 interrupt sources, each of which can be enabled or disabled. When enabled, each interrupt can be assigned one of two priority levels. There are five interrupts that are common to the 80C51. Two of these are external interrupts (EX0 and EX1); the other three are timer interrupts (ET0, ET1 and ET2). In addition to the conventional 80C51, two application specific interrupts are incorporated internal to the device, with the following functionality:

- **Closed Caption Data Ready interrupt (ECC).** This interrupt is generated when the device is configured in Closed Caption Acquisition mode. The interrupt is activated at the end of the currently selected Slice Line, as defined in the CCLIN SFR.
- **Display Busy interrupt (EBUSY).** An interrupt is generated when the display enters either a Horizontal or Vertical Blanking Period. i.e. indicates when the microcontroller can update the Display RAM without causing undesired effects on the screen. This interrupt can be configured in one of two modes using the Memory Mapped Register (MMR) Configuration Register (address 87FFH, bit TXT/V).
  - Text Display Busy: An interrupt is generated on each active horizontal display line when the Horizontal Blanking Period is entered.
  - Vertical Display Busy: An interrupt is generated on each vertical display field when the Vertical Blanking Period is entered.

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There are four interrupts connected to the 80C51 microcontroller peripherals, as follows:

- I<sup>2</sup>C-bus Transmit/Receive
- UART Receive
- UART Transmit
- UART Receive/Transmit.

Four additional general purpose external interrupts are incorporated in the SAA56xx with programmable edge detection (INT2 {EX2}, INT3 {EX3}, INT4 {EX4} and INT5 {EX5}). The EXTINT SFR is used to configure each of these interrupts as either level activated, rising edge, falling edge or both edges sensitive, see Table 10.

### 12.1 Interrupt enable structure

Each of the individual interrupts can be enabled or disabled by setting or clearing the relevant bit in the interrupt enable SFRs (IE and IEN1). All interrupt sources can also be globally disabled by clearing bit EA (IE.7), as shown in Fig.10.

### 12.2 Interrupt enable priority

Each interrupt source can be assigned one of two priority levels. The interrupt priorities are defined by the interrupt priority SFRs (IP and IP1).

A low priority interrupt can be interrupted by a high priority interrupt, but not by another low priority interrupt. A high priority interrupt cannot be interrupted by any other interrupt source.

If two requests of different priority level are received simultaneously, the request with the higher priority level is serviced. If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus, within each priority level there is a second priority structure determined by the polling sequence as defined in Table 12.

### 12.3 Interrupt vector address

The processor acknowledges an interrupt request by executing a hardware generated LCALL to the appropriate servicing routine. The interrupt vector addresses for each source are shown in Table 12.

### 12.4 Level/edge interrupt

The external interrupt can be programmed to be either level activated or transition activated by setting or clearing the IT0/IT1 bits in the Timer Control SFR (TCON), see Table 11.

The external interrupt INT1 differs from the standard 80C51 interrupt in that it is activated on both edges when in edge sensitive mode. This is to allow software pulse width measurement for handling remote control inputs.

The four other external interrupts INT2, INT3, INT4 and INT5 are configured using the EXTINT register, as shown in Table 10.

**Table 10** Configuration of external interrupts (INT2 to INT5)

SFR EXTINT; EXnCFG<1:0>; n = 2 to 5	MODE
00	level sensitive - active LOW
01	rising edge sensitive
10	falling edge sensitive
11	both edges sensitive

**Table 11** External interrupt activation

BIT	LEVEL	EDGE
IT0	active LOW	
IT1	-	INT0 = negative edge
		INT1 = positive and negative edge



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**Table 12** Interrupt priority (within same level)

SOURCE	PRIORITY WITHIN LEVEL	INTERRUPT VECTOR	RELATED SFR	INT NUMBER
EX0	highest	0003H	IEN0	0
ES2		002BH	IEN0	5
EURX		0053H	IEN1	10
ET0		000BH	IEN0	1
EBUSY		0033H	IEN0	6
EX2		005BH	IEN1	11
EX1		0013H	IEN0	2
ET2		003BH	IEN1	7
EX3		0063H	IEN1	12
ET1		001BH	IEN0	3
EUART		0043H	IEN1	8
EX4		006BH	IEN1	13
ECC		0023H	IEN0	4
EUTX		004BH	IEN1	9
EX5	lowest	0073H	IEN1	14

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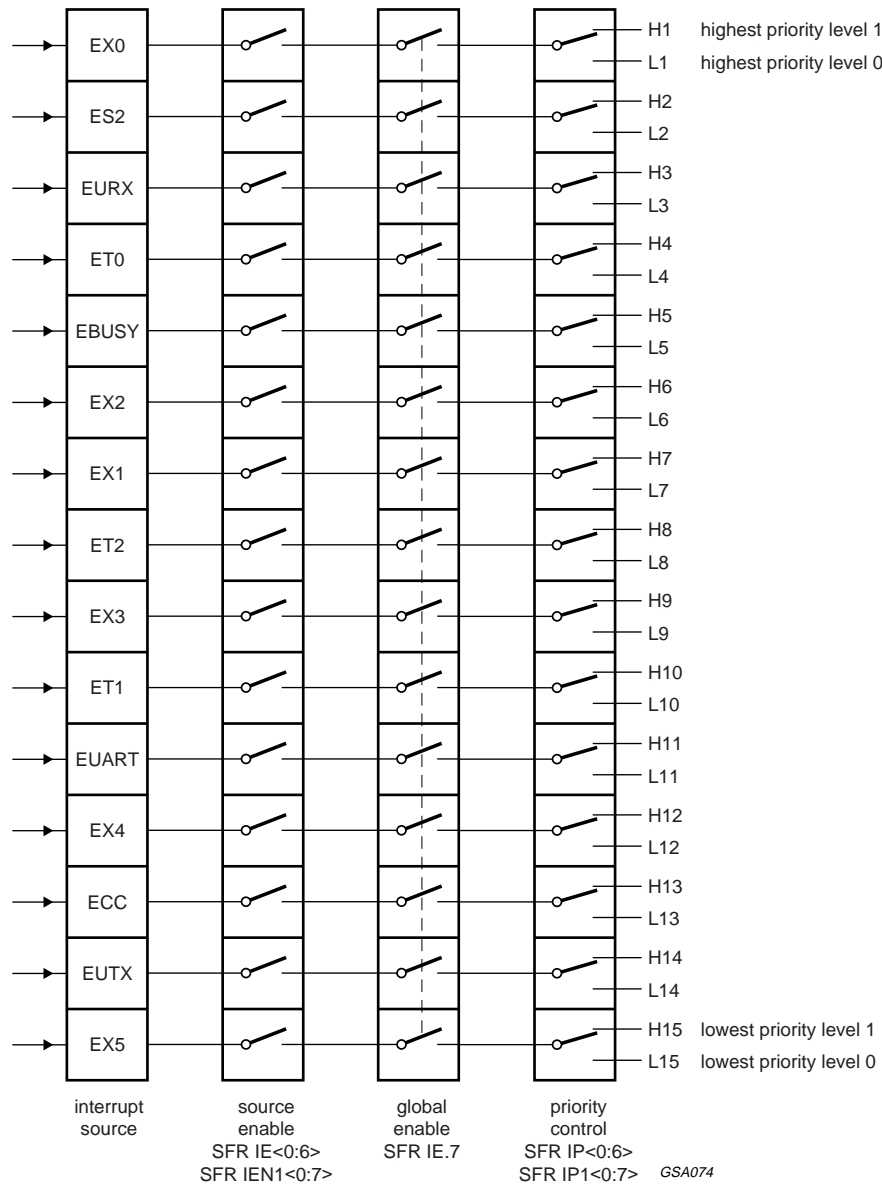


Fig.10 Interrupt structure.

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## 13 TIMERS/COUNTERS

Three 16-bit Timers/counters are incorporated: Timer 0, Timer 1 and Timer 2. Each can be configured to operate as either timers or event counters. Timer 2 is new for the SAA56xx, whereas Timer 0 and Timer 1 are standard 80C51 Timer/counters, refer to “*Handbook IC20 80C51-Based 8-bit Microcontrollers*”. **Remark:** It should be noted that because the SAA56xx uses both clock edges, the division factor is 6 instead of 12.

When the Timers/counters are configured as timers, the period depends on the microcontroller clock frequency of 12 MHz.

In Timer mode, the register is incremented on every machine cycle, so that machine cycles are counted. Since the machine cycle consists of six oscillator periods, the count rate is  $\frac{1}{6}f_{clk}$  (where  $f_{clk}$  is the microcontroller clock frequency: 12 MHz).

In Counter mode, the register is incremented in response to a negative transition at its corresponding external pin T0/T1/T2. Since pins T0/T1/T2 are sampled once per machine cycle, it takes two machine cycles to recognise a transition. This gives a maximum count rate of  $\frac{1}{12}f_{clk}$  (where  $f_{clk}$  is the microcontroller clock frequency, 12 MHz).

### 13.1 Timer/counter 0 and Timer/counter 1

There are six Special Function Registers used to control Timer/counter 0 and Timer/counter 1.

**Table 13** Timer/counter 0 and Timer/counter 1 registers

SFR	ADDRESS
TCON	88H
TMOD	89H
TL0	8AH
TH0	8BH
TL1	8CH
TH1	8DH

The Timer/counter function is selected by control bits C/T in the Timer Mode SFR(TMOD). These two Timers/counters have four operating modes, which are selected by bit-pairs (M1 and M0) in TMOD. Details of the modes of operation is given in “*Handbook IC20, 80C51-Based 8-Bit Microcontrollers*”.

TL0 and TH0 are the actual Timer/counter registers for Timer 0. TL0 is the low byte and TH0 is the high byte. TL1 and TH1 are the actual Timer/counter registers for Timer 1. TL1 is the low byte and TH1 is the high byte.

### 13.2 Timer/counter 2

Timer 2 is controlled using the following SFRs:

**Table 14** Timer 2 Special Function Registers

SFR	ADDRESS
T2CON	F1H
T2MOD	F2H
RCAP2L	F3H
RCAP2H	F4H
TL2	F5H
TH2	F6H

Timer 2 can operate in four different modes (see Table 15):

- Auto-reload
- Capture
- Baud rate generation
- Clock output.

The count-down option is only possible in the Auto-reload mode with DCEN in T2MOD set and the external trigger input disabled.

**Table 15** Timer 2 operating mode

RCLK0 OR TCLK0 OR RCLK1 OR TCLK1	CP/RL2	T2OE	C/T2	OPERATING MODE
0	0	0	X	16-bit Auto-reload
0	1	0	X	16-bit Capture
1	X	X	X	Baud rate generation
X	0	1	0	Clock output

#### 13.2.1 CAPTURE MODE

In the Capture mode, registers RCAP2L/RCAP2H are used to capture the TL2/TH2 data. By setting/clearing bit EXEN2 in T2CON, the external trigger input T2EX (P3.4) can be enabled/disabled. If EXEN2 = 0, Timer 2 is a 16-bit Timer/counter which, upon overflow, sets TF2 flag in T2CON. If EXEN2 = 1, then Timer 2 does the above, but with the added feature that a HIGH-to-LOW transition at T2EX on Port 3.4 causes the current Timer 2 value (TL2/TH2 data) to be captured into RCAP2L/RAP2H, and bit EXF2 in T2CON to be set.

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### 13.2.2 AUTO-RELOAD MODE

In the Auto-reload mode, Timer 2 can be programmed to count up/down by clearing/setting bit DCEN in T2MOD.

### 13.2.3 COUNTING UP (DCEN = 0)

In the Auto-reload mode and when counting up, registers RCAP2L/RCAP2H are used to hold a reload value for TL2/TH2 when Timer 2 rolls over. By setting/clearing bit EXEN2 in T2CON, external trigger T2EX on Port 3.4 can be enabled/disabled. If EXEN2 = 0, Timer 2 is a 16-bit timer/counter which, upon overflow, sets TF2 and reloads TL2/TH2 with the reload value in RCAP2L/RCAP2H. If EXEN2 = 1, Timer 2 does the above, but with the added feature that a HIGH-to-LOW transition at the external trigger T2EX on Port 3.4 causes the current RCAP2L/RCAP2H value to be loaded into TL2/TH2 respectively, and bit EXF2 in T2CON to be set.

Timer 2 interrupt is set if EXF2 or TF2 is set.

### 13.2.4 COUNTING UP (DCEN = 1 AND T2EX = 1)

In this mode Timer 2 counts up. When Timer 2 overflows (FFFFH state), bit TF2 is set. This reloads TL2 and TH2 with the contents of RCAP2L and RCAP2H, respectively. On overflow, bit EXF2 is inverted and hence toggles during operation, so that bit EXF2 can be used as 17<sup>th</sup> bit, if desired.

Timer 2 interrupt will be set only if TF2 is set.

### 13.2.5 COUNTING DOWN (DCEN = 1 AND T2EX = 0)

In this mode Timer 2 counts down. Underflow will occur when the contents of TL2/TH2 match the contents of RCAP2L/RCAP2H. A Timer 2 roll-over from 0000H to FFFFH is not considered as an underflow. Upon underflow, bit TF2 will be set and registers TL2/TH2 will be loaded with FFFFH. In addition, an underflow will cause bit EXF2 to be inverted, such that it can be used as the 17<sup>th</sup> bit, if desired.

Timer 2 interrupt is set only if TF2 is set.

### 13.2.6 BAUD RATE GENERATION MODE

In this mode, timer overflow will load TL2 and TH2 with the contents of RCAPL and RCAPH respectively and it will not set TF2. Bit EXF2 will be set if EXEN2 is set and a HIGH-to-LOW transition is detected on pin T2EX (Port 3.4).

When Timer 2 is configured for timer operation, the timer increments every state. Normally, as a timer, it would increment every machine cycle.

Timer 2 interrupt is set only if EXF2 is set.

### 13.2.7 CLOCK OUTPUT MODE

In the clock output mode, external pin T2 is used as a clock output. A timer overflow causes TL2 and TH2 to be loaded with T2CAPL and T2CAPH, respectively. An overflow toggles bit EXF2, which is connected to pin T2. The frequency of T2 will be half the overflow frequency. Timer overflow will not set TF2. A HIGH-to-LOW transition on the external trigger T2EX on Port 3.4 sets EXF2. It is possible to configure Timer 2 in clock-out mode and baud generator mode simultaneously.

Timer 2 interrupt is set only if EXF2 is set.

## 14 WATCHDOG TIMER

The Watchdog Timer is a counter that, once in an overflow state, forces the microcontroller into a reset condition. The purpose of the Watchdog Timer is to reset the microcontroller if it enters an erroneous processor state (possibly caused by electrical noise or RFI) within a reasonable period of time. When enabled, the Watchdog circuit generates a system reset if the user program fails to reload the Watchdog Timer within a specified length of time, known as the Watchdog Interval.

The Watchdog Timer consists of an 8-bit counter with a 16-bit prescaler. The prescaler is fed with a signal whose frequency is  $\frac{1}{6}f_{clk}$  (2 MHz for 12 MHz 80C51 core). The 8-bit counter is incremented every 't' seconds where:

$$t = \left(6 \frac{1}{f_{clk}}\right) \times 2^{16} = \frac{6 \times 65536}{12 \text{ MHz}} = 32.768 \text{ ms}$$

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### 14.1 Watchdog Timer operation

The Watchdog Timer operation is activated when bit WLE in the Power Control SFR (PCON) is set. The Watchdog can be disabled by software by loading the value 55H into the Watchdog Timer Key SFR (WDTKEY). This must be performed before entering Idle/Power-down mode to prevent exiting the mode prematurely.

Once activated, the Watchdog Timer SFR (WDT) must be reloaded before the timer overflows. Bit WLE must be set to enable loading of the WDT SFR. Once loaded, bit WLE is reset by hardware, to prevent erroneous software from loading the WDT SFR.

The value loaded into the WDT defines the Watchdog Interval (WI):

$$WI = (256 - WDT) \times t$$

For a 12 MHz microcontroller clock,  $t = 32.768$  ms.

The range of intervals is from WDT = 00H, this gives 8.38 ms to WDT = FFH, which gives 32.768 ms.

### 15 PORT ALTERNATIVE FUNCTIONS

Ports 1, 2 and 3 are shared with alternative functions to enable control of external devices and circuits. These functions are enabled by setting the appropriate SFR and also writing a logic 1 to the port bit that the function occupies.

### 16 PULSE WIDTH MODULATORS

The device has eight 6-bit PWM outputs for analog control of e.g. volume, balance, bass, treble, brightness, contrast, hue and saturation. The PWM outputs generate pulse patterns with a repetition rate of 21.33  $\mu$ s, with the high time equal to the PWM SFR value multiplied by 0.33  $\mu$ s. The analog value is determined by the ratio of the high time to the repetition time. A DC voltage proportional to the PWM setting is obtained by means of an external integration network (low-pass filter).

#### 16.1 PWM control

The relevant PWM is enabled by setting the PWM enable bit PWxE in the PWMx Control Register. The high time is defined by the value PWxV<5:0>.

### 16.2 Tuning Pulse Width Modulator (TPWM)

The device has a single 14-bit TPWM that can be used for Voltage Synthesis Tuning. The method of operation is similar to the normal PWM, except that the repetition period is 42.66  $\mu$ s.

#### 16.2.1 TPWM CONTROL

Two SFRs are used to control the TPWM: TDACL and TDACH. The TPWM is enabled by setting bit TPWE in the TDACH SFR. The most significant bits TD<13:7> alter the high period between 0 and 42.33  $\mu$ s. The seven least significant bits TD<6:0> extend certain pulses by a further 0.33  $\mu$ s. For example, if TD<6:0> = 01H, 1 in 128 periods will be extended by 0.33  $\mu$ s. If TD<6:0> = 02H, 2 in 128 periods will be extended.

The TPWM will not start to output a new value until TDACH has been written to. Therefore, if the value is to be changed, TDACL should be written before TDACH.

### 16.3 Software ADC (SAD)

Four successive approximation ADCs can be implemented in software by using the on-board 8-bit Digital-to-Analog Converter and Analog Comparator.

#### 16.3.1 SAD CONTROL

The control of the required analog input is done using channel select bits CH<1:0> in the SAD SFR. This selects the required analog input to be passed to one of the inputs of the comparator. The second comparator input is generated by the DAC, whose value is set by bits SAD<7:0> in the SAD and SADB SFRs. A comparison between the two inputs is made when the start compare bit ST in the SAD SFR is set. This must be at least one instruction cycle after the SAD<7:0> value has been set. The result of the comparison is given on VHI one instruction cycle after bit ST is set.

#### 16.3.2 SAD INPUT VOLTAGE

The external analog voltage that is used for comparison with the internally generated DAC voltage does not have the same voltage range due to the 5 V tolerance of the pin. It is limited to  $V_{DDP} - V_{tn}$  where  $V_{tn}$  is a maximum of 0.75 V. For further details, refer to the "SAA55XX and SAA56XX Software Analogue to Digital Converter Application Note SPG/AN99022".

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### 16.3.3 SAD DC COMPARATOR MODE

The SAD module (see Fig.11) incorporates a DC Comparator mode, which is selected using the 'DC\_COMP' control bit in the SADB SFR. This mode enables the microcontroller to detect a threshold crossing at the input to the selected analog input pin (P3.0/ADC0, P3.1/ADC1, P3.2/ADC2 or P3.3/ADC3) of the software ADC. A level sensitive interrupt is generated when the analog input voltage level at the pin falls below the analog output level of the SAD DAC.

This mode is intended to provide the device with a wake-up mechanism from Power-down or Idle mode when a key-press on the front panel of the TV is detected.

The following software sequence should be used when utilizing this mode for Power-down or Idle mode:

1. Disable INT1 using the IEN0 SFR.
2. Set INT1 to level sensitive using the TCON SFR.
3. Set the DAC digital input level to the desired threshold level using SAD/SADB SFRs and select the required input pin (P3.0, P3.1, P3.2 or P3,3) using CH1 and CH0 in the SAD SFR.
4. Enter DC Compare mode by setting the 'DC\_COMP' enable bit in the SADB SFR.
5. Enable INT1 using the IEN0 SFR.
6. Enter Power-down/Idle mode. Upon wake-up, the SAD should be restored to its conventional operating mode by disabling the 'DC\_COMP' control bit.

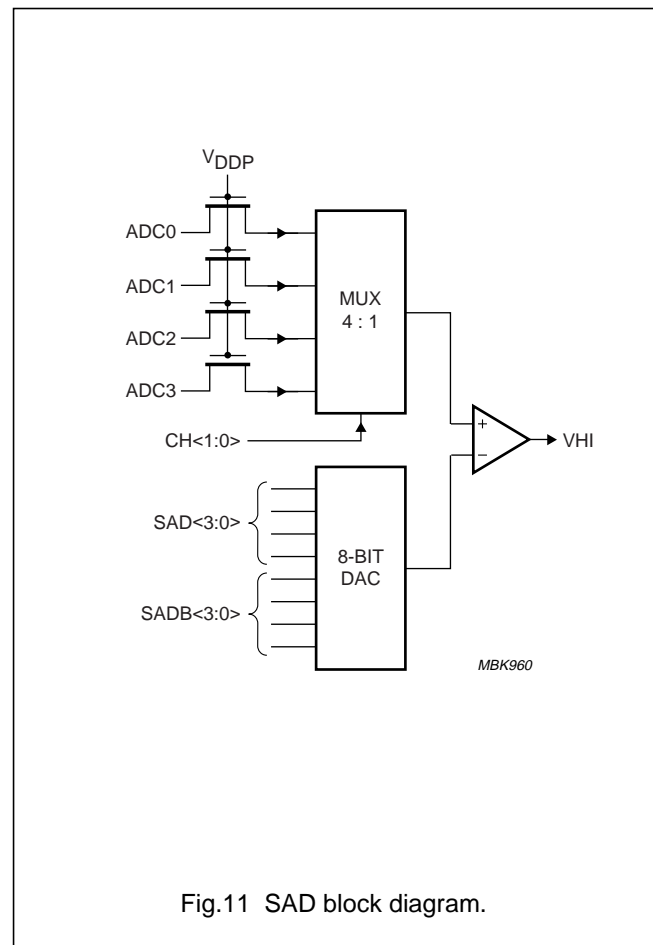


Fig.11 SAD block diagram.

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### 17 I<sup>2</sup>C-BUS SERIAL I/O

The I<sup>2</sup>C-bus consists of a serial data line (SDA) and a serial clock line (SCL). The definition of the I<sup>2</sup>C-bus protocol can be found in "The I<sup>2</sup>C-bus and how to use it (including specification). Philips Semiconductors".

The device operates in four modes:

- Master transmitter
- Master receiver
- Slave transmitter
- Slave receiver.

The microcontroller peripheral is controlled by the Serial Control SFR (S1CON) and its status is indicated by the Status SFR (S1STA). Information is transmitted/received to/from the I<sup>2</sup>C-bus using the Data SFR (S1DAT). The Slave Address SFR (S1ADR) is used to configure the slave address of the peripheral.

The byte level I<sup>2</sup>C-bus serial port is identical to the I<sup>2</sup>C-bus serial port on the P8xC558, except for the clock rate selection bits CR<2:0>. The operation of the subsystem is described in detail in the "P8xC558 data sheet".

#### 17.1 I<sup>2</sup>C-bus modes

Three different I<sup>2</sup>C-bus selection tables for CR<2:0> can be configured using the ROMBK SFR (IIC\_LUT<1:0>), as shown in Table 16.

##### 17.1.1 NOMINAL MODE (IIC\_LUT<1:0> = 00)

This option accommodates the P8xC558 I<sup>2</sup>C-bus, refer to "Handbook IC20, 80C51-Based 8-Bit Microcontrollers". The various serial rates are shown in Table 16:

**Table 16** I<sup>2</sup>C-bus serial rates in 'P8xC558 nominal mode'

CR2	CR1	CR0	12 MHz DIVISOR	I <sup>2</sup> C-BUS BIT FREQUENCY (kHz)
0	0	0	60	200
0	0	1	1600	7.5
0	1	0	40	300
0	1	1	30	<b>400</b>
1	0	0	240	50
1	0	1	3200	3.75
1	1	0	160	75
1	1	1	120	<b>100</b>

##### 17.1.2 FAST MODE (IIC\_LUT<1:0> = 01)

This option accommodates the P8xC558 I<sup>2</sup>C-bus doubled rates, as shown in Table 17.

**Table 17** I<sup>2</sup>C-bus serial rates in 'P8xC558 fast mode'

CR2	CR1	CR0	12 MHz DIVISOR	I <sup>2</sup> C-BUS BIT FREQUENCY (kHz)
0	0	0	30	<b>400</b>
0	0	1	800	15
0	1	0	20	600
0	1	1	15	800
1	0	0	120	<b>100</b>
1	0	1	1600	7.5
1	1	0	80	150
1	1	1	60	200

##### 17.1.3 SLOW MODE' (IIC\_LUT<1:0> = 10)

This option accommodates the P8xC558 I<sup>2</sup>C-bus rates, divided by 2, as shown in Table 18.

**Table 18** I<sup>2</sup>C-bus serial rates 'P8xC558 slow mode'

CR2	CR1	CR0	12 MHz DIVISOR	I <sup>2</sup> C-BUS BIT FREQUENCY (kHz)
0	0	0	120	<b>100</b>
0	0	1	3200	3.75
0	1	0	80	150
0	1	1	60	200
1	0	0	480	25
1	0	1	6400	1.875
1	1	0	320	37.5
1	1	1	240	50

### 17.2 I<sup>2</sup>C-bus port selection

Two I<sup>2</sup>C-bus ports are available: SCL0/SDA0 and SCL1/SDA1. The ports are selected by using TXT21.I<sup>2</sup>C Port 0 and TXT21.I<sup>2</sup>C Port 1. When a port is enabled, any information transmitted from the device goes onto the enabled port. Information transmitted to the device can only be acted on if the port is enabled.

If both ports are enabled, then data transmitted from the device is seen on both ports. However, data transmitted to the device on one port cannot be seen on the other port.

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### 18 UART PERIPHERAL

The 80C51 microcontroller incorporates a full duplex UART with a single byte receive buffer, meaning that it can commence reception of a second byte before the first is read from the receive buffer. This register is implemented twice. Writing to S0BUF writes to the transmit buffer. Reading from S0BUF reads from the receive buffer. Only hardware can read from the transmit buffer and write to the receive buffer.

For further details please refer to the “SAA56xx UART Operation Application Note SPG/AN01010”.

The UARTs TX and RX pins connect to P0.1 and P0.0, respectively.

Two registers (S0CON, S0BUF) and one bit (SMOD in PCON register) control the UART.

**Table 19** UART Special Function Registers

SFR	ADDRESS
S0CON	99H
S0BUF	9AH

#### 18.1 UART modes

The serial port can operate in four modes:

- **Mode 0:** Serial data enters and exits through RX. TX outputs the shift clock. Eight bits are transmitted and received (LSB first). The baud rate is fixed at  $\frac{1}{6}f_{clk}$ .
- **Mode 1:** Ten bits are transmitted (through TX) or received (through RX): a start bit (logic 0), eight data bits (LSB first) and a stop bit (logic 1). On receive, the stop bit goes into RB8 in SFR S0CON. The baud rate can be varied at either Timer 1 or Timer 2 overflow rate.
- **Mode 2:** Eleven bits are transmitted (through TX) or received (through RX): start bit (logic 0), eight data bits (LSB first), a 9<sup>th</sup> data bit and a stop bit (logic 1). On transmit, the 9<sup>th</sup> data bit, TB8 in S0CON, can be assigned the value of logic 0 or logic 1. For example, the parity bit could be moved into TB8. On receive, the 9<sup>th</sup> data bit goes into RB8 in S0CON, while the stop bit is ignored. The baud rate can be programmed to either  $\frac{1}{32}f_{clk}$  or  $\frac{1}{16}f_{clk}$ .
- **Mode 3:** Eleven bits are transmitted (through TX) or received (through RX): a start bit (logic 0), eight data bits (LSB first), a 9<sup>th</sup> data bit and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate can be varied at either Timer 1 or Timer 2 overflow rate.

In all four modes, transmission is initiated by any instruction that uses S0BUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. In the other modes, reception is initiated by the incoming start bit if REN = 1.

#### 18.2 UART multiprocessor communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, nine data bits are received. The 9<sup>th</sup> bit goes into RB8, followed by a stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in S0CON. A way to use this feature in multiprocessor systems is as follows.

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte. The 9<sup>th</sup> bit is logic 1 in an address byte and logic 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte reception.

An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will follow. The slaves that were not being addressed leave their SM2 bits set and carry on the task they were performing.

Bit SM2 has no effect in Mode 0; in Mode 1, it can be used to check the validity of the stop bit. When receiving in Mode 1 (if SM2 = 1), the receive interrupt will not be activated unless a valid stop bit is received.

#### 18.3 S0BUF registers

This register is implemented twice. Writing to S0BUF writes to the transmit buffer. Reading from S0BUF reads from the receive buffer. Only hardware can read from the transmit buffer and write to the receive buffer.



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### 18.4 UART baud rates

For full details of the UART operation please refer to “*Handbook IC20,80C51-Based 8-bit Microcontrollers*”.

**Remark:**  $f_{clk}$  used refers to the microcontroller clock frequency (12 MHz). The SAA56xx family of devices uses both clock edges, so the division factor is 6 instead of 12.

The serial port can operate with different baud rates, depending on its mode.

- **Mode 0** (SM0 = 0, SM1 = 0); in shift register mode the baud rate is fixed at  $\frac{1}{6}f_{clk}$
- **Mode 2** (SM0 = 0, SM1 = 1); in this fixed baud rate mode, the baud rate is determined by the SMOD bit in the PCON register:  $baud\ rate = \frac{2^{SMOD}}{32} \times f_{clk}$
- **Modes 1** (SM0 = 0, SM1 = 1); **and 3** (SM0 = 1, SM1 = 0); in these modes the baud rate is variable and is determined by either Timer 1 or Timer 2; see Section 13.

**Timer 1:** can be used in either Timer or Counter mode, when the baud rate is determined by the timer overflow rate and the value of SMOD as follows:

$$baud\ rate = \frac{2^{SMOD}}{32} \times \text{Timer 1 overflow rate i.e. } rate = \frac{2^{SMOD}}{32} \times \frac{f_{clk}}{6 \times (256 - T1H)}$$

where T1H is the decimal value of the register contents.

When Timer 1 is configured for timer operation, it is normal to use the 8-bit auto-reload mode, however 16-bit mode can be used for very low baud rates. In this case the Timer 1 interrupt will need to do a 16-bit software reload.

**Timer 2:** will be placed in Baud generator mode when RCLK0 and/or TCLK0 bits in the T2CON register are set. When Timer 2 is clocked internally it has the following

$$baud\ rate: \frac{f_{clk}}{16 \times [65536 - (TH2, TL2)]}$$

Where TH2 and TL2 is the decimal value of the 16-bit contents of there respective SFRs.

When Timer 2 is configured as a counter, using pin T2 the baud rate equals the Timer 2 overflow rate divided by 16.

### 19 LED SUPPORT

Port pins P0.5 and P0.6 have an 8 mA current sinking capability to enable LEDs in series with current limiting resistors to be driven directly, without the need for additional buffering circuits.

### 20 EXTERNAL SRAM/ROM INTERFACE

The external address/data bus of the 80C51 microprocessor may be interfaced to:

- Additional SRAM Data memory for multi-page acquisition applications
- External Program ROM.

The application circuit can be achieved using either the multiplexed address and data I/O or the de-multiplexed address and data I/O.

**External SRAM Data Memory:** it is possible to interface up to 256 kbytes of external data memory using pins RAMBK<1:0> and A15\_BK. Each of the four Data memory banks is selected by RAMBK<1:0> (SFR ROMBK<4:3>), see Table 20.

Figure 12 shows an example of the interfacing connections for external SRAM data memory; see also Section 30.

**Table 20** RAMBK selection

RAMBK<1:0>	BANK	EXTERNAL ADDRESS RANGE
00	Bank 0	0 to 64 kbytes
01	Bank 1	64 to 128 kbytes
10	Bank 2	128 to 192 kbytes
11	Bank 3	192 to 256 kbytes

**External program ROM (pin  $\overline{EA}$  tied LOW):** the internal microcontroller logic makes it possible to only address 192 bytes of external program ROM with linear addressing. Figure 13 shows the interface connections.

**Remark:** For emulating the external program ROM pins A15\_BK, ROMBK0, ROMBK1 and ROMBK2 are used to address up to 256 kbytes. With additional glue logic these address lines can be used to address up to 256 kbytes os external ROM. Figure 14 shows the additional glue logic.

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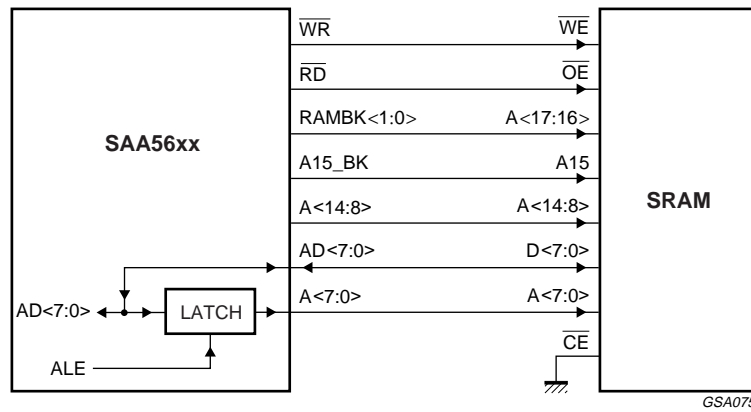


Fig.12 External SRAM configuration.

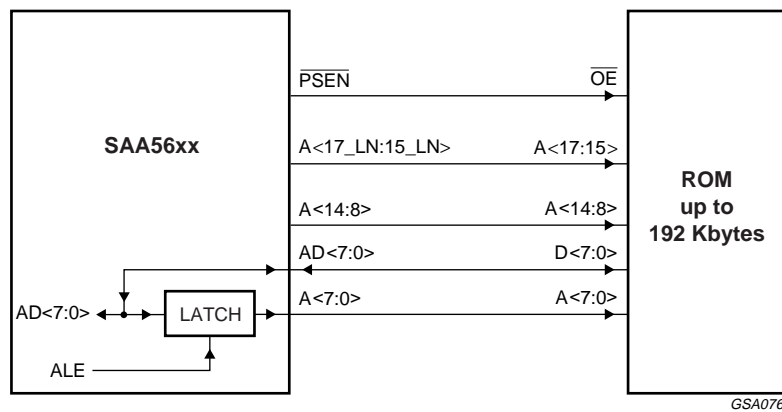


Fig.13 External ROM configuration.

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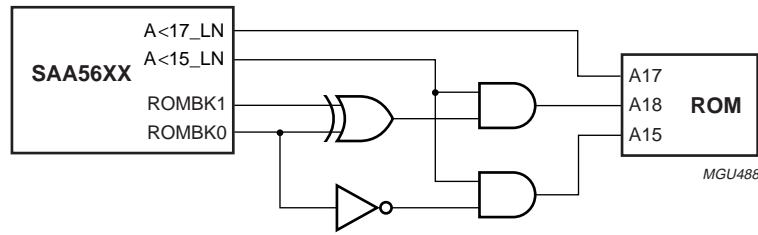


Fig.14 Additional glue logic required to address 256 kbytes of external ROM.

21 MEMORY INTERFACE

The memory interface controls access to the embedded DRAM, refreshing of the DRAM and page clearing. The DRAM is shared between Data Capture, display and microcontroller sections.

The Data Capture section uses the DRAM to store acquired information that has been requested. The display reads from the DRAM information and converts it to RGB values. The microcontroller uses the DRAM as embedded auxiliary RAM.

21.1 Memory structure

The memory is partitioned into two distinct areas, the dedicated Auxiliary RAM area and the Display RAM area. When not being used for Data Capture or display, the Display RAM area can be used as an extension to the auxiliary RAM area.

21.1.1 AUXILIARY RAM

The Auxiliary RAM is not initialised at power-up and must be initialised by the application software. Its contents are maintained during Idle mode and Standby mode, but are lost if Power-down mode is entered.

21.1.2 DISPLAY RAM

The Display RAM is initialised on power-up to a value of 20H throughout. The contents of the Display RAM are maintained when entering Idle mode. If Idle mode is exited using an interrupt, the contents are unchanged, if Idle mode is exited using an external reset, the contents are initialised to 20H.

Full Closed Caption display requires display RAM from 8000H to 845FH. The memory from 8460H to 84FFH (must be initialised by the application software) can be utilised as an extension to the dedicated contiguous Auxiliary RAM that occupies 0000H to 07FFH.

21.2 Memory mapping

The dedicated auxiliary RAM area occupies 2 kbytes, with an address range from 0000H to 07FFH. The Display RAM occupies a maximum of 12 kbytes with an address range from 2000H to 5000H for TXT mode and 8000H to 84FFH for CC mode (see Fig.15). Although having different address ranges, the two modes occupy physically the same DRAM area.

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### 21.3 CCBASE SFR

The SAA56xx incorporates a CCBASE SFR, which enables CC Display data to be accessed from any 1-kbyte partition within the Display memory. This SFR allows the CC Base address for Closed Caption Display memory to overlap Teletext memory at the following hexadecimal boundaries of the 80C51 microcontroller 'MOVX' address space:

2000H (same as SAA55x default), 2400H, 2800H, 2C00H, 3000H, 3400H, 3800H, 3C00H, 4000H, 4400H, 4800H, 4C00H, 5000H, 5400H, 5800H, 5C00H, 6000H, 6400H, 6800H and 6C00H.

The reset value for the CCBASE Address SFR is 20H, thus ensuring software compatibility with other variants in the SAA55xx family. Register bits CCBASE1 and CCBASE0 must always be set to zero at 1-kbyte boundaries.

Figure 15 shows the default setting for the CC Display memory.

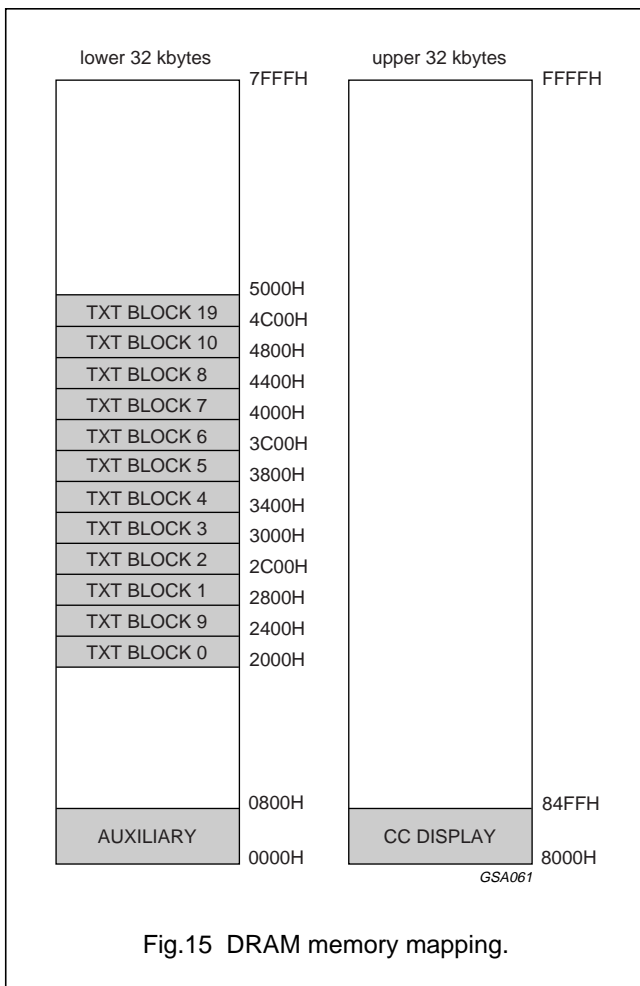


Fig.15 DRAM memory mapping.

### 21.4 Addressing memory

The memory can be addressed by the microcontroller in two ways, either directly using a MOVX command or via SFRs, depending on what address is required.

The dedicated Auxiliary RAM, and Display memory in the range 8000H to 86FFH can only be accessed using the MOVX command.

The Display memory in the range 2000H to 47FFH can either be directly accessed using the MOVX command, or via the SFRs.

#### 21.4.1 TXT DISPLAY MEMORY SFR ACCESS

When in TXT mode (see Fig.16), the Display memory is configured as 40 columns wide by 25 rows and occupies 1K × 8-bit of memory. There can be a maximum of 12 display pages. Using TXT15.BLOCK<3:0> and TXT15.MICRO BANK, the required display page can be selected to be written to. The row and column within that block is selected using TXT9.R<4:0> and TXT10.C<5:0>. The data at the selected position can be read or written using TXT11.D<7:0>.

Whenever a read or write is performed on TXT11, the row values stored in TXT9 and column value stored in TXT10 are automatically incremented. For rows 0 to 24, the column value is incremented up to a maximum of 39, at which point it resets to 0 and increments the row counter value. When row 25 column 23 is reached, the values of the row and column are both reset to 0.

Writing values outside the valid range for TXT9 or TXT10 will cause undetermined operation of the auto-incrementing function for accesses to TXT11.

#### 21.4.2 TXT DISPLAY MEMORY MOVX ACCESS

For the generation of OSD displays that use this mode of access, it is important to understand the mapping of the MOVX address onto the display row and column value. This mapping of row and column onto address is shown in Table 21. The values shown are added onto a base address for the required memory block (see Fig.16) to give a 16-bit address.

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**Table 21** Column and row to 'MOVX' address (lower 10 bits of address in hexadecimal)

ROW	COL. 0	.....	COL. 23	.....	COL. 31	COL. 32	.....	COL. 39
Row 0	000	.....	017	.....	01F	3F8	.....	3FF
Row 1	020	.....	037	.....	03F	3F0	.....	3F7
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
Row 23	2E0	.....	3F7	.....	2FF	340	.....	347
Row 24	300	.....	317	.....	31F	338	.....	33F
Row 25	320	.....	337					

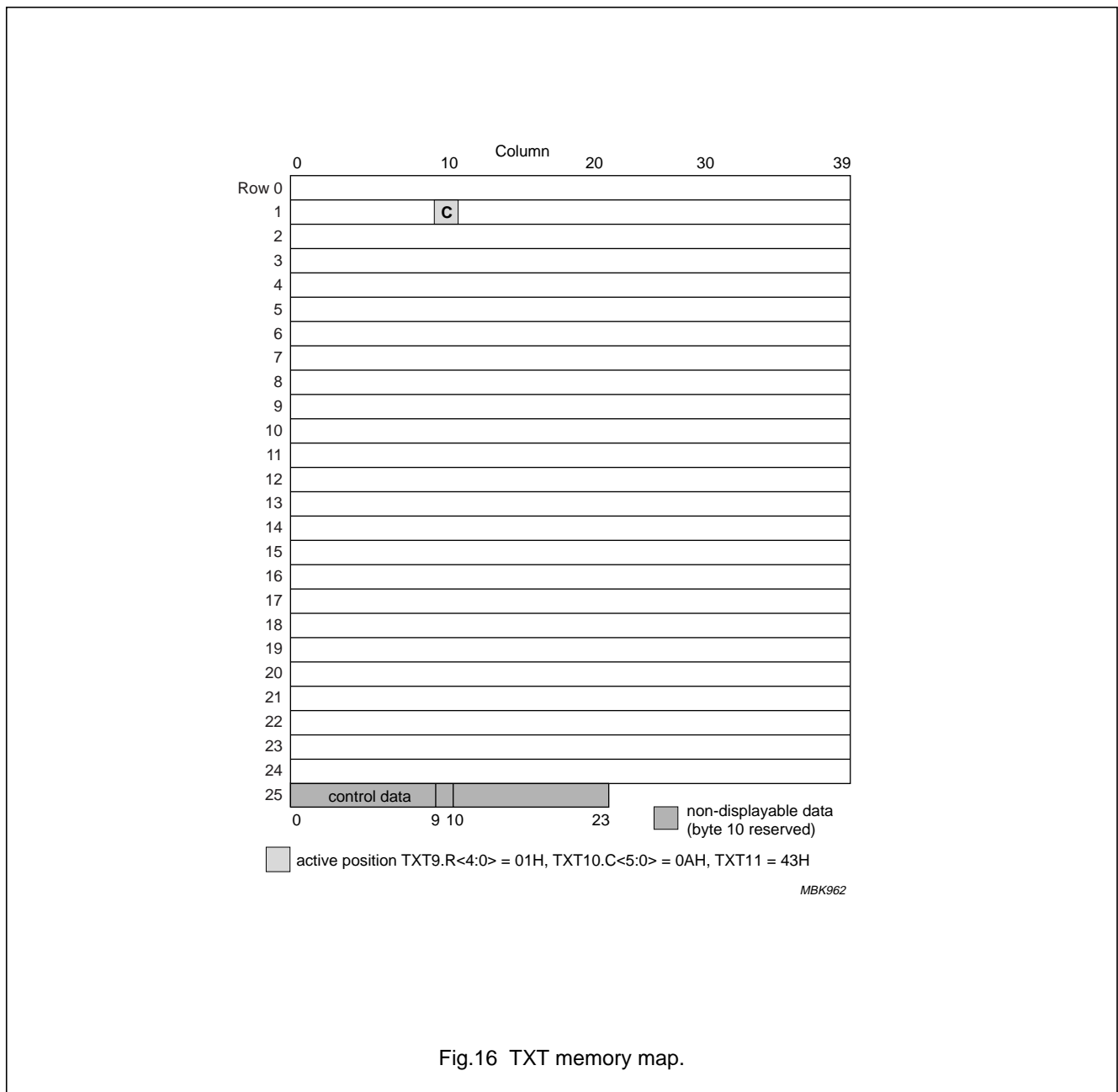


Fig.16 TXT memory map.

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### 21.5 Page clearing

Page clearing is performed on request from the Data Capture section or the microcontroller, under the control of the embedded software.

At power-on and reset, the whole of the page memory is cleared. Bit TXT13.PAGE CLEARING is set while this takes place.

#### 21.5.1 DATA CAPTURE PAGE CLEAR

When a page header is acquired for the first time after a new page request or a page header is acquired with the erase (C4) bit set, the page memory is 'cleared' to spaces before the rest of the page arrives.

When this occurs, the space code (20H) is written into every location of rows 1 to 23 of the basic page memory, the appropriate packet 27 row of the extension packet memory and the row where Teletext packet 24 is written. This last row is either row 24 of the basic page memory (if the TXT0.X24 POSN bit is set) or row 0 of the extension packet memory (if the bit is not set).

Page clearing is done before the end of the TV line in which the header arrived which initiated the page clear. This means that the 1 field gap between the page header and the rest of the page which is necessary for many Teletext decoders is not required.

#### 21.5.2 SOFTWARE PAGE CLEAR

The software can also initiate a page clear by setting bit TXT9.CLEAR MEMORY. Now, every location in the memory block pointed to by TXT15.BLOCK<3:0> is cleared to a space code (20H). Bit CLEAR MEMORY is not latched, so the software does not have to reset it after it has been set.

Only one page can be cleared in a TV line. Therefore, if the software requests a page clear, it will be carried out on the next TV line on which the Data Capture hardware does not force the page to be cleared. A flag (TXT13.PAGE CLEARING) is provided to indicate that a software requested page clear is being carried out. The flag is set when a logic 1 is written to bit TXT9.CLEAR MEMORY and is reset when the page clear has been completed.

All locations are cleared to 00H if bit TXT0.INV ON = 1 and a page clear is initiated on Block 8.

### 21.6 Multi-page operations

When using SAA56xx in a multi-page application with external SRAM, bit TXT28.MULTI PAGE should be set. This allows the 80C51 microcontroller to copy acquired data between internal Display memory and external SRAM without hindrance.

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### 22 DATA CAPTURE

The Data Capture section (see Fig.17) takes in the analog Composite Video and Blanking Signal (CVBS), and extracts the required data from it in the digital domain. The data is then decoded and stored in memory. The first stage converts the analog CVBS signal to digital form, using ADC sampling at 12 MHz. Data and clock recovery is then performed by a Multi-rate Video Input Processor (MulVIP). Next, the following types of data are extracted: WST Teletext (625/525), VPS, Closed Caption (CC) and WSS. The extracted data is stored in either memory (DRAM) via the Memory Interface or in SFR locations.

#### 22.1 Data Capture features

- Two CVBS inputs
- Video Signal Quality detector
- Data Capture for 625-line WST
- Data Capture for 525-line WST
- Data Capture for line 21 data service (Closed Caption)
- Data Capture for VPS data (PDC system A)
- Data Capture for WSS bit decoding
- Automatic selection between 525 WST/625 WST
- Automatic selection between 625 WST/VPS on line 16 of Vertical Blanking Interval (VBI)
- Real-time capture and decoding for WST Teletext in hardware, to enable optimized microprocessor throughput
- Up to 12 pages stored on-chip
- Inventory of transmitted Teletext pages stored in the Transmitted Page Table and Subtitle Page Table
- Automatic detection of Fasttext transmission
- Real-time packet 26 engine in hardware for processing accented, G2 and G3 characters
- Signal quality detector for WST/VPS data types
- Comprehensive Teletext language coverage
- Full-Field and VBI Data Capture of WST data.

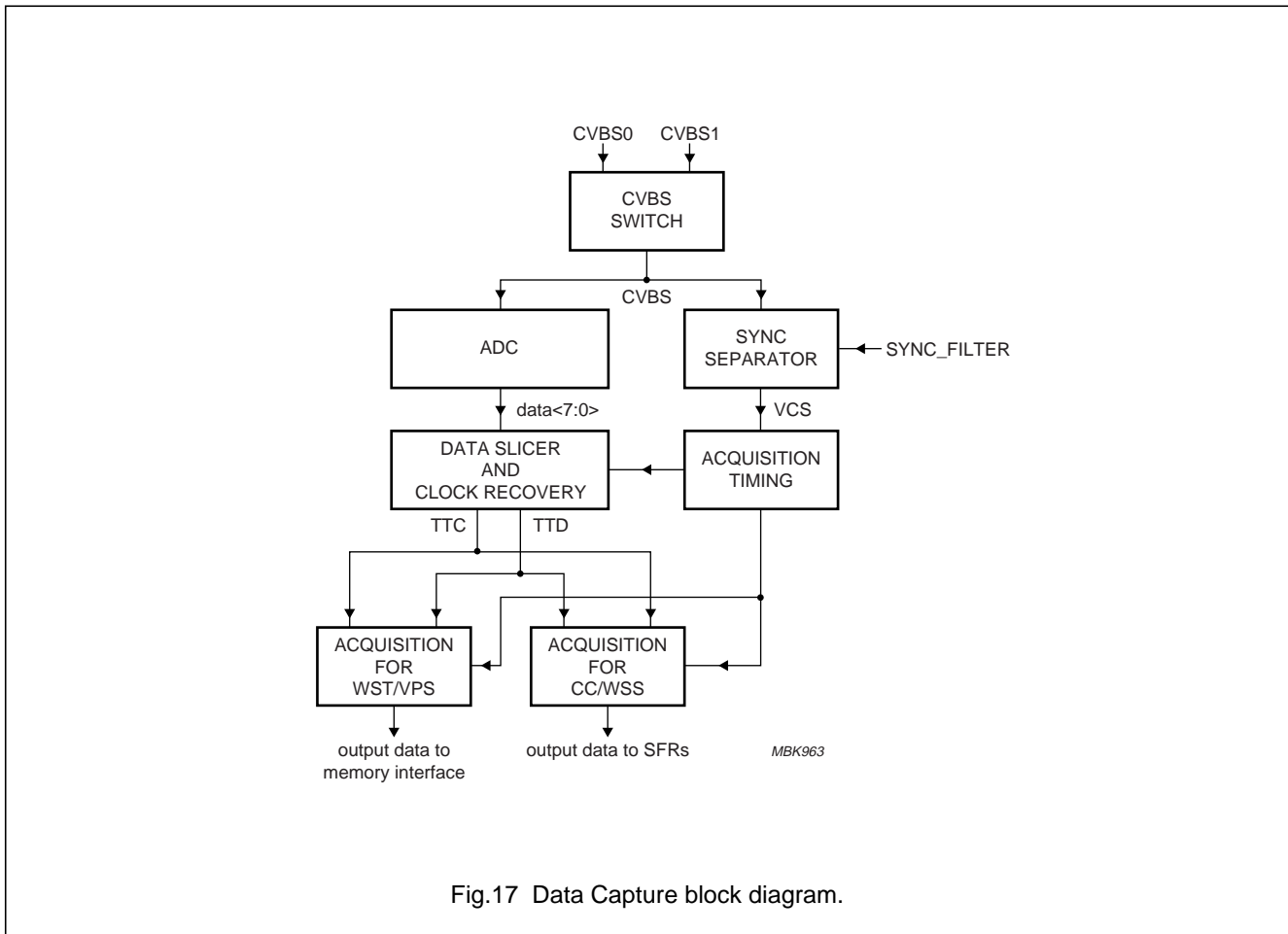


Fig.17 Data Capture block diagram.

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### 22.1.1 CVBS SWITCH

The CVBS switch is used to select the required analog input, depending on the value of TXT8.CVBS1/CVBS0.

### 22.1.2 ANALOG-TO-DIGITAL CONVERTER

The output of the CVBS switch is passed to a Differential-to-Single-Ended Converter (DIVIS, not shown in Fig.17), although here it is used in single-ended configuration with a reference. A full-flash ADC with a sampling rate of 12 MHz converts the analog output of the DIVIS to a digital representation.

### 22.1.3 MULTI-RATE VIDEO INPUT PROCESSOR (MULVIP)

The MulVIP (used for data and clock recovery) is a Digital Signal Processor designed to extract the data and recover the clock from a digitized CVBS signal.

### 22.1.4 DATA STANDARDS AND CLOCK RATES

The data standards and clock rates that can be recovered are shown in Table 22.

**Table 22** Data standards and clock rates

DATA STANDARD	CLOCK RATE
625 WST	6.9375 MHz
525 WST	5.7272 MHz
VPS	5.0 MHz
WSS	5.0 MHz
Closed Caption	500 kHz

### 22.1.5 DATA CAPTURE TIMING

The Data Capture timing section uses the synchronisation information extracted from the CVBS signal to generate the required horizontal and vertical reference timings.

The timing section automatically recognizes and selects the appropriate timings for either 625 (50 Hz) synchronisation or 525 (60 Hz) synchronisation.

A TXT12.VIDEO SIGNAL QUALITY flag is set when the timing section is locked correctly to the incoming CVBS signal. When TXT12.VIDEO SIGNAL QUALITY is set, another flag TXT12.525/625 SYNC can be used to identify the standard.

### 22.1.6 ACQUISITION

The acquisition section extracts the relevant information from the serial stream of data from the MulVIP and stores it in memory.

### 22.1.6.1 Making a page request

A page is requested by writing a series of bytes into the TXT3.PRD<4:0> SFR, which corresponds to the number of the page required. The bytes written into TXT3 are stored in a RAM with an auto-incrementing address. The start address for the RAM is set using the TXT2.SC<2:0> (to define which part of the page request is being written) and TXT2.REQ<3:0> (along with TXT2.ACQ BANK) is used to define which of the 12 page request blocks is being modified.

If TXT2.REQ<3:0> is greater than 09H, then data being written to TXT3 is ignored (applies to Bank 0 and Bank 1).

Table 23 shows the contents of the page request RAM.

Up to 12 pages of Teletext can be acquired on the 12 page device, when TXT1.EXT PKT OFF is set to logic 1, and up to 10 pages can be acquired when this bit is set to logic 0.

**Table 23** The contents of the Page request RAM

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do Care Magazine	HOLD	MAG2	MAG1	MAG0
1	Do Care Page Tens	PT3	PT2	PT1	PT0
2	Do Care Page Units	PU3	PU2	PU1	PU0
3	Do Care Hour Tens	X	X	HT1	HT0
4	Do Care Hours Units	HU3	HU2	HU1	HU0
5	Do Care Minutes Tens	X	MT2	MT1	MT0
6	Do Care Minutes Units	MU3	MU2	MU1	MU0
7	X	X	X	E1	E0

If the 'Do Care' bit for part of the page number is set to logic 0, then that part of the page number is ignored when the Teletext decoder is deciding whether a page being received off-air should be stored or not. For example, if the 'Do Care' bits for the four subcode digits are all set to logic 0, then every subcode version of the page will be captured.



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When bit  $\overline{\text{HOLD}}$  is set to a logic 0, the Teletext decoder will not recognise any page as having the correct page number and no pages will be captured. In addition to providing the user requested hold function, this bit should be used to prevent the inadvertent capture of an unwanted page when a new page request is being made. For example, if the previous page request was for page 100 and this was being changed to page 234, it would be possible to capture page 200 if this arrived after only the requested magazine number had been changed.

Bits E1 and E0 control the error checking, which should be carried out on packets 1 to 23 when the page being requested is captured. This is described in more detail in Section 22.1.6.3.

For a multi-page device, each packet can only be written into one place in the Teletext RAM. Therefore, if a page matches more than one of the page requests, the data is written into the area of memory corresponding to the lowest numbered matching page request.

At power-up, each page request defaults to any page, hold on and error check Mode 0.

### 22.1.6.2 Rolling headers and time

When a new page is requested, it is conventional for the decoder to turn the header row of the display green and to display each page header as it arrives until the correct page is found.

When a page request is changed (i.e. when the TXT3 SFR is written to), a flag (PBLF) is written into bit 5, column 9, row 25 of the corresponding block of the page memory. The state of the flag for each block is updated every TV line 1. If it is set for the current display block, the acquisition section writes all valid page headers that arrive into the display block and automatically writes an alphanumeric green character into column 7 of row 0 of the display block every TV line.

When a requested page header is acquired for the first time, rows 1 to 23 of the relevant memory block are cleared to space, i.e. have 20H written into every column, before the rest of the page arrives. Row 24 is also cleared if bit TXT0.X24 POSN is set. If bit TXT1.EXT PKT OFF is set, the extension packets corresponding to the page are also cleared.

The last eight characters of the page header are used to provide a time display and are always extracted from every valid page header as it arrives and written into the display block.

Bit TXT0.DISABLE HEADER ROLL prevents any data being written into row 0 of the page memory, except when a page is acquired off-air, i.e. rolling headers and time are not written into the memory. Bit TXT1.ACQ OFF prevents any data being written into the memory by the Teletext acquisition section.

When a parallel magazine mode transmission is being received, only headers in the magazine of the page requested are considered valid for the purposes of rolling headers and time. Only one magazine is used even if the Do Care magazine bit is set to logic 0. When a serial magazine mode transmission is being received, all page headers are considered to be valid.

### 22.1.6.3 Error checking

Teletext packets are error checked before they are written into the page memory. The error checking carried out depends on the packet number, the byte number, the error check mode bits in the page request data and bit TXT1.8-BIT (see Fig.18).

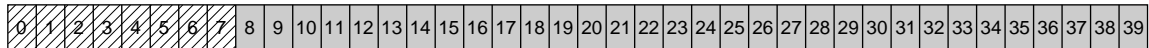
If an uncorrectable error occurs in one of the Hamming checked addressing and control bytes in the page header or in the Hamming checked bytes in packet 8/30, bit 4 of the byte written into the memory is set, to act as an error flag to the software. If uncorrectable errors are detected in any other Hamming checked data, the byte is not written into the memory.

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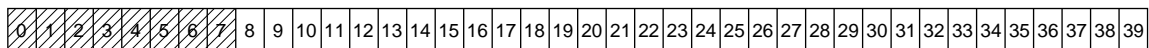
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Packet X/0

'8-bit' bit = 0

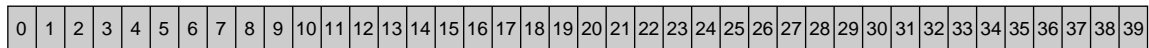


'8-bit' bit = 1

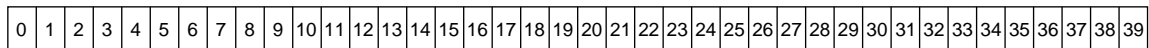


Packet X/1-23

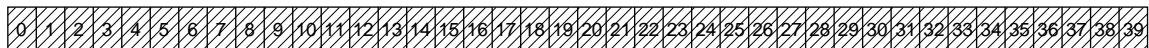
'8-bit' bit = 0, error check mode = 0



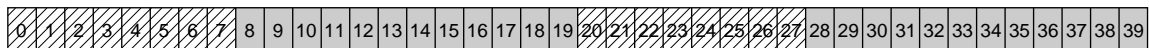
'8-bit' bit = 0, error check mode = 1



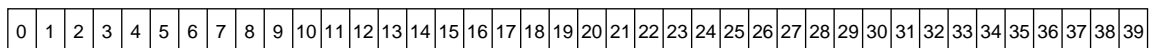
'8-bit' bit = 0, error check mode = 2



'8-bit' bit = 0, error check mode = 3

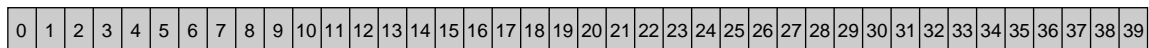


'8-bit' bit = 1

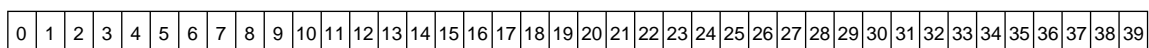


Packet X/24

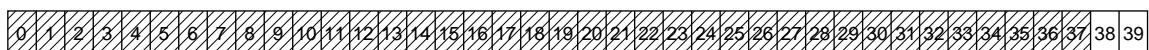
'8-bit' bit = 0



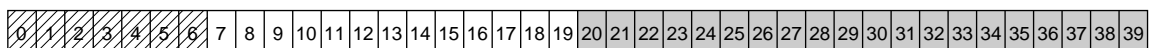
'8-bit' bit = 1



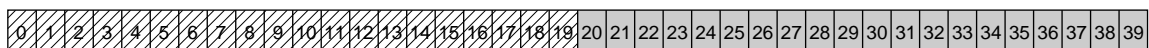
Packet X/27/0



Packet 8/30/0,1



Packet 8/30/2,3,4-15



MGK465

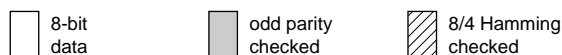
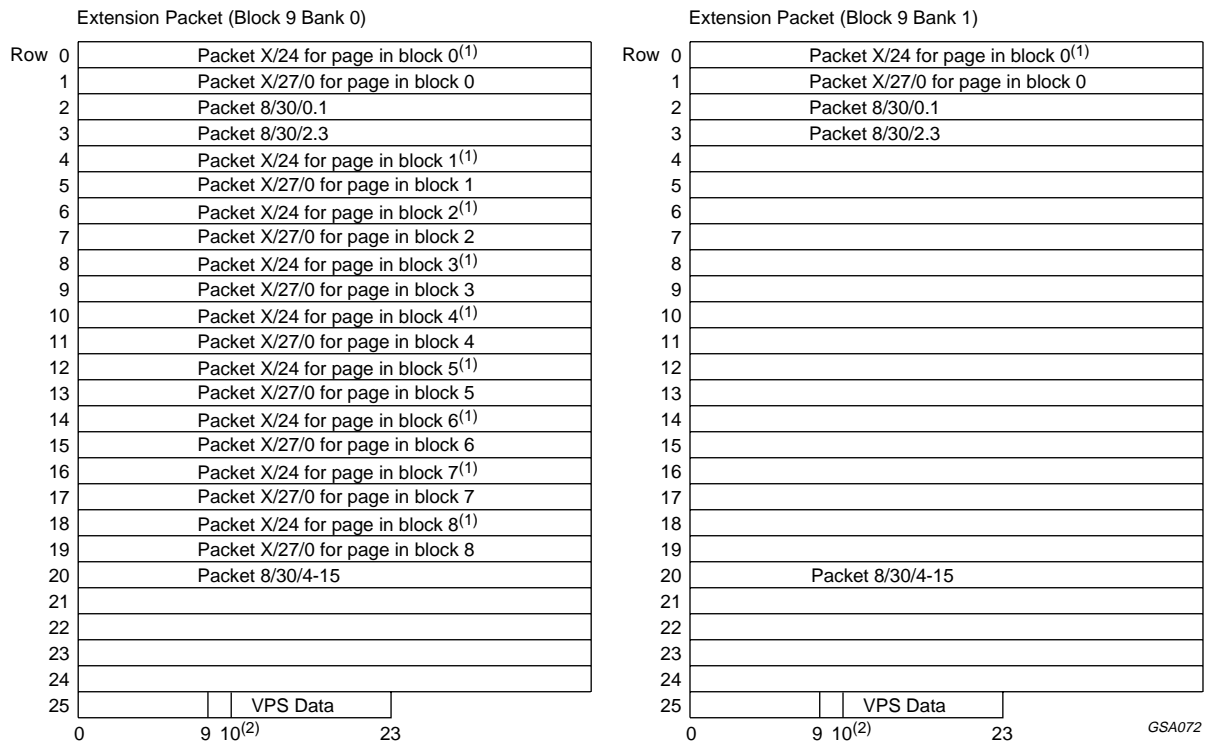


Fig.18 Error checking.



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(1) If 'X24 POSN' bit = 0.  
 (2) Byte 10 reserved.

Fig.20 Extension packet storage locations.

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### 22.1.6.5 Row 25 data contents

The Hamming error flags are set if the on-board 8/4 Hamming checker detects that there has been an uncorrectable (2-bit) error in the associated byte. It is possible for the page to still be acquired if some of the page address information contains uncorrectable errors if that part of the page request was a 'Don't Care'. There is no error flag for the magazine number because an uncorrectable error in this information prevents the page being acquired.

The interrupt sequence (C9) bit is automatically dealt with by the acquisition section, so that rolling headers do not contain a discontinuity in the page number sequence.

The magazine serial bit (C11) indicates whether the magazine transmission is serial or parallel. This affects how the acquisition section operates and is dealt with automatically.

The newsflash (C5), subtitle (C6), suppress header (C7), inhibit display (C10) and language control (C12 to 14) bits are dealt with automatically by the display section.

The update bit (C8) has no effect on the hardware. The remaining 32 bytes of the page header are parity checked and written into columns 8 to 39 of row 0. Bytes that pass the parity check have the MSB set to a logic 0 and are written into page memory. Bytes with parity errors are not written into the memory.

**Table 24** The data in row 25 of the basic page memory

COL	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	Hamming error	PU3	PU2	PU1	PU0
1	0	0	0	Hamming error	PT3	PT2	PT1	PT0
2	0	0	0	Hamming error	MU3	MU2	MU1	MU0
3	0	0	0	Hamming error	C4	MT2	MT1	MT0
4	0	0	0	Hamming error	HU3	HU2	HU1	HU0
5	0	0	0	Hamming error	C6	C5	HT1	HT0
6	0	0	0	Hamming error	C10	C9	C8	C7
7	0	0	0	Hamming error	C14	C13	C12	C11
8	0	0	0	$\overline{\text{FOUND}}$	0	MAG2	MAG1	MAG0
9	0	0	PBLF	0	0	0	0	0
10 to 23	–	–	–	unused	–	–	–	–

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### 22.1.6.6 Inventory page

If bit TXT0.INV ON is a logic 1, memory block 8 of Bank 0 is used as an inventory page. This consists of two tables: the Transmitted Page Table (TPT) and the Subtitle Page Table (SPT); see Fig.21.

In each table, every possible combination of the page tens and units digit, 00H to FFH, is represented by a byte, see Fig.22. Each bit of these bytes corresponds to a magazine number so each page number, from 100H to 8FFH, is represented by a bit in the table.

The bit for a particular page in the TPT is set when a page header is received for that page. The bit in the SPT is set when a page header for the page is received which has the 'subtitle' page header control bit (C6) set. The bit for a particular page in the TPT is set when a page header is received for that page. The bit in the SPT is set when a page header for the page is received which has the 'subtitle' page header control bit (C6) set.

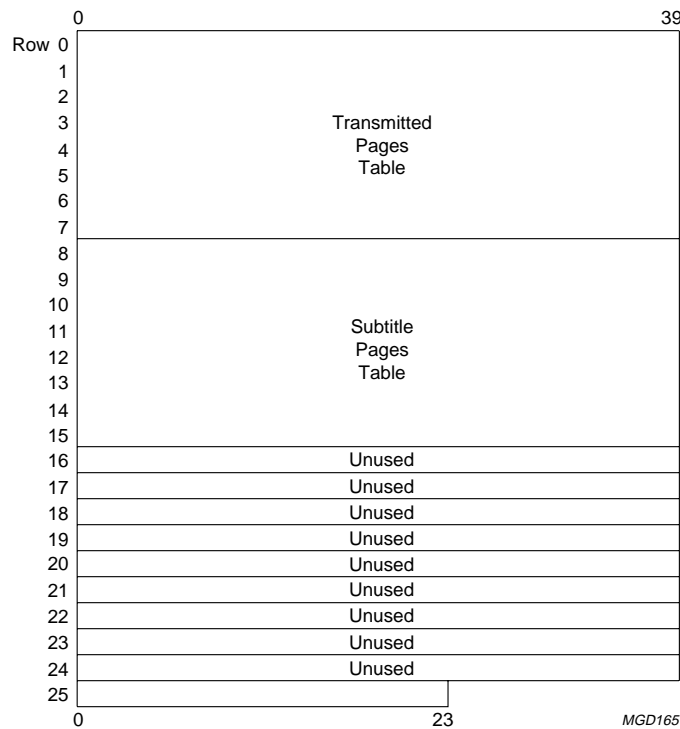


Fig.21 Inventory page organisation.



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The tabulation bit is also used with extension packets.

The first eight data bytes of packet X/1/24 are used to extend the Fastext prompt row to 40 characters. These characters are written into whichever part of the memory the packet 24 is being written into (determined by the 'X24 POSN' bit).

Packets X/0/27/0 contain five Fastext page links and the link control byte. They are captured, Hamming checked and stored in the same way as are packets X/27/0 in 625-line text. Packets X/1/27/0 are not captured.

Because there are only two magazine bits in 525-line text, packets with the magazine bits all set to a logic 0 are referred to as being in magazine 4. Therefore, the broadcast service data packet is packet 4/30, rather than packet 8/30.

As in 625-line text, the first 20 bytes of packet 4/30 contain encoded data that is decoded in the same way as in packet 8/30. The last 12 bytes of the packet contains half of the parity encoded status message. Packet 4/0/30 contains the first half of the message and packet 4/1/30 contains the second half. The last four bytes of the message are not written into memory. The first 20 bytes of the each version of the packet are the same, so they are stored whenever either version of the packet is acquired.

In 525-line text, each packet 26 only contains ten 24/18 Hamming encoded data triplets, rather than the 13 found in 625-line text. The tabulation bit is used as an extra bit (the MSB) of the designation code, allowing 32 packet 26s to be transmitted for each page. The last byte of each packet 26 is ignored.

	0	6 7 8		39
Row 0	OSD only	aw/ag	Packet X/0/0	Rolling time
1			Packet X/0/1	Packet X/1/1
2			Packet X/0/2	
3			Packet X/0/3	
4			Packet X/0/4	Packet X/1/4
5			Packet X/0/5	
6			Packet X/0/6	
7			Packet X/0/7	
8			Packet X/0/8	Packet X/1/8
9			Packet X/0/9	
10			Packet X/0/10	
11			Packet X/0/11	
12			Packet X/0/12	Packet X/1/12
13			Packet X/0/13	
14			Packet X/0/14	
15			Packet X/0/15	
16			Packet X/0/16	Packet X/1/16
17			Packet X/0/17	
18			Packet X/0/18	
19			Packet X/0/19	
20			Packet X/0/20	Packet X/1/20
21			Packet X/0/21	
22			Packet X/0/22	
23			Packet X/0/23	
24			Packet X/0/24 <sup>(1)</sup>	Packet X/1 /24 <sup>(1)</sup>
25	Control Data			
	0	9 10 <sup>(2)</sup>	23	GSA004

(1) If X24 POSN bit = 1.  
 (2) Byte 10 reserved.

Fig.23 Packet storage locations, 525-line.



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### 22.1.6.9 Fasttext detection

When a packet 27, designation code 0 is detected, whether or not it is acquired, bit TXT13.FASTTEXT is set. If the device is receiving 525-line Teletext, a packet X/0/27/0 is required to set the flag. The flag can be reset by writing a logic 0 into the SFR bit.

When a packet 8/30 is detected (or a packet 4/30 when the device is receiving a 525-line transmission), flag TXT13.PKT 8/30 is set. The flag can be reset by writing a logic 0 into the SFR bit.

### 22.1.6.10 Broadcast Service Data Detection

When a packet 8/30 is detected (or a packet 4/30 when the device is receiving a 525-line transmission), flag TXT13. PKT 8/30 is set. The flag can be reset by writing a logic 0 into the SFR bit.

### 22.1.6.11 VPS acquisition

When bit TXT0.VPS ON is set, any VPS data present on line 16, field 0 of the CVBS signal at the input of the Teletext decoder is error checked and stored in row 25, block 9 of the basic page memory, see Fig.24. The device automatically detects whether Teletext or VPS is being transmitted on this line and decodes the data appropriately.

Each VPS byte in the memory consists of four biphasic decoded data bits (bits 0 to 3), a biphasic error flag (bit 4) and three logic 0s (bits 5 to 7).

The most significant bit of the VPS data cannot be set to logic 1.

Bit TXT13.VPS Received is set by the hardware whenever VPS data is acquired.

Full details of the VPS system can be found in the specification *“Domestic Video Program Delivery Control System (PDC); EBU Tech. 3262-E”*.

### 22.1.7 WST ACQUISITION

The SAA56xx family is capable of acquiring Level 1.5 625-line and 525-line World System Teletext.

### 22.1.8 WSS ACQUISITION

The WSS data transmitted on line 23 gives information on the aspect ratio and display position of the transmitted picture, the position of subtitles and on the camera/film mode. Some additional bits are reserved for future use. A total of 14 data bits are transmitted.

All of the available data bits transmitted by the WSS signal are captured and stored in SFRs WSS1, WSS2 and WSS3. The bits are stored as groups of related bits and an error flag is provided for each group to indicate when a transmission error has been detected in one or more of the bits in the group.

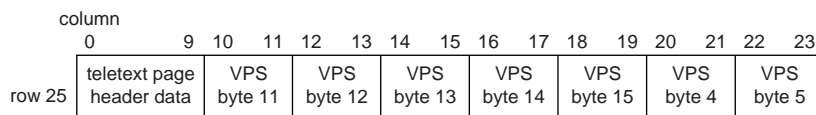
WSS data is only acquired when the TXT8.WSS ON bit is set. Bit TXT8.WSS RECEIVED is set by the hardware whenever WSS data is acquired. The flag can be reset by writing a logic 0 into the SFR bit.

### 22.1.9 CLOSED CAPTION ACQUISITION

The US Closed Caption data is transmitted on line 21 (525-line timings) and is used for Captioning information, Text information and Extended Data Services. Full details can be found in the document *“Recommended Practise for Line 21 Data Service EIA-608”*. Closed Caption data is only acquired when bit TXT21.CC ON is set.

Two bytes of data are stored per field in SFRs. The first byte is stored in CCDAT1 and the second byte is stored in CCDAT2. The value in the CCDAT registers is reset to 00H at the start of the Closed Caption line defined by CCLIN.CS<4:0>. At the end of the Closed Caption line, an interrupt is generated if IEN0.ECC is active.

The Closed Caption data is software-processed to convert it into a displayable format.



MBK964

Fig.24 VPS data storage.

# Enhanced TV microcontrollers with On-Screen Display (OSD)

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### 23 DISPLAY

The display section (see Fig.25) is based on the requirements for a Level 1.5 WST Teletext and US Closed Caption. There are some enhancements for use with locally generated on-screen displays.

The display section reads the contents of the Display memory and interprets the control/character codes. From this information and other global settings, the display produces the required RGB signals and Video/Data (Fast Blanking) signal for a TV signal processing device.

The display is synchronized to the TV signal processing device by horizontal and vertical sync signals from external circuits (Slave Sync mode). All display timings are derived from these signals.

The SAA56xx display section incorporates a number of enhancements over the rest of the SAA55xx family, including 100 Hz (2H/2V only) operation, two page mode (50/60 Hz only), increased DRCS/Special Graphics and a larger Character ROM.

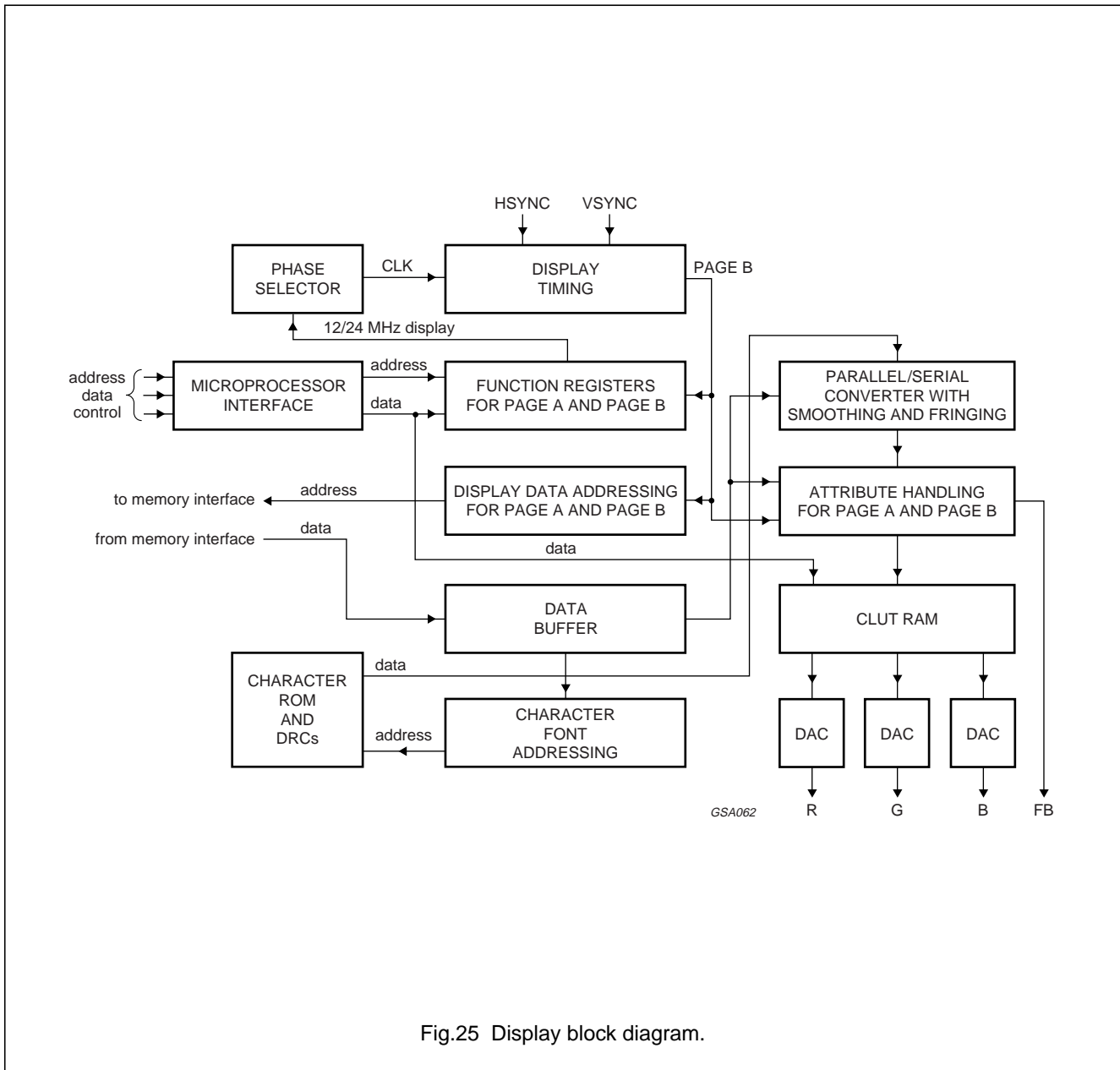


Fig.25 Display block diagram.

## Enhanced TV microcontrollers with On-Screen Display (OSD)

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### 23.1 Display features

- Teletext and Enhanced OSD modes
- Level 1.5 WST features
- US Closed Caption features
- 50/60 Hz or 100/120 Hz display timing modes
- Two page operation (50/60 Hz only)
- Serial and parallel display attributes
- Single/double/quadruple width and height for characters
- Smoothing capability of double size, double width, double height and quadruple size characters
- Scrolling of display region
- Variable flash rate controlled by software
- Globally selectable scan lines per row 9/10/13/16
- Globally selectable character matrix (H × V) 12 × 9, 12 × 10, 12 × 13 and 12 × 16
- Italics
- Soft colours using CLUT with 4096 colour palette
- Underline
- Overline
- Fringing (shadow) selectable from N-S-E-W direction
- Fringe colour selectable
- Meshing of defined area
- Contrast reduction of defined area (both CC and Teletext display modes)
- Cursor
- Special graphics characters with two planes, allowing four colours per character
- 64 dynamically redefinable characters for OSDs
- Up to 4 WST character sets (G0/G2) user programmable in a single device (e.g. Latin, Cyrillic, Greek and Arabic)
- G1 Mosaic graphics, Limited G3 Line drawing characters
- WST character sets and Closed Caption character set user programmable in a single device.

### 23.2 Display modes

The display section has two distinct modes with different features available in each:

- **TXT:** This is the WST mode with additional serial and global attributes. A TXT window is configured as a fixed 25 rows with 40 characters per row.
- **CC:** This is the US Closed Caption mode. A CC window is configured as a maximum of 16 rows with a maximum of 48 characters per row.

In both of the above modes, the character matrix and TV lines per row can be defined. There is an option of a character matrix (H × V) of 12 × 9, 12 × 10, 12 × 13, or 12 × 16, which have 9, 10, 13 and 16 TV lines per display row, respectively.

Table 25 gives the possible number of display rows for each combination, as allowed by the hardware.

**Table 25** Maximum number of display rows

CHARACTER MATRIX	MAX NUMBER OF DISPLAY ROWS		
	TXT 625	TXT 525	CC
12 x 9	25	25	16
12 x 10	25	23	16
12 x 13	21	18	16
12 x 16	17	14	14

SFR TXT21 and memory mapped registers are used to control the mode selection. The features will now be described and their function in each of the modes given. If the feature is different in either mode then this is stated.

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### 23.2.1 FEATURES AVAILABLE AND CHARACTERS IN EACH MODE

Table 26 shows a list of features available in each mode, and also if the setting is a serial/parallel attribute, or has a global effect on all the display.

**Table 26** Display features and characters in each mode

FEATURE	TXT	CC
Flash	serial	serial
Boxes	TXT/OSD (serial)	serial
Horizontal size	×1, ×2 or ×4 (serial)	×1 or ×2 (serial)
Vertical size	×1 or ×2 (serial); ×4 (global)	×1 or ×2 (serial)
Italic	n/a	serial
Foreground colours	8 (serial)	8 + 8 (parallel)
Background colours	8 (serial)	16 (serial)
Soft colours (CLUT)	16 from 4096	16 from 4096
Underline	n/a	serial
Overline	n/a	serial
Fringe	N + S + E + W	N + S + E + W
Fringe colour	16 (global)	16 (serial)
Meshing of background	black or colour (global)	all (global)
Fast Blanking Polarity	yes	yes
Screen colour	16 (global)	16 (global)
DRCS	64 (global)	64 (global)
Character matrix (H × V)	12 × 9, 12 × 10, 12 × 13 or 12 × 16	12 × 9, 12 × 10, 12 × 13 or 12 × 16
Number of rows	25	16
Number of columns	40	48
Number of characters displayable	1 000	768
Cursor	yes	yes
Special graphics (2 planes per character)	32	32 (default), 128 if extended special graphics on
Scroll	no	yes
Smoothing	yes (global)	yes (global)
Contrast reduction	yes (global)	yes (serial)

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### 23.3 Display timing modes

The display can be configured for either 50/60 Hz or 100/120 Hz (2H/2V only) using the display configuration MMR 87FFH.

**Table 27** Display timing modes

DISPLAY TIMING (MMR 87FFH)		SUPPORTED HSYNC/VSYNC RATE	DISPLAY CLOCK	NUMBER OF CHARACTERS
100 HZ BIT	TWO_PAGE BIT			
0	0	1H/1V	12 MHz	40 (single window)
X	1	1H/1V	24 MHz	80 (double window)
1	0	1H/1V; 2H/2V	24 MHz	40 (single window)

#### 23.3.1 DOUBLE WINDOW OPERATION

This mode enables two different pages to be displayed side-by-side for use with 16:9 TV screens. The display section clock runs at 24 MHz in this mode. Fig.26 shows the combination of two page display possible on the SAA56xx device.

Two page mode is selected using MMR 87FFH bit 0. The two pages displayed are separated by two character spaces to allow the display logic to switch correctly from one window to the other. The facility is restricted to 1H/1V (i.e. 50/60Hz display TVs).

Two control bits exist in double window mode to select Closed Caption display or text display in each window: TXT21.CC/TXT for Page A and TXT28.CC\_TXT B for Page B.

**TXT:** When displaying two Teletext pages side by side, the memory block being displayed in Page A is selected using SFR TXT14<3:0> and for Page B using SFR TXT28<3:0>.

The Data Capture section writes the header and time information only to the memory block corresponding to the active page. This active page is determined with the TXT28.ACTIVE PAGE bit. When set to logic 0, Page A is active, set to logic 1, Page B is active.

Operation of the REVEAL bit (TXT7.5) and CURSOR ON bit (TXT7.6) only affects the active page.

**CC:** When CC display mode is selected in two page mode, only one window may be used for CC/OSD and the other either Text or Video. Two page CC display (either captions or OSD) side-by-side is not possible because there is only one area of memory available for the CC data.

#### 23.3.2 SINGLE WINDOW OPERATION

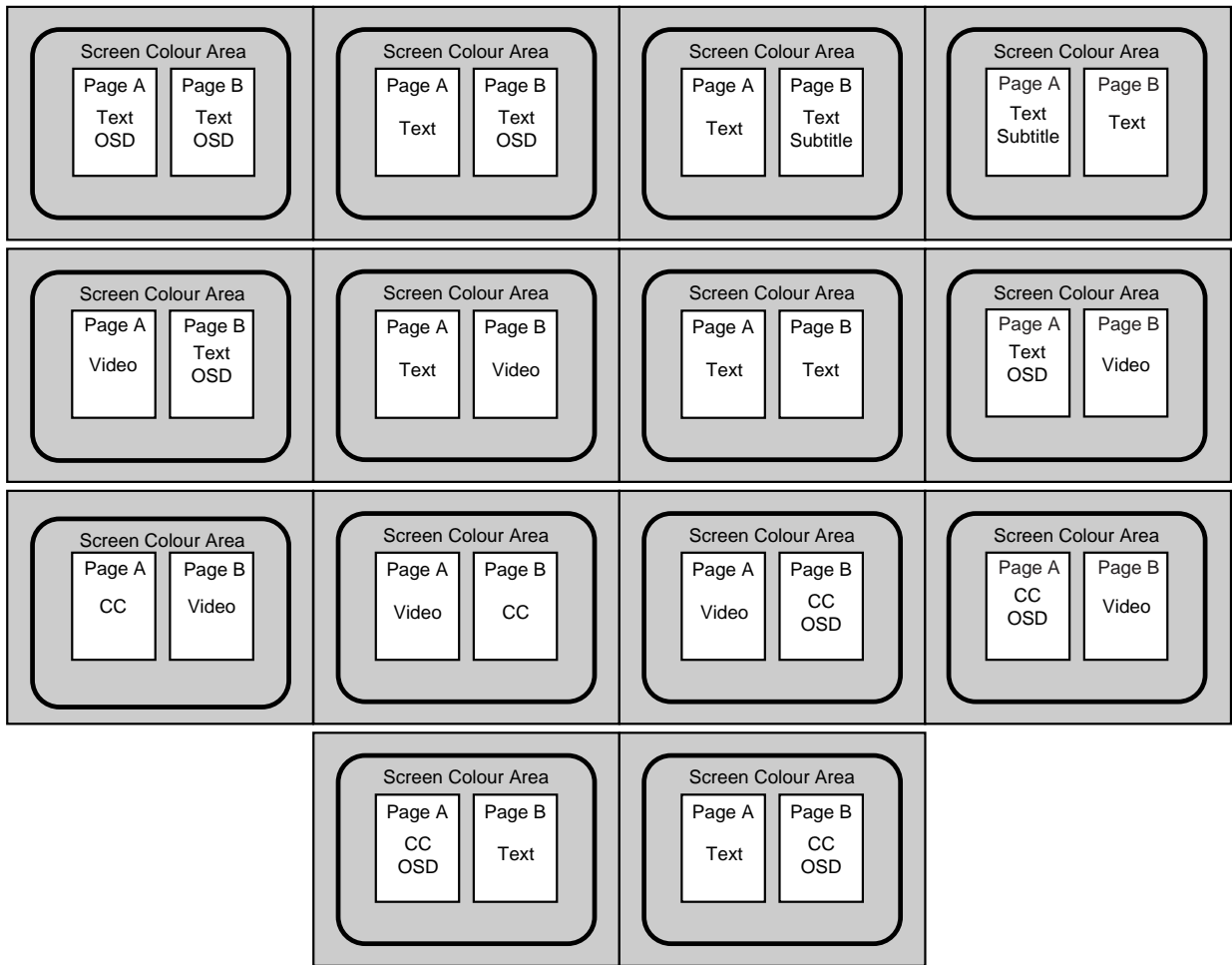
At reset, the device defaults to single window mode, which corresponds to 87FFH bit 0 set to logic 0. In this mode, the settings applying to the window displayed are those that would apply to Page A in double window mode.

For 2H/2V display TVs, the 100 Hz bit, MMR 87FFH bit 1, must be set to logic 1 to fit a whole display window.

For 1H/1V display TVs, when MMR 87FFH bit 1 is set to logic 0, the display window occupies the whole screen, whereas if MMR 87FFH bit 1 is set to logic 1, only half the screen would be occupied by the display window. This latter configuration would give the same kind of display as in the double window mode with Page A: CC or Text Page B: Video.

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GSA077

Fig.26 Two-page Text/CC/video combinations.

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### 23.4 Display feature descriptions

All display features are now described in detail for both TXT and CC modes.

#### 23.4.1 FLASH

Flashing causes the foreground colour pixels to be displayed as the background pixels. The flash frequency is controlled by software setting and resetting the MMR Status (see Table 41) at the appropriate interval.

**CC:** This attribute is valid from the time set (see Table 33) until the end of the row of a display window, or until otherwise modified.

**TXT:** This attribute is set by the control character 'flash' (08H) (see Fig.35) and remains valid until the end of a row of a display window, or until reset by the control character 'steady' (09H).

#### 23.4.2 BOXES

**CC:** This attribute is valid from the time set until the end of a row of a display window, or otherwise modified if set with Serial Mode 0. If set with Serial Mode 1, then it is set from the next character onwards.

In text mode (within CC mode), the background colour is displayed regardless of the setting of the box attribute bit. Boxes take effect only during mixed mode. Where boxes are set in this mode, the background colour is displayed. Character locations where boxes are not set show video/screen colour (depending on the setting in the MMR Display Control) instead of the background colour.

**TXT:** Two types of boxes exist: the Teletext box and the OSD box. The Teletext box is activated by the 'start box' control character (0BH). Two start box characters are required to begin a Teletext box, with the box starting between the two characters. The box ends at the end of the line or after an 'end box' control character.

TXT mode can also use OSD boxes, which are started using size implying OSD control characters (BCH/BDH/BEH/BFH). The box starts after the control character (set after) and ends either at the end of a row of a display window, or at the next size implying OSD character (set at).

The attributes flash, Teletext box, conceal, separate graphics, twist and hold graphics are all reset at the start of an OSD box, as they are at the start of the row.

OSD boxes are only valid in TV mode, which is defined by TXT5 = 03H and TXT6 = 03H.

#### 23.4.3 SIZE

The size of the characters can be modified in both the horizontal and vertical directions.

**CC:** Two sizes are available in both the horizontal and vertical directions. The sizes available are normal ( $\times 1$ ), double ( $\times 2$ ) height/width and any combination of these. The attribute setting is always valid for the whole row of a display window. Mixing of sizes within a row is not possible.

**TXT:** Three horizontal sizes are available: normal ( $\times 1$ ), double ( $\times 2$ ), quadruple ( $\times 4$ ). The control characters 'normal size' (0CH/BCH) enable normal size. The 'double width' or double size (0EH/BEH/0FH/BFH) control characters enable double width characters.

Any two consecutive combinations of 'double width' or 'double size' (0EH/BEH/0FH/BFH) control characters activate quadruple width characters, provided quadruple width characters are enabled by TXT4.QUAD WIDTH ENABLE.

Three vertical sizes are available normal ( $\times 1$ ), double ( $\times 2$ ) and quadruple ( $\times 4$ ). The control characters 'normal size' (0CH/BCH) enable normal size, the 'double height' or 'double size' (0DH/BDH/0FH/BFH) enable double height characters. Quadruple height characters are achieved by using double height characters and setting the global attributes TXT7.DOUBLE HEIGHT (expand) and TXT7.BOTTOM/TOP.

If double height characters are used in Teletext mode, single height characters in the lower row of the double height character are automatically disabled.

#### 23.4.4 ITALIC

**CC:** This attribute is valid from the time set until the end of a row of a display window, or otherwise modified. The attribute causes the character foreground pixels to be offset horizontally by 1 pixel per 4 scan lines (interlaced mode). The base is the bottom left character matrix pixel. The pattern of the character is indented, as shown in Fig.27.

**TXT:** The Italic attribute is not available.

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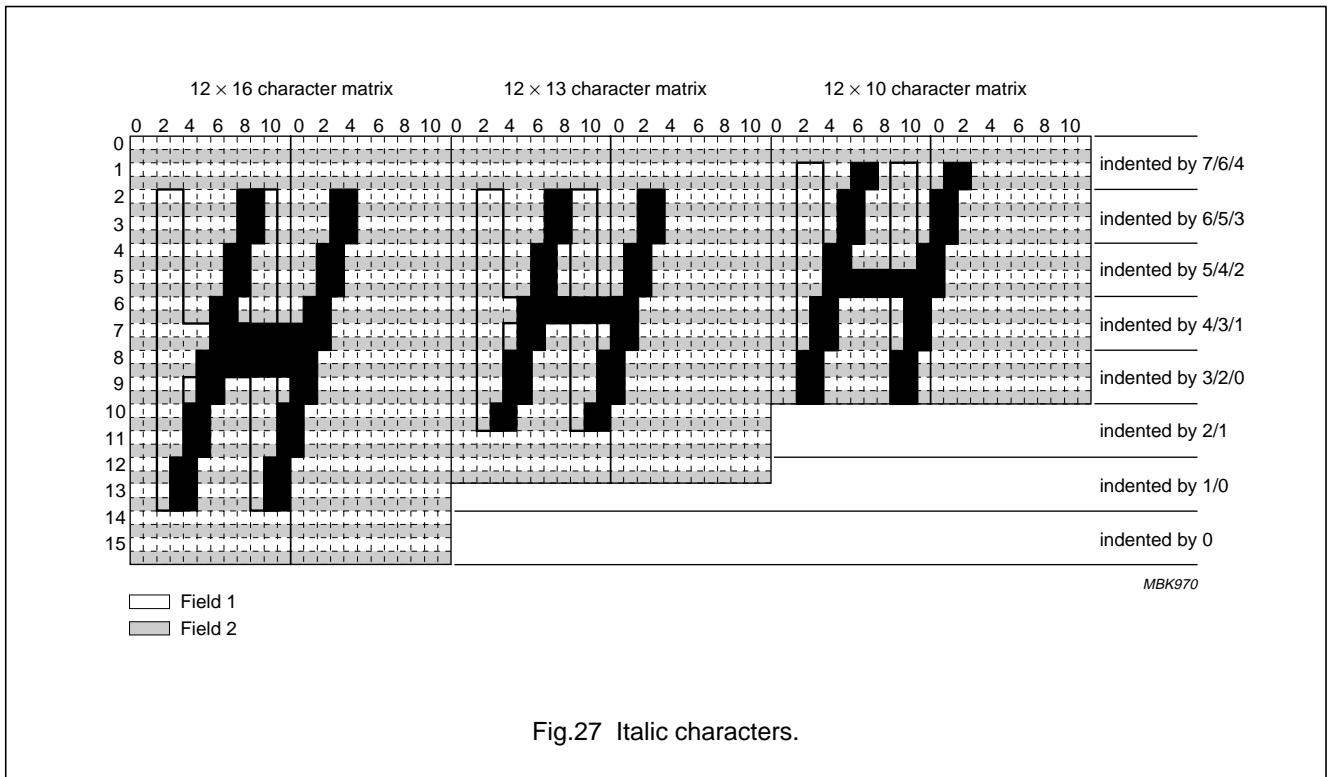


Fig.27 Italic characters.

### 23.4.5 COLOURS

A Colour Look-Up Table (CLUT) with 16 colour entries is provided. The colours can be programmed from a palette of 4096 (4 bits per R, G and B), as shown in Table 28. The CLUT is defined by writing data to a RAM that resides in the MOVX address space of the 80C51. When set, the colours are global and apply to all display windows.

Table 28 CLUT colour values

RED<3:0> (B11 TO B8)	GREEN<3:0> (B7 TO B4)	BLUE<3:0> (B3 TO B0)	COLOUR ENTRY
0000	0000	0000	0
0000	0000	1111	1
...	...	...	...
1111	1111	0000	14
1111	1111	1111	15

### 23.4.6 FOREGROUND COLOUR

**CC:** The foreground colour can be chosen from eight colours on a character by character basis. Two sets of eight colours are provided. A serial attribute switches between the banks (see Table 33 Serial Mode 1, bit 7). The colours are the CLUT entries 0 to 7 or 8 to 15.

**TXT:** The foreground colour is selected via a control character (see Fig.33). The colour control characters takes effect at the start of the next character ('set after') and remain valid until the end of a row of a display window, or until modified by a control character. Only eight foreground colours are available.

The TEXT foreground control characters map to the CLUT entries, as shown in Table 29.

Table 29 Foreground CLUT mapping

CONTROL CODE	DEFINED COLOUR	CLUT ENTRY
00H	black	0
01H	red	1
02H	green	2
03H	yellow	3
04H	blue	4
05H	magenta	5
06H	cyan	6
07H	white	7



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### 23.4.7 BACKGROUND COLOUR

**CC:** This attribute is valid from the time set until the end of a row of a display window, or otherwise modified if set with Serial Mode 0. If set with Serial Mode 1, then the colour is set from the next character onwards.

The background colour can be chosen from all 16 CLUT entries.

**TXT:** The control character 'New background' (1DH) is used to change the background colour to the current foreground colour. The selection is immediate (set at) and remains valid until the end of a row of a display window, or until otherwise modified.

The TEXT background control characters map to the CLUT entries, as shown in Table 30.

**Table 30** Background CLUT mapping

CONTROL CODE	DEFINED COLOUR	CLUT ENTRY
00H + 1DH	black	8
01H + 1DH	red	9
02H + 1DH	green	10
03H + 1DH	yellow	11
04H + 1DH	blue	12
05H + 1DH	magenta	13
06H + 1DH	cyan	14
07H + 1DH	white	15

### 23.4.8 BACKGROUND DURATION

When set, the attribute takes effect from the current position until the end of the display window. This is defined in the MMR Text Area End in single window mode and in double window mode for Page A, with MMR Text Area End B for Page B.

**CC:** The background duration attribute (see Table 33, bit 8) in combination with the End Of Row attribute (see Table 33, bit 9) forces the background colour to be displayed on the row until the end of the text area is reached.

**TXT:** This attribute is not available.

### 23.4.9 UNDERLINE

The underline attribute causes the characters to have the bottom scan line of the character cell forced to foreground colour, including spaces. If background duration is set, then underline is set until the end of the display window.

**CC:** The underline attribute (see Table 33, bit 4) is valid from the time set until the end of row of a display window, or otherwise modified.

**TXT:** This attribute is not available.

### 23.4.10 OVERLINE

The overline attribute causes the characters to have the top scan line of the character cell forced to foreground colour, including spaces. If background duration is set, then overline is set until the end of the display window.

**CC:** The overline attribute (see Table 33, bit 5) is valid from the time set until the end of a row of a display window, or otherwise modified. Overlining of italic characters is not possible.

**TXT:** This attribute is not available.

### 23.4.11 END OF ROW

**CC:** The number of characters in a row is flexible and can be determined by the end of row attribute (see Table 33, bit 9). However, the maximum number of character positions displayed is determined by the setting of the MMR Text Area Start or Text Area Start B, and MMR Text Area End or Text Area End B.

Note that, when using the end of row attribute, the next character location after the attribute should always be occupied by a 'space'.

**TXT:** This attribute is not available, the row length is fixed at 40 characters.

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### 23.4.12 FRINGING

A fringe (shadow) can be defined around characters. The fringe direction is individually selectable in any of the North, South, East and West directions using the MMR Fringing Control.

The colour of the fringe can also be defined as one of the entries in the CLUT, again using MMR Fringing Control. An example of fringing is shown in Fig.28.

**CC:** The fringe attribute (see Table 33, bit 9) is valid from the time set until the end of a row of a display window, or otherwise modified.

**TXT:** Bit TXT4.SHADOW ENABLE controls the display of fringing in single page mode and in double Page A. Bit TXT26.SHADOW ENABLE B controls the display of fringing for Page B in double window mode.

When set, all the alphanumeric characters being displayed are shadowed, graphics characters are not shadowed.

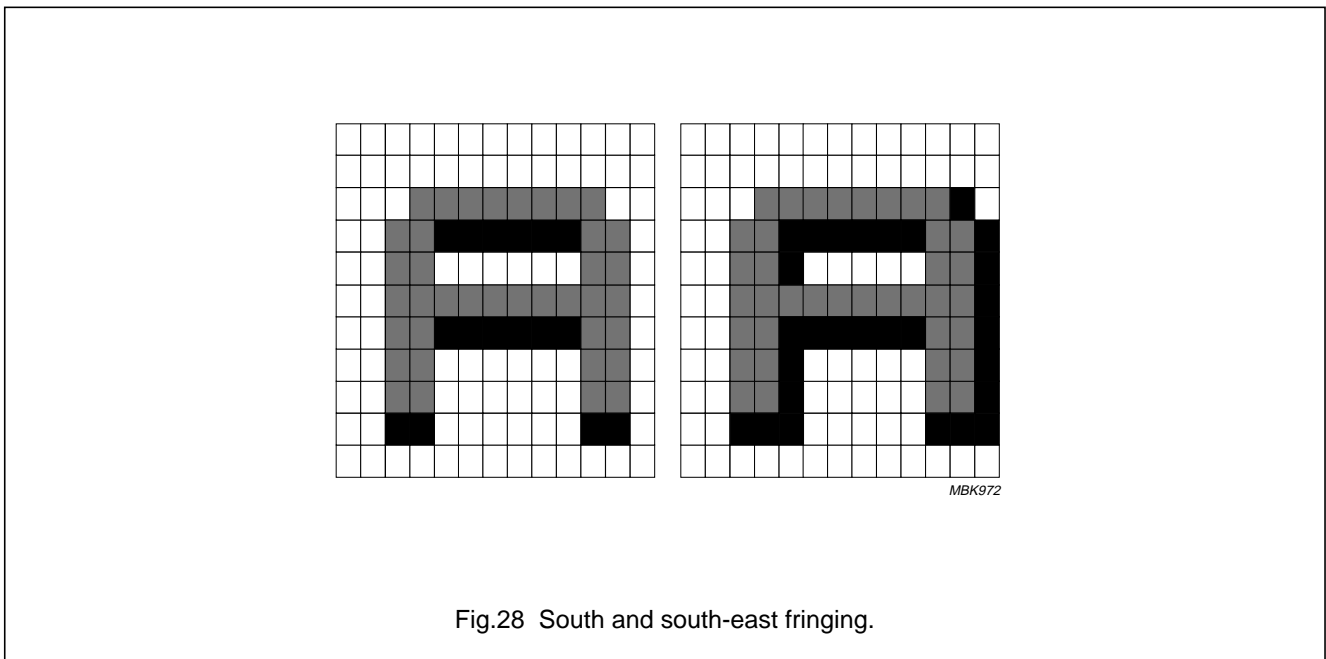


Fig.28 South and south-east fringing.

### 23.4.13 MESHING

This attribute affects the background colour being displayed. Alternate pixels are displayed as the background colour or video. The structure is offset by one pixel from scan line to scan line, thus achieving a checker board display of the background colour and video. An example of meshing and meshing/fringing is shown in Fig.29.

**CC:** The setting of the MSH bit in MMR Display Control has the effect of meshing any background colour.

**TXT:** There are two meshing attributes. One only affects black background colours TXT4.B MESH ENABLE in single window mode or in double window mode for Page A, and TXT26.B MESH ENABLE B for Page B. A second only affects backgrounds other than black TXT4.C MESH ENABLE in single window mode or in double window mode for Page A, and TXT26.C MESH ENABLE B for Page B. A black background is defined as CLUT entry 8, a non-black background is defined as CLUT entry 9 to 15.

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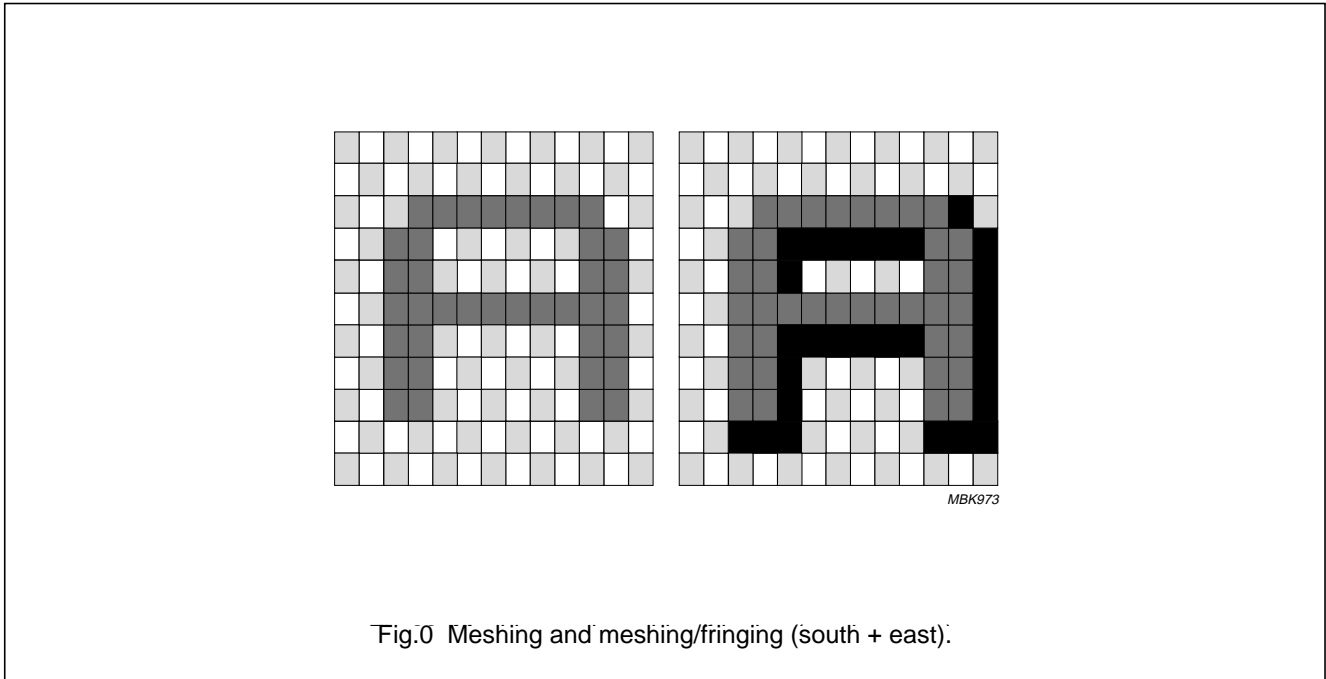


Fig.0 Meshing and meshing/fringing (south + east).

23.4.14 CURSOR

The cursor operates by reversing the background (see Fig.30) and foreground colours in the character position pointed to by the current cursor position in the active page.

The cursor is enabled using TXT7.CURSOR ON. When set, the row on which the cursor appears is defined by TXT9.R<4:0>; the column is defined by TXT10.C<5:0>.

The active page is defined by TXT28.ACTIVE PAGE in double window mode and the displayed window is in single window mode. The position of the cursor can be fixed using TXT9.CURSOR FREEZE.

**CC:** The valid range for row is 0 to 15. The valid range for column is 0 to 47. The cursor remains rectangular at all times, its shape is not affected by italic attribute, therefore it is not advised to use the cursor with italic characters.

**TXT:** The valid range for row positioning is 0 to 24. The valid range for column is 0 to 39.

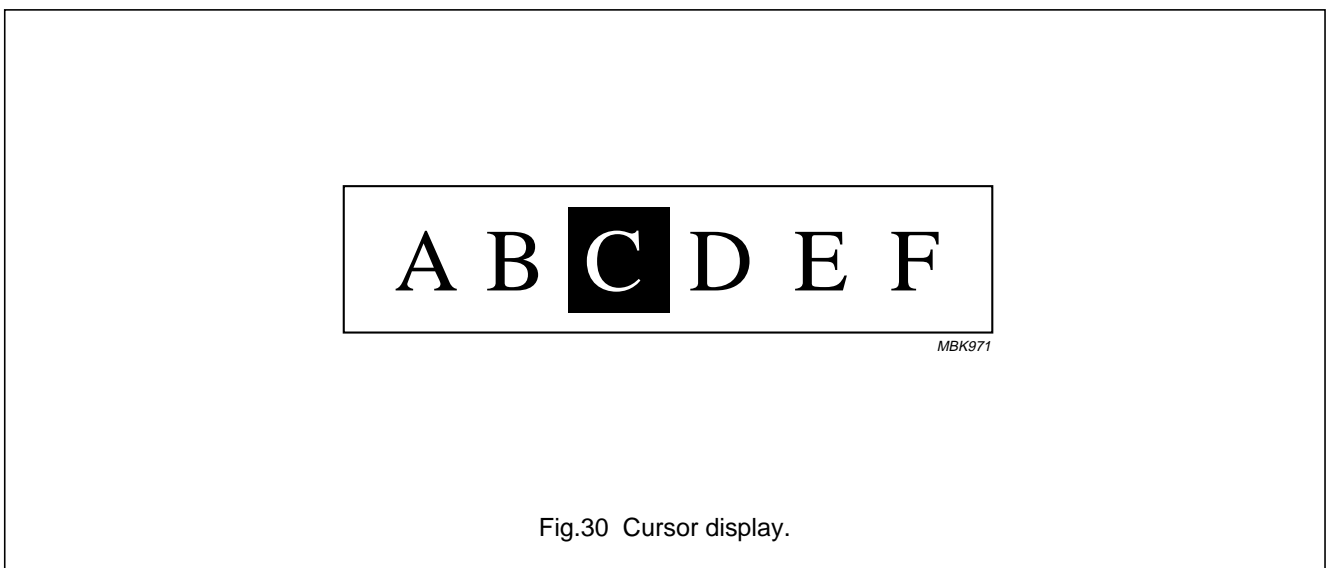


Fig.30 Cursor display.

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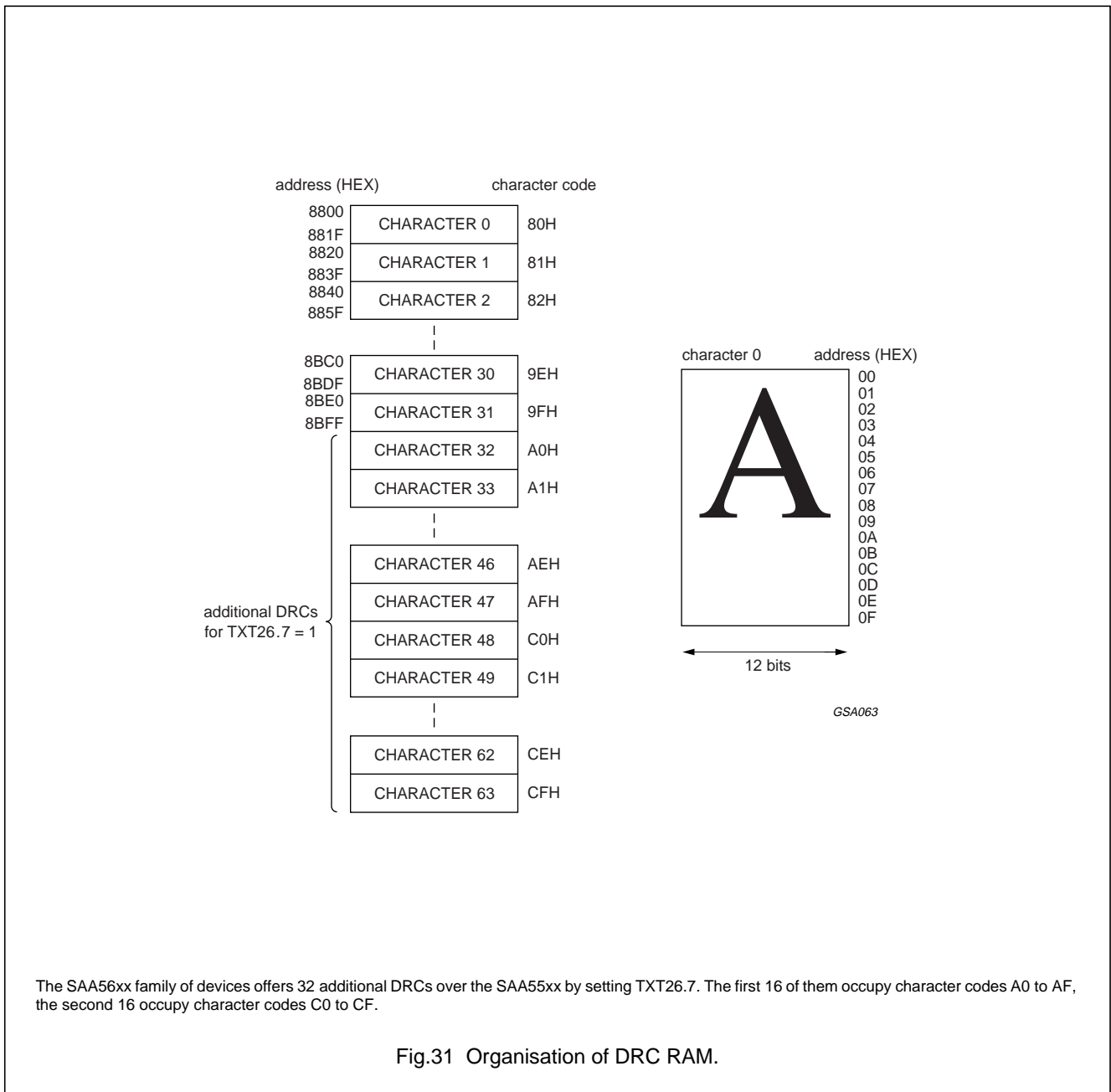
### 23.4.15 DYNAMICALLY REDEFINABLE CHARACTERS (DRCs)

A number of DRCs are available (see Fig.31). These are mapped onto the normal character codes, and replace the predefined Character ROM value.

By default there are 32 DRCs occupying the character codes 80H to 8FH. The SAA56xx family of devices offers 32 additional DRCs over the SAA55xx by setting TXT26. The first 16 of them occupy the character codes A0 to AF, the second 16 occupy the character codes C0 to CF.

The remapping of the standard OSD to the DRCs is activated when the TXT20.DRCS ENABLE bit for single page mode or for Page A in double window mode, and TXT23.DRCS B ENABLE for Page B in double window mode.

Each character is stored in a matrix of  $12 \times 16 \times 1$  (V  $\times$  H  $\times$  planes), this allows for all possible character matrices to be defined within a single location.



The SAA56xx family of devices offers 32 additional DRCs over the SAA55xx by setting TXT26.7. The first 16 of them occupy character codes A0 to AF, the second 16 occupy character codes C0 to CF.

Fig.31 Organisation of DRC RAM.

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### 23.4.16 DEFINING CHARACTERS

The DRC RAM is mapped into the 80C51 RAM address space and starts at location 8800H. The character matrix is 12 bits wide and therefore requires two bytes to be written for each word. The first byte (even addresses), addresses the lower eight bits and the lower nibble of the second byte (odd addresses) addresses the upper four bits.

For characters of 9, 10 or 16 lines high, the pixel information starts in the first address and continues sequentially for the required number of addresses.

Characters of 13 lines high are defined with an initial offset of one address, to allow for the correct generation of fringing across boundaries of clustered characters (see Fig.32). The characters continue sequentially for 13 lines, after which a further line can again be used for the generation of correct fringing across boundaries of clustered characters.

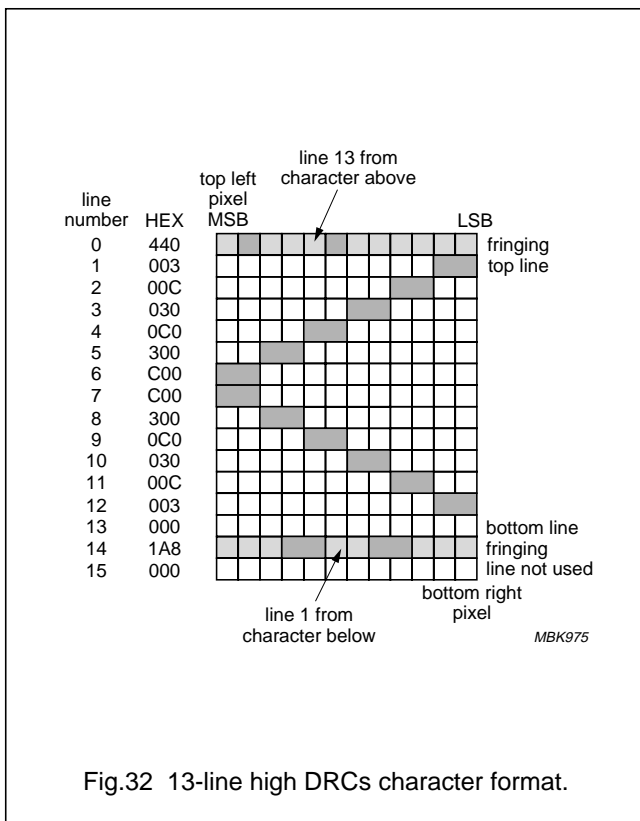


Fig.32 13-line high DRCs character format.

### 23.4.17 SPECIAL GRAPHICS CHARACTERS

**CC/TXT:** several special graphics characters (see Fig.33) are provided for improved OSD effects. These characters provide a choice of four colours within a character cell; see Table 31. Each special graphics character uses two consecutive normal characters.

Table 31 Special graphics character colour allocation

PLANE 1	PLANE 0	COLOUR ALLOCATION
0	0	background colour
0	1	foreground colour
1	0	CLUT entry 6
1	1	CLUT entry 7

By default (for backwards compatibility with the SAA55xx family of devices), there are 16 special graphics characters. They are stored in the character codes 8XH and 9XH of the character table (32 ROM characters), or in the DRCS RAM.

The SAA56xx family of devices allow for 32 special graphics characters, if TXT26.EXTENDED DRCS is set. They are stored in character codes 8XH, 9XH, AXH and CXH, or in the DRCs RAM, including the extended location (64 characters).

Special graphics characters are activated when the double plane decoding for the special graphics is set by TXT20.OSD PLANES in single window mode or for Page A in double window mode, or by setting TXT29.OSD PLANES B for Page B in double window mode.

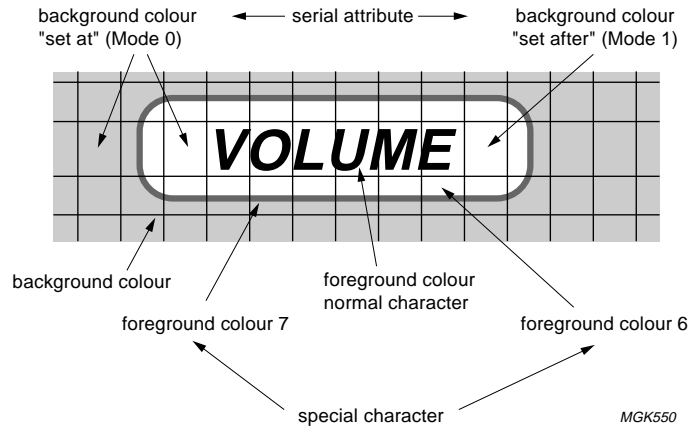
**CC:** Additional special graphics characters are allowed in CC OSD mode by enabling the Extended Special Graphics SFR. So when TXT20.5 = 1, any character location can be used as special graphics using bit 14 of its parallel code (see Table 32), extended special graphic attributes.

**Remark:** Fringing, underline, overline and smoothing are not possible for special graphics.

If the screen colour is transparent (implicit in mixed mode) and the box attribute is set inside the object, the object is surrounded by video. If the box attribute is not set, the background colour inside the object will also be displayed as transparent.

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This example could also be done with 8 special characters.

Fig.33 Example of a special graphics character.

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### 23.4.18 SMOOTHING

To improve the appearance of the display, the SAA56xx family of devices incorporates a smoothing algorithm to insert extra pixels for all character sizes other than normal size (see Fig.34). Smoothing is available in both TXT and CC modes.

MMR 87E4H bit 4 enables smoothing in single page mode and for Page A in double window mode. MMR 87E4H bit 5 enables smoothing for Page B in double window mode.

The appearance of special graphics characters and fringed characters cannot be improved with the smoothing algorithm.

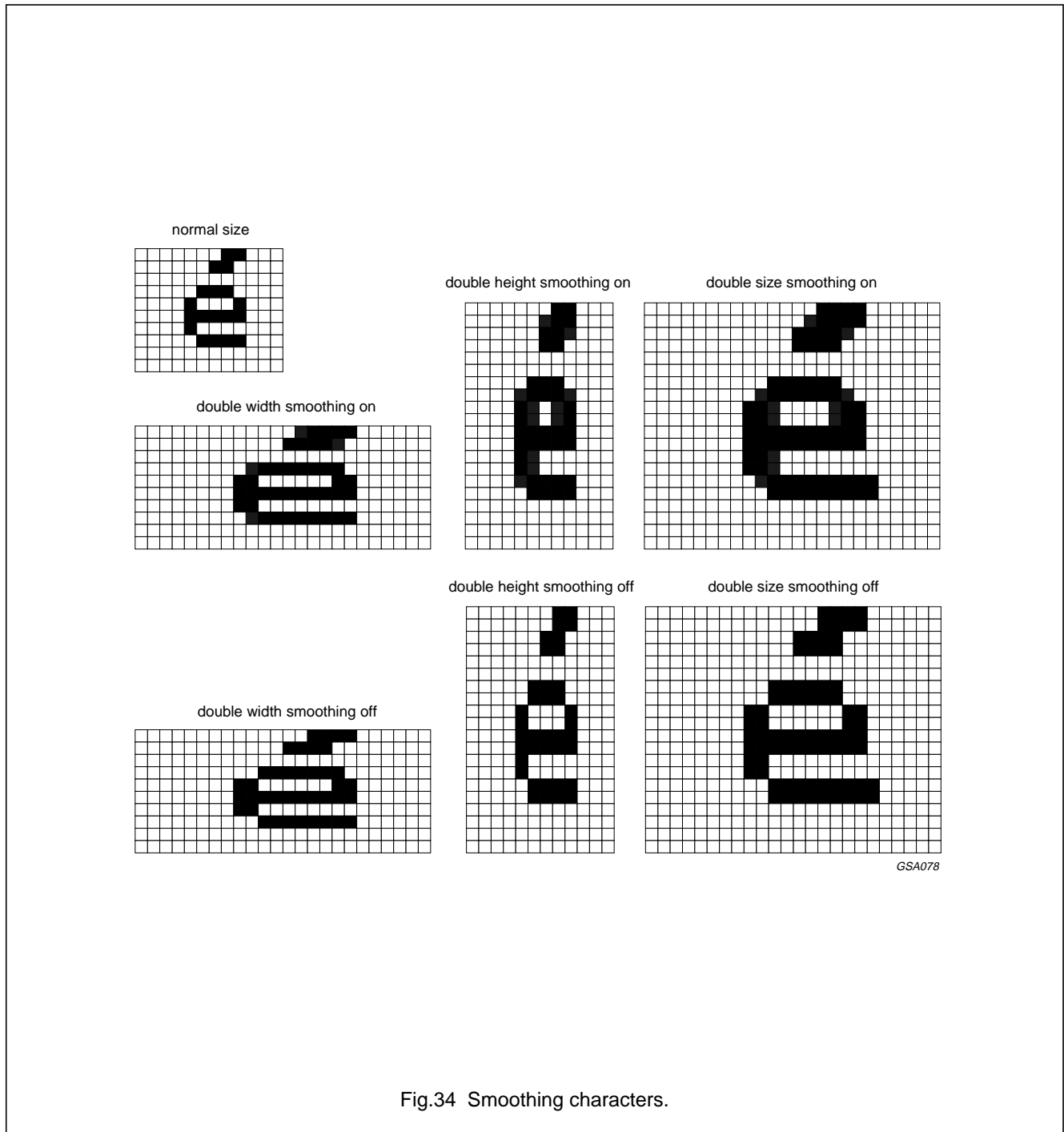


Fig.34 Smoothing characters.

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### 23.4.19 CONTRAST REDUCTION

The device can act on the TV's display circuit to reduce contrast of the video by driving the  $\overline{\text{COR}}$  output LOW. Contrast reduction improves the readability of characters in mixed mode.

**TXT:** Bits  $\overline{\text{COR}}$  IN in SFRs TXT5 and TXT6 control when the  $\overline{\text{COR}}$  output of the device is activated. These bits allow, for example, the display to be set-up so that the areas inside Teletext boxes are contrast reduced when a subtitle is displayed, leaving the rest of the screen displayed as in normal conditions.

**CC:** Here, the contrast reduction is controlled by the contrast reduction attribute (see Table 33). This attribute is valid from the time set until the end of a row of a display window, or otherwise modified if set with Serial Mode 0. If set with Serial Mode 1, it is set from the next character onwards.

### 23.5 Character and attribute coding

This section describes the character and attribute coding for each mode.

#### 23.5.1 CC MODE

Character coding is split into character oriented attributes (parallel, see Table 32) and character group coding (serial, see Table 33). The serial attributes take effect either at the position of the attribute (set at), or at the following location (set after) and remain effective until either modified by a new serial attribute or until the end of a row of a display window. A serial attribute is represented as a space (the space character itself however is not used for this purpose). The attributes that are still active, e.g. overline and underline, are visible during the display of the space.

The default setting at the start of a row is:

- 1× size
- Flash off
- Overline off
- Underline off
- Italics off
- Display mode = superimpose
- Fringing off
- Background colour duration = 0
- End of row = 0.

The coding is done in 15-bit words. The codes are stored sequentially in the Display memory. A maximum of 768 character positions can be defined for a single display.

#### 23.5.2 TXT MODE

Character coding is in a serial format, with only one attribute being changed at any single location. The serial attributes take effect either at the position of the attribute (set at), or at the following location (set after). The attribute remains effective until either modified by new serial attributes or until the end of a row of a display window.

The default settings at the start of a row are:

- Foreground colour white (CLUT address 7)
- Background colour black (CLUT address 8)
- Horizontal size ×1, vertical size ×1 (normal size)
- Alphanumeric on
- Contiguous Mosaic Graphics
- Release Mosaics
- Flash off
- Box off
- Conceal off
- Twist off.

The attributes have individual codes which are defined in the basic character table (see Fig.35).

#### 23.5.3 PARALLEL CHARACTER CODING

**Table 32** Parallel character coding

BITS	DESCRIPTION
0 to 7	8-bit character code
8 to 10	three bits for eight foreground colours
11	mode bit: 0 = parallel code
12 to 13	character set selection; see Section 23.11.2
14	special graphics; see Section 23.4.17



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### 23.5.4 SERIAL CHARACTER CODING

**Table 33** Serial character coding

BITS	DESCRIPTION		
	SERIAL MODE 0 ('SET AT')	SERIAL MODE 1	
		CHAR.POS. 1 ('SET AT')	CHAR.POS. >1 ('SET AFTER')
0 to 3	4 bits for 16 background colours	4 bits for 16 background colours	4 bits for 16 background colours
4	Underline switch: 0 = Underline off 1 = Underline on	Horizontal size: 0 = normal 1 = ×2	Underline switch: 0 = Underline off 1 = Underline on
5	Overline switch: 0 = Overline off 1 = Overline on	Vertical size: 0 = normal 1 = ×2	Overline switch: 0 = Overline off 1 = Overline on
6	Display mode: 0 = Superimpose 1 = Boxing	Display mode: 0 = Superimpose 1 = Boxing	Display mode: 0 = Superimpose 1 = Boxing
7	Flash switch: 0 = Flash off 1 = Flash on	Foreground colour switch: 0 = Bank 0 (colours 0 to 7) 1 = Bank 1 (colours 8 to 15)	Foreground colour switch: 0 = Bank 0 (colours 0 to 7) 1 = Bank 1 (colours 8 to 15)
8	Italic switch: 0 = Italics off 1 = Italics on	Background colour duration: 0 = stop BGC 1 = set BGC to end of row	Background colour duration (set at): 0 = stop BGC 1 = set BGC to end of row
9	Fringing switch: 0 = Fringing off 1 = Fringing on	End of Row 0 = Continue Row 1 = End Row:	End of Row (set at): 0 = Continue Row 1 = End Row
10	Switch for serial coding: 0 = Mode 0 1 = Mode 1	Switch for serial coding: 0 = Mode 0 1 = Mode 1	Switch for serial coding: 0 = Mode 0 1 = Mode 1
11	Mode bit: 1 = serial code	Mode bit: 1 = serial code	Mode bit: 1 = serial code
12	Contrast switch: 0 = contrast reduction off 1 = contrast reduction on	Contrast switch: 0 = contrast reduction off 1 = contrast reduction on	Contrast switch: 0 = contrast reduction off 1 = contrast reduction on



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### 23.6 Screen and global controls

A number of attributes are available that affect the whole display region of a display window, and cannot be applied selectively to regions of the display.

#### 23.6.1 TV SCAN LINES PER ROW

The number of TV scan lines per field used for each display row can be defined, the value is independent of the character size being used. The number of lines can be 10, 13 or 16 per display row. The number of TV scan lines per row is defined by TXT21.DISP LINES<1:0>.

A value of nine lines per row can be achieved if the display is forced into 525-line display mode by TXT17.FORCE DISP<1:0>, or if the device is in 10-line mode and the automatic detection circuit within display finds 525-line display syncs.

The number of TV lines per row is then set for both the display windows in double window mode.

#### 23.6.2 CHARACTER MATRIX (H × V)

There are three different character matrices available: 12 × 10, 12 × 13 and 12 × 16. The selection is made using TXT21.CHAR SIZE<1:0> and is independent of the number of display lines per row.

If the character matrix is less than the number of TV scan lines per row, the matrix is padded with blank lines. If the character matrix is greater than the number of TV scan lines, the character is truncated.

The character matrix is set for all display windows.

#### 23.6.3 DISPLAY MODES

**CC:** When the superimpose or boxing attribute (see Table 33, Serial Mode 0/1, bit 6) is set, the resulting display depends on the setting of the following screen control mode bits in the MMR Display Control (see Table 34).

**TXT:** The display mode is controlled by the bits in TXT5 and TXT6 in single window mode or for Page A in double window mode, and by the bits in bytes TXT24 and TXT25 in Page B in double window mode. There are three control functions: Text on, Background on and Picture on (see Table 35). Separate sets of bits are used inside and outside Teletext boxes so that different display modes can be invoked. Bit(s) TXT6 and/or TXT25 are used if the newflash (C5) or subtitle (C6) bits in row 25 of the basic page memory are set; otherwise, byte TXT5 and/or TXT24 is/are used. This allows the software to set up the type of display required on newflash and subtitle pages (e.g. text inside boxes, TV picture outside). This will be invoked without any further software intervention when such a page is acquired.

When Teletext box control characters are present in the display page memory, the appropriate Box control bit must be set, TXT<n>.Box ON 0 (B), TXT<n>.Box ON Row 1–23 (B), TXT<n>.Box ON 24 (B) where <n> is:

- 7 in single page mode or for Page A in double window mode
- 26 for double window mode for Page B.

This allows the display mode to be different inside the Teletext box compared to outside. These control bits are present to allow boxes in certain areas of the screen to be disabled. The use of Teletext boxes for OSD messages has been superseded in this device by the OSD box concept. However, these bits remain to allow Teletext boxes to be used, if required.

**Table 34** Selection of display modes

MOD1	MOD0	DISPLAY MODE	DESCRIPTION
0	0	Video	Disables all display activities, sets the RGB to true black and VDS to video.
0	1	Full Text	Displays screen colour at all locations not covered by character foreground or background colour. The box attribute has no effect.
1	0	Mixed Screen Colour	Displays screen colour at all locations not covered by character foreground, within boxed areas or, background colour.
1	1	Mixed Video	Displays video at all locations not covered by character foreground, within boxed areas or, background colour.

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**Table 35** TXT display control bits

PICTURE ON	TEXT ON	BACKGROUND ON	EFFECT
0	0	X	Text mode, black screen
0	1	0	Text mode, background always black
0	1	1	Text mode
1	0	X	Video mode
1	1	0	Mixed text and TV mode
1	1	1	Text mode, TV picture outside text area

### 23.7 Screen colour

Screen colour is displayed from 10.5 to 62.5 ms after the active edge of the HSYNC input, on TV lines 23 to 310 inclusive for a 625-line display, and on TV lines 17 to 260 inclusive for a 525-line display.

**CC:** The screen colour is defined by the MMR Display Control and points to a location in the CLUT table. The screen colour covers the full video width. It is visible when the Full Text or Mixed Screen Colour mode is set and no foreground or background pixels are being displayed.

**TXT:** Register bits TXT17.SCREEN COL<2:0> can be used to define a colour to be displayed instead of TV picture and the black background colour. If the bits are all set to zero, the screen colour is defined as 'transparent', and TV picture and background colour are displayed as normal. Otherwise, the bits define CLUT entries 9 to 15.

In double window mode, TXT17.SCREEN COL<2:0> applies to Text Area A and TXT27.SCRB<2:0> applies to Text Area B.

### 23.8 Text display controls

#### 23.8.1 TEXT DISPLAY CONFIGURATION (CC MODE)

Two types of areas are possible. The one area is static and the other is dynamic. The dynamic area allows scrolling of a region to take place. The areas cannot cross each other. Only one scroll region is possible.

#### 23.8.2 DISPLAY MAP

The display map (see Fig.36) allows a flexible allocation of data in the memory to individual rows.

Sixteen words are provided in the Display memory for this purpose. The lower ten bits address the first word in the memory where the row data starts. This value is an offset in terms of 16-bit words from the start of Display memory (8000H). The most significant bit enables the display when not within the scroll (dynamic) area (see Table 36).

The display memory map is fixed at the first 16 words in the Closed Caption Display memory.

**Table 36** Display map bit allocation

BIT	FUNCTION
11	Text display enable, valid outside Soft Scroll Area. 0 = disable; 1 = enable.
10	This bit is reserved, should be set to logic 0.
9 to 0	Pointer to row data.

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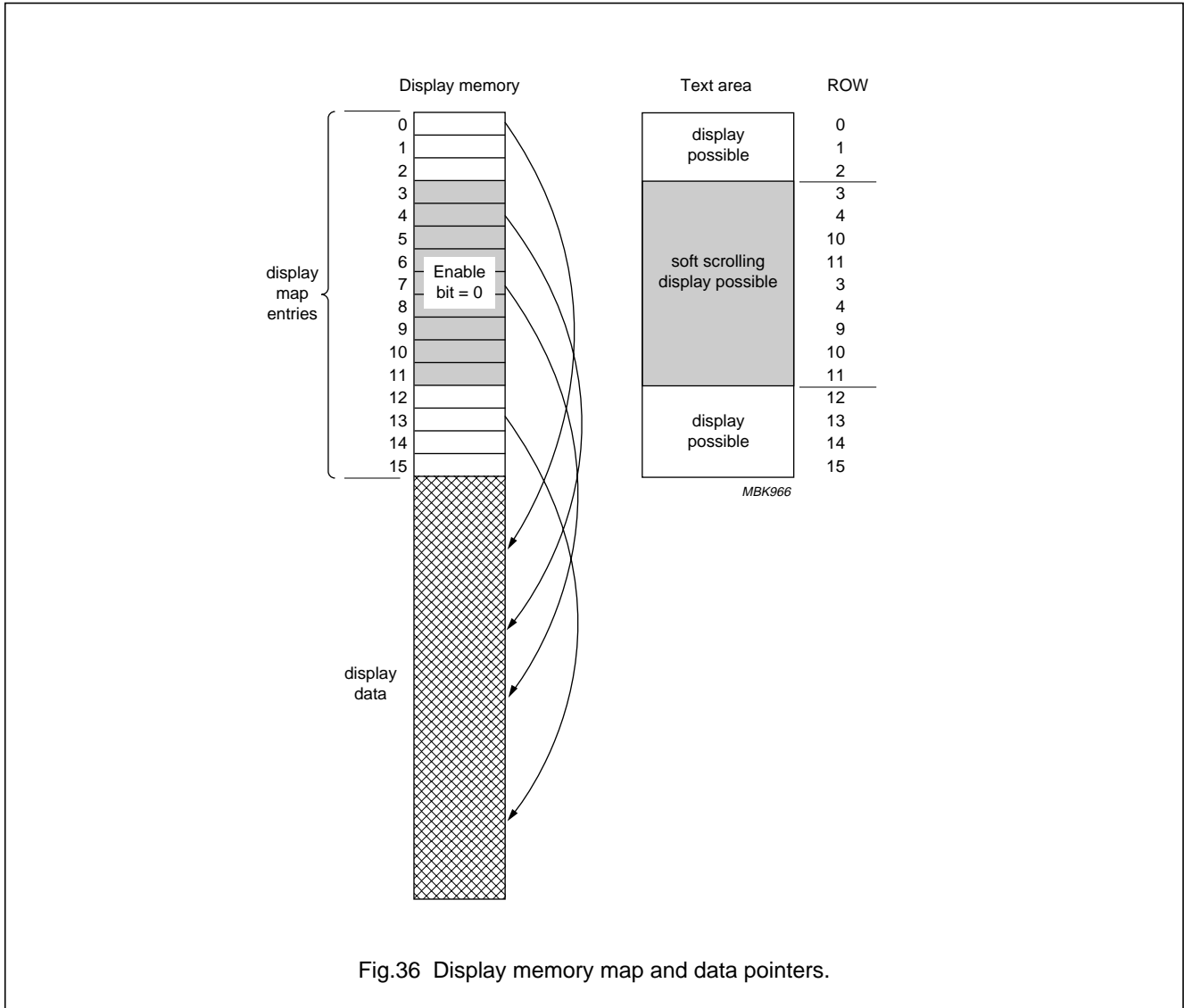


Fig.36 Display memory map and data pointers.

**23.9 Soft scroll action**

The MMR Scroll Area, MMR Scroll Range, MMR Top Scroll line and the MMR Status define the dynamic scroll region. The soft scroll area (see Fig.37) is enabled when the SCON bit is set in MMR Status. Fig.38 shows the CC text areas and Fig.39 shows the TXT areas.

Bits SSP<3:0> define the position of the soft scroll area window and bits SSH<3:0> define the height of the window. Both are in MMR Scroll Range. Bits STS<3:0> and bits SPS<3:0> define the rows that are scrolled through the window. Both are in MMR Scroll Area.

Soft scrolling is done by modifying the Scroll Line value SCL<3:0> in MMR Top Scroll Line and the first Scroll Row value SCR<3:0> in the MMR Status.

If the number of rows allocated to the scroll counter is larger than the defined visible scroll area, parts of rows at the top and bottom may be displayed during the scroll function. The registers can be written throughout the field and the values are updated for display with the next field sync. Care should be taken that the register pairs are written to by the software in the same field.

Only a region that contains only single height rows or only double height rows can be scrolled.

**TXT:** The display is organised as a fixed size of 25 rows (0 to 24) of 40 columns (0 to 39), This is the standard size for Teletext transmissions. The Control Data in row 25 is not displayed but is used to configure the display page correctly.

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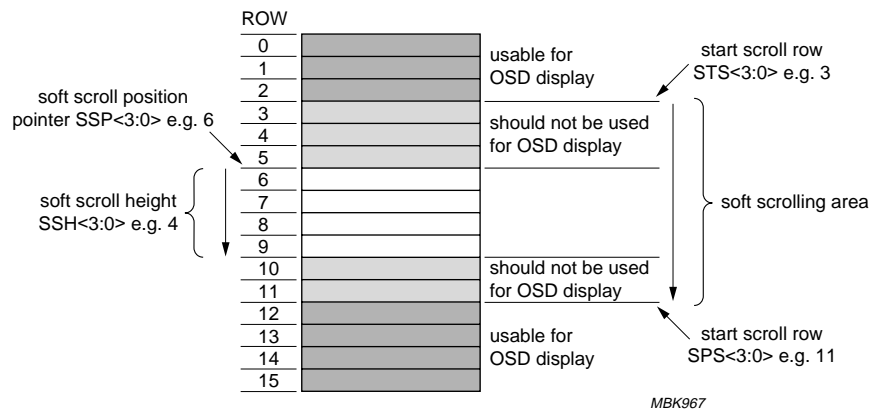


Fig.37 Soft scroll area.

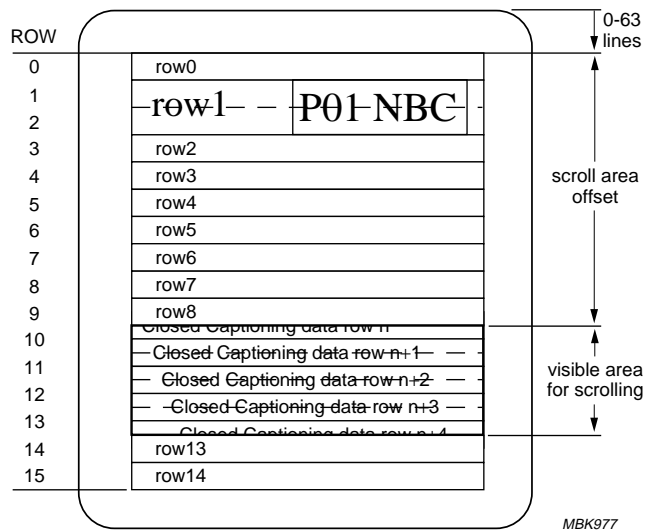
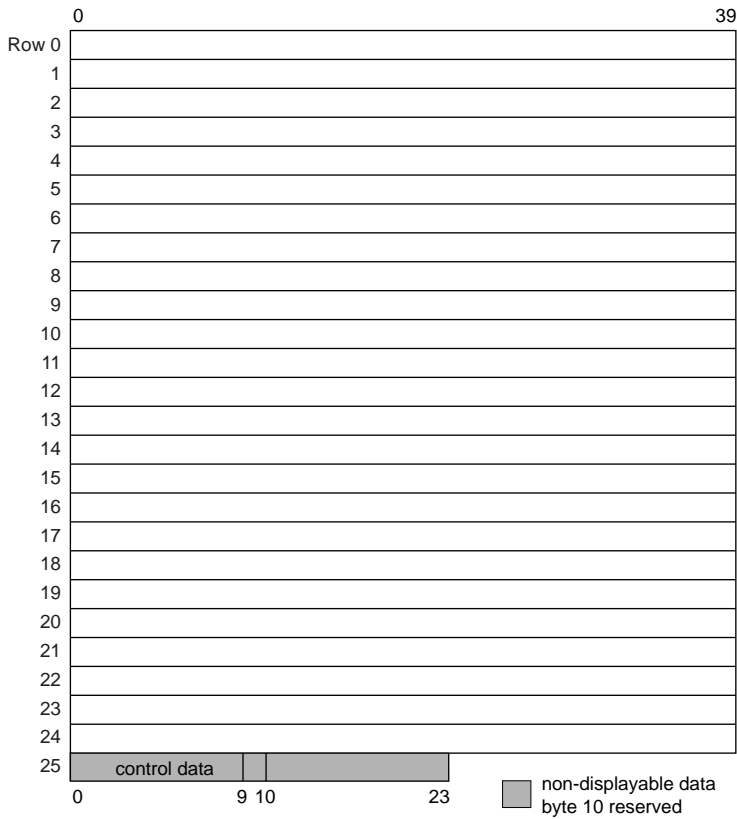


Fig.38 CC text areas.

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MBK968

Fig.39 TXT text area.

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## 23.10 Display positioning

### 23.10.1 SINGLE WINDOW MODE

The display consists of the **screen colour** covering the whole screen and the **text area** that is placed within the visible screen area (see Fig.40).

The screen colour extends over a large vertical and horizontal range so that no offset is needed. The text area is offset in both directions relative to the vertical and horizontal sync pulses.

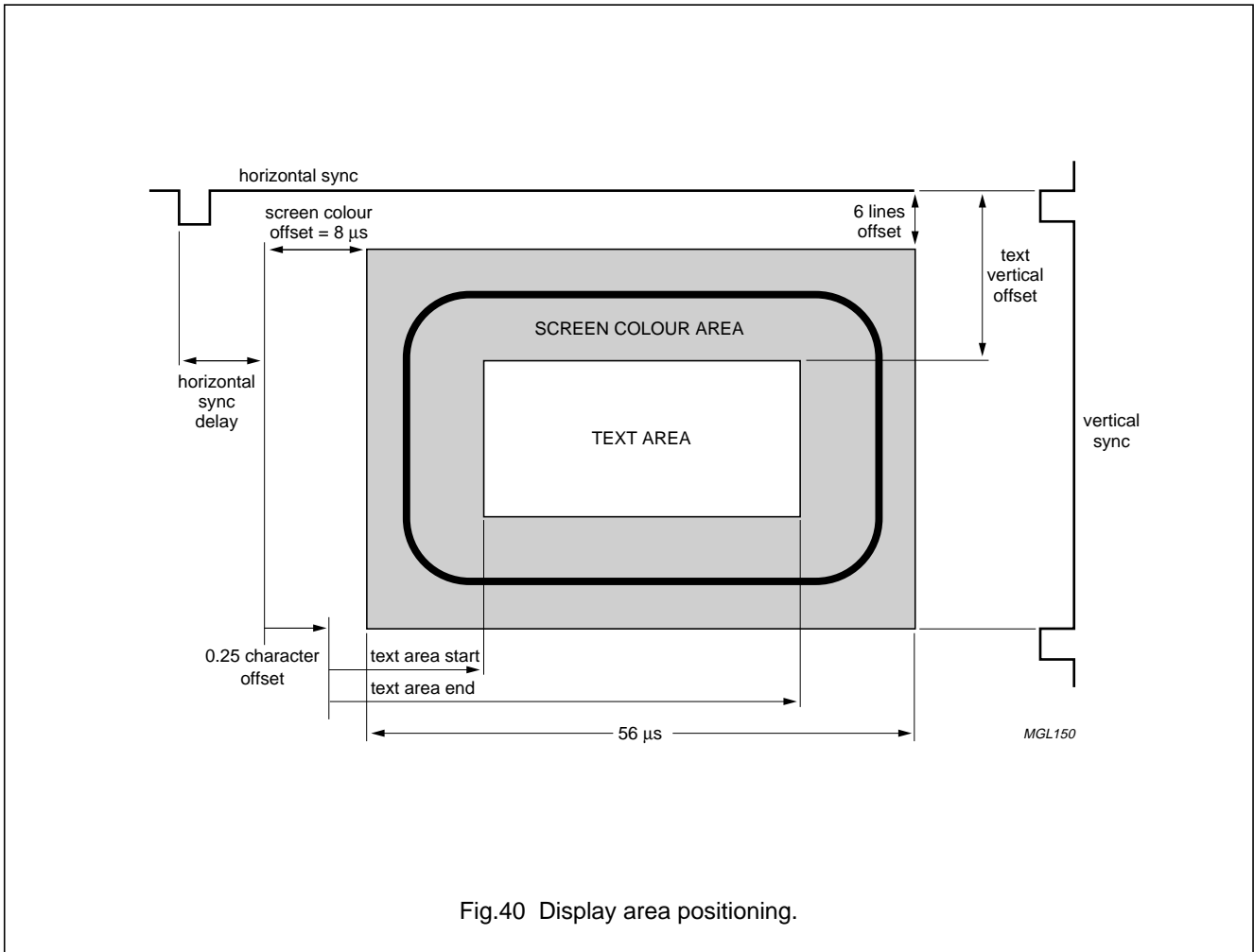


Fig.40 Display area positioning.



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### 23.10.2 DOUBLE WINDOW MODE

The display (see Fig.41) consists of the **two screen colours** covering each half of the screen and two **text areas** that are placed within the visible screen area. The screen colour extends over a large vertical and horizontal range so that no offset is needed. Both text areas are offset in both directions relative to the vertical and horizontal sync pulses.

The second page may be positioned relative to the HSYNC delay using the Page B Position MMR.

The visible text area for Page A is controlled using the Text Area Start and Text Area End MMRs. Page B visible text area is controlled using the Text Area Start B and Text Area End B MMRs.

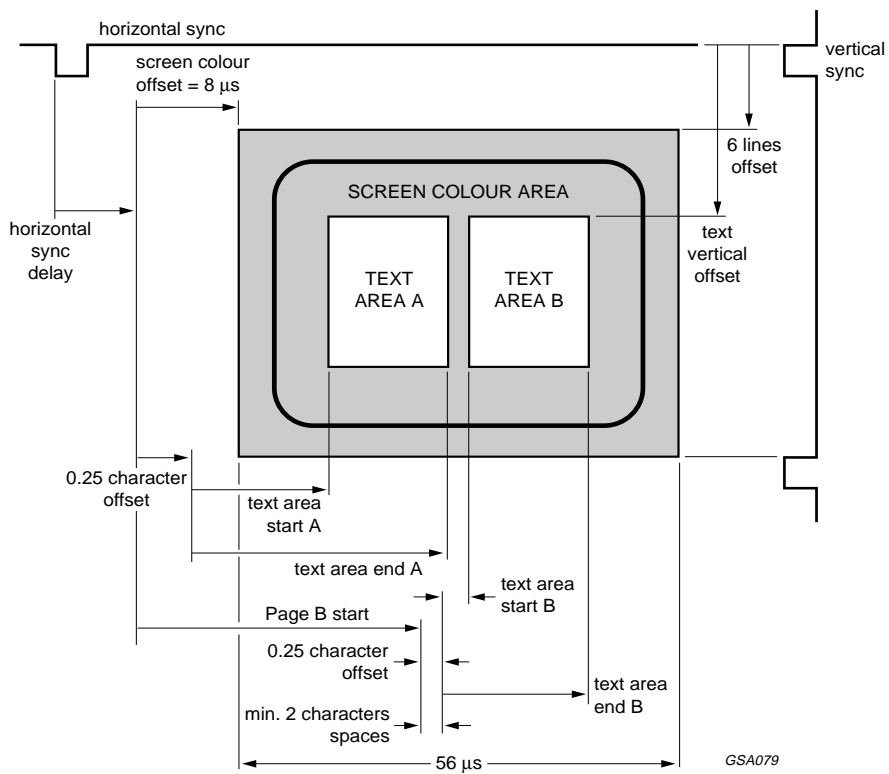


Fig.41 Page positioning.

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### 23.10.3 SCREEN COLOUR DISPLAY AREA

This area is covered by the screen colour, and starts with a fixed offset of 8  $\mu$ s from the leading edge of the horizontal sync pulse in the horizontal direction. A vertical offset is not necessary. For a summary, see the following:

**Horizontal:** Start at 8  $\mu$ s after leading edge of horizontal sync for 56  $\mu$ s.

**Vertical:** Line 9, field 1 (321, field 2) to leading edge of vertical sync (line numbering using 625 Standard).

### 23.10.4 TEXT DISPLAY AREA (SINGLE PAGE)

The text area can be defined to start with an offset in both the horizontal and vertical directions. For a summary, see following:

**Horizontal:** Up to 48 full-sized characters per row. Start position setting from 3 to 64 characters relative to HSYNC delay. Fine adjustment in quarter characters.

**Vertical:** 256 Lines (nominal 41 to 297). Start position setting from leading edge of vertical sync, legal values are 4 to 64 lines (line numbering using 625 Standard).

The horizontal offset is set in MMR Text Area Start. The offset is done in full-width characters using TAS<5:0>, with quarter characters using HOP<1:0> for fine setting. Values 00H to 03H for TAS<5:0> result in a corrupted display.

The width of the text area is defined in the Text Area End Register by setting the end character value TAE<5:0>. This number determines where the background colour of the text area will end if set to extend to the end of the row. It will also terminate the character fetch process, thus eliminating the necessity of a **row end** attribute. However, this entails writing to all positions.

The vertical offset is set in the Text Position Vertical Register. The offset value VOL<5:0> is done in number of TV scan lines.

Note that the Text Position Vertical Register should not be set to 00H as the Display Busy interrupt is not generated in these circumstances.

### 23.10.5 TEXT DISPLAY AREA (TWO\_PAGE)

Control of Page A in two page mode is as per the control in single page mode. Three extra memory mapped registers control the position of the second page: the Text Area Start B, Text Area End B and the Page B Position Register.

Page B positioning register controls the positioning of Text Area B relative to HSYNC delay. A minimum two character gap should be allowed between each page to allow the reset of attributes.

The vertical offset must be the same for both pages, i.e. RANGE<1:0> and VOL<5:0> = RANGE<1:0> and VOLB<5:0> in Text Position Vertical and Vertical Range Registers (MMR 87F1H, MMR 87E3H and MMR 87E4H). The text area can be defined to start with an offset in the horizontal direction, as follows:

- Up to 48 full-sized characters per row. Start position setting from 3 to 64 characters relative to value in Page B position register. Fine adjustment in quarter characters.
- The horizontal offset is set in the Text Area Start Register. The offset is done in full-width characters using TAS B<5:0>, with quarter characters using HOP B<1:0> for fine setting.
- The width of the text area is defined in the Text Area End Register by setting the end character value TAE B<5:0>. This number determines where the background colour of the Text Area B will end if set to extend to the end of the row. It will also terminate the character fetch process thus eliminating the necessity of a row end attribute. However, this entails writing to all positions.

### 23.11 Character set

To facilitate the global nature of the device, the character set can accommodate a large number of characters, which can be stored in different matrices.

#### 23.11.1 CHARACTER MATRICES

The character matrices that can be accommodated in both display modes are:

(H  $\times$  V  $\times$  planes) 12  $\times$  9  $\times$  1, 12  $\times$  10  $\times$  1, 12  $\times$  13  $\times$  1 and 12  $\times$  16  $\times$  1.

These modes allow two colours per character position.

In CC mode, two additional character matrices are available to allow four colours per character:

(H  $\times$  V  $\times$  planes) 12  $\times$  13  $\times$  2 and 12  $\times$  16  $\times$  2.

The characters are stored physically in ROM in a 12  $\times$  10 or 12  $\times$  16 matrix.

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### 23.11.2 CHARACTER SET SELECTION

Four character sets are available in the device. A set can consist of alphanumeric characters, as required by the WST Teletext or FCC Closed Captioning, Customer definable OSD characters, and Special Graphic characters.

**CC:** Within a Closed Caption information transmission, only one character set can be used for display. This is selected using the Basic Set selection TXT18.BS<1:0> in single window mode and for Page A in double window mode, and TXT23.BS B<1:0> for Page B in double window mode. When selecting a character set in CC mode, the Twist Set selection TXT19.TS<1:0> should be set to the same value as TXT18.BS<1:0> for correct operation.

**TXT:** Two character sets can be displayed at once. These are the basic G0 set or the alternative G0 set (Twist Set).

The basic set is selected using TXT18.BS<1:0> in single window mode or for Page A in double window mode, and TXT23.BS B<1:0> for Page B in double window mode. The alternative character set is defined by TXT19.TS<1:0> in single window mode for Page A in double window mode, and TXT29.TS B<6:5> for Page B in double window mode.

Since the alternative character set is an option, it can be enabled or disabled using TXT19.TEN for TXT19.TS<1:0> and by TXT29.TEN B for TXT29.TS B<6:5>. Also, the language code that is defined for the alternative set is defined by TXT19.TC<2:0> for TXT19.TS<1:0> and by TXT30.TC B<7:6> for TXT29.TS B<6:5>.

The National Option Table is selected using TXT18.NOT<3:0>. A maximum of 31 National Option Tables can be defined when combined with the EAST/WEST control bit located in register TXT4.

In CC OSD mode, characters from the four character sets can be displayed on the screen at the same time, providing that all four of the character sets are of the same matrix. This is done using bits 12 to 13 of the parallel code of the character (see Table 37).

**Table 37** Character set bits coding

BITS <13:12>	CHARACTER SET
00	set 0
01	set 1
10	set 2
11	set 3

### 23.12 RGB brightness control

A brightness control is provided to adjust the RGB upper output voltage level. The nominal value is 1 V into a 150 Ω resistor, but can be varied between 0.7 and 1.2 V.

The brightness is set in the RGB Brightness Register, see Table 38.

**Table 38** RGB brightness

BRI3 TO BRI0	RGB BRIGHTNESS
0000	lowest value
...	...
1111	highest value

## 24 MEMORY MAPPED REGISTERS (MMRs)

The memory mapped registers are used to control the display as for the SAA55xx. Some additional MMRs are used for the SAA56xx; see Tables 39 to 41.

**Table 39** MMR address summary

REGISTER NUMBER	MEMORY ADDRESS	FUNCTION
0	87F0H	Display Control
1	87F1H	Text Position Vertical
2	87F2H	Text Area Start
3	87F3H	Fringing Control
4	87F4H	Text Area End
5	87F5H	Scroll Area
6	87F6H	Scroll Range
7	87F7H	RGB Brightness
8	87F8H	Status
9	87F9H	Reserved
10	87FAH	Reserved
11	87FBH	Reserved
12	87FCH	HSYNC Delay
13	87FDH	VSYSN Delay
14	87FEH	Top Scroll Line
15	87FFH	Configuration
16	87E0H	Text Area Start B
17	87E1H	Text Area End B
18	87E2H	Page B Position
19	87E3H	Text Position Vertical B
20	87E4H	Vertical Range

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Table 40 MMR map

ADDRESS	R/W	NAME	7	6	5	4	3	2	1	0	RESET
87F0H	R/W	Display Control	SRC3	SRC2	SRC1	SRC0	–	MSH	MOD1	MOD0	00H
87F1H	R/W	Text Position Vertical	VPOL	HPOL	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0	00H
87F2H	R/W	Text Area Start	HOP1	HOP0	TAS5	TAS4	TAS3	TAS2	TAS1	TAS0	00H
87F3H	R/W	Fringing Control	FRC3	FRC2	FRC1	FRC0	FRDN	FRDE	FRDS	FRDW	00H
87F4H	R/W	Text Area End	–	–	TAE5	TAE4	TAE3	TAE2	TAE1	TAE0	00H
87F5H	R/W	Scroll Area	SSH3	SSH2	SSH1	SSH0	SSP3	SSP2	SSP1	SSP0	00H
87F6H	R/W	Scroll Range	SPS3	SPS2	SPS1	SPS0	STS3	STS2	STS1	STS0	00H
87F7H	R/W	RGB Brightness	VDSPOL	–	–	–	BRI3	BRI2	BRI1	BRI0	00H
87F8H	R	Status	BUSY	FIELD	SCON	FLR	SCR3	SCR2	SCR1	SCR0	00H
	W		–	–	SCON	FLR	SCR3	SCR2	SCR1	SCR0	00H
87FCH	R/W	HSYNC Delay	–	HSD6	HSD5	HSD4	HSD3	HSD3	HSD1	HSD0	00H
87FDH	R/W	VSYNC Delay	–	VSD6	VSD5	VSD4	VSD3	VSD2	VSD1	VSD0	00H
87FEH	R/W	Top Scroll Line	–	–	–	–	SCL3	SCL2	SCL1	SCL0	00H
87FFH	R/W	Configuration	CC	VDEL2	VDEL1	VDEL0	TXT/V	–	100 Hz	Two_Page	00H
87E0H	R/W	Text Area Start B	HOPB1	HOPB0	TASB5	TASB4	TASB3	TASB2	TASB1	TASB0	00H
87E1H	R/W	Text Area End B	–	–	TAEB5	TAEB4	TAEB3	TAEB2	TAEB1	TAEB0	00H
87E2H	R/W	Page B Position	PGB7	PGB6	PGB5	PGB4	PGB3	PGB2	PGB1	PGB0	00H
87E3H	R/W	Text Position Vertical B	–	–	VOLB5	VOLB4	VOLB3	VOLB2	VOLB1	VOLB0	00H
87E4H	R/W	Vertical Range	–	–	SMTHB	SMTH	RANGE1	RANGE0	RANGEB1	RANGEB0	00H

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**Table 41** MMR bit definition

REGISTER	FUNCTION
<b>Display Control</b>	
SRC3 to SRC0	screen colour definition
MSH	meshing all background colours (logic 1)
MOD2 to MOD0	00 = Video 01 = Full Text 10 = Mixed Screen Colour 11 = Mixed Video
<b>Text Position Vertical</b>	
VPOL	inverted input polarity (logic 1)
HPOL	inverted input polarity (logic 1)
VOL5 to VOL0	display start vertical offset from VSYNC (lines)
<b>Text Area Start</b>	
HOP1 to HOP0	fine horizontal offset in quarter of characters, in single page mode or for Page A in double window mode
TAS5 to TAS0	text area start, in single page mode or for Page A in double window mode
<b>Fringing Control</b>	
FRC3 to FRC0	fringing colour, value address of CLUT
FRDN	fringe in north direction (logic 1)
FRDE	fringe in east direction (logic 1)
FRDS	fringe in south direction (logic 1)
FRDW	fringe in west direction (logic 1)
<b>Text Area End</b>	
TAE5 to TAE0	text area end, in full characters, in single page mode or for Page A in double window mode
<b>Scroll Area</b>	
SSH3 to SSH0	soft scroll height
SSP3 to SSP0	soft scroll position
<b>Scroll Range</b>	
SPS3 to SPS0	stop scroll row
STS3 to STS0	start scroll row
<b>RGB Brightness</b>	
VDSPOL	VDS polarity 0 = RGB (1), Video (0) 1 = RGB (0), Video (1)
BRI3 to BRI0	RGB brightness control

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REGISTER	FUNCTION
<b>Status read</b>	
BUSY	access to Display memory could cause display problems (logic 1)
FIELD	even field (logic 1)
FLR	active flash region background only displayed (logic 1)
SCR3 to SCR0	first scroll row
<b>Status write</b>	
SCON	scroll area enabled (logic 1)
FLR	active flash region background colour only displayed (logic 1)
SCR3 to SCR0	first scroll row
<b>HSYNC Delay</b>	
HSD6 to HSD0	HSYNC delay, in full size characters
<b>VSYNC Delay</b>	
VSD6 to VSD0	VSYNC delay in number of 8-bit 12 MHz clock cycles
<b>Top Scroll Line</b>	
SCL3 to SCL0	top line for scroll
<b>Configuration</b>	
CC	Closed Caption mode (logic 1)
VDEL2 to VDEL0	pixel delay between VDS and RGB output 000 = VDS switched to video, not active 001 = VDS active one pixel earlier then RGB 010 = VDS synchronous to RGB 100 = VDS active one pixel after RGB
TXT/V	BUSY signal switch; horizontal (logic 1)
100 Hz	100 Hz mode select; 100Hz/120Hz timing mode (logic 1)
Two_Page	two page mode select; dual page (logic 1)
<b>Text Area Start B</b>	
HOP1 to HOP0	fine horizontal offset in quarter of characters
TAS5 to TAS0	text area start
<b>Text Area End B</b>	
TAE5 to TAE0	text area end, in full characters
<b>Page B Position</b>	
PGB7 to PGB0	Page B position
<b>Text Position Vertical B</b>	
VOLB5 to VOLB0	Page B display start vertical offset from VSYNC (lines) should equal VOL5 to VOL0 in double window mode (MMR 87F1H<5:0>)
<b>Vertical Range</b>	
SMTHB	smoothing on, on Page B (logic 1)

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REGISTER	FUNCTION
SMTH	smoothing on, on Page A (logic 1)
RANGE1 to RANGE0	additional two bits for display vertical offset
RANGEB1 to RANGEB0	additional two bits for display vertical offset on Page B

### 25 IN-SYSTEM PROGRAMMING INTERFACE

A serial programming interface is available for late OTP programming. The interface is based on the IEEE1149 (JTAG) standard, but only two instructions are utilized.

Table 42 shows which port pins are used for ISP.

Care should be taken during system design to ensure the pins used for serial programming do not cause conflict with the application circuit. It is advised to dedicate the port pins (P2.1, P2.2, P2.3 and P2.4) to ISP, and not use them in application.

However, if it is necessary to use them in application then they must be assigned as output.

The device is placed in ISP mode using the RESET pin. Pin P0.2 must be held HIGH during ISP mode. Power to the device during ISP may be sourced either from the application or from an external source. Ground reference between the programmer and the target should be common.

For further details, refer to the "In-System Programming Application Note SPG/AN01008".

**Table 42** Port pins used for ISP

PIN	NAME	FUNCTION
P2.0	EN	Enables JTAG operations (specific to SAA56xx)
P2.1	TCK	Test clock
P2.2	TMS	Test Mode Select
P2.3	TDI	Test Data In
P2.4	TDO	Test Data Out
VPE	VPE	9 V Programming Voltage
RESET	RESET	Device reset/mode selection
$\overline{\text{RESET}}$ (alternative)	$\overline{\text{RESET}}$	Device reset/mode selection
XTALIN	CLK	Clock 12 MHz

### 26 LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DDX}$	supply voltage (all supplies)		-0.5	+4.0	V
$V_I$	input voltage (any input)	note 1	-0.5	( $V_{DD} + 0.5$ ) or 4.1	V
$V_O$	output voltage (any output)		-0.5	$V_{DD} + 0.5$	V
$I_O$	output current (each output)		-	10	mA
$I_{IOK}$	DC input or output diode current		-	20	mA
$T_j$	operating junction temperature		-20	+125	°C
$T_{stg}$	storage temperature		-55	+125	°C

#### Note

- For 5 V tolerant I/Os, the maximum value may be 6 V only when  $V_{DD}$  is present.

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### 27 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$T_{res(j-a)}$	package thermal resistance from junction to ambient	in free air	52	$^{\circ}\text{C}/\text{W}$
$T_{res(j-c)}$	package thermal resistance from junction to case		8	$^{\circ}\text{C}/\text{W}$

### 28 CHARACTERISTICS

$V_{DD} = 3.3 \text{ V} \pm 10\%$ ;  $V_{SS} = 0 \text{ V}$ ;  $T_{amb} = -20 \text{ to } +70 \text{ }^{\circ}\text{C}$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies</b>						
$V_{DDX}$	any supply voltage ( $V_{DD}$ to $V_{SS}$ )		3.0	3.3	3.6	V
$I_{DDP}$	periphery supply current	note 1	1	–	–	mA
$I_{DDC}$	core supply current		–	15	18	mA
$I_{DDC(id)}$	Idle mode core supply current		–	4.6	6	mA
$I_{DDC(pd)}$	Power-down mode core supply current		–	0.76	1	mA
$I_{DDA}$	analog supply current		–	45	48	mA
$I_{DDA(id)}$	Idle mode analog supply current		–	0.87	1	mA
$I_{DDA(pd)}$	Power-down mode analog supply current		–	0.45	0.7	mA
<b>Digital inputs</b>						
<b>RESET</b>						
$V_{IL}$	LOW-level input voltage		–	–	1.00	V
$V_{IH}$	HIGH-level input voltage		1.85	–	5.5	V
$V_{hys}$	hysteresis voltage of Schmitt trigger input		0.44	–	0.58	V
$I_{LI}$	input leakage current	$V_I = 0$	–	–	0.17	$\mu\text{A}$
$R_{pd}$	equivalent pull-down resistance	$V_I = V_{DD}$	55.73	70.71	92.45	$\text{k}\Omega$
<b>RESET, EA, INTD</b>						
$V_{IL}$	LOW-level input voltage		–	–	0.98	V
$V_{IH}$	HIGH-level input voltage		1.73	–	5.5	V
$V_{hys}$	hysteresis voltage of Schmitt trigger input		0.41	–	0.5	V
$I_{LI}$	input leakage current	$V_I = V_{DD}$	–	–	0.00	$\mu\text{A}$
$R_{pu}$	equivalent pull-up resistance	$V_I = 0$	46.07	55.94	70.01	$\text{k}\Omega$
<b>HSYNC, VSYNC</b>						
$V_{IL}$	LOW-level input voltage		–	–	0.96	V
$V_{IH}$	HIGH-level input voltage		1.80	–	5.5	V
$V_{hys}$	hysteresis of Schmitt trigger input		0.40	–	0.56	V
$I_{LI}$	input leakage current	$V_I = 0 \text{ to } V_{DD}$	–	–	0.00	$\mu\text{A}$



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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Digital outputs</b>						
FRAME, VDS, $\overline{RD}$ , $\overline{WR}$ , $\overline{PSEN}$ , ALE, A0 TO A7, A16, A17, MOVX_WR, MOVX_RD, A15_BK, ROMBK0 TO ROMBK2, RAMBK0, RAMBK1 (PUSH-PULL OUTPUTS)						
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 3 mA	–	–	0.13	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = 3 mA	2.84	–	–	V
t <sub>r</sub>	output rise time	10% to 90% of V <sub>DD</sub> , C <sub>L</sub> = 70 pF	7.50	8.85	10.90	ns
t <sub>f</sub>	output fall time	10% to 90% of V <sub>DD</sub> , C <sub>L</sub> = 70 pF	6.70	7.97	10.00	ns
$\overline{COR}$ (OPEN-DRAIN OUTPUT), A8 TO A15 (PUSH-PULL OUTPUTS)						
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 3 mA	–	–	0.14	V
V <sub>OH</sub>	HIGH-level pull-up output voltage	I <sub>OL</sub> = –3 mA; push-pull	2.84	–	–	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 0 to V <sub>DD</sub>	–	–	0.12	μA
t <sub>r</sub>	output rise time	10% to 90% of V <sub>DD</sub> , C <sub>L</sub> = 70 pF	7.20	8.64	11.10	ns
t <sub>f</sub>	output fall time	10% to 90% of V <sub>DD</sub> , C <sub>L</sub> = 70 pF	4.90	7.34	9.40	ns
<b>Digital input/outputs</b>						
P0.0 TO P0.4, P0.7, P1.0 TO P1.1, P2.1 TO P2.7, P3.0 TO P3.7						
V <sub>IL</sub>	LOW-level input voltage		–	–	0.98	V
V <sub>IH</sub>	HIGH-level input voltage		1.78	–	5.50	V
V <sub>hys</sub>	hysteresis of Schmitt trigger input		0.41	–	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 0 to V <sub>DD</sub>	–	–	0.01	μA
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 4 mA	–	–	0.18	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = –4 mA push-pull	2.81	–	–	V
t <sub>r</sub>	output rise time	10% to 90% of V <sub>DD</sub> , C <sub>L</sub> = 70 pF push-pull	6.50	8.47	10.70	ns
t <sub>f</sub>	output fall time	10% to 90% of V <sub>DD</sub> , C <sub>L</sub> = 70 pF	5.70	7.56	10.00	ns
P1.2, P1.3 AND P2.0						
V <sub>IL</sub>	LOW-level input voltage		–	–	0.99	V
V <sub>IH</sub>	HIGH-level input voltage		1.80	–	5.50	V
V <sub>hys</sub>	hysteresis voltage of Schmitt trigger input		0.42	–	0.56	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 0 to V <sub>DD</sub>	–	–	0.02	μA
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 4 mA	–	–	0.17	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = –4 mA push-pull	2.81	–	–	V
t <sub>r</sub>	output rise time	10% to 90% of V <sub>DD</sub> ; C <sub>L</sub> = 70 pF push-pull	7.00	8.47	10.50	ns
t <sub>f</sub>	output fall time	10% to 90% of V <sub>DD</sub> ; C <sub>L</sub> = 70 pF	5.40	7.36	9.30	ns

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P0.5 AND P0.6						
V <sub>IL</sub>	LOW-level input voltage		–	–	0.98	V
V <sub>IH</sub>	HIGH-level input voltage		1.82	–	5.50	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 0 to V <sub>DD</sub>	–	–	0.11	μA
V <sub>hys</sub>	hysteresis voltage of Schmitt trigger input		0.42	–	0.58	V
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 8 mA	–	–	0.20	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = –8 mA push-pull	2.76	–	–	V
t <sub>r</sub>	output rise time	10% to 90% of V <sub>DD</sub> ; C <sub>L</sub> = 70 pF push-pull	7.40	8.22	8.80	ns
t <sub>f</sub>	output fall time	10% to 90% of V <sub>DD</sub> ; C <sub>L</sub> = 70 pF	4.20	4.57	5.20	ns
P1.4 TO P1.7 (OPEN-DRAIN)						
V <sub>IL</sub>	LOW-level input voltage		–	–	1.08	V
V <sub>IH</sub>	HIGH-level input voltage		1.99	–	5.50	V
V <sub>hys</sub>	hysteresis voltage of Schmitt trigger input		0.49	–	0.60	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 0 to V <sub>DD</sub>	–	–	0.13	μA
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 8 mA	–	–	0.35	V
t <sub>f</sub>	output fall time	10% to 90% of V <sub>DD</sub> ; C <sub>L</sub> = 70 pF	69.70	83.67	103.30	ns
t <sub>f(I2C)</sub>	output fall time in relation to the I <sup>2</sup> C-bus specifications	3 V to 1.5 V at I <sub>OL</sub> = 3 mA C <sub>L</sub> = 400 nF	–	57.80	–	ns
AD0 TO AD7 (QUASI-BIDIRECTIONAL)						
V <sub>IL</sub>	LOW-level input voltage		–	–	0.98	V
V <sub>IH</sub>	HIGH-level input voltage		1.82	–	5.50	V
V <sub>hys</sub>	hysteresis voltage of Schmitt trigger input		0.40	–	0.58	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 0, V <sub>DD</sub> /2, V <sub>DD</sub>	–	–	0.12	μA
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 3 mA	–	–	0.14	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OL</sub> = –3 mA; push-pull	2.84	–	–	V
t <sub>r</sub>	output rise time	10% to 90% of V <sub>DD</sub> ; C <sub>L</sub> = 70 pF	7.20	8.64	11.10	ns
t <sub>f</sub>	output fall time	10% to 90% of V <sub>DD</sub> ; C <sub>L</sub> = 70 pF	4.90	7.34	9.40	ns

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Analog inputs</b>						
CVBS0 AND CVBS1						
$V_{\text{sync}}$	sync voltage amplitude		0.1	0.3	0.6	V
$V_{\text{vid(p-p)}}$	video input voltage amplitude (peak-to-peak value)		0.7	1.0	1.4	V
$Z_{\text{source}}$	source impedance		0	–	250	$\Omega$
$V_{\text{IH}}$	HIGH-level input voltage		3.0	–	$V_{\text{DDA}} + 0.3$	V
$C_{\text{I}}$	input capacitance		–	–	10	pF
IREF						
$R_{\text{gnd}}$	resistor to ground	resistor tolerance 2%	–	24	–	k $\Omega$
ADC0 TO ADC3						
$V_{\text{IH}}$	HIGH-level input voltage	input range = $V_{\text{DDP}} - V_{\text{TN}}$	–	–	$V_{\text{DDA}}$	V
$C_{\text{I}}$	input capacitance		–	–	10	pF
VPE						
$V_{\text{IH}}$	HIGH-level input voltage		–	–	9.0	V
<b>Analog outputs</b>						
R, G AND B						
$I_{\text{OL}}$	output current (black level)	$V_{\text{DDA}} = 3.3 \text{ V}$	–10	–	+10	$\mu\text{A}$
$I_{\text{OH}}$	output current (maximum intensity)	$V_{\text{DDA}} = 3.3 \text{ V}$ , intensity level code = 31 decimal	6.0	6.67	7.3	mA
	output current (70% of full intensity)	$V_{\text{DDA}} = 3.3 \text{ V}$ , intensity level code = 0 decimal	4.2	4.7	5.1	mA
$R_{\text{load}}$	load resistor to $V_{\text{SSA}}$	resistor tolerance 5%	–	150	–	$\Omega$
$C_{\text{L}}$	load capacitance		–	–	15	pF
$t_{\text{r}}$	output rise time	10% to 90% full intensity	–	16.1	–	ns
$t_{\text{f}}$	output fall time	10% to 90% full intensity	–	14.5	–	ns
<b>Analog input/output</b>						
SYNC_FILTER						
$C_{\text{sync}}$	storage capacitor to ground		–	100	–	nF
$V_{\text{sync}}$	sync filter level voltage for nominal sync amplitude		0.35	0.55	0.75	V
<b>Crystal oscillator</b>						
XTALIN						
$V_{\text{IL}}$	LOW-level input voltage		$V_{\text{SSA}}$	–	–	V
$V_{\text{IH}}$	HIGH-level input voltage		–	–	$V_{\text{DDA}}$	V
$C_{\text{I}}$	input capacitance		–	–	10	pF
XTALOUT						
$C_{\text{O}}$	output capacitance		–	–	10	pF

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Crystal specification; notes 2 and 3</b>						
$f_{\text{xtal}}$	nominal frequency	fundamental mode	–	12	–	MHz
$C_L$	crystal load capacitance		–	–	30	pF
$C_1$	crystal motional capacitance	$T_{\text{amb}} = 25\text{ °C}$	–	–	20	fF
$R_r$	resonance resistance	$T_{\text{amb}} = 25\text{ °C}$	–	–	60	$\Omega$
$C_{\text{osc}}$	capacitors at XTALIN, XTALOUT	$T_{\text{amb}} = 25\text{ °C}$	–	note 4	–	pF
$C_0$	crystal holder capacitance	$T_{\text{amb}} = 25\text{ °C}$	–	–	note 5	pF
$T_{\text{xtal}}$	temperature range		–20	+25	+85	$^{\circ}\text{C}$
$X_j$	adjustment tolerance	$T_{\text{amb}} = 25\text{ °C}$	–	–	$\pm 50 \times 10^{-6}$	
$X_d$	drift		–	–	$\pm 100 \times 10^{-6}$	

**Notes**

- Peripheral current is dependent on external components and voltage levels on I/Os.
- Crystal order number 4322 143 05561.
- If the 4322 143 05561 crystal is not used, then the formulae in the crystal specification should be used. Where  $C_{\text{IO}} = 7\text{ pF}$ , the mean of the capacitances due to the chip at XTALIN and at XTALOUT.  $C_{\text{ext}}$  is a value for the mean of the stray capacitances due to the external circuit at XTALIN and XTALOUT. The maximum value for the crystal holder capacitance is to ensure start-up,  $C_{\text{osc}}$  may need to be reduced from the initially selected value.
- $C_{\text{osc}(\text{typ})} = 2C_L - C_{\text{IO}} - C_{\text{ext}}$
- $C_{0(\text{max})} = 35 - \frac{1}{2}(C_{\text{osc}} + C_{\text{IO}} + C_{\text{ext}})$

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### 29 QUALITY AND RELIABILITY

This device will meet Philips Semiconductors General Quality Specification for Integrated Circuits "SNW-FQ-611D". The principal requirements are shown in Tables 43 to 45.

#### 29.1 Lot acceptance

**Table 43** Acceptance tests per lot

TEST	REQUIREMENTS <sup>(1)</sup>
Mechanical	cumulative target: <80 ppm
Electrical	cumulative target: <100 ppm

#### Note

1. ppm = fraction of defective devices, in parts per million.

#### 29.2 Reliability Performance

**Table 44** Reliability tests (by process family)

TEST	CONDITIONS	REQUIREMENTS <sup>(1)</sup>
High temperature operating life	168 hours at $T_j = 150\text{ °C}$	<500 FPM
Humidity life	temperature, humidity, bias 1000 hours, 85 °C, 85% RH (or equivalent test)	<1000 FPM
Temperature cycling performance	-65 to 150 °C	<2000 FPM

#### Note

1. FPM = fraction of devices failing at test condition, in Failures Per Million.

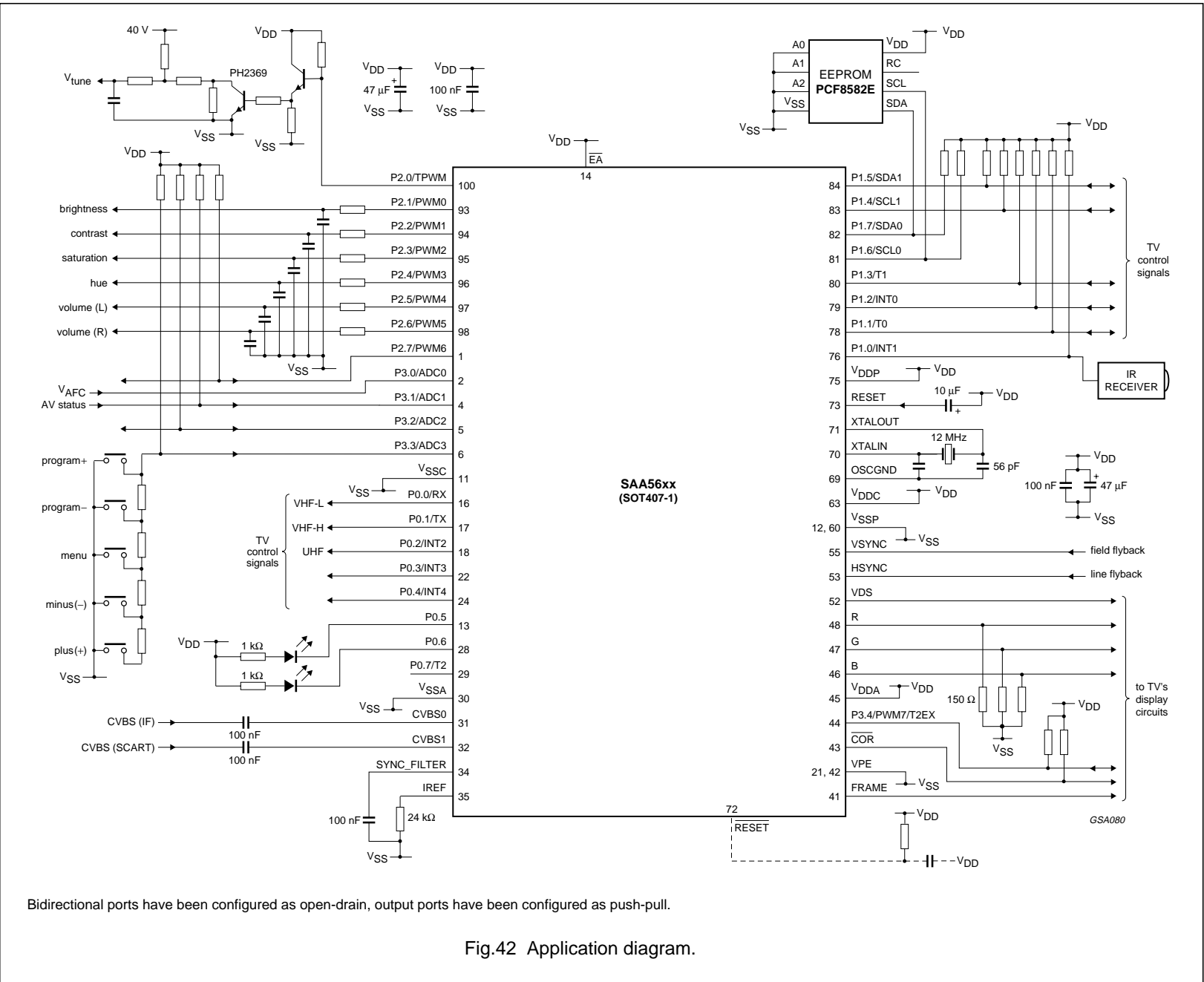
**Table 45** Reliability tests (by device type)

TEST	CONDITIONS	REQUIREMENTS
ESD and latch-up	ESD Human body model 100 pF, 1.5 k $\Omega$	2000 V
	ESD Machine model 200 pF, 0 $\Omega$	200 V
	latch-up	100 mA, $1.5 \times V_{DD(max)}$

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## 30 APPLICATION INFORMATION



Bidirectional ports have been configured as open-drain, output ports have been configured as push-pull.

Fig.42 Application diagram.

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### 30.1 External SRAM implementation

#### 30.1.1 APPLICATION DIAGRAM

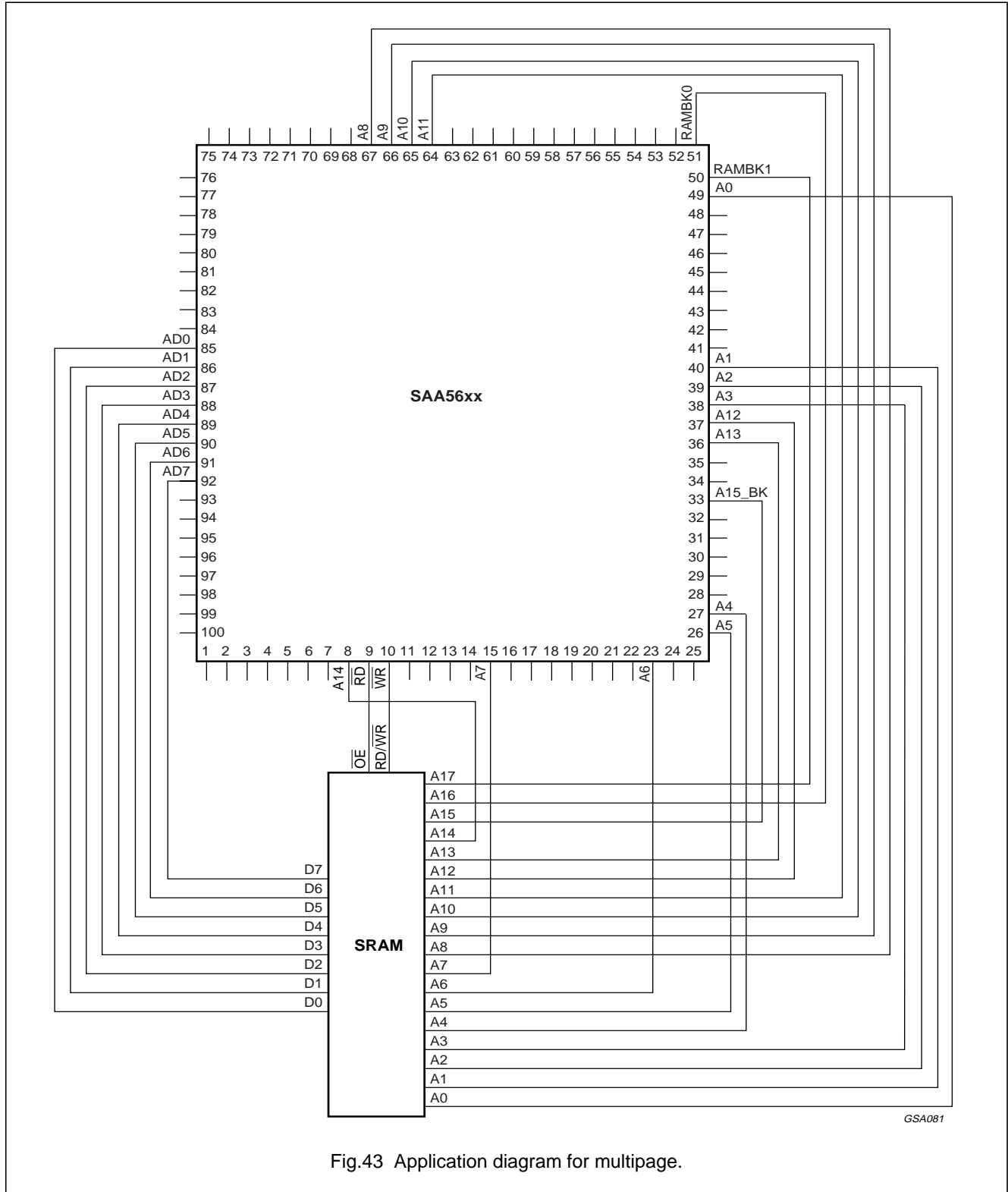


Fig.43 Application diagram for multipage.

GSA081

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### 30.1.2 APPLICATION NOTES

Ports AD0 to AD7 of the microcontroller can be connected to pins D0 to D7 of the SRAM in any order.

For the addressing, the lower group of address lines (A0 to A8) and the upper group of address lines (A9 to A14, A15\_BK, RAMBK0 and RAMBK1) may be connected in any order within the groups, provided that the full 256 kbytes of external SRAM is used.

Fig.43 shows the application diagram for multipage.

When using an external SRAM smaller than 256 kbytes, the relevant number of bits from the microcontroller address bus should be disconnected, always removing the most significant bits first.

For power saving modes, it might be advisable to control the  $\overline{CE}$  pin of the SRAM module(s) using one of the microcontroller ports to de-select the SRAM.

### 30.1.3 EXTERNAL DATA MEMORY ACCESS

**Table 46** External data memory access

See Figs. 44 and 45.

SYMBOL	PARAMETER	TYPICAL <sup>(1)</sup>	UNIT
$t_{RLRH}$	$\overline{RD}$ pulse width	250	ns
$t_{WLWH}$	$\overline{WR}$ pulse width	250	ns
$t_{RLDV}$	$\overline{RD}$ LOW to valid data in	198	ns
$t_{RHDZ}$	Data hold after $\overline{RD}$	0	ns
$t_{RHDZ}$	Data float after $\overline{RD}$	tbd	ns
$t_{LLWL}$	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW	132	ns
$t_{AVWL}$	Address valid to $\overline{WR}$ LOW or $\overline{RD}$ LOW	172	ns
$t_{QVWX}$	Data valid to $\overline{WR}$ LOW	89	ns
$t_{WHQX}$	Data hold after $\overline{WR}$	15	ns
$t_{RLAZ}$	$\overline{RD}$ LOW to address float	tbd	ns
$t_{WHLH}$	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	40	ns

#### Note

1. The external SRAM is intended to be used with the multipage software, therefore only the 12 MHz clock microcontroller timings are provided.

### 30.1.3.1 Symbol explanations

Each timing symbol has five characters. The first character is always 't' (time). Depending on their positions, the other characters indicate the name of a signal or the logical status of that signal. The designations are:

A = Address

C = Clock

D = Input data

H = Logic level HIGH

I = Instruction (program memory contents)

L = Logic level LOW, or ALE

P = PSEN

Q = Output data

R = RD signal

t = Time

V = Valid

W = WR signal

X = No longer a valid logic level

Z = Float

Examples:

$t_{AVLL}$  = Time for address valid to ALE LOW.

$t_{LLPL}$  = Time for ALE to PSEN LOW.



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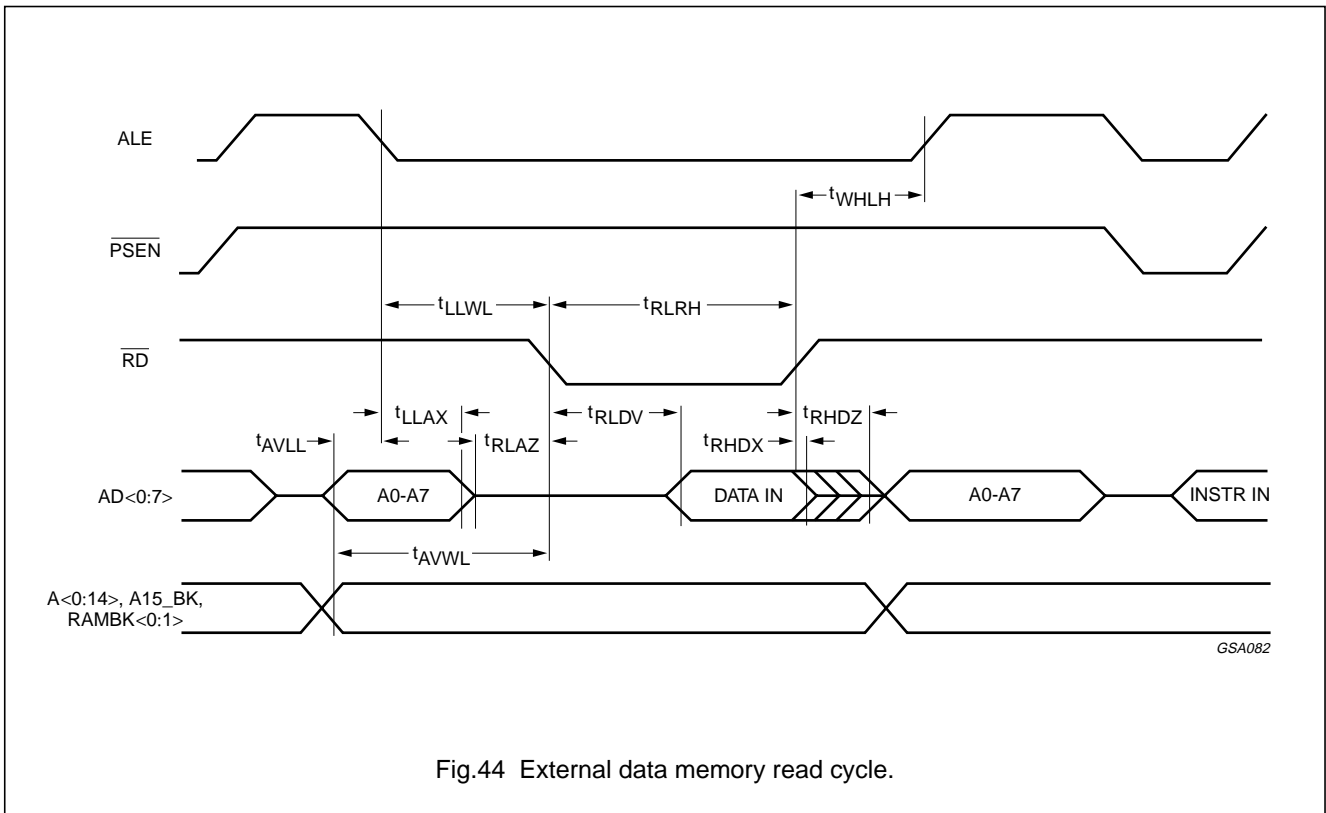


Fig.44 External data memory read cycle.

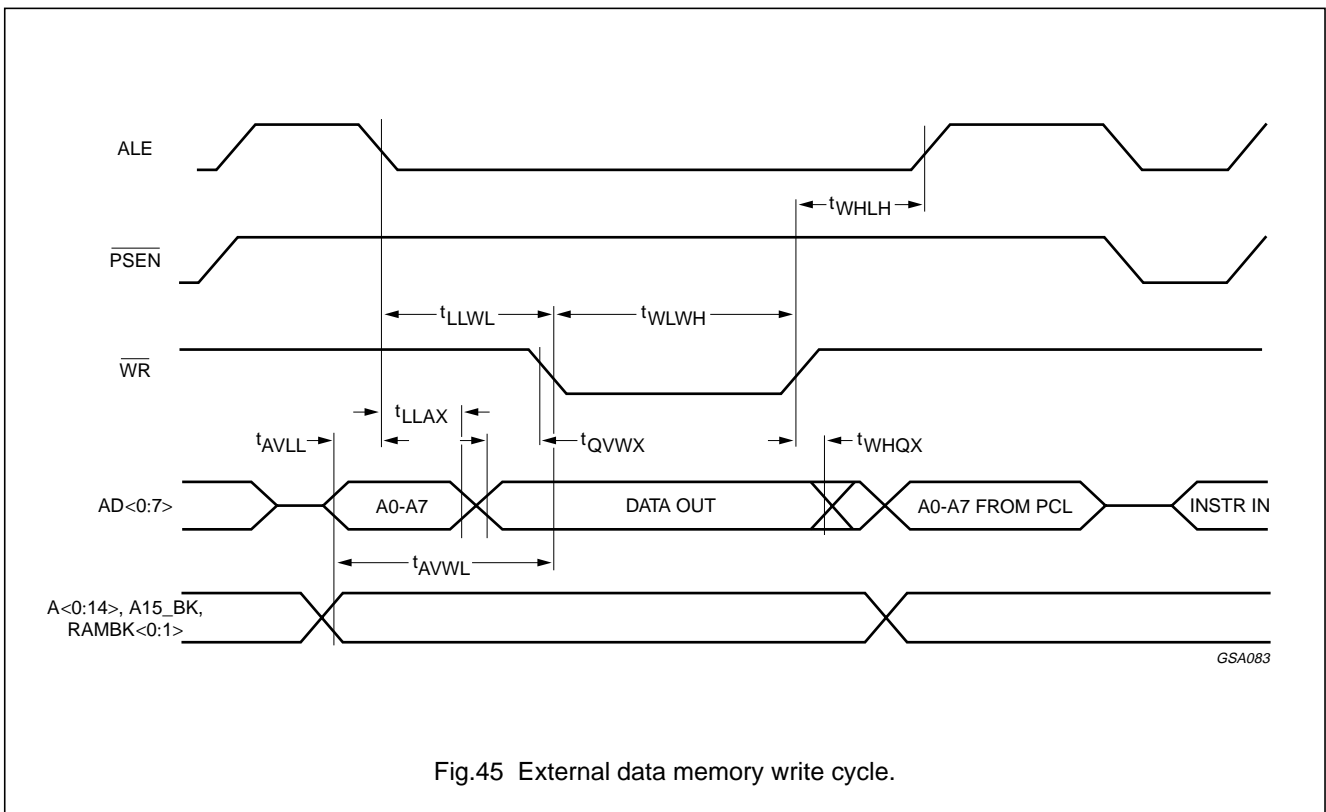


Fig.45 External data memory write cycle.

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### 31 EMC GUIDELINES

Optimization of circuit return paths and minimization of common mode emission will be assisted by using a double sided printed-circuit board with low inductance ground plane.

On a single sided printed-circuit board, a local ground plane under the whole IC should be present, as shown in Fig.46. This should be connected by the widest possible connection back to the PCB ground connection, and bulk electrolytic decoupling capacitor. It should preferably not connect to other grounds on the way and no wire links should be present in this connection. The use of wire links increases ground bounce by introducing inductance into the ground.

The supply pins can be decoupled at the pin to the ground plane under the IC. This is easily accomplished using surface mount capacitors, which are more effective than leaded components at high frequency.

Using a device socket will unfortunately add to the area and inductance of the external bypass loop.

A ferrite bead or inductor with resistive characteristics at high frequencies may be utilised in the supply line close to the decoupling capacitor to provide a high impedance. To prevent pollution by conduction onto the signal lines (which may then radiate), signals connected to the  $V_{DD}$  supply via a pull-up resistor should not be connected to the IC side of this ferrite component.

Pin OSCGND should be connected only to the crystal load capacitors and not the local or circuit GND.

Physical connection distances to associated active devices should be short.

Output traces should be routed with close proximity mutually coupled ground return paths.

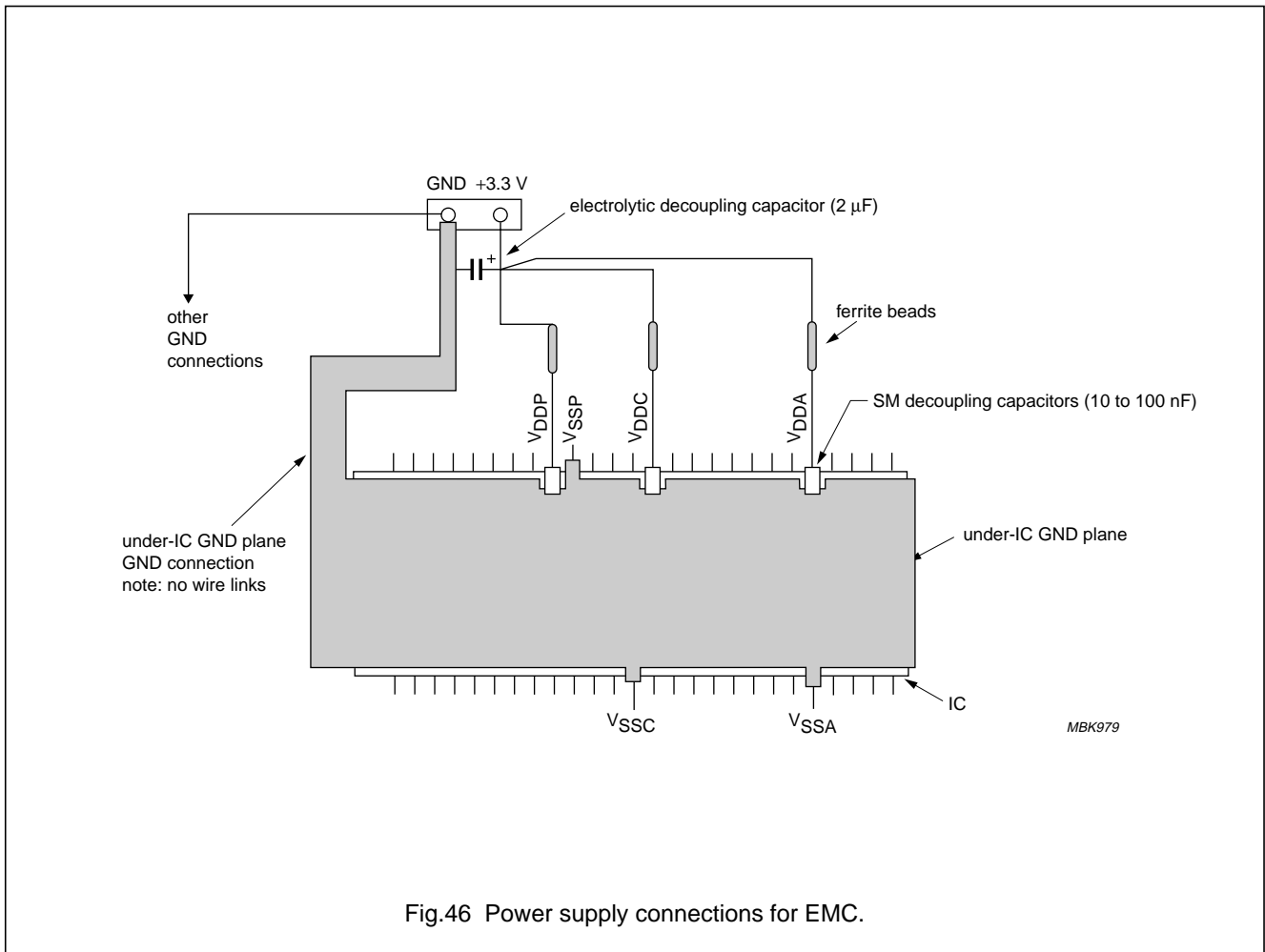


Fig.46 Power supply connections for EMC.

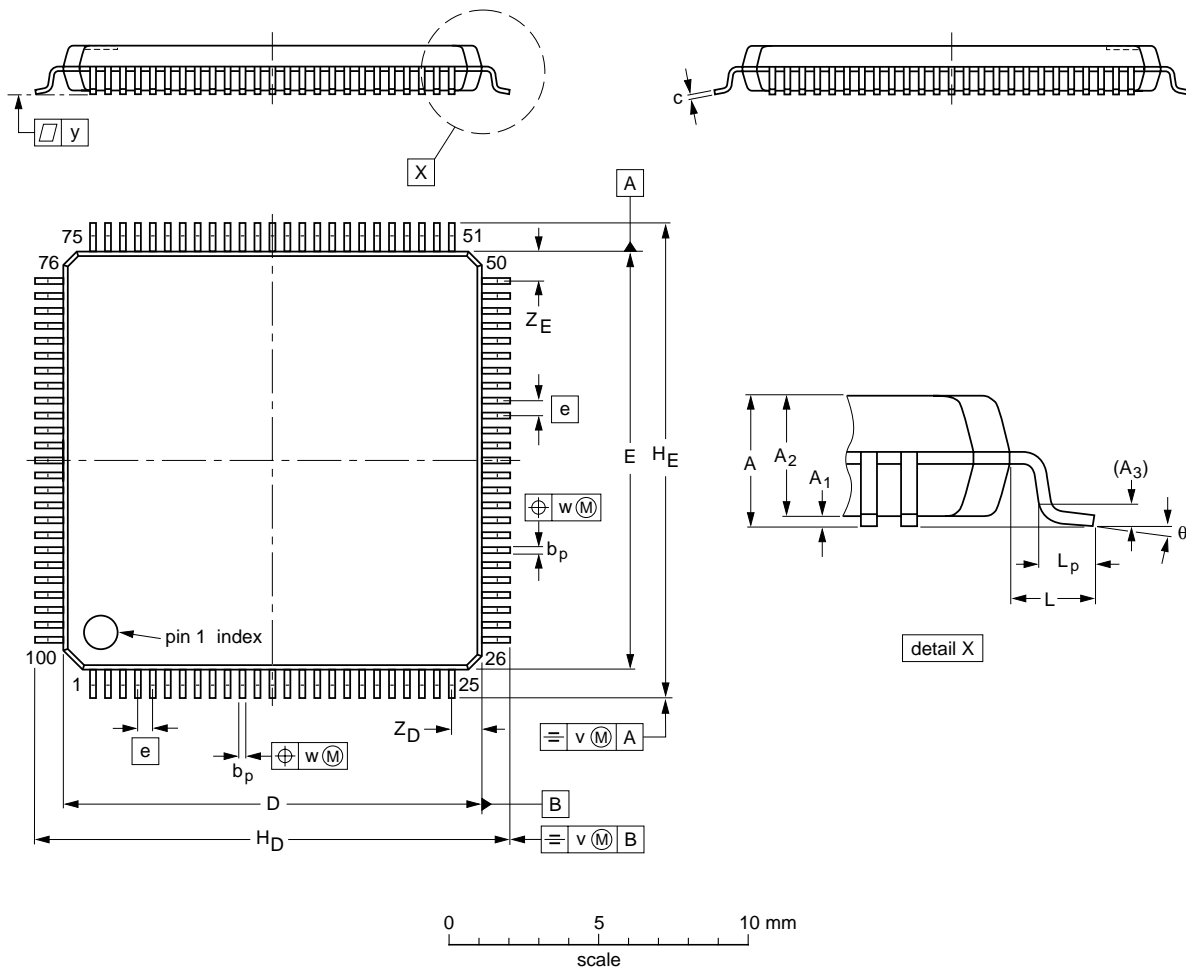
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## 32 PACKAGE OUTLINE

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm

SOT407-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>D</sub>	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup>	Z <sub>E</sub> <sup>(1)</sup>	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1.0	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT407-1	136E20	MS-026				00-01-19 00-02-01

## Enhanced TV microcontrollers with On-Screen Display (OSD)

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### 33 SOLDERING

#### 33.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

#### 33.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

#### 33.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### 33.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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### 33.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW <sup>(1)</sup>
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable <sup>(2)</sup>	suitable
PLCC <sup>(3)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(3)(4)</sup>	suitable
SSOP, TSSOP, VSO	not recommended <sup>(5)</sup>	suitable

#### Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

### 34 DATA SHEET STATUS

DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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- The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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### 35 DEFINITIONS

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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