Stereo BTL audio output amplifier with DC volume control

TDA7053A

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and switch-off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7053A (2 × 1 W) and TDA7053AT (2 × 0.5 W) are stereo BTL output amplifiers with DC volume control. The devices are designed for use in TV and monitors, but are also suitable for battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		4.5	–	18	V
P_{out}	output power	V_P = 6 V				
	TDA7053A	R_L = 8 Ω	0.85	1.0	–	W
	TDA7053AT	R_L = 16 Ω	0.5	0.6	–	W
G_v	voltage gain		39.5	40.5	41.5	dB
G_C	gain control		68.0	73.5	–	dB
$I_{q(tot)}$	total quiescent current	V_P = 6 V; R_L = ∞	–	22	25	mA
THD	total harmonic distortion					
	TDA7053A	P_{out} = 0.5 W	–	0.3	1	%
	TDA7053AT	P_{out} = 0.25 W	–	0.3	1	%

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA7053A	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
TDA7053AT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

BLOCK DIAGRAM

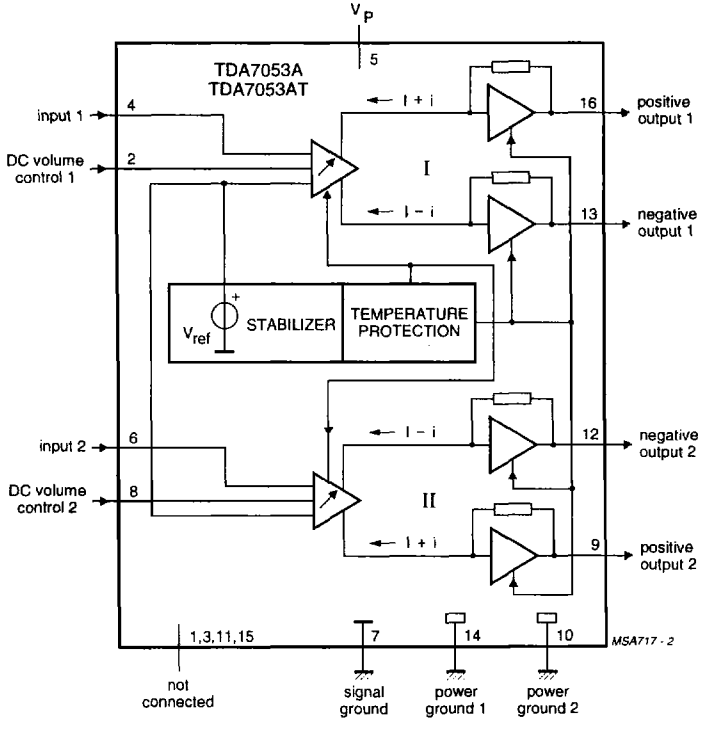


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
VC1	2	DC volume control 1
n.c.	3	not connected
$V_{I(1)}$	4	voltage input 1
V_P	5	positive supply voltage
$V_{I(2)}$	6	voltage input 2
SGND	7	signal ground
VC2	8	DC volume control 2
OUT2+	9	positive output 2
PGND2	10	power ground 2
n.c.	11	not connected
OUT2−	12	negative output 2
OUT1−	13	negative output 1
PGND1	14	power ground 1
n.c.	15	not connected
OUT1+	16	positive output 1

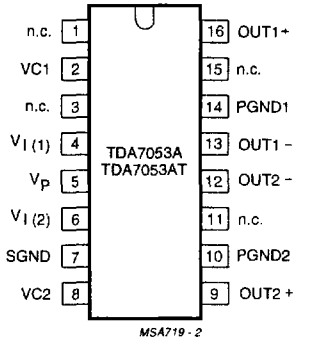


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA7053A and TDA7053AT are stereo output amplifiers with two DC volume control stages, designed for TV and monitors, but also suitable for battery-fed portable recorders and radios.

In conventional DC volume control circuits the control or input stage is AC coupled to the output stage via external capacitors to keep the offset voltage low.

The two DC volume control stages are integrated into the input stages so that no coupling capacitors are required and a low offset voltage is still maintained. The minimum supply voltage also remains low.

The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.

Consequently, a reduced power supply with smaller capacitors can be used which results in cost reductions.

For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 40.5 dB. The DC volume control stages have a logarithmic control characteristic. Therefore, the total gain can be controlled from +40.5 to −33 dB.

If the DC volume control voltage falls below 0.4 V, the device will switch to the mute mode.

The amplifier is short-circuit protected to ground, V_P and across the load. A thermal protection circuit is also implemented. If the crystal temperature rises above 150 °C the gain will be reduced, thereby reducing the output power.

Special attention is given to switch-on and switch-off clicks, low HF radiation and a good overall stability.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	18	V
I_{ORM}	repetitive peak output current		–	1.25	A
I_{OSM}	non-repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C			
	TDA7053A		–	2.5	W
	TDA7053AT		–	1.32	W
t_{sc}	short-circuit time		–	1	hr
V_n	input voltage pins 2, 4, 6 and 8		–	5	V
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TDA7053A	50	K/W
	TDA7053AT	95	K/W

Power dissipation

TDA7053A:

Assume $V_P = 6$ V and $R_L = 8\ \Omega$.

The maximum sine wave dissipation is 2×0.9 W = 1.8 W.

The $R_{th\ j\text{-}a}$ of the package is 50 K/W therefore $T_{amb(max)} = 150 - (50 \times 1.8) = 60$ °C.

TDA7053AT:

Assume $V_P = 6$ V and $R_L = 16\ \Omega$.

The maximum sine wave dissipation is 2×0.46 W = 0.92 W.

The $R_{th\ j\text{-}a}$ of the package is 95 K/W therefore $T_{amb(max)} = 150 - (95 \times 0.92) = 62.6$ °C.

CHARACTERISTICS

V_P = 6 V; T_{amb} = 25 °C; f_i = 1 kHz; TDA7053A: R_L = 8 Ω; TDA7053AT: R_L = 16 Ω; unless otherwise specified (see Fig.13).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		4.5	–	18	V
$I_{q(tot)}$	total quiescent current	V_P = 6 V; R_L = ∞; note 1	–	22	25	mA
Maximum gain; $V_{2,8} \geq$ 1.4 V						
P_{out}	output power	THD = 10%				
	TDA7053A		1.0	1.1	–	W
	TDA7053AT		0.5	0.6	–	W
THD	total harmonic distortion					
	TDA7053A	P_{out} = 0.5 W	–	0.3	1	%
	TDA7053AT	P_{out} = 0.25 W	–	0.3	1	%
G_v	voltage gain		39.5	40.5	41.5	dB
$V_{I(rms)}$	input signal handling (RMS value)	G_v = 0 dB; THD < 1%	1	–	–	V
V_{no}	noise output voltage	f_i = 500 kHz; note 2	–	210	–	μV
B	bandwidth	at −1 dB	–	note 3	–	Hz
SVRR	supply voltage ripple rejection	note 4	34	38	–	dB
$V_{O(os)}$	DC output offset voltage	$\lvert V_{16} - V_{13} \rvert$ and $\lvert V_{12} - V_9 \rvert$	–	0	200	mV
Z_i	input impedance (pins 4 and 6)		15	20	25	kΩ
α_{cs}	channel separation	R_S = 5 kΩ	40	–	–	dB
$\lvert G_v \rvert$	channel unbalance	note 5	–	–	1	dB
		G_1 = 0 dB; note 6	–	–	1	dB
Mute position; $V_{2,8}$ = 0.4 V ±30 mV						
V_O	output voltage in mute position	V_i = 1.0 V; note 7	–	–	30	μV
DC volume control						
G_C	gain control		68.5	73.5	–	dB
I_{DC}	volume control current	$V_2 = V_8$ = 0 V	−20	−25	−30	μA

Notes

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L.
2. The noise output voltage (RMS value) at f_i = 500 kHz is measured with R_S = 0 Ω and bandwidth = 5 kHz.
3. 20 Hz to 300 kHz (typical).
4. The ripple rejection is measured with R_S = 0 Ω and f_i = 100 Hz to 10 kHz. The ripple voltage of 200 mV (RMS value) is applied to the positive supply rail.
5. The channel unbalance is measured with $V_{DC1} = V_{DC2}$.
6. The channel unbalance at G_1 = 0 dB is measured with $V_{DC1} = V_{DC2}$.
7. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted.

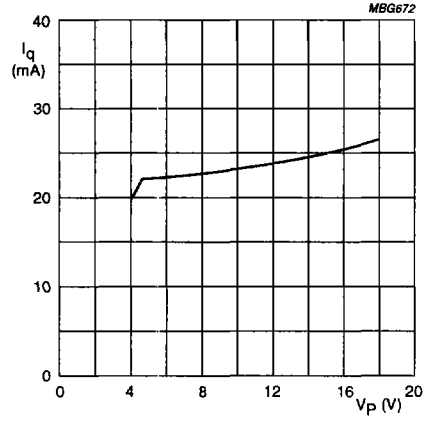
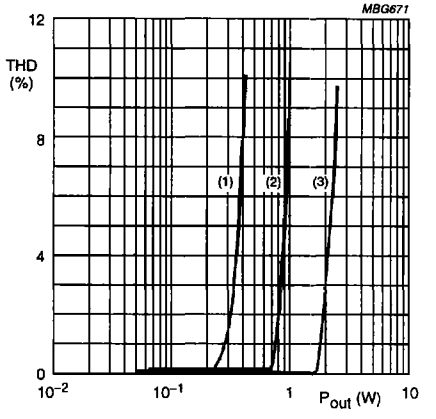
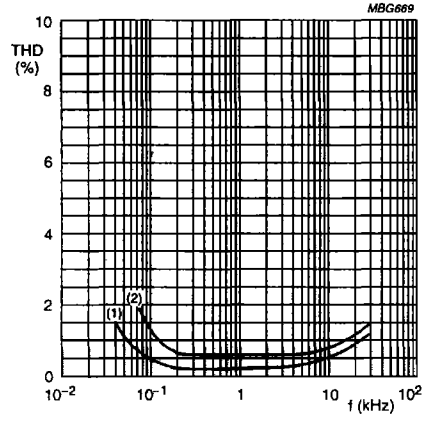


Fig.3 Quiescent current as a function of supply voltage.



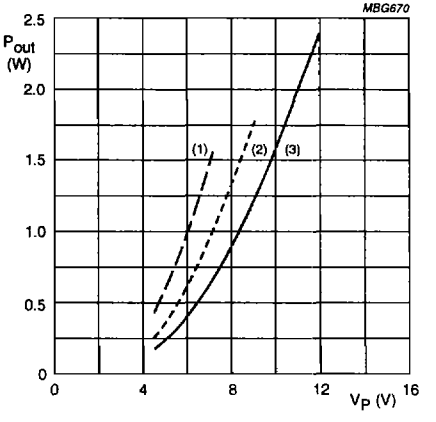
(1) V_P = 4.5 V.
(2) V_P = 6 V; R_L = 8 Ω.
(3) V_P = 12 V; R_L = 25 Ω.

Fig.4 THD as a function of output power.



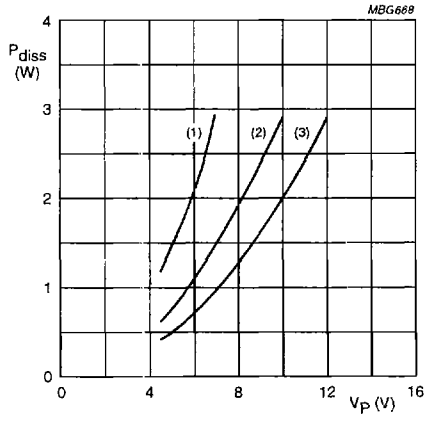
(1) G_v = 30 dB; P_o = 0.1 W.
(2) G_v = 40 dB; P_o = 0.1 W.

Fig.5 THD as a function of frequency.



(1) R_L = 8 Ω.
(2) R_L = 16 Ω.
(3) R_L = 25 Ω.

Fig.6 Output power as a function of supply voltage.



(1) R_L = 8 Ω.
(2) R_L = 16 Ω.
(3) R_L = 25 Ω.

Fig.7 Total worst case power dissipation as a function of supply voltage.

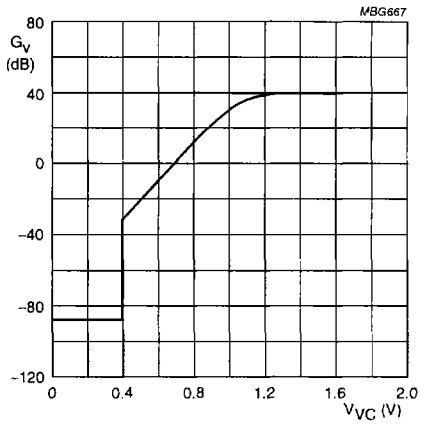
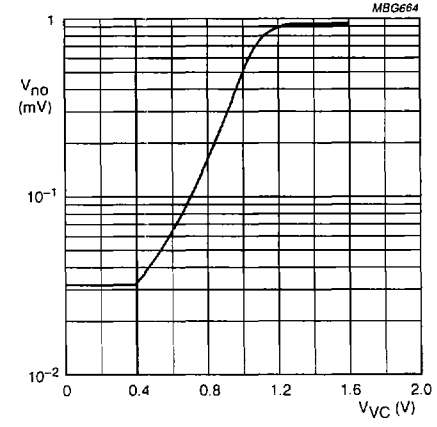
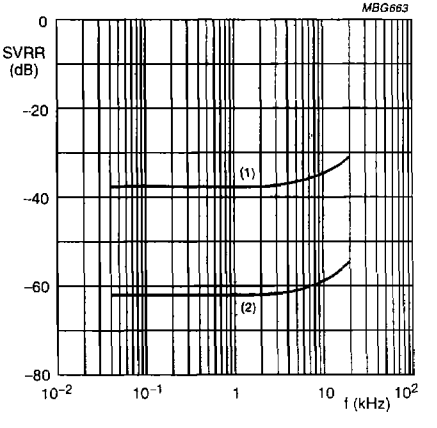


Fig.8 Voltage gain as a function of volume control voltage.



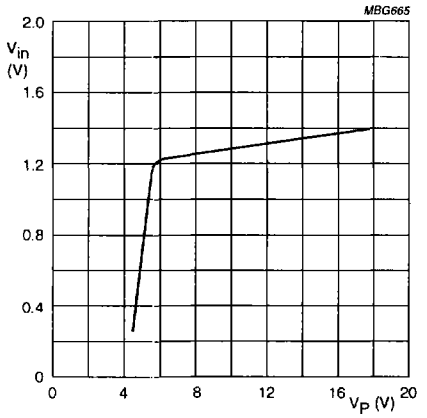
f = 22 Hz to 22 kHz.

Fig.9 Noise voltage as a function of volume control voltage.



(1) V_{DC} = 1.4 V; V_{ripple} = 0.2 V.
(2) V_{DC} = 0.4 V; V_{ripple} = 0.2 V.

Fig.10 SVRR as a function of frequency.



THD = 1 %.

Fig.11 Input signal handling.

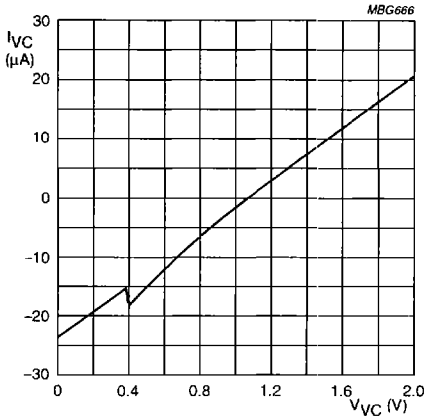


Fig.12 Volume control current as a function of volume control voltage.

APPLICATION INFORMATION

The application diagram is illustrated in Fig.13.

Test conditions

T_{amb} = 25 °C unless otherwise specified; V_P = 6 V; V_{DC} = 1.4 V; f_i = 1 kHz; R_L = 8 Ω.

The quiescent current has been measured without load impedance.

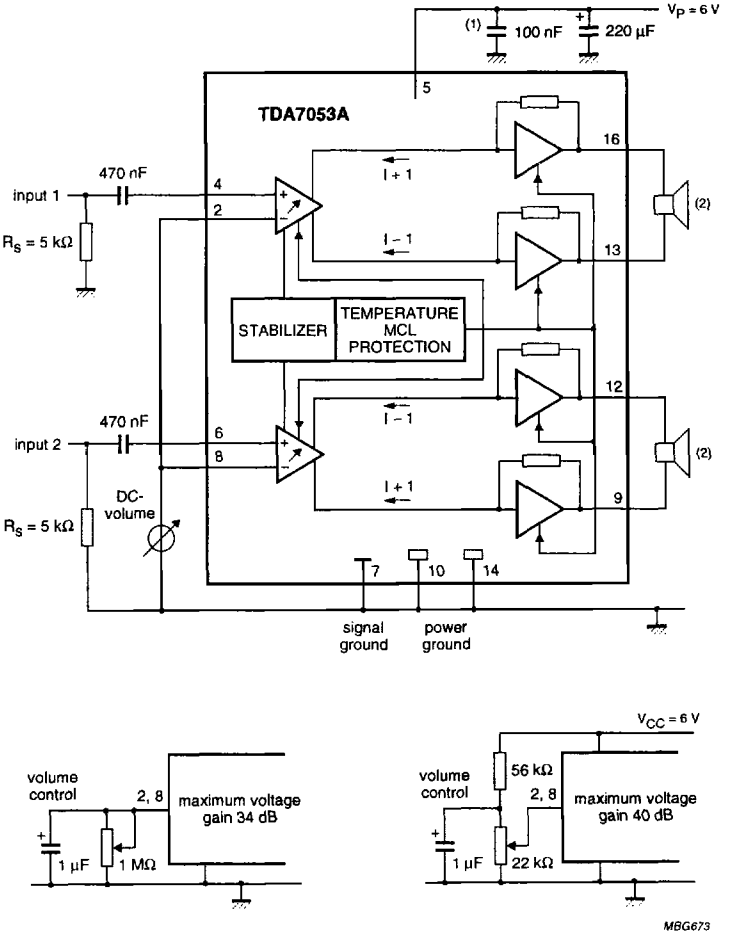
The output power as a function of the supply voltage has been measured at THD = 10%. The maximum output power is limited by the maximum power dissipation and the maximum available output current.

The maximum input signal voltage is measured at THD = 1% at the output with a voltage gain of 0 dB.

To avoid instabilities and too high distortion, the input ground and power ground must be separated as far as possible and connected as close as possible to the IC.

The DC volume control can be applied in several ways. Two possible circuits are shown below the main application diagram. The circuits at the control pin will influence the switch-on and switch-off behaviour and the maximum voltage gain.

For single-end applications the output peak current must not exceed 100 mA. At higher output currents the short-circuit protection (MCL) will be active.



(1) This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 5.
(2) R_L = 8 Ω.

Fig.13 Test and application diagram.