



SiI9187B HDMI Port Processor

Data Brief

Document # SiI-DB-1071-A02

September 2010

Copyright Notice

Copyright © 2009-2010 Silicon Image, Inc. All rights reserved. These materials contain proprietary and confidential information (including trade secrets, copyright, and other interests) of Silicon Image, Inc. You may not use these materials except only for your bona fide non-commercial evaluation of your potential purchase of products and/or services from Silicon Image or its affiliates, and/or only in connection with your purchase of products and/or services from Silicon Image or its affiliates, and only in accordance with the terms and conditions herein. You have no right to copy, modify, transfer, sublicense, publicly display, create derivative works of or distribute these materials, or otherwise make these materials available, in whole or in part, to any third party.

Trademark Acknowledgment

Silicon Image™, VastLane™, SteelVine™, PinnaClear™, Simplay™, Simplay HD™, Satalink, InstaPort™, TMDS™, and LiquidHD™ are trademarks or registered trademarks of Silicon Image, Inc. in the United States and other countries. HDMI®, the HDMI logo and High-Definition Multimedia Interface™ are trademarks or registered trademarks of, and are used under license from, HDMI Licensing, LLC. x.v.Color™ is a trademark of Sony Corporation.

Export Controlled Document

This document contains information subject to the Export Administration Regulations (EAR) and has a classification of EAR99 or is controlled for Anti-Terrorism (AT) purposes. Transfer of this information by any means to an EAR Country Group E:1 or foreign national thereof (whether in the U.S. or abroad) may require an export license or other approval from the U.S. Department of Commerce. For more information, contact the Silicon Image Director of Global Trade Compliance.

Further Information

To request other materials, detailed hardware and software guides, and additional information, contact your local Silicon Image, Inc. sales office or visit the Silicon Image, Inc. web site at www.siliconimage.com. Information about obtaining licenses required for using HDMI and HDCP technologies is available from www.hdmi.org and www.digital-cp.com.

© 2009-2010 Silicon Image, Inc. All rights reserved.

Introduction

The SiI9187B HDMI Port Processor is the second generation of HDMI® devices that support the HDMI Specification. With four HDMI inputs and a single output, the SiI9187B port processor enhances the functionality of digital TVs using single system on a chip (SoC) solutions with integrated HDMI receivers. The port processor provides a simple, low-cost method of retransmitting digital audio and video to give consumers a truly all-digital experience. Built-in backward compatibility with DVI 1.0 allows HDMI systems to connect to any DVI 1.0 source.

Features

The SiI9187B device brings cutting edge innovations, such as:

- Enhanced cable equalization for long cable support, even at Deep Color resolutions that enables the SiI9187B device to work with noisy signals and many sources, making the sink devices highly interoperable
- Integrated EDID and CEC functions
- Improved ESD protection on all signals connected to the HDMI connector.

HDMI Inputs and Output

- Four HDMI input ports and single output port
- HDMI, HDCP, and DVI compatibility
- TMDS™ cores run at 25–225 MHz
- Supports video resolutions up to 1080p, 60 Hz, 12-bit or 720p/1080i, 120 Hz, 12-bit.

Control Capability

- Consumer Electronics Control (CEC) interface incorporates an HDMI-compliant CEC I/O and an integrated CEC Programming Interface (CPI); these simplify design and lower cost and software overhead
- Integrated EDID and DDC support for 4 HDMI/DVI ports and 1 VGA port with a 256-byte NVRAM shared between ports that loads into separate 256-byte SRAM for each of 5 ports
- Individual control of Hot Plug Detect (HPD) for each of the 4 HDMI/DVI ports
- TPWR (TMDS clock detect) output to help speed soft mute of audio while plugging and unplugging cables
- Controllable by the local I²C bus.

Power Management

- Flexible power management provides extremely low standby power consumption
- Standby power can be supplied from a separate +3.3 V or 5 V standby power pin
- Port power only can be used to read EDID
- Single power 3.3-V source
- Integrated 5 V to 3.3 V Voltage regulator.

Package

- 72-pin, 10 mm x 10 mm, 0.5 mm pitch QFN package with enhanced ePad™.

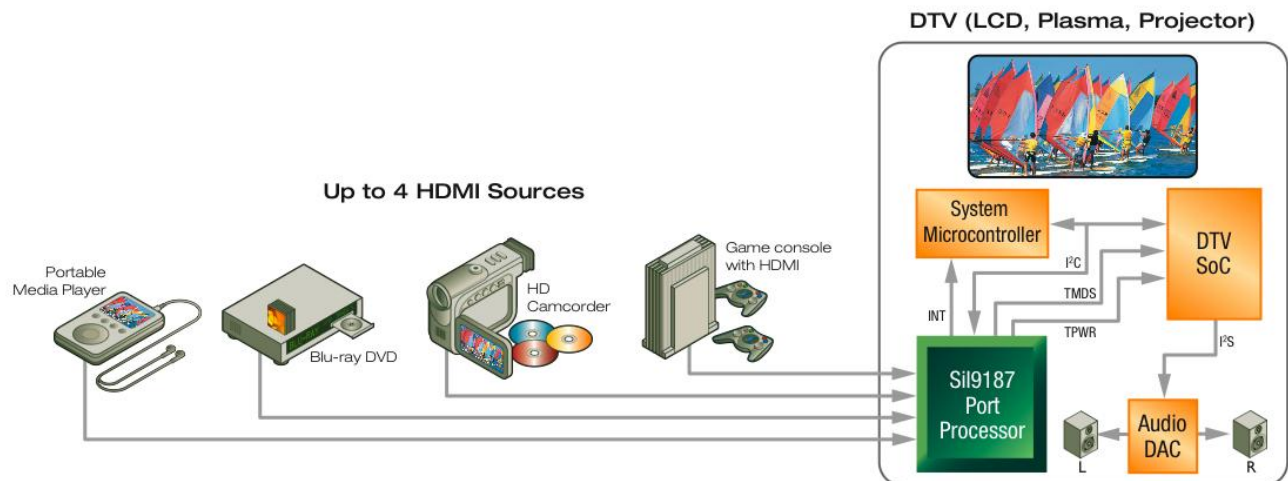
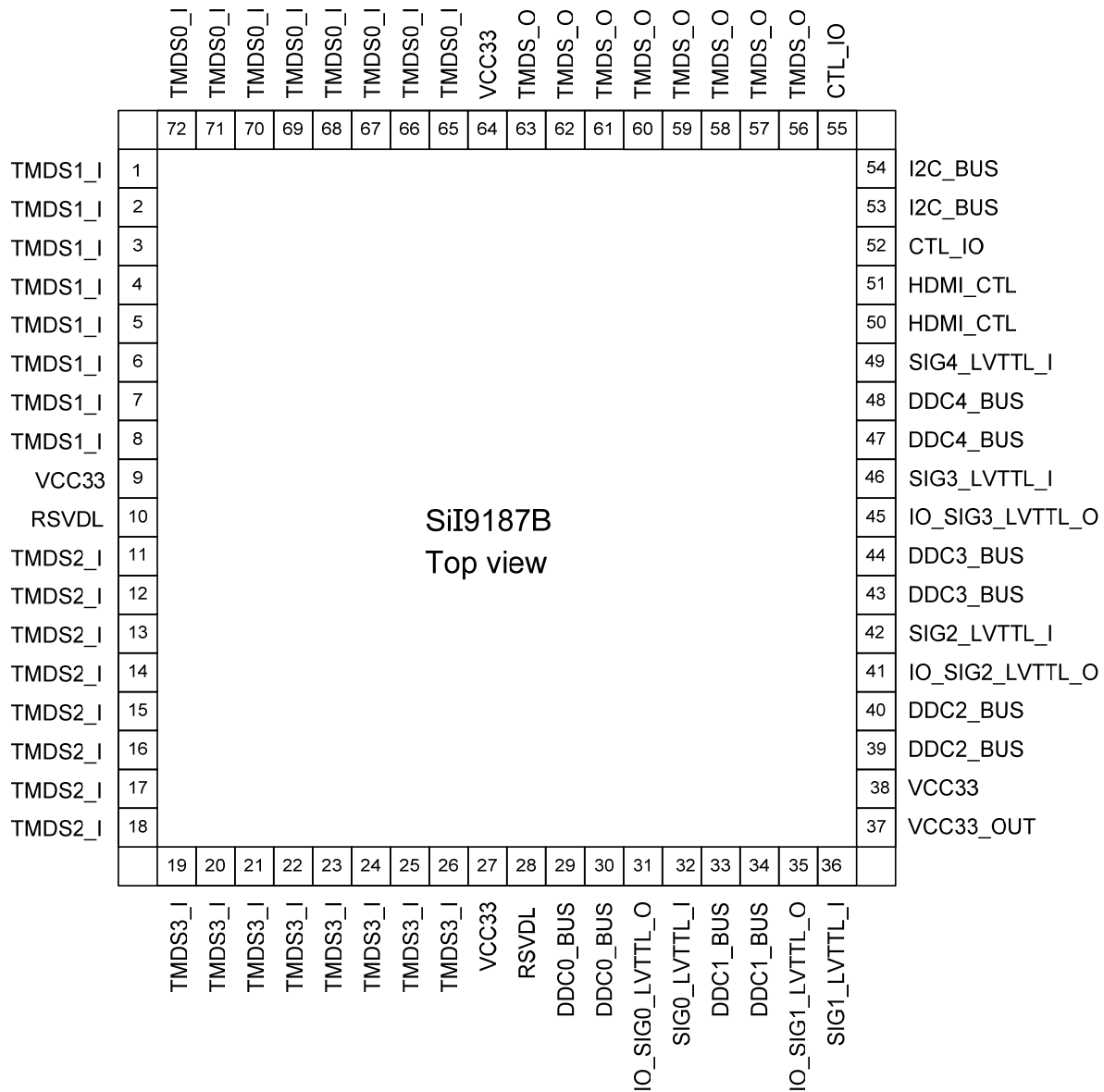


Figure 1. Typical Application of SiI9187B HDMI Port Processor

Pin Diagram

Figure 2 shows the pin diagram for the SiI9187B port processor. Pin names are generalized by type for this document. The list below the diagram describes the purpose of each type.



TMDS0/1/2/3_I-- TMDS Input Port-Specific Signals DDC0/1/2/3_BUS-- DDC Port-Specific Bus, OD, 5-V Tolerant
 SIG0/1/2/3/4_LVTTL_I-- TMDS Port Power Signal, 5-V Tolerant I2C_BUS-- I²C Bus, 5-V Tolerant
 IO_SIG0/1/2/3/_LVTTL_O-- TMDS Port Detect, 5-V Tolerant/MHL IO CTL_IO-- Control Input or Output
 HDMI_CTL-- HDMI CEC Control Signals RSVDL-- Reserved, tie to ground
 TMDS_O-- TMDS Output Port-Specific Signals

Figure 2. Pin Diagram (Top View)

Package Information

ePad Requirements

The SiI9187B HDMI Port Processor is packaged in a 72-pin 10 mm x 10 mm QFN package with an ExposedPad™ (ePad) that is used for the electrical ground of the chip and for improved thermal transfer characteristics. The ePad dimensions are 4.7 mm x 4.7 mm with a tolerance of ± 0.15 mm. Soldering the ePad to the ground plane of the PCB is **required** to meet package power dissipation requirements at full speed operation and to connect the chip circuitry to electrical ground. A clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid electrical shorts.

The thermal land area on the PCB can use thermal vias to improve heat removal from the package. These thermal vias can double as ground connections, attaching internally in the PCB to the ground plane. An array of vias can be designed into the PCB beneath the package. For optimum thermal performance, Silicon Image recommends that the via diameter be 12 to 13 mils (0.30 to 0.33 mm) and the via barrel be plated with 1-ounce copper to plug the via. This plating helps avoid solder wicking inside the via during the soldering process, which can result in voids in solder between the exposed pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be tented with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1 mm) larger than the via diameter.

Package stand-off is also a consideration. For a nominal stand-off of approximately 0.1 mm the stencil thickness of 5 to 8 mils should provide a good solder joint between the ePad and the thermal land.

[Figure 3](#) on the next page shows the package dimensions of the SiI9187B package.

Package Dimensions

These drawings are not to scale.

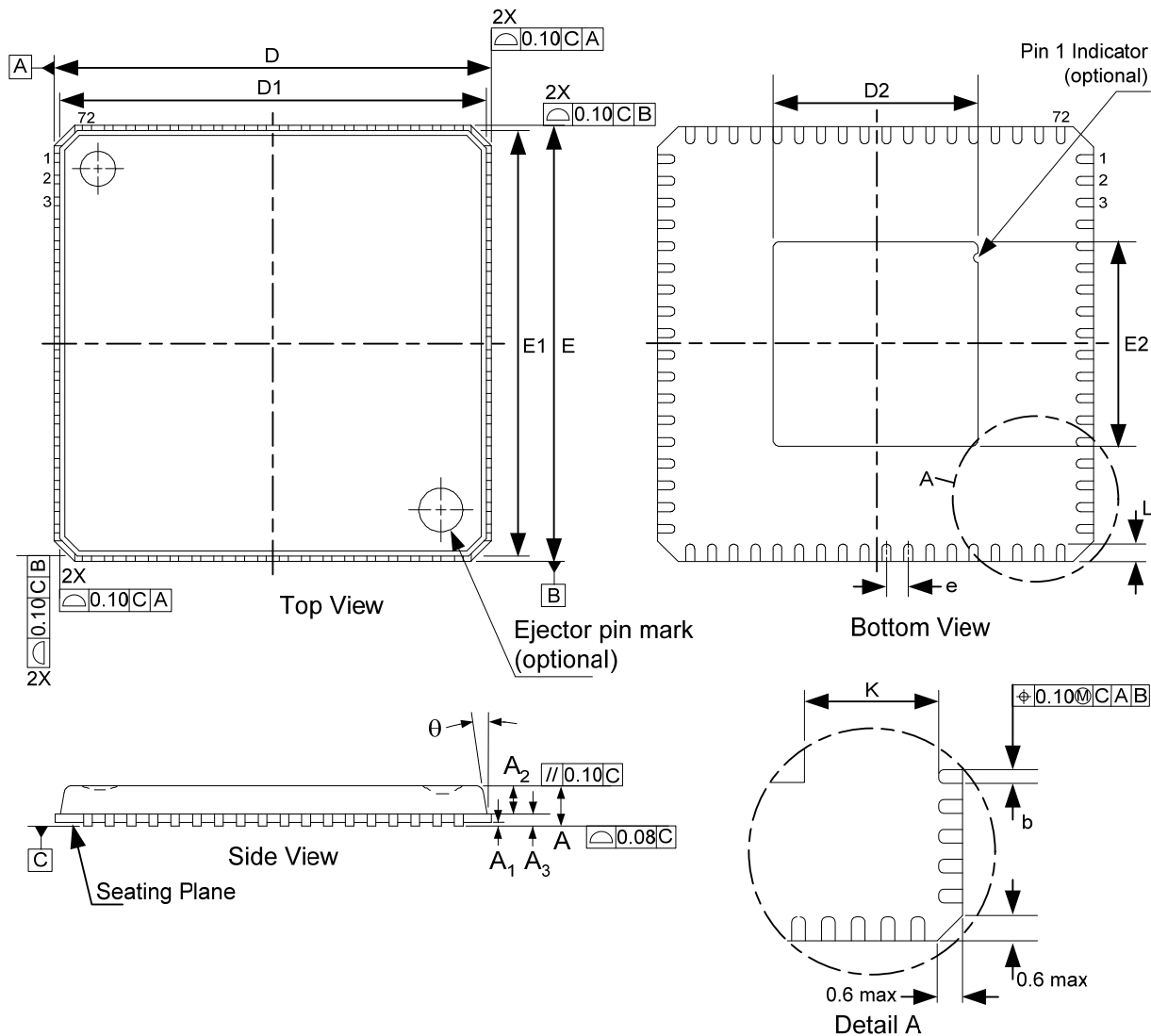


Figure 3. Package Diagram
JEDEC Package Code MO-220

| Item | Description | Min | Typ | Max |
|------|----------------|-----------|------|------|
| A | Thickness | — | 0.85 | 0.90 |
| A1 | Stand-off | 0.00 | 0.01 | 0.05 |
| A2 | Body thickness | — | 0.65 | 0.70 |
| A3 | Base thickness | 0.20 REF | | |
| D | Footprint | 10.00 BSC | | |
| E | Footprint | 10.00 BSC | | |
| D1 | Body size | 9.75 BSC | | |
| E1 | Body size | 9.75 BSC | | |

| Item | Description | Min | Typ | Max |
|----------|-----------------------|----------|------|------|
| D2 | ePad size | 4.55 | 4.70 | 4.85 |
| E2 | ePad size | 4.55 | 4.70 | 4.85 |
| b | Plated lead width | 0.18 | 0.23 | 0.30 |
| e | Lead pitch | 0.50 BSC | | |
| K | ePad-to-pin clearance | 0.20 | — | — |
| L | Lead foot length | 0.30 | 0.40 | 0.50 |
| θ | Lead foot angle | — | — | 14° |

Marking Specification

This drawing is not to scale.

Pin 1 location

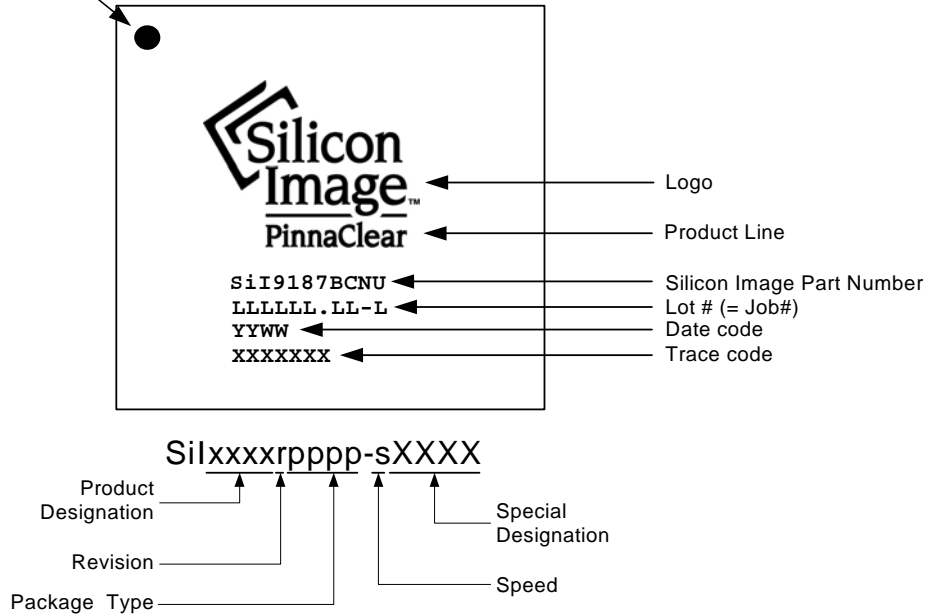


Figure 4. Marking Diagram

Ordering Information

Production Part Numbers:

| Device | Part Number |
|----------|-------------|
| Standard | SiI9187BCNU |

The universal package may be used in lead-free and ordinary process lines.

Disclaimers

These materials are provided on an “AS IS” basis. Silicon Image, Inc. and its affiliates disclaim all representations and warranties (express, implied, statutory or otherwise), including but not limited to: (i) all implied warranties of merchantability, fitness for a particular purpose, and/or non-infringement of third party rights; (ii) all warranties arising out of course-of-dealing, usage, and/or trade; and (iii) all warranties that the information or results provided in, or that may be obtained from use of, the materials are accurate, reliable, complete, up-to-date, or produce specific outcomes. Silicon Image, Inc. and its affiliates assume no liability or responsibility for any errors or omissions in these materials, makes no commitment or warranty to correct any such errors or omissions or update or keep current the information contained in these materials, and expressly disclaims all direct, indirect, special, incidental, consequential, reliance and punitive damages, including WITHOUT LIMITATION any loss of profits arising out of your access to, use or interpretation of, or actions taken or not taken based on the content of these materials.

Silicon Image, Inc. and its affiliates reserve the right, without notice, to periodically modify the information in these materials, and to add to, delete, and/or change any of this information.

Notwithstanding the foregoing, these materials shall not, in the absence of authorization under U.S. and local law and regulations, as required, be used by or exported or re-exported to (i) any U.S. sanctioned or embargoed country, or to nationals or residents of such countries; or (ii) any person, entity, organization or other party identified on the U.S. Department of Commerce's Denied Persons or Entity List, the U.S. Department of Treasury's Specially Designated Nationals or Blocked Persons List, or the Department of State's Debarred Parties List, as published and revised from time to time; (iii) any party engaged in nuclear, chemical/biological weapons or missile proliferation activities; or (iv) any party for use in the design, development, or production of rocket systems or unmanned air vehicles.

Products and Services

The products and services described in these materials, and any other information, services, designs, know-how and/or products provided by Silicon Image, Inc. and/or its affiliates are provided on an “AS IS” basis, except to the extent that Silicon Image, Inc. and/or its affiliates provides an applicable written limited warranty in its standard form license agreements, standard Terms and Conditions of Sale and Service or its other applicable standard form agreements, in which case such limited warranty shall apply and shall govern in lieu of all other warranties (express, statutory, or implied). EXCEPT FOR SUCH LIMITED WARRANTY, SILICON IMAGE, INC. AND ITS AFFILIATES DISCLAIM ALL REPRESENTATIONS AND WARRANTIES (EXPRESS, IMPLIED, STATUTORY OR OTHERWISE), REGARDING THE INFORMATION, SERVICES, DESIGNS, KNOW-HOW AND PRODUCTS PROVIDED BY SILICON IMAGE, INC. AND/OR ITS AFFILIATES, INCLUDING BUT NOT LIMITED TO, ALL IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND/OR NON-INFRINGEMENT OF THIRD PARTY RIGHTS. YOU ACKNOWLEDGE AND AGREE THAT SUCH INFORMATION, SERVICES, DESIGNS, KNOW-HOW AND PRODUCTS HAVE NOT BEEN DESIGNED, TESTED, OR MANUFACTURED FOR USE OR RESALE IN SYSTEMS WHERE THE FAILURE, MALFUNCTION, OR ANY INACCURACY OF THESE ITEMS CARRIES A RISK OF DEATH OR SERIOUS BODILY INJURY, INCLUDING, BUT NOT LIMITED TO, USE IN NUCLEAR FACILITIES, AIRCRAFT NAVIGATION OR COMMUNICATION, EMERGENCY SYSTEMS, OR OTHER SYSTEMS WITH A SIMILAR DEGREE OF POTENTIAL HAZARD. NO PERSON IS AUTHORIZED TO MAKE ANY OTHER WARRANTY OR REPRESENTATION CONCERNING THE PERFORMANCE OF THE INFORMATION, PRODUCTS, KNOW-HOW, DESIGNS OR SERVICES OTHER THAN AS PROVIDED IN THESE TERMS AND CONDITIONS.



1060 E. Arques Avenue
Sunnyvale, CA 94085
T 408.616.4000 F 408.830.9530
www.siliconimage.com