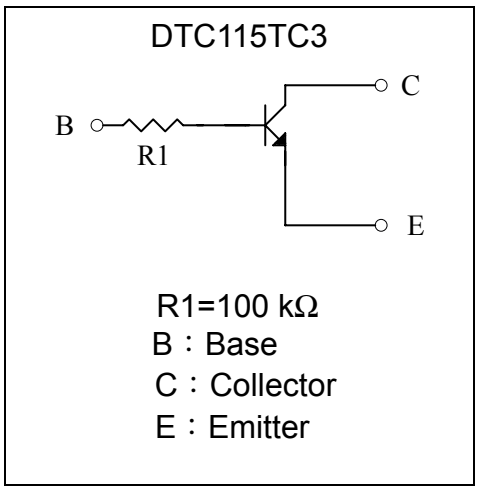
NPN Digital Transistors (Built-in Resistors)

DTC115TC3

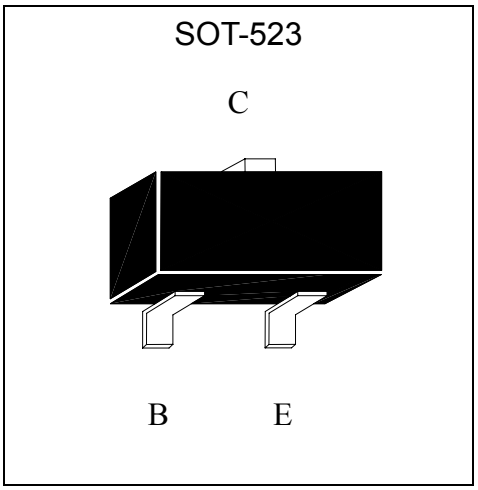
Features

- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- The bias resistors consist of thin-film resistors with complete isolation to allow negative biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- Only the on/off conditions need to be set for operation, making device design easy.
- Complements the DTA115TC3

Equivalent Circuit



Outline



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	50	V
Collector-Emitter Voltage	V_{CEO}	50	V
Emitter-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	100	mA
Power Dissipation	Pd	150	mW
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	-55~+150	°C

Electrical Characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Collector-Base Breakdown Voltage	V_{CBO}	50	-	-	V	I_C=50μA
Collector-Emitter Breakdown Voltage	V_{CEO}	50	-	-	V	I_C=1mA
Emitter-Base Breakdown Voltage	V_{EBO}	5	-	-	V	I_E=50μA
Collector-Base Cutoff Current	I_{CBO}	-	-	0.5	μA	V_{CB}=50V
Emitter-Base Cutoff Current	I_{EBO}	-	-	0.5	μA	V_{EB}=4V
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	-	-	0.3	V	I_C=1mA, I_B=0.1mA
DC Current Gain	h_{FE}	100	-	600	-	V_{CE}=5V, I_C=1mA
Input Resistance	R	70	100	130	kΩ	-
Transition Frequency	f_T	-	250	-	MHz	V_{CE}=10V, I_C=5mA, f=100MHz *

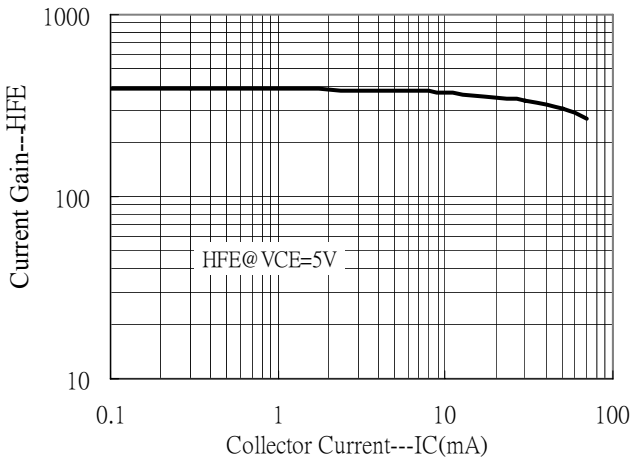
* Transition frequency of the device

Ordering Information

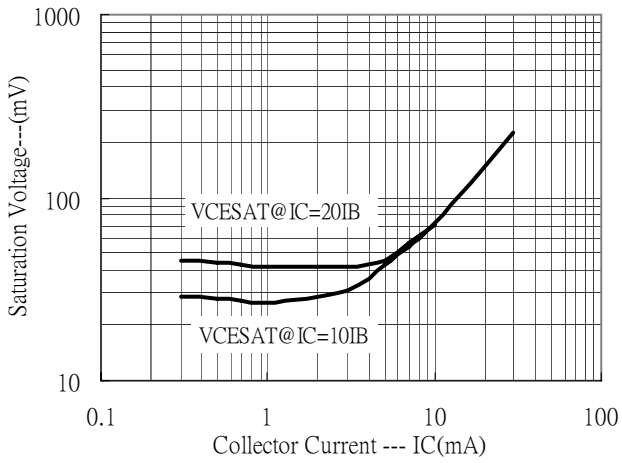
Device	Package	Shipping	Marking
DTC115TC3	SOT-523 (Pb-free & Halogen-free package)	3000 pcs / Tape & Reel	8U

Characteristic Curves

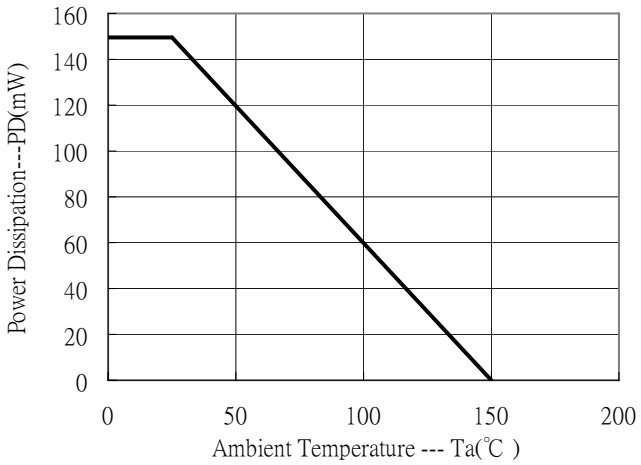
Current Gain vs Collector Current



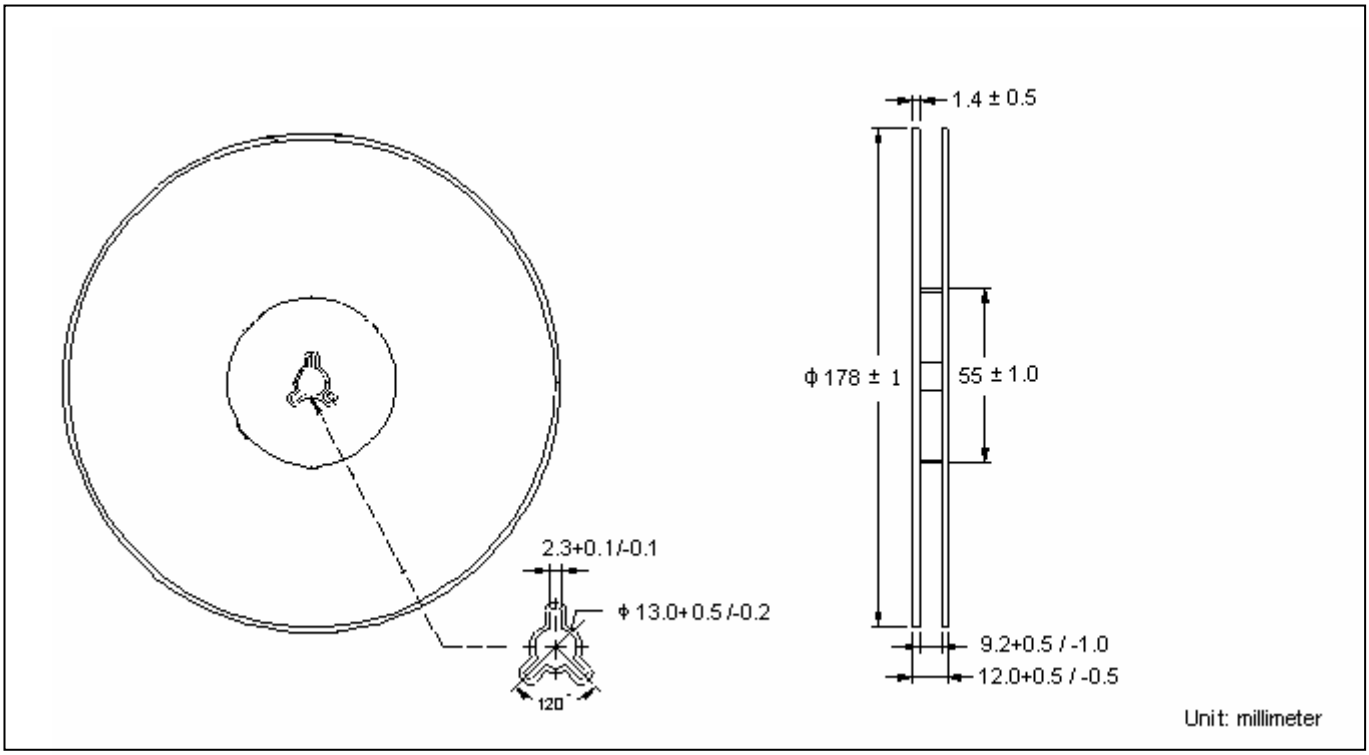
Saturation Voltage vs Collector Current



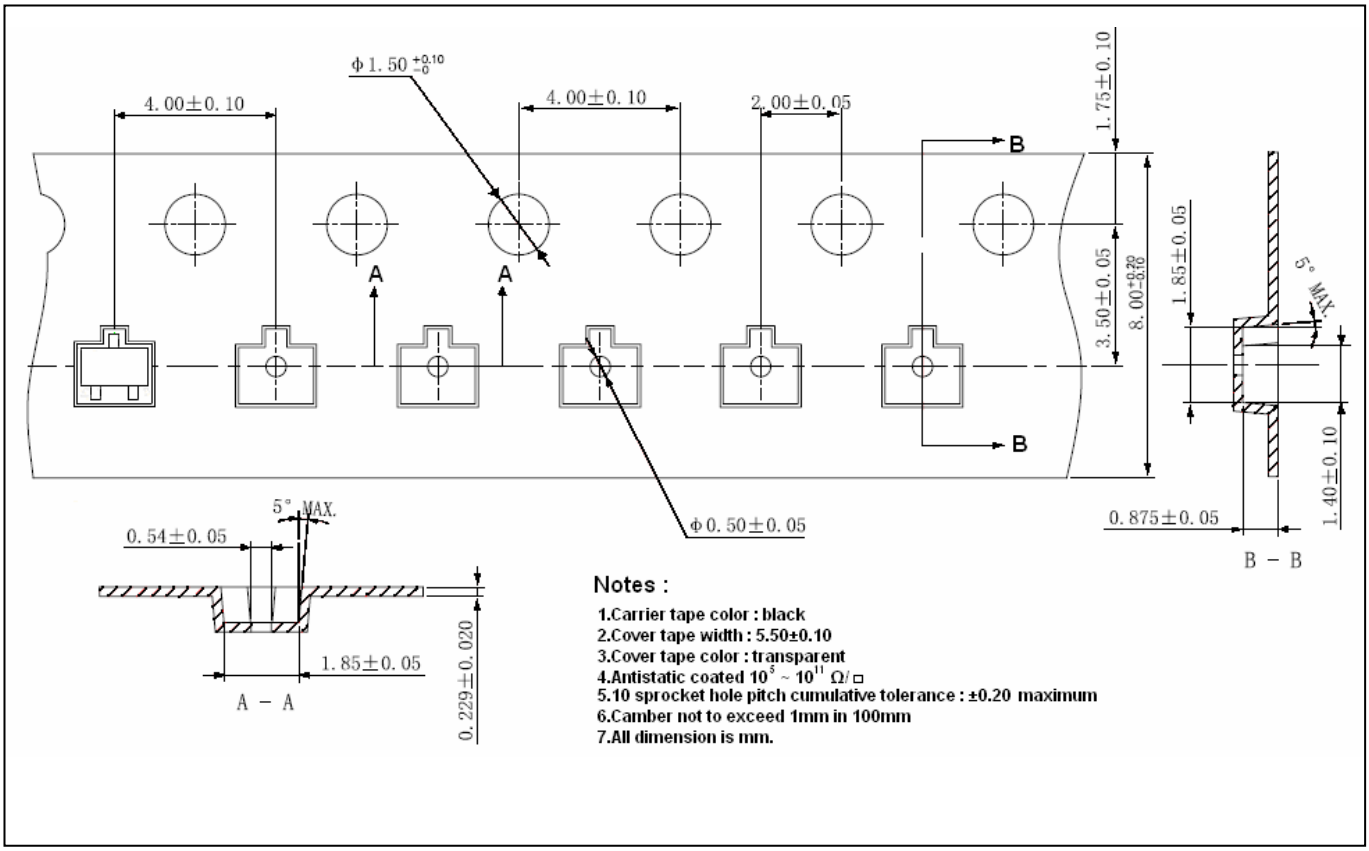
Power Derating Curve



Reel Dimension



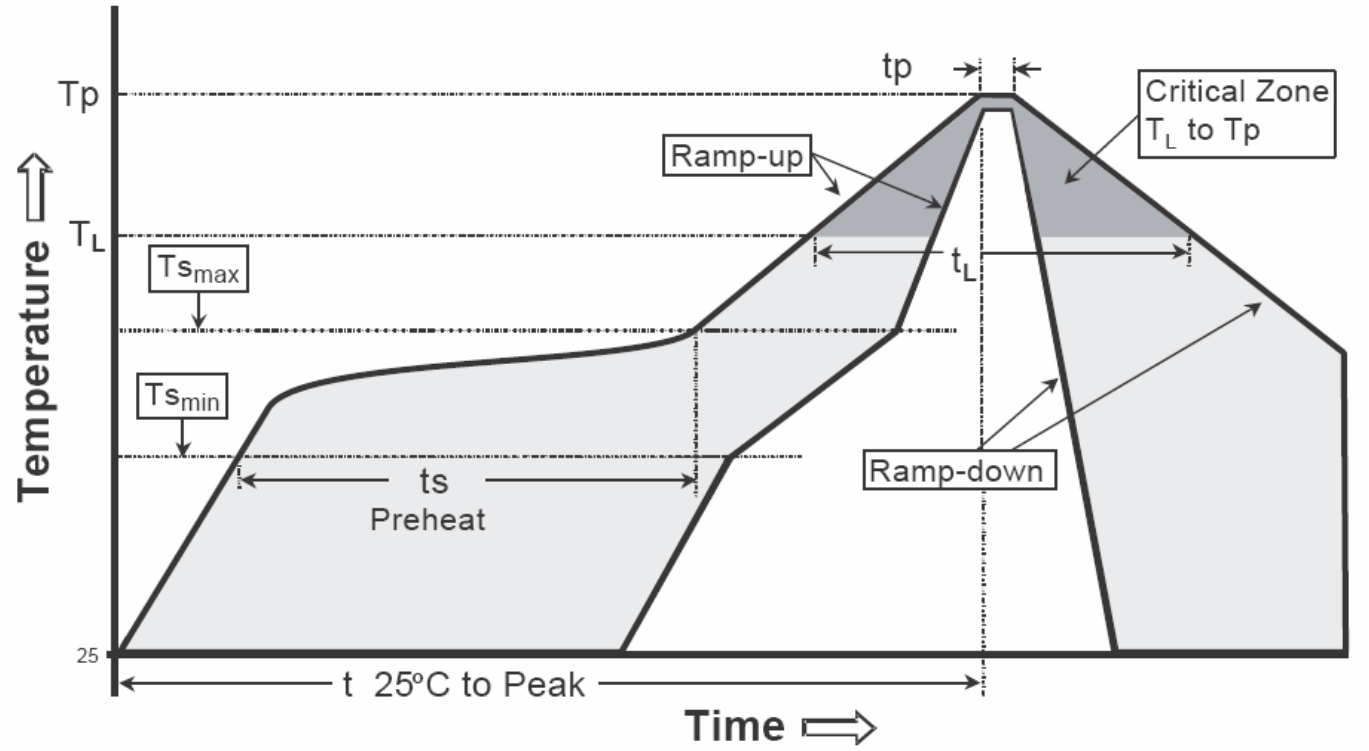
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

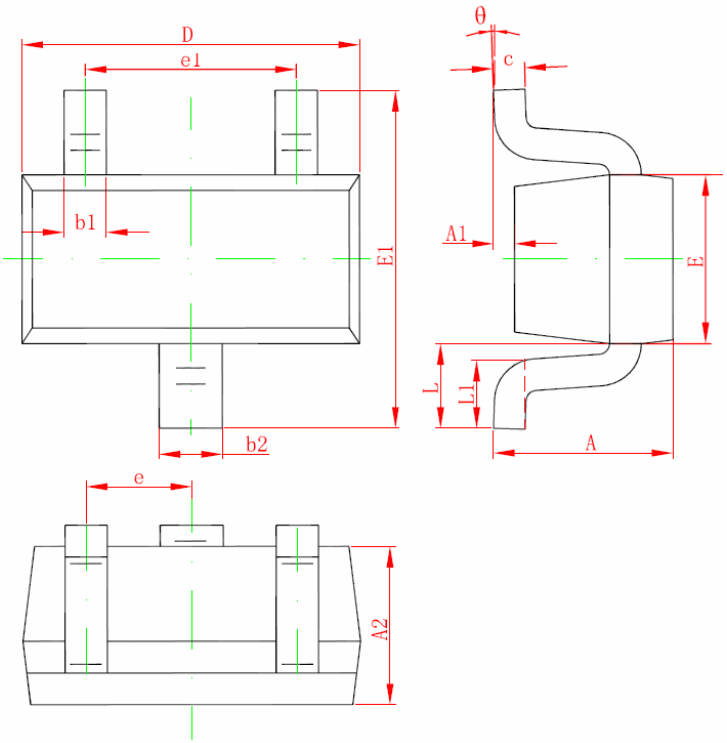
Recommended temperature profile for IR reflow



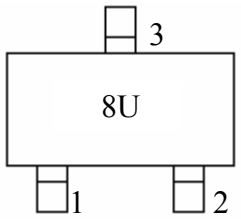
Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(T_S min) −Temperature Max(T_S max) −Time($t_{s\ min}$ to $t_{s\ max}$)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (T_L) − Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(T_P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-523 Dimension



Marking:



3-Lead SOT-523 Plastic
Surface Mounted Package
CYStek Package Code: C3

Style: Pin 1.Base
2.Emitter
3.Collector

*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.028	0.035	0.700	0.900	E	0.028	0.035	0.700	0.900
A1	0.000	0.004	0.000	0.100	E1	0.057	0.069	1.450	1.750
A2	0.028	0.031	0.700	0.800	e	0.020*		0.500*	
b1	0.006	0.010	0.150	0.250	e1	0.035	0.043	0.900	1.100
b2	0.010	0.014	0.250	0.350	L	0.016 REF		0.400 REF	
c	0.004	0.008	0.100	0.200	L1	0.010	0.018	0.260	0.460
D	0.059	0.067	1.500	1.700	θ	0°	8°	0°	8°

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0