



STL26NM60N

N-channel 600 V, 0.160 Ω , 19 A PowerFLAT™ 8x8 HV ultra low gate charge MDmesh™ II Power MOSFET

Features

Order code	V _{DSS} @ T _{Jmax}	R _{DS(on)} max	I _D
STL26NM60N	650 V	< 0.185 Ω	19 A ⁽¹⁾

1. The value is rated according to R_{thj-case}

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

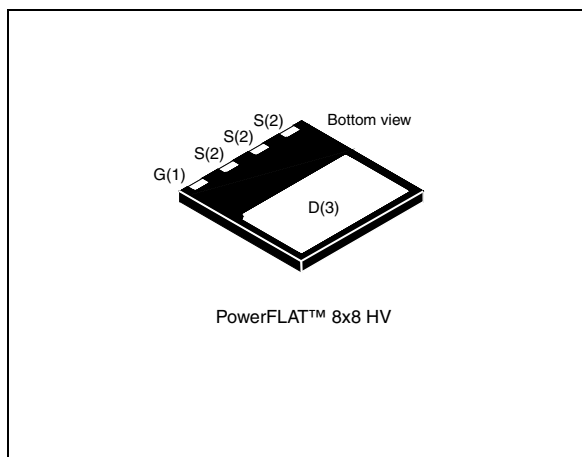
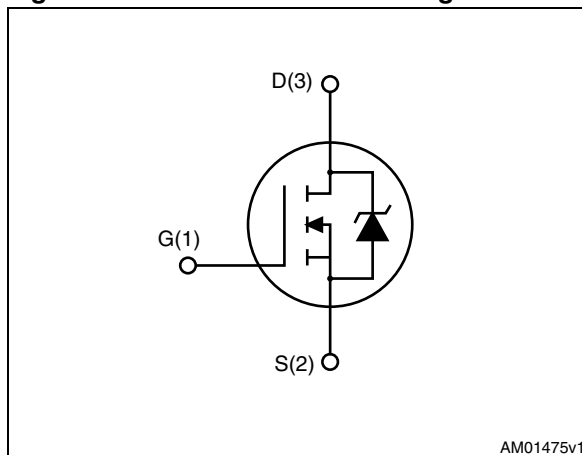


Figure 1. Internal schematic diagram



AM01475v1

Table 1. Device summary

Order code	Marking	Package	Packaging
STL26NM60N	26NM60N	PowerFLAT™ 8x8 HV	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	600	V
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	19	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	12	A
$I_D^{(2)}$	Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$	2.7	A
$I_D^{(2)}$	Drain current (continuous) at $T_{amb} = 100\text{ }^\circ\text{C}$	1.7	A
$I_{DM}^{(2),(3)}$	Drain current (pulsed)	10.8	A
$P_{TOT}^{(2)}$	Total dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	3	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	125	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	7.5	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	400	mJ
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. The value is rated according to $R_{thj-case}$
2. When mounted on FR-4 board of 1 inch^2 , 2oz Cu
3. $I_{SD} \leq 19\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS\ peak} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.83	$^\circ\text{C}/\text{W}$
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb max	45	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch^2 FR-4 board, 2 oz Cu

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}, V_{GS} = 0$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 600\text{ V}$ $V_{DS} = 600\text{ V}, T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		0.160	0.185	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	1800	-	pF
C_{oss}	Output capacitance			115		pF
C_{rss}	Reverse transfer capacitance			1.1		pF
$C_{oss(eq)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }480\text{ V}, V_{GS} = 0$	-	310	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	2.8	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 19\text{ A},$ $V_{GS} = 10\text{ V}$ (see Figure 14)	-	60	-	nC
Q_{gs}	Gate-source charge			8.5		nC
Q_{gd}	Gate-drain charge			30		nC

1. $C_{oss(eq)}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 10\text{ A}$,		13		ns
t_r	Rise time	$R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$	-	25	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 15),		85		ns
t_f	Fall time	(see Figure 18)		50		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		19	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		76	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 19\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 19\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	370		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100\text{ V}$ (see Figure 15)	-	5.8		μC
I_{RRM}	Reverse recovery current			31.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 19\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	450		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$	-	7.5		μC
I_{RRM}	Reverse recovery current	(see Figure 15)		32.5		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

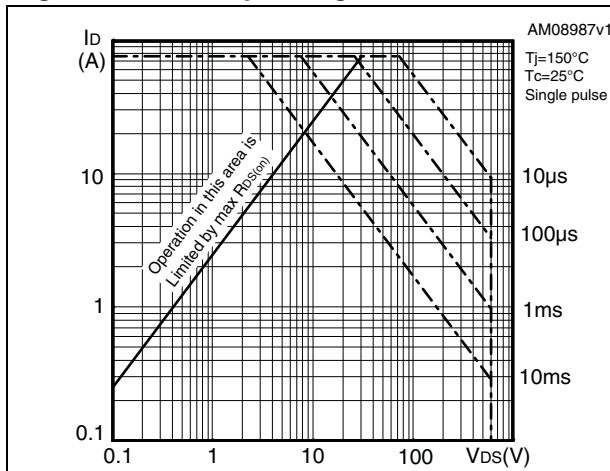


Figure 3. Thermal impedance

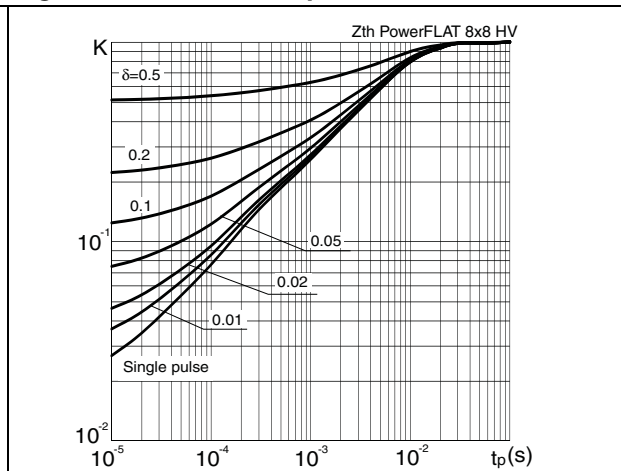


Figure 4. Output characteristics

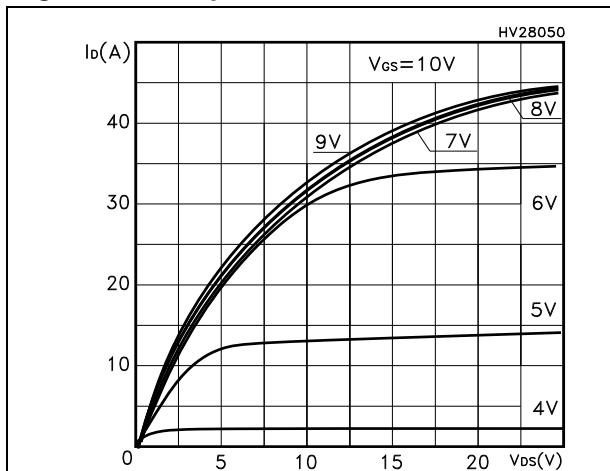


Figure 5. Transfer characteristics

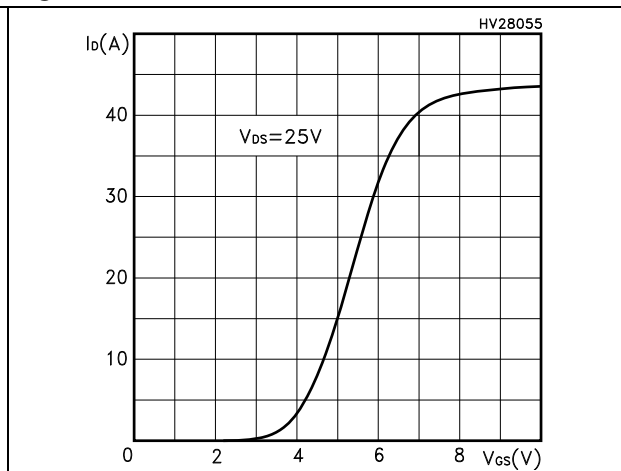


Figure 6. Normalized V_{DS} vs temperature

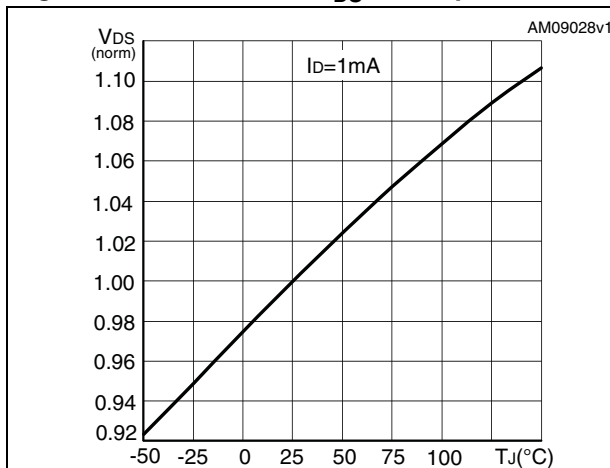


Figure 7. Static drain-source on resistance

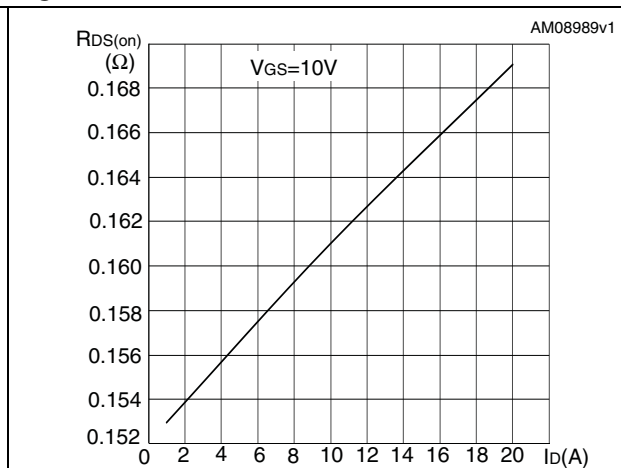


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

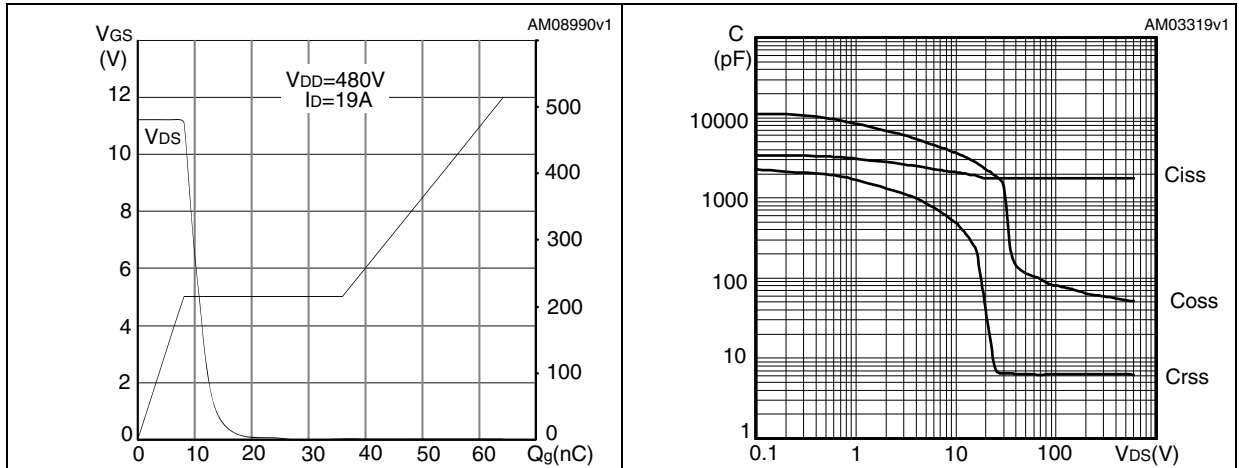


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

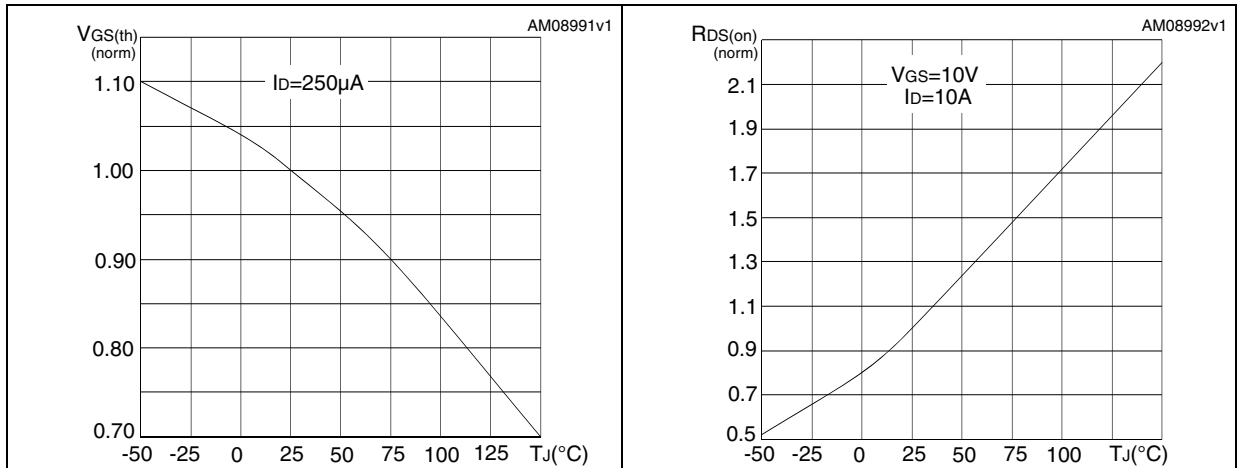
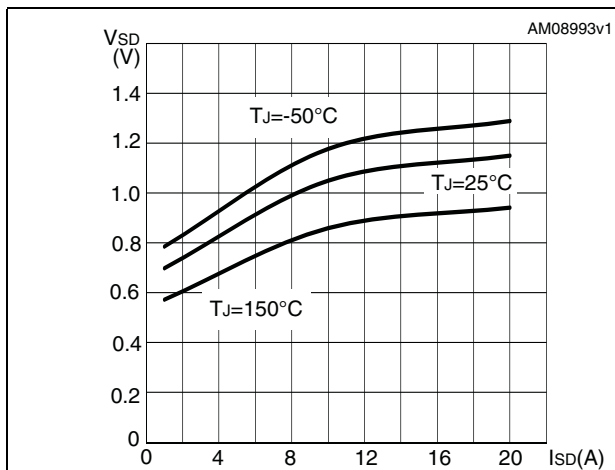


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

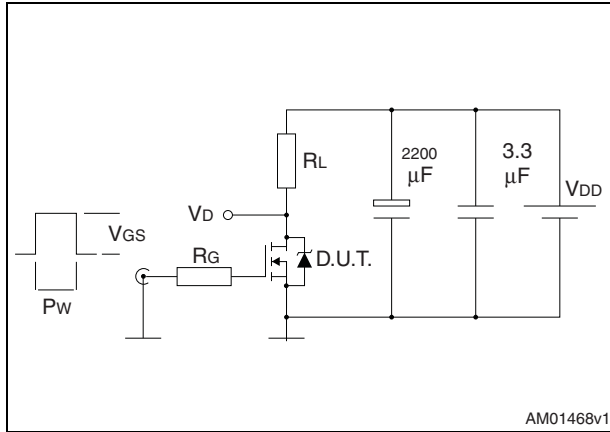


Figure 14. Gate charge test circuit

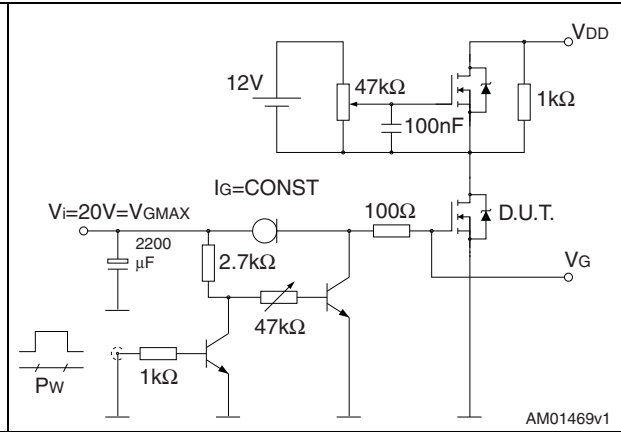


Figure 15. Test circuit for inductive load switching and diode recovery times

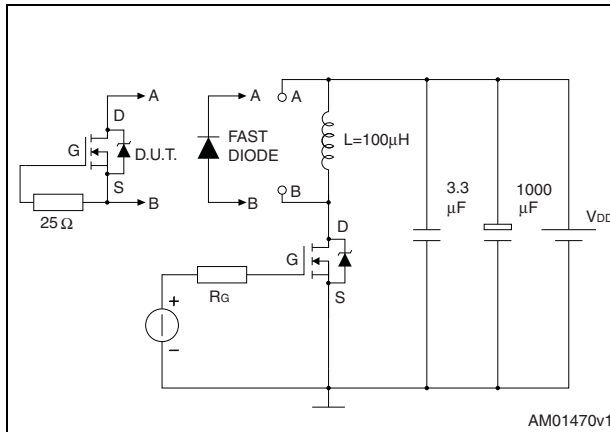


Figure 16. Unclamped inductive load test circuit

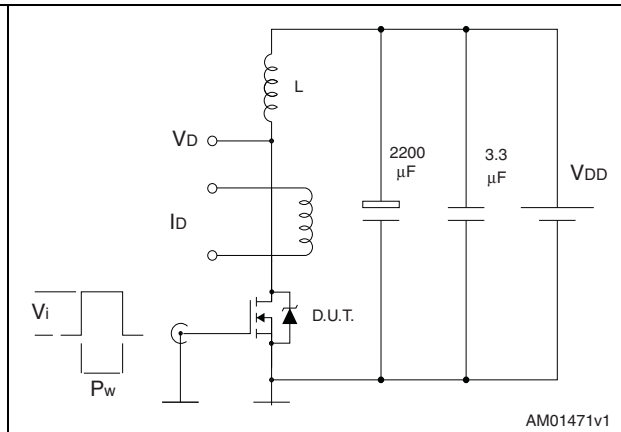


Figure 17. Unclamped inductive waveform

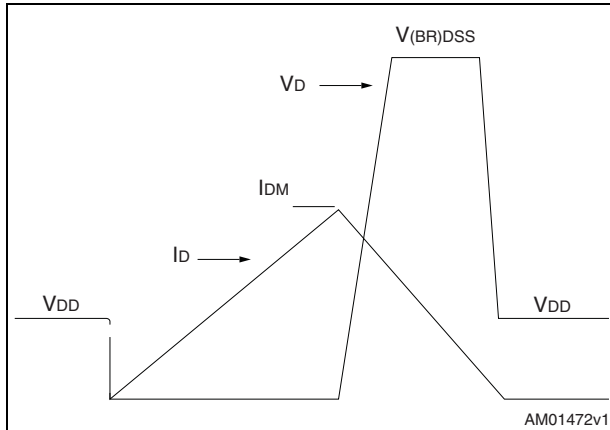
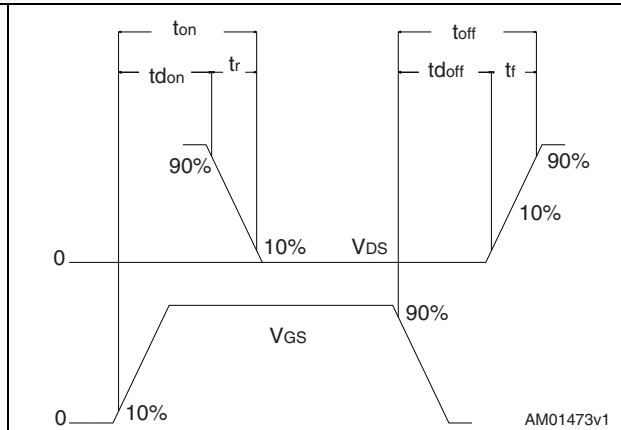


Figure 18. Switching time waveform



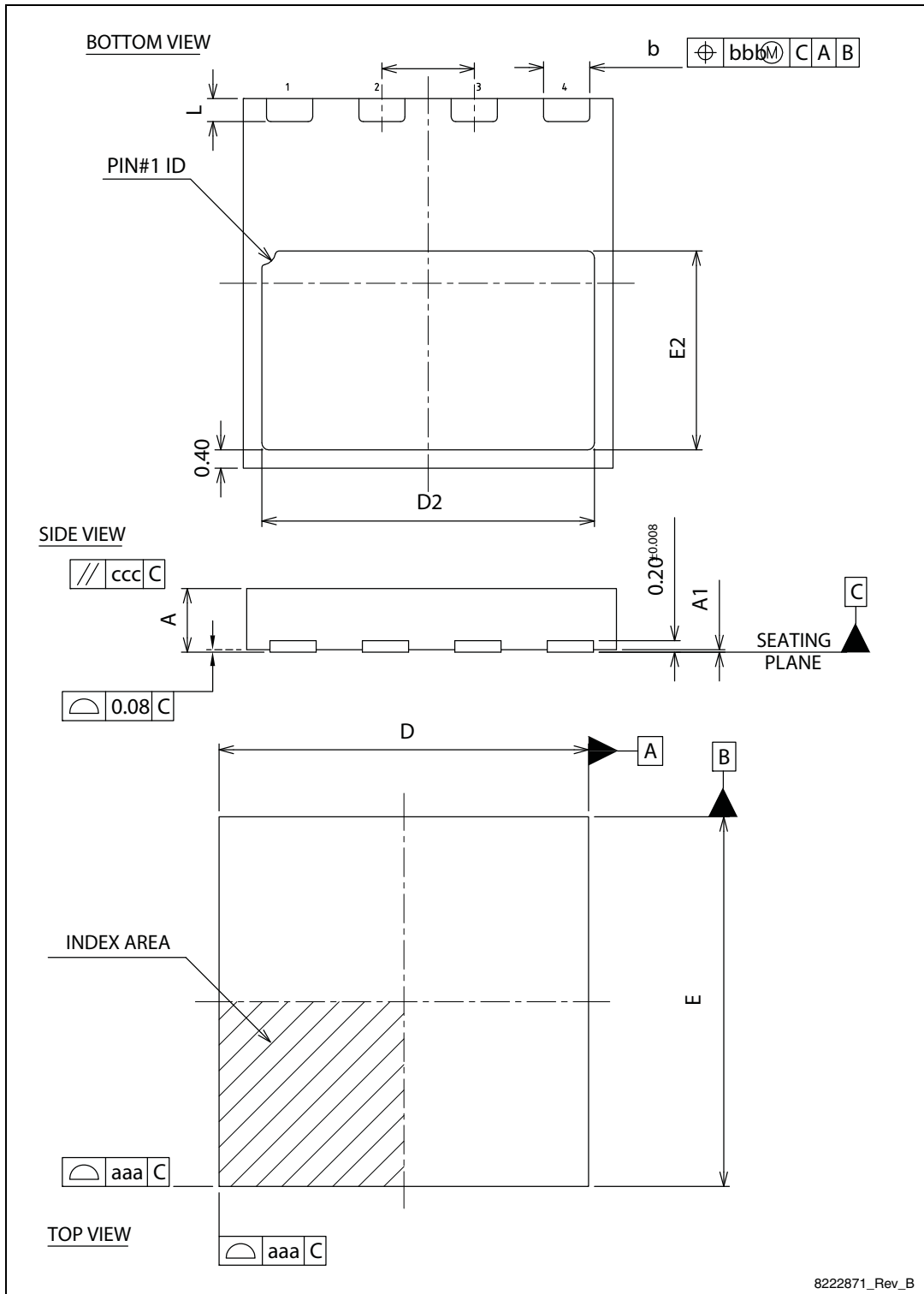
4 Package mechanical data

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Table 8. PowerFLAT™ 8x8 HV mechanical data

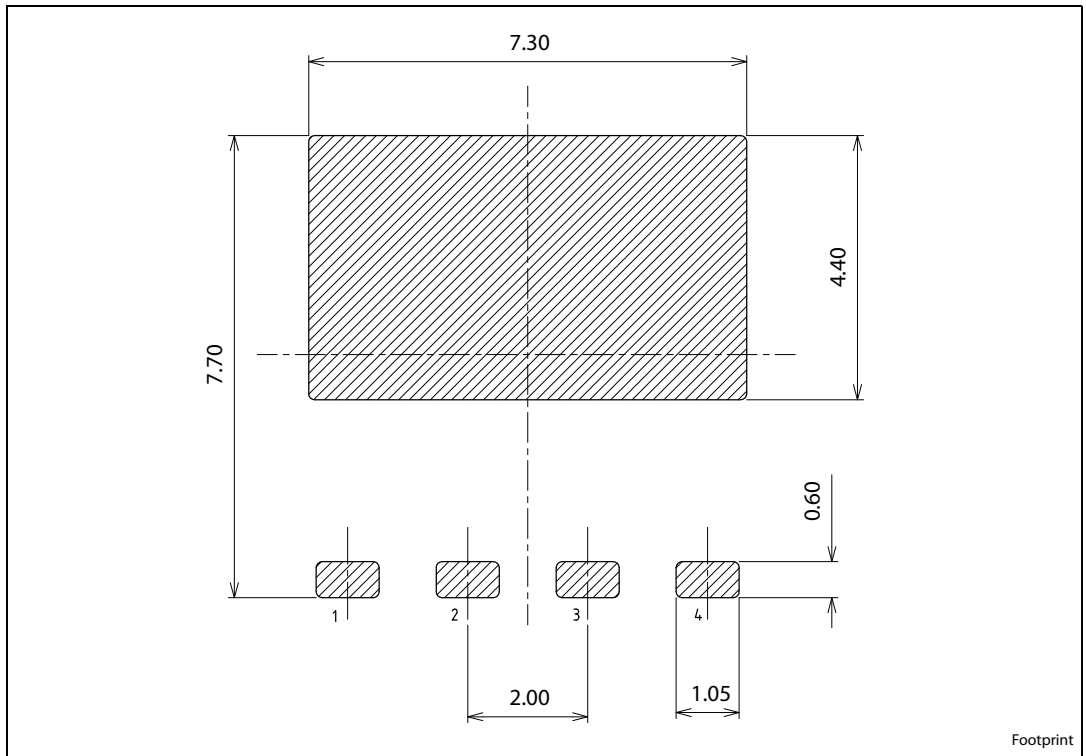
Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60
aaa		0.10	
bbb		0.10	
ccc		0.10	

Figure 19. PowerFLAT™ 8x8 HV drawing mechanical data



8222871_Rev_B

Figure 20. PowerFLAT™ 8x8 HV recommended footprint



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
14-Feb-2011	1	First release.
03-Nov-2011	2	Section 4: Package mechanical data has been updated. Minor text changes.

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