

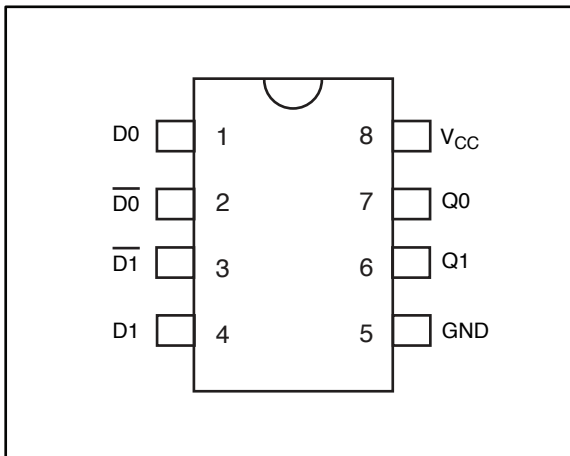


PO100HSTL23A

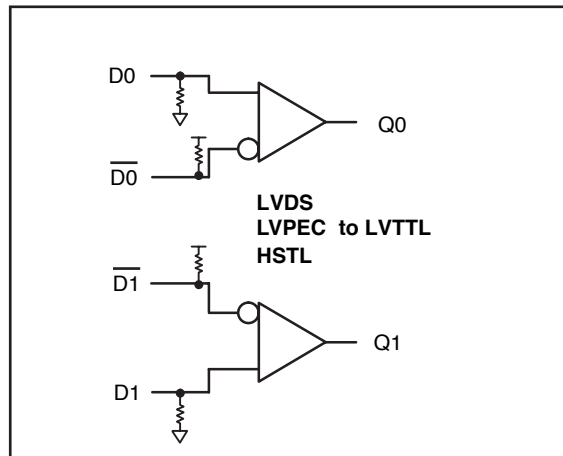
High Frequency Noise Cancellation Translator

FEATURES:	DESCRIPTION:
<ul style="list-style-type: none"> • Patented Technology • Differential LVDS/LVPECL/HSTL to LVTTTL Translator • Operating frequency up to 1GHz with 2pf load • Operating frequency up to 800MHz with 5pf load • Operating frequency up to 450MHz with 15pf load • Very low output pin to pin skew < 150ps • Propagation delay < 1.8ns max with 15pf load • 2.4V to 3.6V power supply • Industrial temperature range: -40°C to 85°C • Available in 8-pin SOIC package • Available in 8-pin TSSOP package 	<p>Potato Semiconductor’s PO100HSTL23A is designed for world top performance using submicron CMOS technology to achieve 1GHz LVTTTL output frequency with less than 1.8ns propagation delay.</p> <p>The PO100HSTL23A is a low-skew, The small outline 8 pin package and the low skew design to make it ideal for applica- tions which require the translation of a clock or a data signal.</p>

Pin Configuration



Logic Block Diagram



Pin Description

Pin	Function
Q0, Q1	LVTTTL Outputs
D0, D1 D0-bar, D1-bar	Differential LVDS/LVPECL/HSTL Inputs
VCC	Positive Supply
GND	Ground



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Maximum Ratings

Description	Max	Unit
Storage Temperature	-65 to 150	°C
Operation Temperature	-40 to 85	°C
Operation Voltage	-0.5 to +4.6	V
Input Voltage	-0.5 to Vcc	V
Output Voltage	-0.5 to Vcc+0.5	V

Note:

stresses greater than listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability specification is not implied.

Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLUP}	Input Pullup Resistor			88		KΩ
R _{PULLDOWN}	Input Pulldown Resistor			88		KΩ

DC Electrical Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V _{OH}	Output High voltage	Vcc=3V Vin=VIH or VIL, IOH= -12mA	2.4	3	-	V
V _{OL}	Output Low voltage	Vcc=3V Vin=VIH or VIL, IOH=12mA	-	0.3	0.5	V
V _{IH}	Input High voltage	Guaranteed Logic HIGH Level (Input Pin)	2	-	Vcc	V
V _{IL}	Input Low voltage	Guaranteed Logic LOW Level (Input Pin)	-0.5	-	0.8	V
I _{IH}	Input High current	Vcc = 3.6V and Vin = Vcc	-	-	1	uA
I _{IL}	Input Low current	Vcc = 3.6V and Vin = 0V	-	-	-1	uA
V _{IK}	Clamp diode voltage	Vcc = Min. And IIN = -18mA	-	-0.7	-1.2	V

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25 °C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = Vcc - 0.6V at rated current



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Power Supply Characteristics

Symbol	Description	Test Conditions (1)	Min	Typ	Max	Unit
I_{ccQ}	Quiescent Power Supply Current	V _{cc} =Max, V _{in} =V _{cc} or GND	-	0.1	30	uA

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{cc} = 3.3V, 25°C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

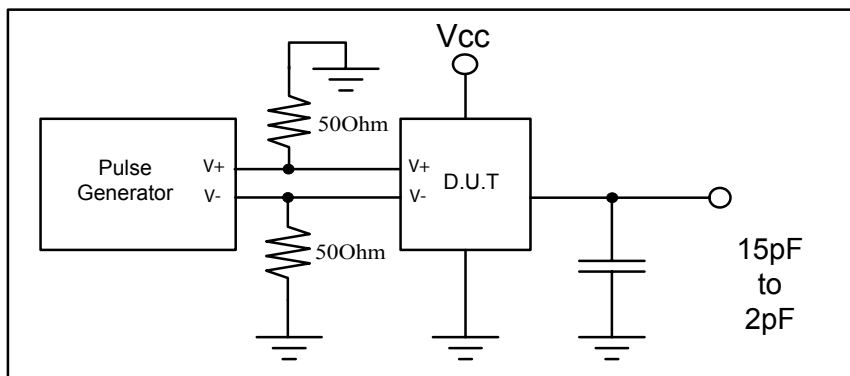
Switching Characteristics

Symbol	Description	Test Conditions (1)	Max	Unit
t_{pD}	Propagation Delay D to Output pair	CL = 15pF	1.8	ns
t_r/t_f	Rise/Fall Time	0.8V – 2.0V	0.8	ns
t_{sk(o)}	Output Pin to Pin Skew (Same Package)	CL = 15pF, 125MHz	150	ps
t_{sk(pp)}	Output Skew (Different Package)	CL = 15pF, 125MHz	300	ps
f_{max}	Input Frequency	CL = 15pF	450	MHz
f_{max}	Input Frequency	CL = 5pF	800	MHz
f_{max}	Input Frequency	CL = 2pF	1000	MHz

Notes:

1. See test circuits and waveforms.
2. t_{pLH}, t_{pHL}, t_{sk(p)}, and t_{sk(o)} are production tested. All other parameters guaranteed but not production tested.
3. Airflow of 1m/s is recommended for frequencies above 133MHz

Test Circuit



Dual Differential LVDS/LVPECL/HSTL to LVTTTL Translator

Test Waveforms

FIGURE 1. LVDS/ PECL/ ECL/ HSTL /DIFFERENTIAL INPUT WAVEFORM DEFINITIONS

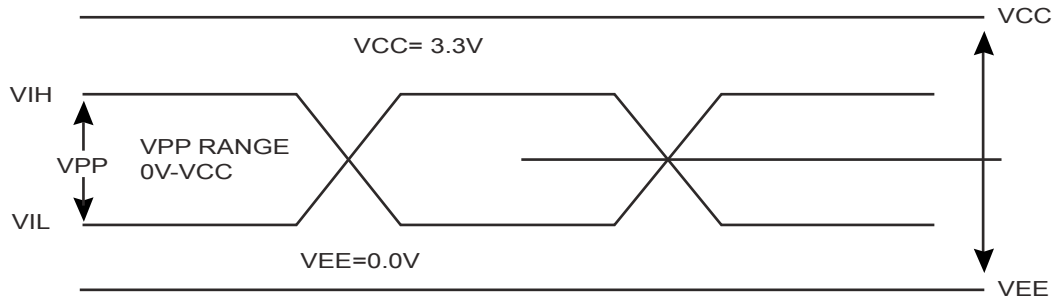


FIGURE 2. LVTTTL OUTPUT

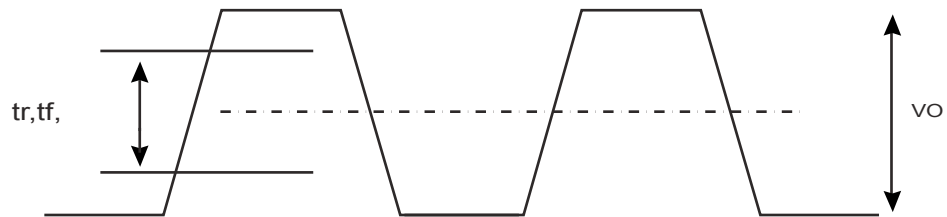
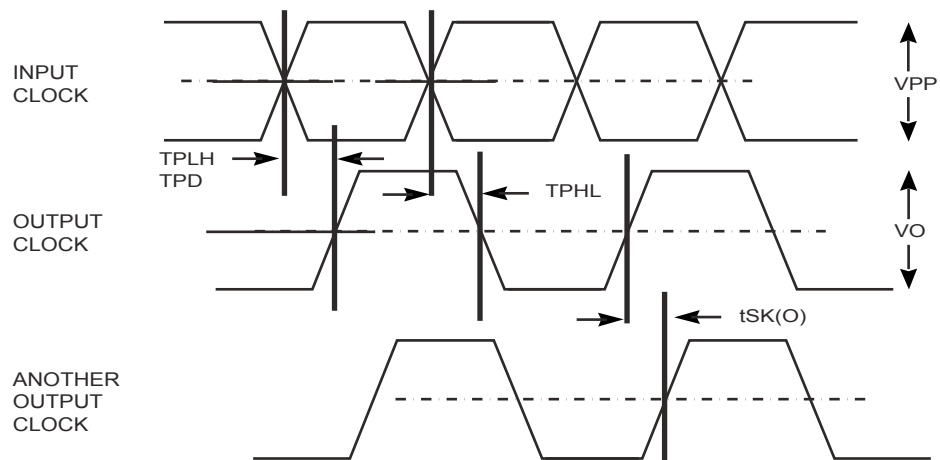


FIGURE 3. Propagation Delay, Output pulse skew, and output-to-output skew for D to output

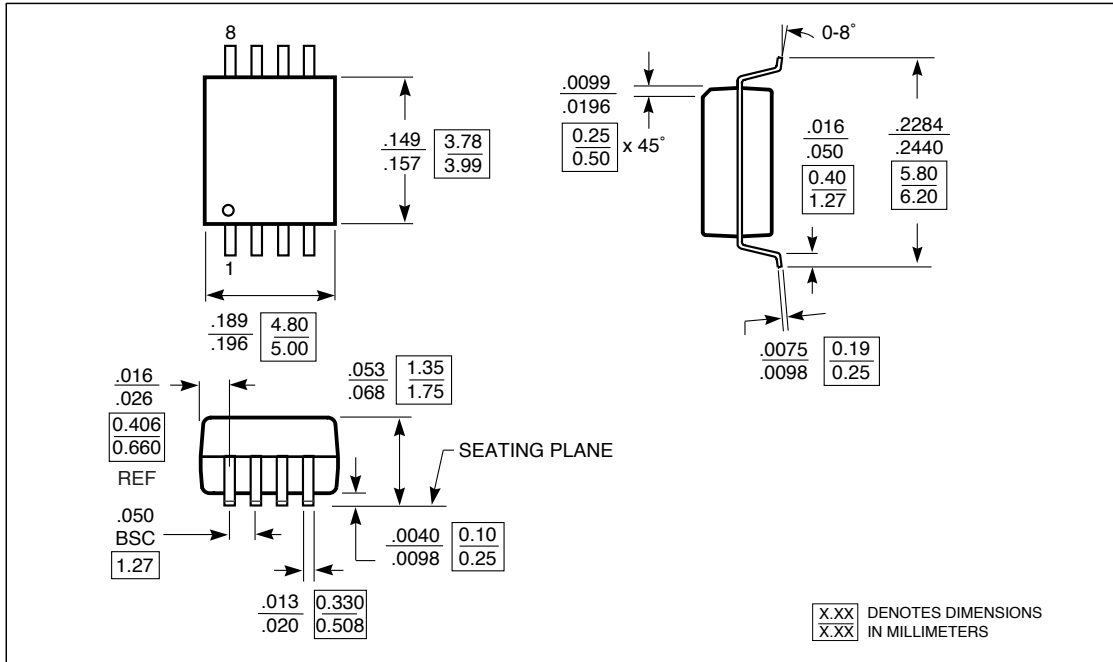




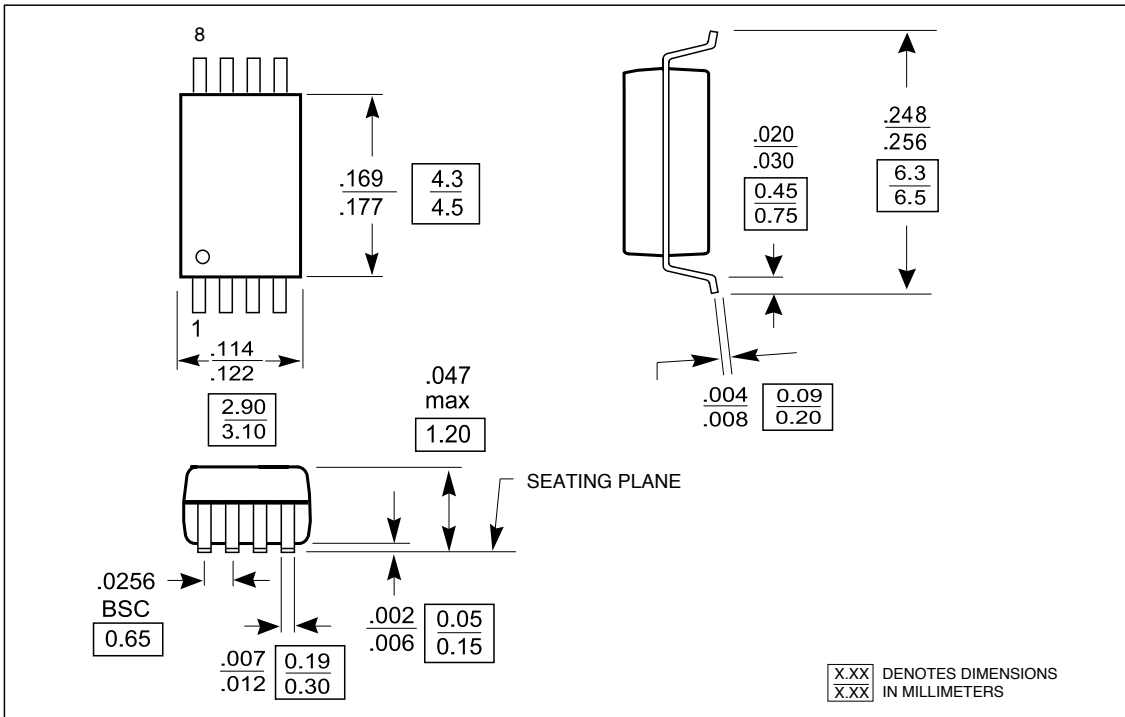
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Packaging Mechanical Drawing: 8 pin SOIC



Packaging Mechanical Drawing: 8 pin TSSOP





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IC Ordering Information

Ordering Code	Package		Top-Marking	T _A
PO100HSTL23ASU for Tube	8 pin 150mil SOIC	Pb-free & Green	PO100HSTL23AS	-40°C to 85°C
PO100HSTL23ASR for Tape & Reel	8 pin 150mil SOIC	Pb-free & Green	PO100HSTL23AS	-40°C to 85°C
PO100HSTL23ATU for Tube	8 pin 173mil TSSOP	Pb-free & Green	PO100HSTL23TS	-40°C to 85°C
PO100HSTL23ATR for Tape & Reel	8 pin 173mil TSSOP	Pb-free & Green	PO100HSTL23TS	-40°C to 85°C

IC Package Information

PACKAGE CODE	PACKAGE TYPE	TAPE WIDTH (mm)	TAPE PITCH (mm)	TAPE & REEL PIN 1 LOCATION	TAPE TRAILER LENGTH	QTY PER TAPE	TAPE LEADER LENGTH	QTY PER TUBE
S	8-pin 150mil SOIC	12	8	Top Left Corner	39 (12")	3000	64 (20")	97
T	8-pin 173mil TSSOP	12	8	Top Left Corner	39 (12")	3000	64 (20")	158