

FDN5618P

General Description

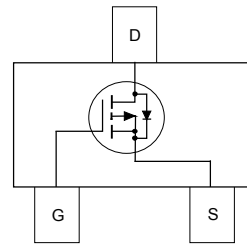
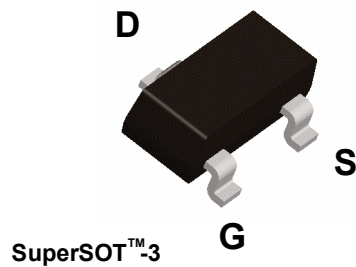
This 60V P-Channel MOSFET uses Fairchild's high voltage PowerTrench process. It has been optimized for power management applications.

Applications

- DC-DC converters
- Load switch
- Power management

Features

- -1.25 A, -60 V. $R_{DS(ON)} = 0.170 \Omega @ V_{GS} = -10 \text{ V}$
 $R_{DS(ON)} = 0.230 \Omega @ V_{GS} = -4.5 \text{ V}$
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	Drain-Source Voltage	-60	V
V _{GSS}	Gate-Source Voltage	±20	V
I _D	Drain Current – Continuous (Note 1a)	-1.25	A
	– Pulsed	-10	
P _D	Maximum Power Dissipation (Note 1a) (Note 1b)	0.5	W
		0.46	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case (Note 1)	75	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
618	FDN5618P	7"	8mm	3000 units

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Electrical Characteristics

 $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C		-58		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -48\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
I_{GSSF}	Gate–Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1	-1.6	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C		4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -10\text{ V}, I_D = -1.25\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -1.0\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -3\text{ A}, T_J = 125^\circ\text{C}$		0.148 0.185 0.245	0.170 0.230 0.315	Ω
$I_{D(on)}$	On–State Drain Current	$V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	-5			A
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -1.25\text{ A}$		4.3		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		430		pF
C_{oss}	Output Capacitance			52		pF
C_{rss}	Reverse Transfer Capacitance			19		pF

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -30\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\text{ }\Omega$		6.5	13	ns
t_r	Turn–On Rise Time			8	16	ns
$t_{d(off)}$	Turn–Off Delay Time			16.5	30	ns
t_f	Turn–Off Fall Time			4	8	ns
Q_g	Total Gate Charge	$V_{DS} = -30\text{ V}, I_D = -1.25\text{ A},$ $V_{GS} = -10\text{ V}$		8.6	13.8	nC
Q_{gs}	Gate–Source Charge			1.5		nC
Q_{gd}	Gate–Drain Charge			1.3		nC

Drain–Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain–Source Diode Forward Current			-0.42		A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -0.42$ (Note 2)		-0.7	-1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 250°C/W when mounted on a
0.02 in² pad of 2 oz. copper.



b) 270°C/W when mounted on a
minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle ≤ 2.0