

TOSHIBA SM12(G,J)48, USM12(G,J)48, SM12(G,J)48A, USM12(G,J)48A

TOSHIBA BI-DIRECTIONAL TRIODE THYRISTOR SILICON PLANAR TYPE

SM12G48, USM12G48, SM12J48, USM12J48 SM12G48A, USM12G48A, SM12J48A, USM12J48A

AC POWER CONTROL APPLICATIONS

- Repetitive Peak Off-State Voltage : $V_{DRM}=400, 600V$
- R.M.S. On-State Current : $I_T(RMS)=12A$
- Gate Trigger Current : $I_{GT}=30mA$ Max.
: $I_{GT}=20mA$ Max. ("A"Type)

Unit in mm

SM12G48, SM12J48, SM12G48A, SM12J48A	USM12G48, USM12J48, USM12G48A, USM12J48A
JEDEC —	JEDEC —
EIAJ —	EIAJ —
TOSHIBA 13-10J1A	TOSHIBA 13-10J2A

Weight : 1.7g

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Repetitive Peak Off-State Voltage	V_{DRM}	400	V
		600	
R.M.S On-State Current	$I_T(RMS)$	12	A
Peak One Cycle Surge On-State Current (Non-Repetitive)	I_{TSM}	120 (50Hz)	A
		132 (60Hz)	
I^2t Limit Value	I^2t	72	A^2s
Critical Rate of Rise of On-State Current (Note 1)	di/dt	50	$A/\mu s$
Peak Gate Power Dissipation	P_{GM}	5	W
Average Gate Power Dissipation	$P_{G(AV)}$	0.5	W
Peak Forward Gate Voltage	V_{GM}	10	V
Peak Forward Gate Current	I_{GM}	2	A
Junction Temperature	T_j	-40~125	°C
Storage Temperature Range	T_{stg}	-40~125	°C

(Note 1) $V_{DRM}=0.5 \times \text{Rated}$
 $I_{TM} \leq 17A$
 $t_{gw} \geq 10\mu s$
 $t_{gr} \leq 250ns$
 $i_{gp} = I_{GT} \times 2.0$

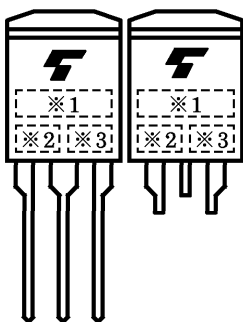
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MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Repetitive Peak Off-State Current		I _{DRM}	V _{DRM} = Rated	—	—	20	μA	
Gate Trigger Voltage	I	V _{GT}	V _D = 12V R _L = 20Ω	T2(+), GATE (+)	—	—	1.5	V
	II			T2(+), GATE (-)	—	—	1.5	
	III			T2(-), GATE (-)	—	—	1.5	
	IV			T2(-), GATE (+)	—	—	—	
Gate Trigger Current	(U)SM12G48 (U)SM12J48	I _{GT}	V _D = 12V R _L = 20Ω	T2(+), GATE (+)	—	—	30	mA
				T2(+), GATE (-)	—	—	30	
				T2(-), GATE (-)	—	—	30	
				T2(-), GATE (+)	—	—	—	
	(U)SM12G48A (U)SM12J48A	I	T2(+), GATE (+)	—	—	20		
		II	T2(+), GATE (-)	—	—	20		
		III	T2(-), GATE (-)	—	—	20		
		IV	T2(-), GATE (+)	—	—	—		
Peak On-State Voltage		V _{TM}	I _{TM} = 17A	—	—	1.5	V	
Gate Non-Trigger Voltage		V _{GD}	V _D = Rated, T _c = 125°C	0.2	—	—	V	
Holding Current		I _H	V _D = 12V, I _{TM} = 1A	—	—	50	mA	
Thermal Resistance		R _{th(j-c)}	Junction to Case, AC	—	—	2.4	°C / W	
Critical Rate of Rise of Off-State Voltage	(U)SM12G48 (U)SM12J48	dv / dt	V _{DRM} = Rated, T _j = 125°C Exponential Rise	—	300	—	V / μs	
	(U)SM12G48A (U)SM12J48A			—	200	—		
Critical Rate of Rise of Off-State Voltage at Commutation	(U)SM12G48 (U)SM12J48	(dv / dt) _c	V _{DRM} = 400V, T _j = 125°C (di / dt) _c = -6.5A / ms	10	—	—	V / μs	
	(U)SM12G48A (U)SM12J48A			4	—	—		

MARKING

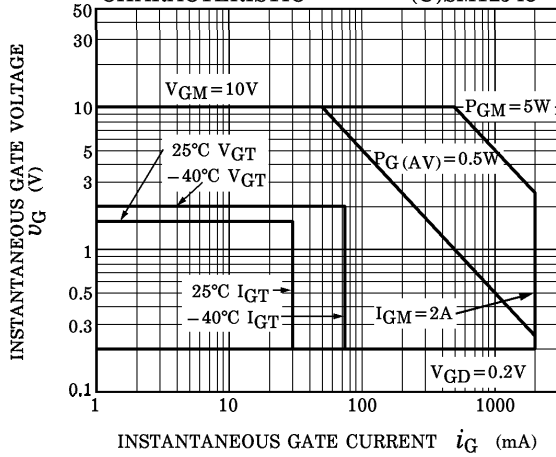


NUMBER	SYMBOL	MARK
※ 1	SM12G48, SM12G48A, USM12G48, USM12G48A	SM12G48
	TYPE SM12J48, SM12J48A, USM12J48, USM12J48A	SM12J48
※ 2	SM12G48A, SM12J48A, USM12G48A, USM12J48A	A
※ 3	Lot Number <div style="display: flex; align-items: center;"> <div style="border: 1px solid black; width: 15px; height: 15px; margin-right: 5px;"></div> <div style="border: 1px solid black; width: 15px; height: 15px; margin-right: 5px;"></div> <div style="margin-left: 5px;">← Month (Starting from Alphabet A)</div> </div> <div style="display: flex; align-items: center; margin-top: 5px;"> <div style="border: 1px solid black; width: 15px; height: 15px; margin-right: 5px;"></div> <div style="margin-left: 5px;">← Year (Last Decimal Digit of the Current Year)</div> </div>	Example 8A: January 1998 8B: February 1998 8L: December 1998

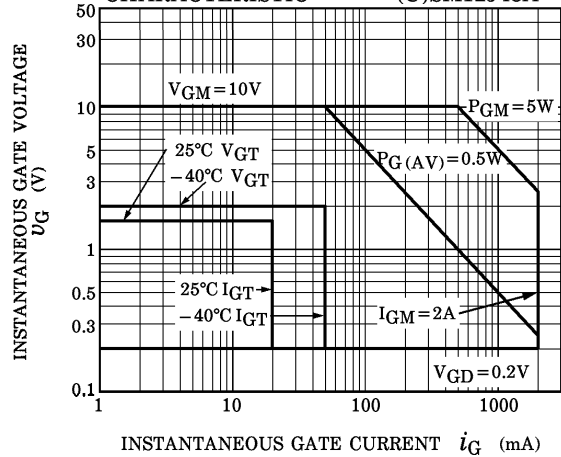
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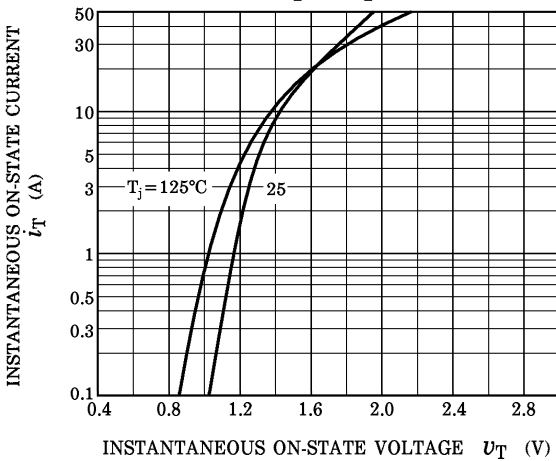
GATE TRIGGER CHARACTERISTIC (U)SM12G48 (U)SM12J48



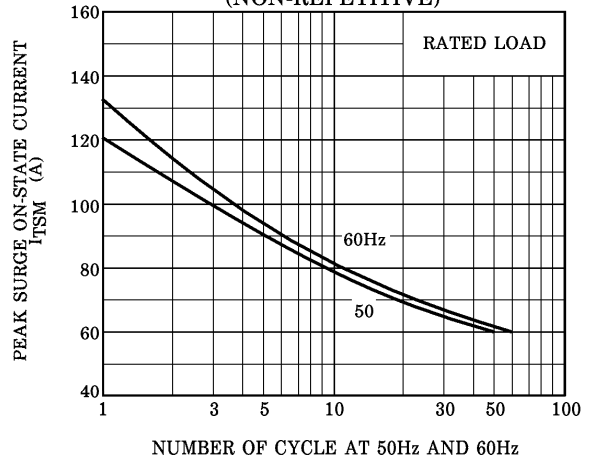
GATE TRIGGER CHARACTERISTIC (U)SM12G48A (U)SM12J48A



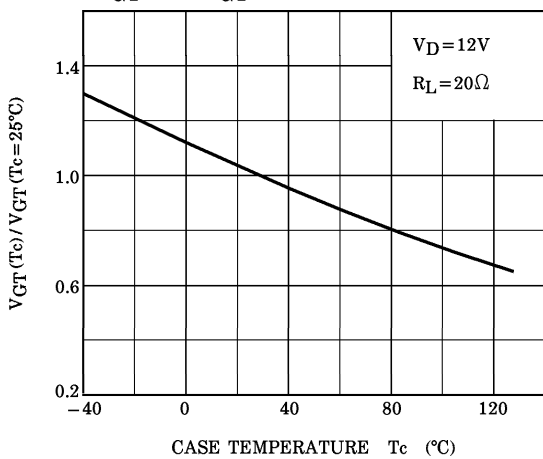
$i_T - v_T$



SURGE ON-STATE CURRENT (NON-REPETITIVE)



$V_{GT}(T_c) / V_{GT}(T_c = 25^\circ C) - T_c$ (TYPICAL)



$I_{GT}(T_c) / I_{GT}(T_c = 25^\circ C) - T_c$ (TYPICAL)

