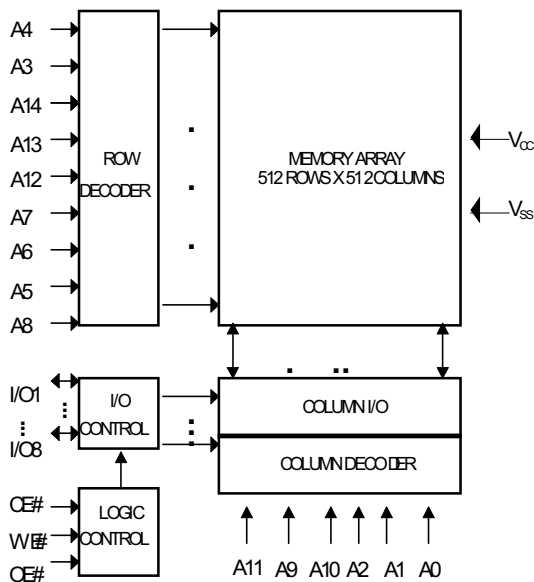




### FEATURES

- Fast access time : 8/10/12/15 ns (max.)
- Low operating power consumption : 80 mA (typical)
- Single 5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Package : 28-pin 300 mil skinny PDIP  
28-pin 300 mil SOJ  
28-pin 330 mil SOP  
28-pin 8x13.4mm TSOP-I

### FUNCTIONAL BLOCK DIAGRAM



### PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
CE#	Chip Enable Inputs
WE#	Write Enable Inputs
OE#	Output Enable Inputs
V <sub>CC</sub>	Power Supply
V <sub>SS</sub>	Ground

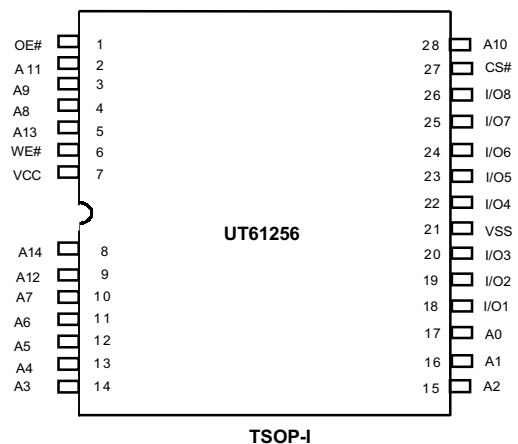
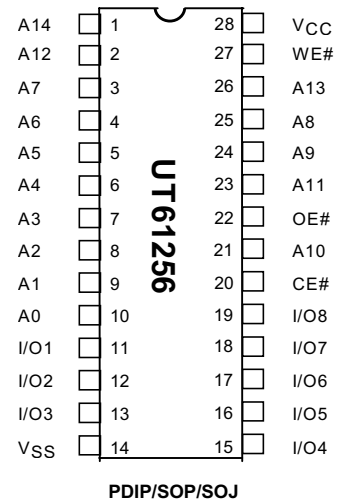
### GENERAL DESCRIPTION

The UT61256 is a 262,144-bit high-speed CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

The UT61256 is designed for high-speed system applications. It is particularly suited for use in high-density high-speed system applications.

The UT61256 operates from a single 5V power supply and all inputs and outputs are fully TTL compatible.

### PIN CONFIGURATION



**ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V <sub>SS</sub>	V <sub>TERM</sub>	-0.5 to +6.5	V
Operating Temperature	T <sub>A</sub>	0 to +70	°C
Storage Temperature	T <sub>STG</sub>	-65 to +150	°C
Power Dissipation	P <sub>D</sub>	1	W
DC Output Current	I <sub>OUT</sub>	50	mA
Soldering Temperature (under 10 sec)	T <sub>solder</sub>	260	°C

\*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

**TRUTH TABLE**

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High - Z	I <sub>SB</sub> , I <sub>SB1</sub>
Output Disable	L	H	H	High - Z	I <sub>CC</sub>
Read	L	L	H	D <sub>OUT</sub>	I <sub>CC</sub>
Write	L	X	L	D <sub>IN</sub>	I <sub>CC</sub>

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.

**DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5V ± 10%, T<sub>A</sub> = 0°C to 70°C)**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT	
Input High Voltage	V <sub>IH</sub>		2.2	V <sub>CC</sub> +0.5	V	
Input Low Voltage	V <sub>IL</sub>		- 0.5	0.8	V	
Input Leakage Current	I <sub>LI</sub>	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	- 1	1	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>SS</sub> ≤ V <sub>I/O</sub> ≤ V <sub>CC</sub> CE# = V <sub>IH</sub> or OE# = V <sub>IH</sub> or WE# = V <sub>IL</sub>	- 1	1	μA	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = - 4mA	2.4	-	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA	-	0.4	V	
Operating Power Supply Current	I <sub>CC</sub>	CE# = V <sub>IL</sub> , I <sub>I/O</sub> = 0mA Cycle=Min.	- 8	-	190	mA
			- 10	-	180	mA
			- 12	-	160	mA
			- 15	-	140	mA
Standby Power Supply Current	I <sub>SB</sub>	CE# = V <sub>IH</sub>	-	30	mA	
	I <sub>SB1</sub>	CE# ≥ V <sub>CC</sub> -0.2V	-	5	mA	

**CAPACITANCE** ( $T_A=25^{\circ}\text{C}$ ,  $f=1.0\text{MHz}$ )

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	$C_{IN}$	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

**AC TEST CONDITIONS**

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L=30\text{pF}$ , $I_{OH}/I_{OL}=-4\text{mA}/8\text{mA}$

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ )**(1) READ CYCLE**

PARAMETER	SYMBOL	UT61256-8		UT61256-10		UT61256-12		UT61256-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	$t_{RC}$	8	-	10	-	12	-	15	-	ns
Address Access Time	$t_{AA}$	-	8	-	10	-	12	-	15	ns
Chip Enable Access Time	$t_{ACE}$	-	8	-	10	-	12	-	15	ns
Output Enable Access Time	$t_{OE}$	-	4	-	5	-	6	-	7	ns
Chip Enable to Output in Low Z	$t_{CLZ}^*$	2	-	2	-	3	-	4	-	ns
Output Enable to Output in Low Z	$t_{OLZ}^*$	0	-	0	-	0	-	0	-	ns
Chip Disable to Output in High Z	$t_{CHZ}^*$	-	4	-	5	-	6	-	7	ns
Output Disable to Output in High Z	$t_{OHZ}^*$	-	4	-	5	-	6	-	7	ns
Output Hold from Address Change	$t_{OH}$	3	-	3	-	3	-	3	-	ns

**(2) WRITE CYCLE**

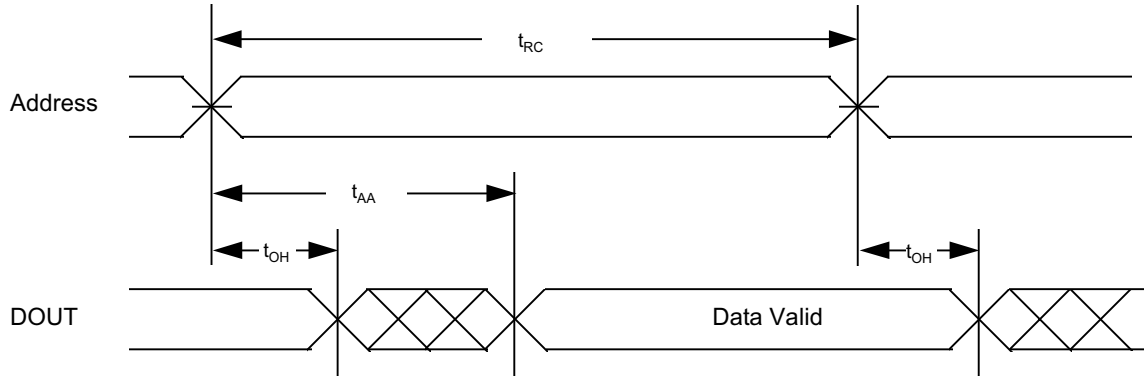
PARAMETER	SYMBOL	UT61256-8		UT61256-10		UT61256-12		UT61256-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	$t_{WC}$	8	-	10	-	12	-	15	-	ns
Address Valid to End of Write	$t_{AW}$	6.5	-	8	-	10	-	12	-	ns
Chip Enable to End of Write	$t_{CW}$	6.5	-	8	-	10	-	12	-	ns
Address Set-up Time	$t_{AS}$	0	-	0	-	0	-	0	-	ns
Write Pulse Width	$t_{WP}$	6.5	-	8	-	9	-	10	-	ns
Write Recovery Time	$t_{WR}$	0	-	0	-	0	-	0	-	ns
Data to Write Time Overlap	$t_{DW}$	5	-	6	-	7	-	8	-	ns
Data Hold from End of Write Time	$t_{DH}$	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	$t_{OW}^*$	1.5	-	2	-	3	-	4	-	ns
Write to Output in High Z	$t_{WHZ}^*$	5	-	-	6	-	7	-	8	ns

\*These parameters are guaranteed by device characterization, but not production tested.

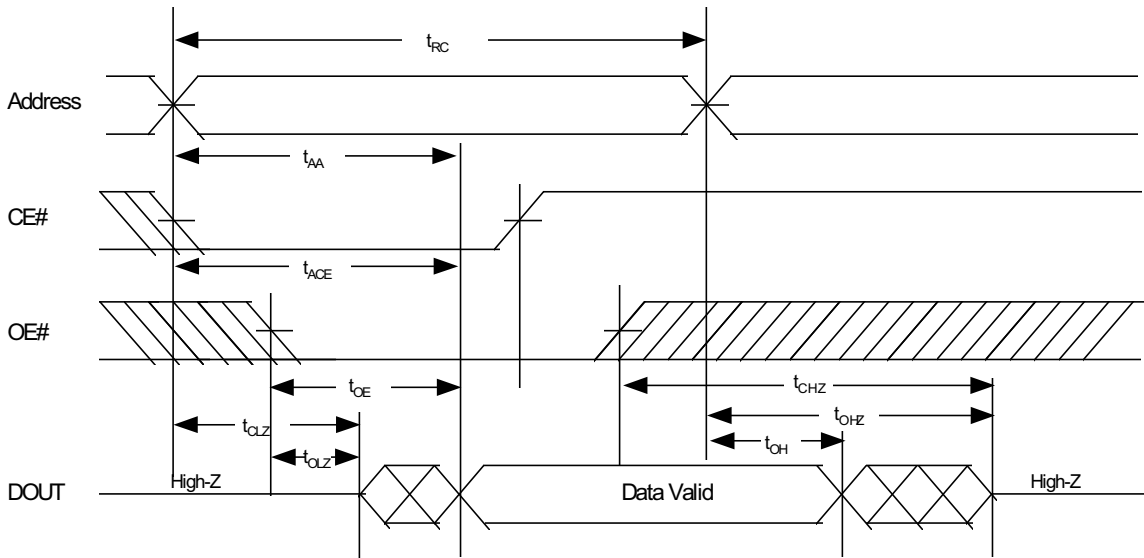


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



READ CYCLE 2 (CE# and OE# Controlled) (1,3,5,6)

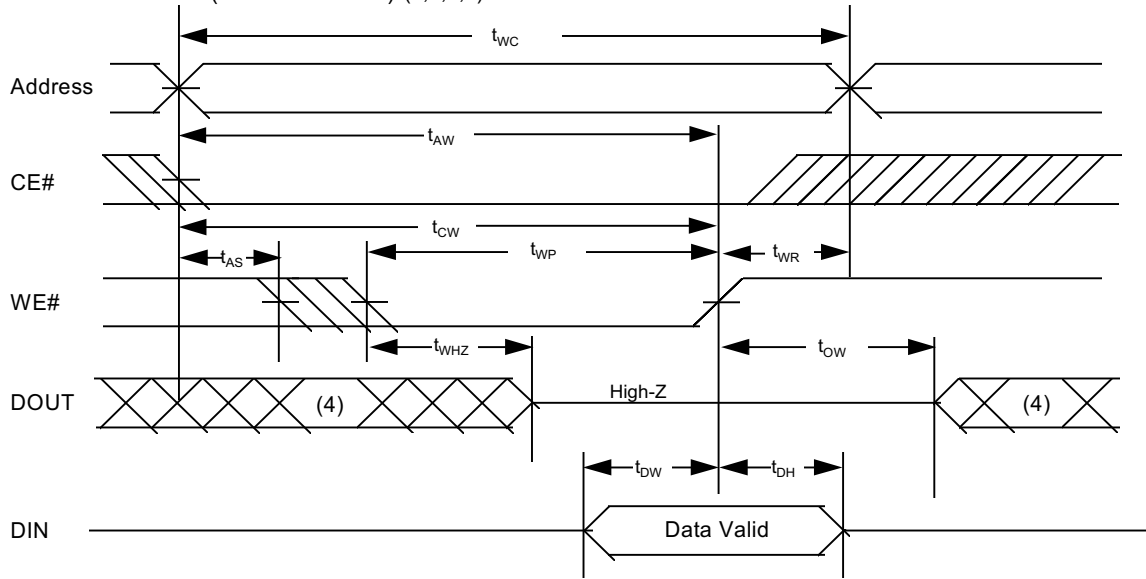


Notes :

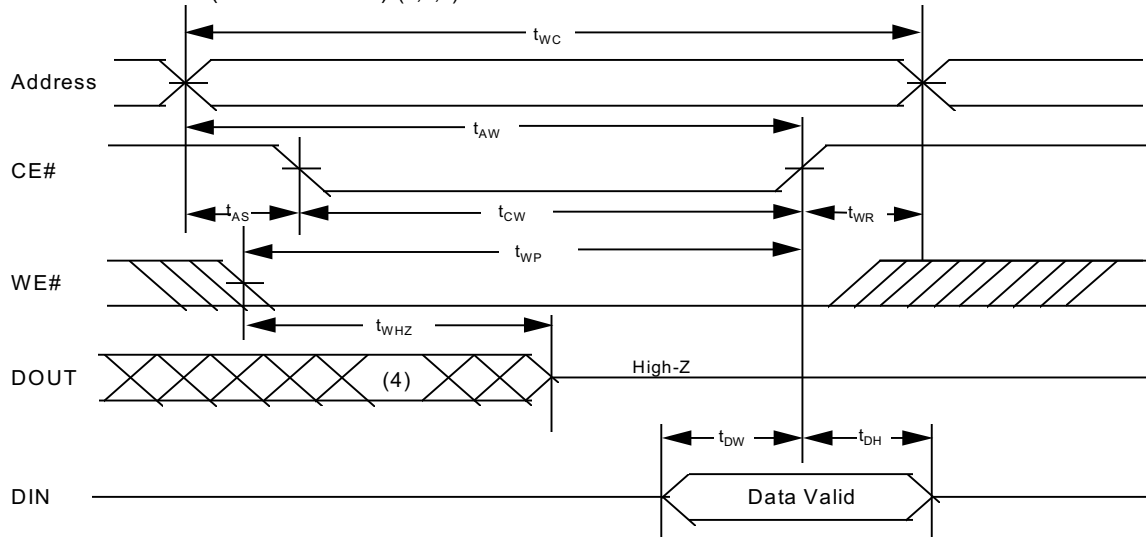
1. WE# is HIGH for read cycle.
2. Device is continuously selected CE#=V<sub>IL</sub>.
3. Address must be valid prior to or coincident with CE# transition; otherwise  $t_{AA}$  is the limiting parameter.
4. OE# is LOW.
5. t<sub>CLZ</sub>, t<sub>OLZ</sub>, t<sub>CHZ</sub> and t<sub>OHZ</sub> are specified with C<sub>L</sub> = 5pF. Transition is measured ± 500mV from steady state.
6. At any given temperature and voltage condition, t<sub>CHZ</sub> is less than t<sub>CLZ</sub>, t<sub>OHZ</sub> is less than t<sub>OLZ</sub>.



**WRITE CYCLE 1 (WE# Controlled) (1,2,3,5)**



**WRITE CYCLE 2 (CE# Controlled) (1,2,5)**



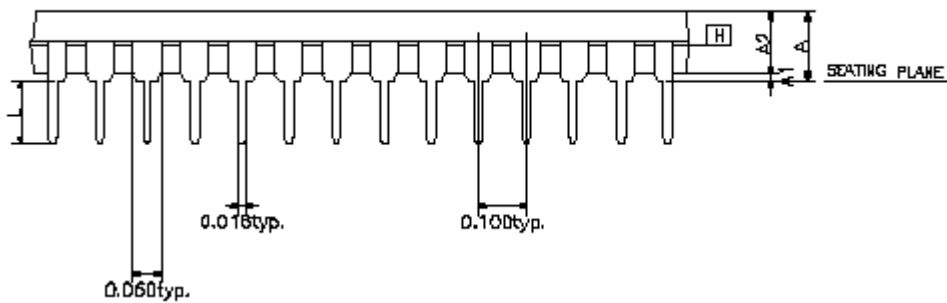
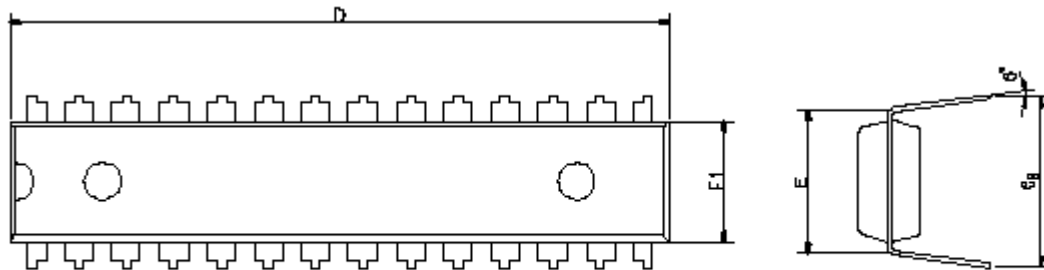
Notes :

1. WE# or CE# must be HIGH during all address transitions.
2. A write occurs during the overlap of a low CE# and a low WE#.
3. During a WE# controlled with write cycle with OE# LOW, t<sub>wp</sub> must be greater than t<sub>whz</sub>+t<sub>dw</sub> to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# LOW transition occurs simultaneously with or after WE# LOW transition, the outputs remain in a high impedance state.
6. t<sub>ow</sub> and t<sub>whz</sub> are specified with C<sub>L</sub> = 5pF. Transition is measured ± 500mV from steady state.



PACKAGE OUTLINE DIMENSION

28 pin 300 mil skinny PDIP PACKAGE OUTLINE DIMENSION



UNIT SYMBOL	MIN	NOR.	MAX
A	-	-	0.210
A1	0.015	-	-
A2	0.125	0.130	0.135
D	1.385	1.390	1.400
E	0.310 BSC		
E1	0.283	0.288	0.293
L	0.115	0.130	0.150
eB	0.330	0.350	0.370
$\theta^\circ$	0	7	15

Note :  
1. JEDEC OUTLINE : N / A

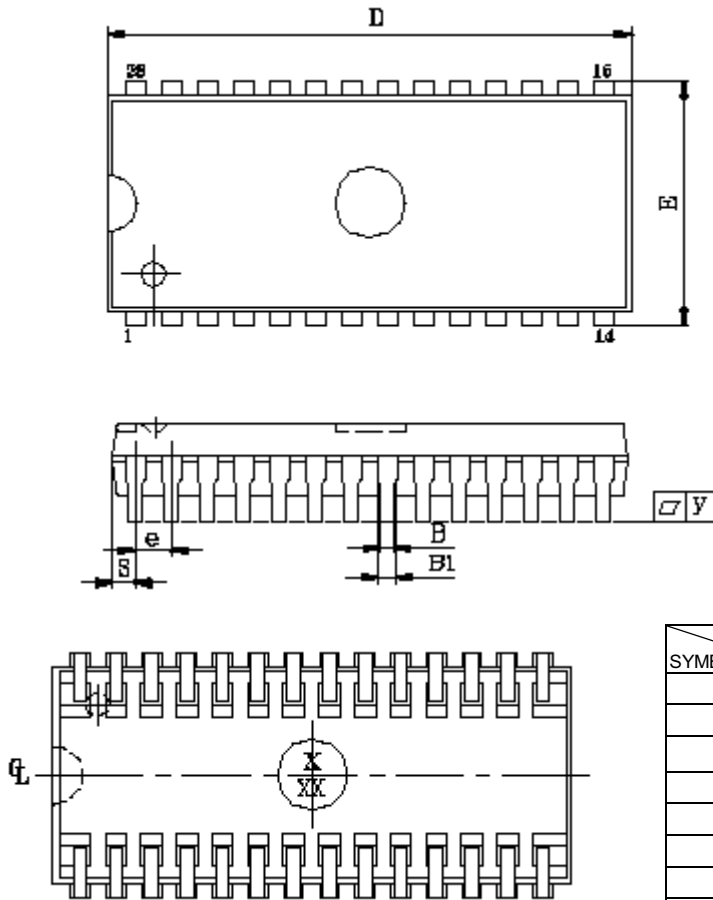


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# UT61256 32K X 8 BIT HIGH SPEED CMOS SRAM

28 pin 300 mil SOJ PACKAGE OUTLINE DIMENSION



UNIT SYMBOL	INCH(BASE)	MM(REF)
A	0.148 (MAX)	3.759 (MAX)
A1	0.026(MIN)	0.660(MIN)
A2	0.100± 0.005	2.540± 0.127
B	0.018 (TYP)	0.457(TYP)
B1	0.028 (TYP)	0.711(TYP)
c	0.010 (TYP)	0.254 (TYP)
D	0.710 (TYP)	18.034 (TYP)
E	0.335(TYP)	8.509(TYP)
E1	0.3 (TYP)	7.620(TYP)
e	0.050 (TYP)	1.270 (TYP)
L	0.087± 0.010	2.210± 0.254
S	0.030 (TYP)	0.762 (TYP)
Y	0.003(MAX)	0.076(MAX)



Note:

1. S/E/D DIM. NOT INCLUDING MOLD FLASH.
2. THE END FLASH IN PACKAGE LENGTHWISE IS NOT MORE THE 10 MILS EACH SIDE.

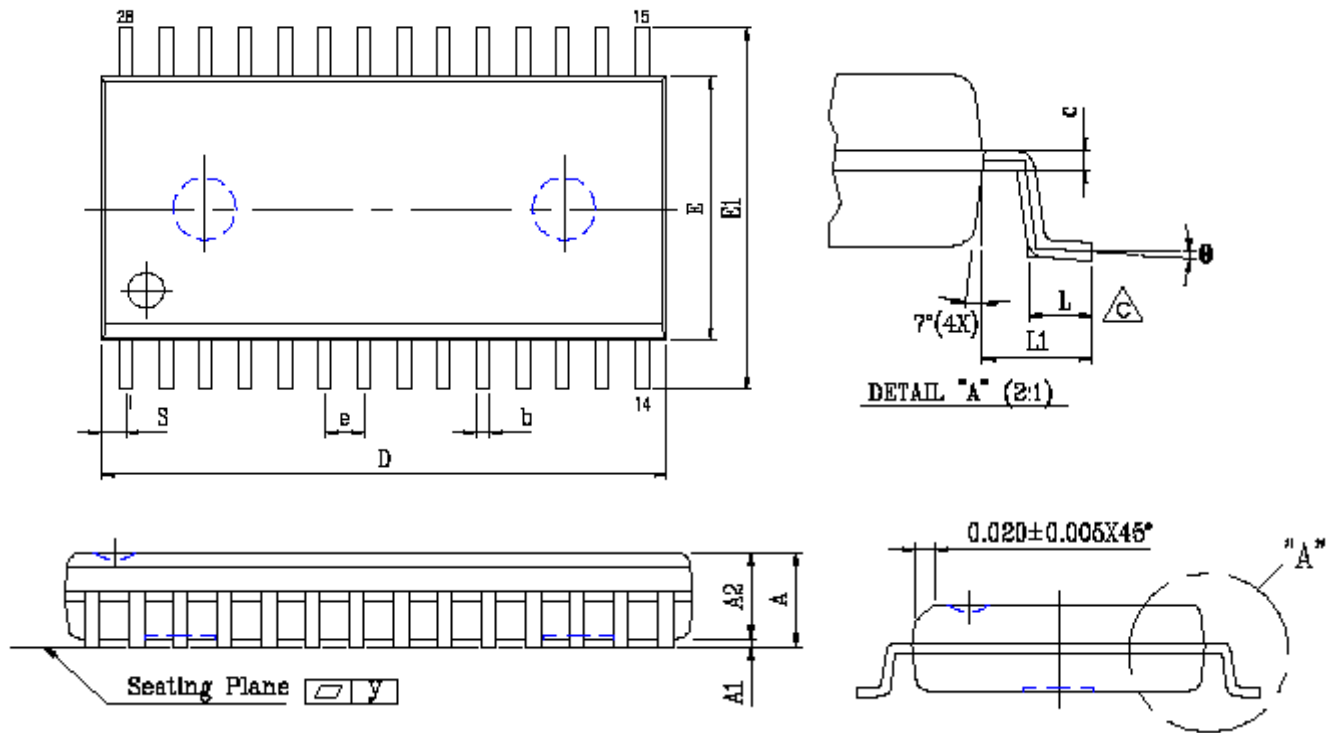


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UT61256  
32K X 8 BIT HIGH SPEED CMOS SRAM

28 pin 330 mil SOP Package Outline Dimension



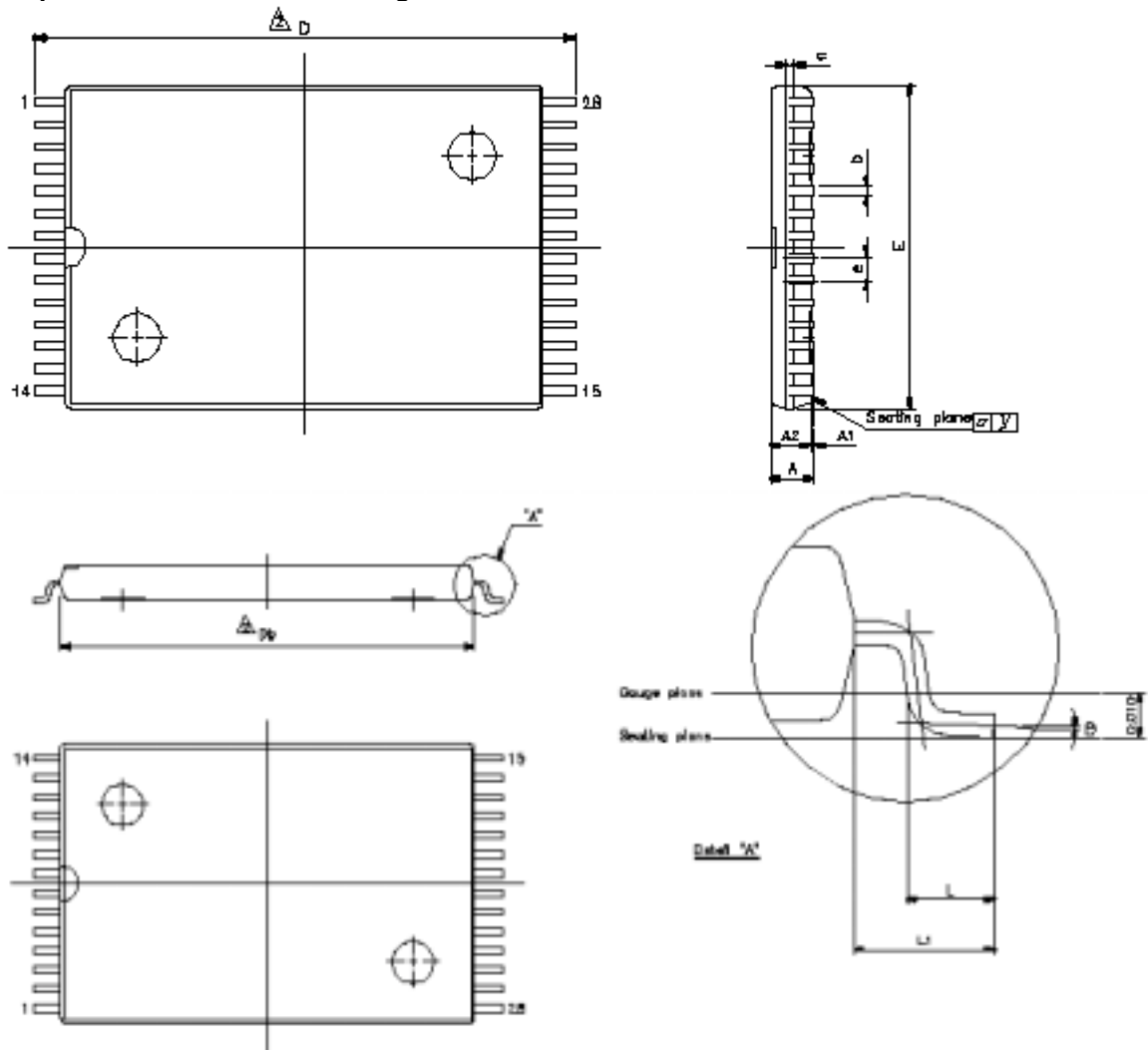
SYMBOL	UNIT	INCH(BASE)	MM(REF)
A		0.120 (MAX)	3.048 (MAX)
A1		0.002(MIN)	0.05(MIN)
A2		0.098± 0.005	2.489± 0.127
b		0.016 (TYP)	0.406(TYP)
c		0.010 (TYP)	0.254(TYP)
D		0.728 (MAX)	18.491 (MAX)
E		0.350 (MAX)	8.890 (MAX)
E1		0.465± 0.012	11.811± 0.305
e		0.050 (TYP)	1.270(TYP)
L		0.05 (MAX)	1.270 (MAX)
L1		0.067± 0.008	1.702± 0.203
S		0.047 (MAX)	1.194 (MAX)
y		0.003(MAX)	0.076(MAX)
θ		0°~ 10° 0	°~ 10°







28 pin 8x13.4mm TSOP-I Package Outline Dimension



Note :  
E dimension is not including end flash  
The total of both sides' end flash is  
Not above 0.3mm.

UNIT SYMBOL	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004± 0.002	0.10± 0.05
A2	0.039± 0.002	1.00± 0.05
b	0.006 (TYP)	0.15(TYP)
c	0.010 (TYP)	0.254(TYP)
$\Delta_2$ Db	0.465± 0.004	11.80± 0.10
E	0.315± 0.004	8.00± 0.10
e	0.022 (TYP)	0.55(TYP)
$\Delta_2$ D	0.528± 0.008	13.40± 0.20
$\Delta_2$ L	0.020± 0.004	0.50± 0.10
$\Delta_2$ L1	0.0315± 0.004	0.80± 0.10
$\Delta_5$ y	0.08(MAX)	0.003(MAX)
$\theta$	0°~5° 0	°~5°



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REV 1.0

**UT61256**  
**32K X 8 BIT HIGH SPEED CMOS SRAM**

**ORDERING INFORMATION**

<b>PART NO.</b>	<b>ACCESS TIME (ns)</b>	<b>PACKAGE</b>
UT61256KC-15	15	28PIN SKINNY PDIP
UT61256SC-15	15	28PIN SOP
UT61256JC-8	8	28PIN SOJ
UT61256JC-12	12	28PIN SOJ
UT61256JC-15	15	28PIN SOJ
UT61256LS-8	8	28PIN TSOP-I
UT61256LS-12	12	28PIN TSOP-I
UT61256LS-15	15	28PIN TSOP-I