Incoming Call Line Identification (ICLID) Receiver with Ring Detection

ICS1660

Description

The **ICS1660** "ICLID" circuit is a monolithic CMOS VLSI device that decodes and detects the Frequency Shift Keying (FSK) signals used in caller identification telephone service. The **ICS1660**, when used in conjunction with some external components, amplifies, filters and demodulates the FSK data transmitted from the central office to the telephone subscriber.

The **ICS1660** detects the first power ring signal and demodulates the 1200 baud FSK data transmitted during the silent interval between the first and second power ring. The FSK data is transmitted from the central office switch to the subscriber line as part of the CLASS service of Calling Number Delivery (CND). This data is then demodulated, amplified and filtered by the **ICS1660** and digitally transmitted to the host controller/processor.

The **ICS1660** is designed to be powered by any off-the-shelf 9.0 volt battery. The on-chip 5.0 voltage regulator powers the host microprocessor and any external circuitry supported by the **ICS1660**. This portion of the circuit can be overridden by connecting the V_{IN} pin (18) to the V_{DD} pin (1) for a common power supply. A low battery detection circuit is also provided on-chip and signals the microprocessor on the FSK/BAT pin (17) when the PWR pin (16) input is pulled low.
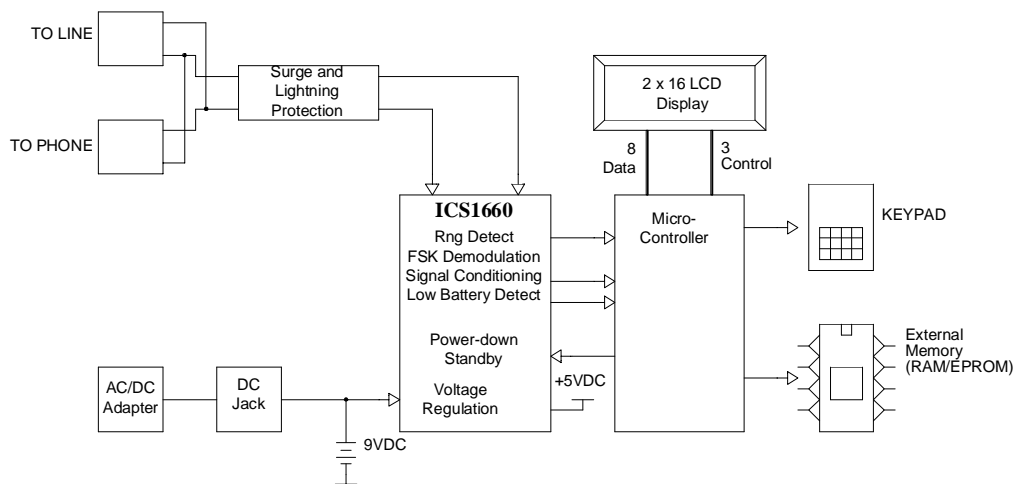
Features

- Ring Detection
- Low Battery Detection
- Internal 5V Regulator - can externally source 25mA
- FSK Demodulation
- Power-down in Standby Mode
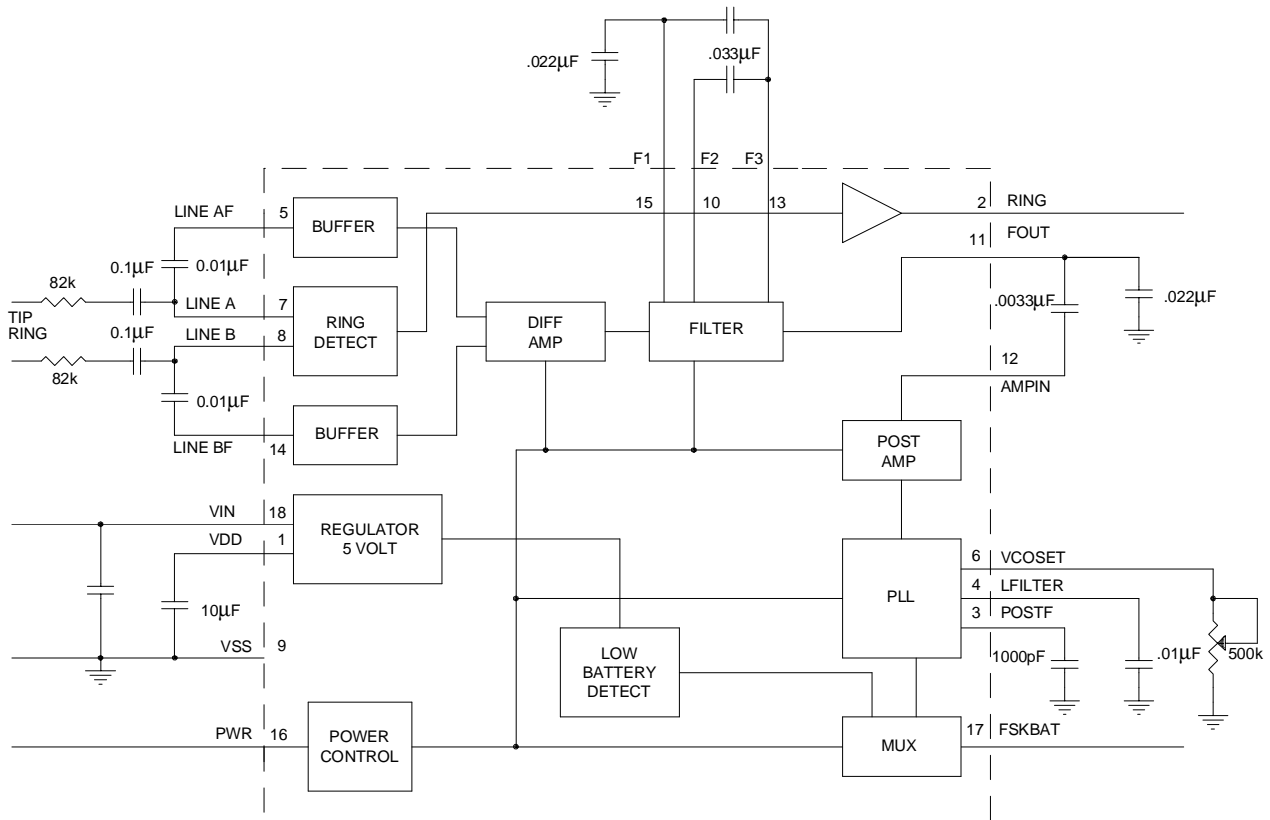- Direct Interface to Host Microprocessor or Microcomputer

Applications

- Telephones
- Facsimile Machines
- Modems
- Telephone Interface Equipment
- Stand-alone ICLID products

ICLID Block Diagram

Block Diagram

Function Description

Power Supply

The **ICS1660** is designed to be powered by a standard 9.0 volt battery. The chip contains a voltage regulator that powers external circuitry and provides the supply voltage for all digital I/O on the circuit. This allows easy interface between the **ICS1660** and other standard logic working at 5.0V. This regulator has short circuit protection and requires an external filter/compensation capacitor with a minimum value of 10uf.

In the event that an external regulated 5.0V supply is available, the V_{IN} and V_{DD} pins can be shorted to permit the entire system to work from a common supply.

A low battery detection circuit is provided. This circuit is designed for a typical trip point of 6.0V with hysteresis of about 200mV above the trip point. This signal is low active and is multiplexed to the FSKBAT output pin when the PWR input is low.

In an effort to keep power dissipation to a minimum and extend battery life, most of the analog circuits are turned off when the circuit is at rest waiting for a ring detect, (PWR pin low). During this time only the regulator, low battery detect, reference generator, and ring detect circuits are active. When the PWR pin is high, all circuits are active.

Ring Detect

As shown in the attached block diagram, the LINEA and LINEB inputs should be connected to the telephone line through external 82kΩ resistors and 0.1uf capacitors. This provides DC isolation and sets up a voltage divider with internal resistors that will detect 35.0V RMS typically. This voltage is applied across the LINEA and LINEB inputs. The design value of the internal resistors is 8.1KΩ ± 20% with relative accuracy of 2%. The RING output is high active.

Differential Front End

As shown in the attached block diagram, the LINEA and LINEB inputs go into a differential amplifier which in turn drives a filter. All resistors are internal to the chip while capacitors are connected as shown in the block diagram. After filtering, the signal is AC coupled into a high gain amplifier that converts the signal to digital. This digital signal in turn acts as the reference frequency for the phase comparator section of the phase locked loop.
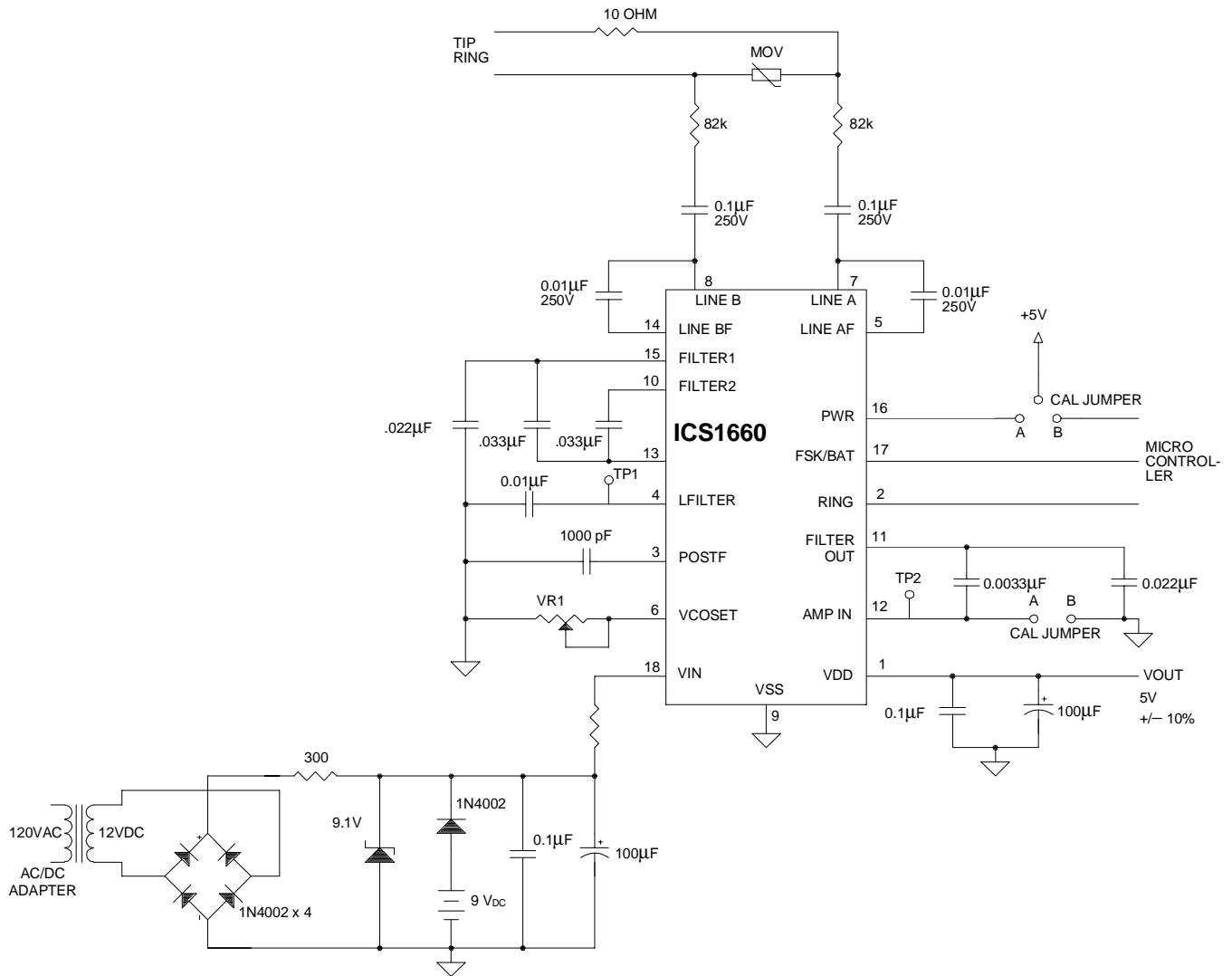
FSK Demodulation

After the signal from the telephone line has been filtered, amplified and converted to digital, it acts as an input to a phase locked loop. This PLL does FSK demodulation. The summing amplifier shown in the block diagram provides a signal to the VCO that should be about 0.5V for MARK frequency (1200 HZ), and 2.0V for SPACE frequency (2200 HZ).

As shown in the block diagram, the LFILTER (loop filter) output has a post filter attached to it. This POSTF signal is sent to a comparator. The other side of the comparator is set to approximately 2.5V. This comparator has a small amount (200mV) of hysteresis and its output is the demodulated FSK data. The FSK output is high for MARK frequency and low for SPACE frequency. FSK data is multiplexed out of the FSKBAT pin when the PWR input is high.

The VCO frequency is set with one external resistor with a value in the range of 300K for a center frequency of 1700 HZ. The lock range will be 660 HZ to 2630 HZ typical. The center frequency reproducibility will be ±15%. The center frequency can be adjusted in the system by connecting AMPIN to VSS, PWR to VDD, and adjusting the external resistor for 1700 HZ. This frequency can be observed at the LFILTER output or the FSK/BAT output.

Typical Application

Pin Descriptions

PIN NUMBER		NAME	DESCRIPTION
DIP	SO		
1	1	VDD	Supply voltage pin to external circuits. Output of 5.0 volt regulator.
2	2	RING	Ring detect output signal to the host microprocessor.
3	3	POSTF	Post loop filter signal used by demodulator.
4	4	LFILTER	Loop filter for PLL.
5	5	LINEAFILTER	Filter input from line "A."
6	6	VCOSET	Center frequency adjustment pin.
7	7	LINEA	"Tip" input from telephone line.
8	8	LINEB	"Ring" input from telephone line.
9	9	VSS	Ground.
10	11	FILTER2	Active filter pin.
11	12	FILTEROUT	Active filter pin.
12	13	AMPIN	Input from active filter.
13	14	FILTER3	Active filter pin.
14	15	LINEBFILTER	Filter input from line "B."
15	16	FILTER1	Active filter pin.
16	17	PWR	Logic input signal to switch from low current standby mode.
17	18	FSK/BAT	Multiplexed output signal controlled by PWR pin. In standby mode, this is a low battery (active low) signal. During FSK demodulation, this is the data line to the µP (mark = high).
18	19	VIN	Input power supply pin.
10	20	NC on SOIC	

	18 PIN DIP	
VDD	1	18 — VIN
RING	2	17 — FSK/BAT
POSTF	3	16 — PWR
LFILTER	4	15 — FILTER1
LINEAFILTER	5	14 — LINEBFILTER
VCOSET	6	13 — FILTER3
LINEA	7	12 — AMPIN
LINEB	8	11 — FILTEROUT
VSS	9	10 — FILTER2

	20 PIN SOIC	
VDD	1	20 — NC
RING	2	19 — VIN
POSTF	3	18 — FSK/BAT
LFILTER	4	17 — PWR
LINEAFILTER	5	16 — FILTER1
VCOSET	6	15 — LINEBFILTER
LINEA	7	14 — FILTER3
LINEB	8	13 — AMPIN
VSS	9	12 — FILTEROUT
NC	10	11 — FILTER2
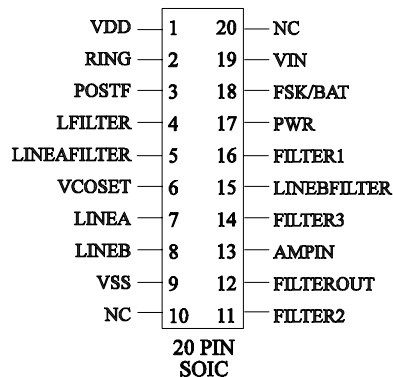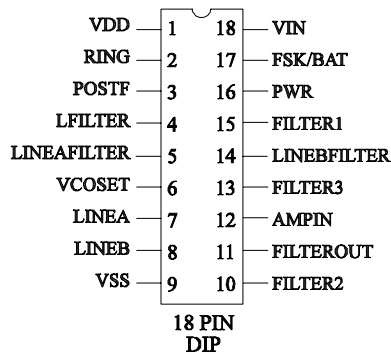
Input/Output Specifications

Digital

RING and FSKBAT outputs are standard CMOS outputs with voltage swings between V_{SS} and V_{DD}.

PWR is a logic input. A level converter circuit is on chip to allow the logic signal that swing between V_{SS} and V_{DD} to be internally converted to signals that swing between V_{SS} and V_{IN}. It should be noted that to minimize power consumption caused by through current in logic gates, the PWR input should always swing to within 100 mV of V_{SS} or V_{DD}. The PWR input signal is low when the **ICS1660** is in lower power mode waiting for an incoming call.

The LFILTER output is a standard CMOS output powered from VDD. This output has an internal resistor with a typical value of 30kΩ. This is used in conjunction with the external capacitor shown in the block diagram to form the loop filter for the PLL.

Analog

The value of the ring detect is as previously discussed 35.0V RMS typical. The actual value is set by the choice of the external resistors that are connected to the LINEA and LINEB inputs. The matching of these resistors to the internal 8.1kΩ resistors is also a factor. The signal level at the chip that will cause a ring is the bandgap voltage, (1.25V) or below.

The chip is designed for an input signal level of -12.5dbm to -28.5dbm into 900 ohms. This translates to a signal that is between 100 mV and 636 mV peak to peak.

The filter section should be connected as shown in the block diagram. Using the external capacitors as shown, and assuming nominal values on the internal resistors, the corner frequencies are 900 HZ and 3860 HZ.

An external resistor with a value of approximately 330kΩ is connected between the LFILTER and POSTF pads. This resistor along with the external capacitor shown in the block diagram form the post filter. This post filter is used in conjunction with the comparator to do the FSK demodulation.

Absolute Maximum Ratings*

(Voltages referenced to V_{SS})

Supply Voltage . . . . V_{IN} . . . . -0.5V to +10V
Voltage at any Input . . . . -0.5V to V_{DD} + 0.5V
Operation Temperature Range . . . . -55°C to +125°C
Storage Temperature Range . . . . -50°C to 150°C

* Absolute maximum ratings are those values beyond which the safety of this device cannot be guaranteed. These values are NOT RECOMMENDED operating conditions.
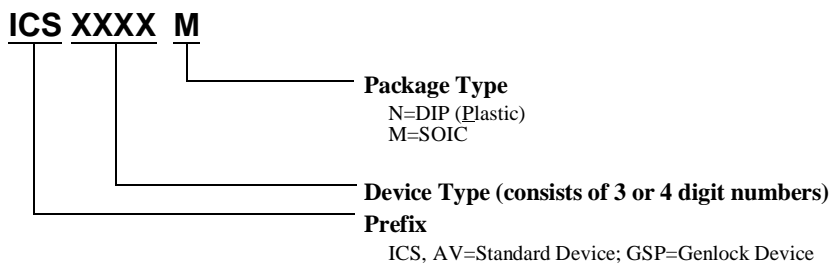
DC Characteristics

V_{IN} = 4.5V - 10.0V; T_A = 0 °C - 70 °C, Recommended Operating Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Standby Current	I_{IN}	PWR LOW, V_{IN} =9.0V, I_{DD}=2µA	-	20	30	uA
Active Current	I_{IN}	PWR HIGH, V_{IN}=9.0V VCOSET=300k	-	-	10	mA
Regulator Output Voltage	V_{DD}		4.5	5.0	5.5	Volts
Regulator Output Current	I_{DD}	Output Current	2.0		25.0	mA
Regulator Dropout	V_{IN}			0.5	1.0	Volts
Low Battery Detect				6.0		Volts
Low Battery Detect Hysteresis		Low Battery Detect - Hysteresis		200		mV
OUTPUT CURRENT SINK/SOURCE						
Ring Source Current	I_{OUT}	$VOUT_H$ = V_{DD} - 0.5V	-500	-	-	uA
FSKBAT and Ring Sink Current	I_{OUT}	$VOUT_L$ = V_{SS} + 0.4V	-	-	500	uA

Ordering Information

ICS1660N or ICS1660M

Example:

ICS XXXX M

Package Type
N=DIP (Plastic)
M=SOIC

Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

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