

Electrical Specifications

ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
P_D	Power Dissipation	–	–	350	mW
V_{CC}	Supply Voltage	–0.5	–	7.0	V
AV_{CC}	Analog Supply Voltage	–0.5	–	7.0	V
V_{IN}	Input Voltage	–0.5	–	$V_{CC}+0.5$	V
T_{OP}	Operating Temperature (Ambient)	0	–	+70	°C
T_{STG}	Storage Temperature	–65	–	+150	°C
T_J	Junction Temperature	–	–	125	°C
T_{SOL}	Maximum Soldering Temperature (10 sec.)	–	–	+260	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

NORMAL OPERATING CONDITIONS

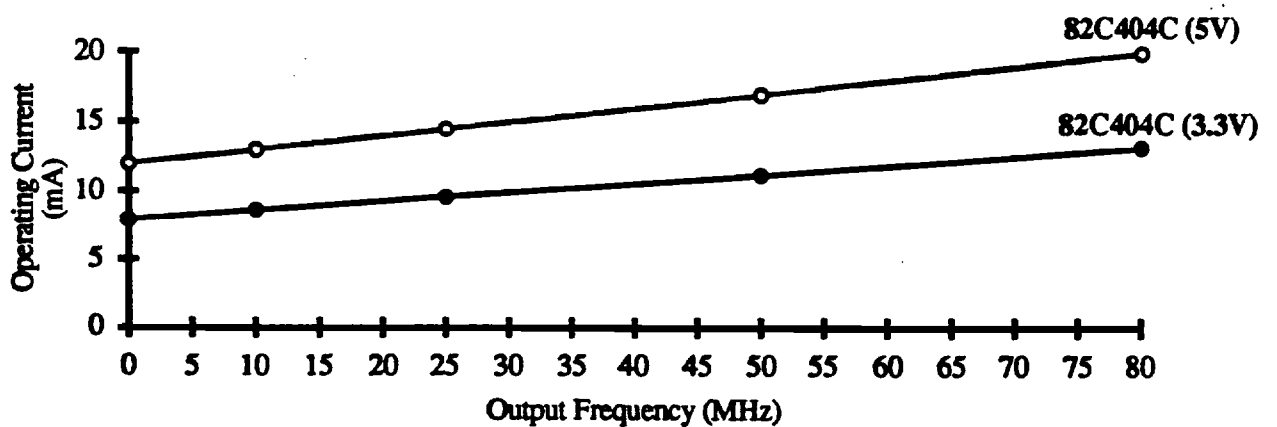
Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	3.0	–	5.5	V
AV_{CC}	Analog Supply Voltage	3.0	–	5.5	V
T_A	Ambient Temperature	0	–	70	°C

Electrical specifications contained herein are preliminary and subject to change without notice.

DC CHARACTERISTICS

(Under Normal Operation Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Max	Units
I_{CC}	Power Supply Current (V_{CC})	5V @ 0°C	15	65	mA
I_{ACC}	Power Supply Current (AV_{CC})	5V	—	10	mA
I_{PD1}	Power Supply Current	Power-Down Mode 1	—	7.5	mA
I_{PD2}	Power Supply Current	Power-Down Mode 2†	—	50	μA
I_{IL}	Input Low Leakage Current	$V_{IL} = 0.0V$	—	−250	μA
I_{IH}	Input High Current	$V_{IH} = 5.25V$	—	100	μA
I_{OZ}	Output Leakage Current	Tri-State	—	10	μA
V_{IL}	Input Low Voltage		$V_{CC}-0.5$	0.8	V
V_{IH}	Input High Voltage		2.0	$V_{CC}+0.5$	V
V_{OL}	Output Low Voltage	$I_{OL} = 4.0\text{ mA}$	—	0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -4.0\text{ mA}$ $V_{CC}=5V$	3.84	—	V
		$I_{OH} = -4.0\text{ mA}$ $V_{CC}=3.3V$	TBD	—	V
C_{IN}	Input Capacitance		—	10	pF
	Bit Jitter	(1σ)	—	±350	ps
	Bit Jitter	Absolute	—	500	ps
R_{BQ}	Equivalent Series Resistance of Reference Crystal		—	150	Ω

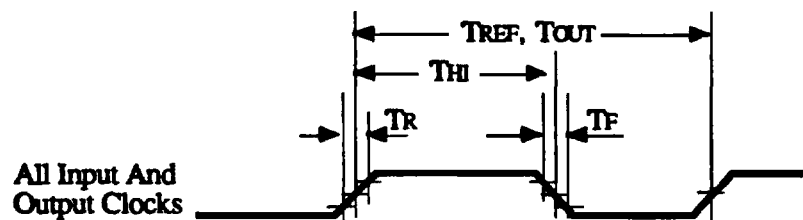
 † INIT0 and INIT1 may produce additional leakage currents as defined by I_{IH} if pulled-up externally


Typical Current vs. Total Output Frequency

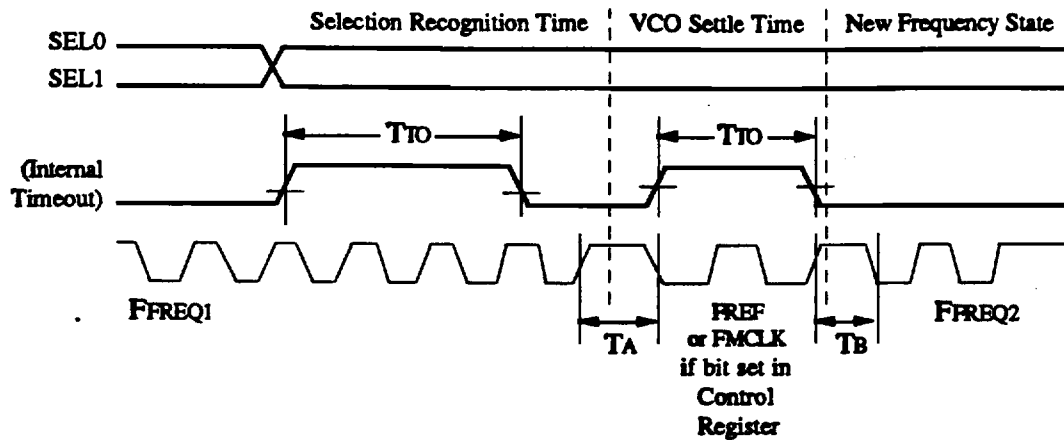
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AC CHARACTERISTICS - Clock Timing

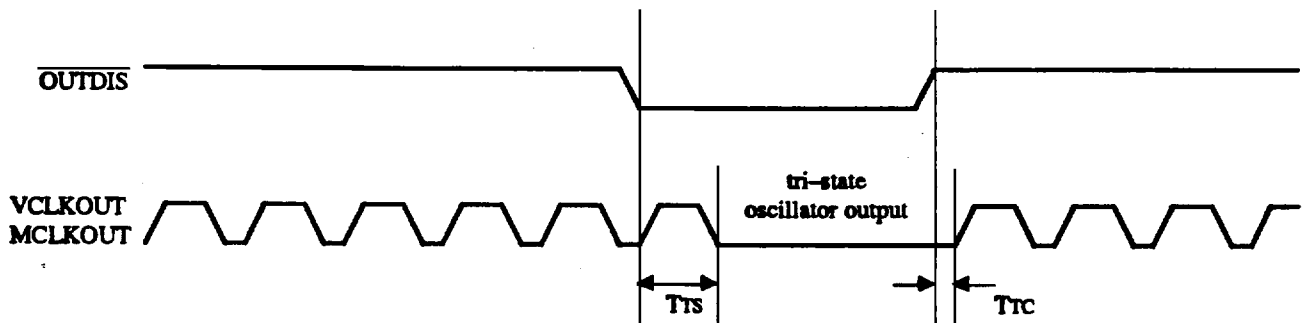
Symbol	Parameter	Notes	Min	Typ	Max	Units
F_{REF}	Reference Frequency	(± 100 ppm)	1	14.31818	60	MHz
T_{REF}	Reference Clock Period	$1/F_{REF}$	16.6	69.84128	1000	nS
T_{HI}/T_{REF}	Reference Clock Duty Cycle		25	—	75	%
T_R	Output Clock Rise Time	25pf Load	—	—	3	nS
T_F	Output Clock Fall Time	25pf Load	—	—	3	nS
T_{HI}/T_{OUT}	Output Clock Duty Cycle	$V_{TH} = 2.5V$	45	—	55	%
T_{OUT}	Output Clock Period (3.3V)	262 KHz - 75 MHz	13.33	—	3817	nS
T_{OUT}	Output Clock Period (5V)	390 KHz - 120 MHz	8.33	—	2564	nS
T_A	F_{REF} Mux Time		$0.5 T_{REF}$	—	$1.5 T_{REF}$	nS
T_B	F_{OUT} Mux Time		$0.5 T_{FREQ2}$	—	$1.5 T_{FREQ2}$	nS
T_{TO}	Timeout Interval		2	5	10	mS
T_{IS}	OUTDIS# Active to Output 3-state		0	—	12	nS
T_{IC}	OUTDIS# Inactive to Valid Clock Out		0	—	12	nS
T_{ID}	PWRDN# Active to VCLKOUT High		0	—	12	nS
T_{PD}	PWRDN# Active to MCLKOUT= $F_{Powerdown}$		0	—	$2/F_{REF}$	nS
T_{PU}	PWRDN# Inactive to Valid Clock Out		0	—	12	nS
T_{MH}	PWRDN# Inactive to MCLKOUT High		0	—	T_{PD}	nS
T_{MD}	MCLK Delay to F_{MCLK} at Output		$0.5 T_{MCLK}$	—	$1.5 T_{MCLK}$	nS
T_{SC}	Clock Period of Serial Clock		$2/T_{REF}$	—	2	mS
T_{SU}	Setup Time		20	—	—	nS
T_{HD}	Hold Time		10	—	—	nS
T_{LD}	Internal Register Load		0	—	$T_{HI} + 30$	nS



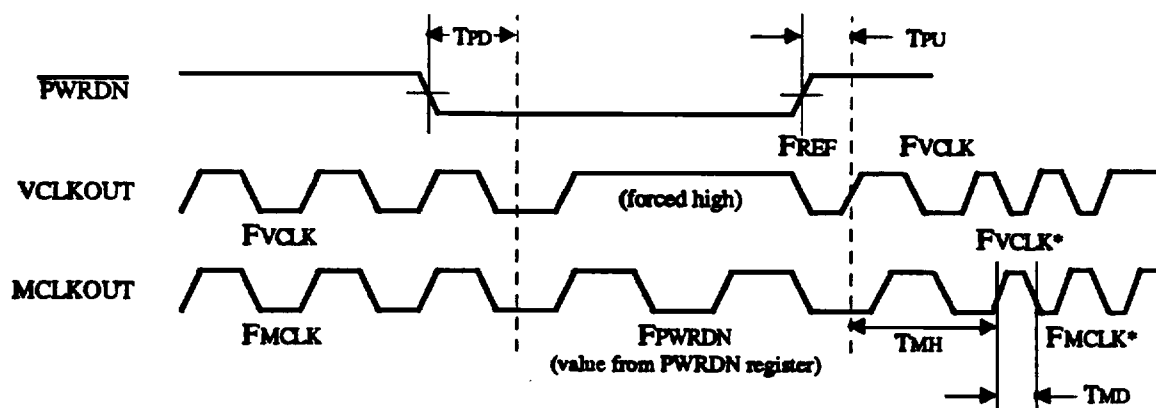
Reference and Output Clock Rise and Fall Times



Frequency Selection Timing

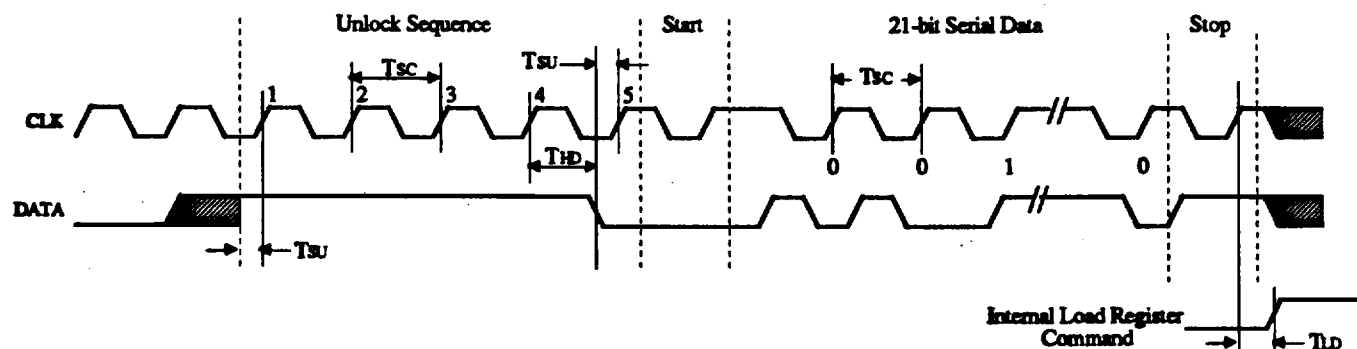


Output Tri-State Timing

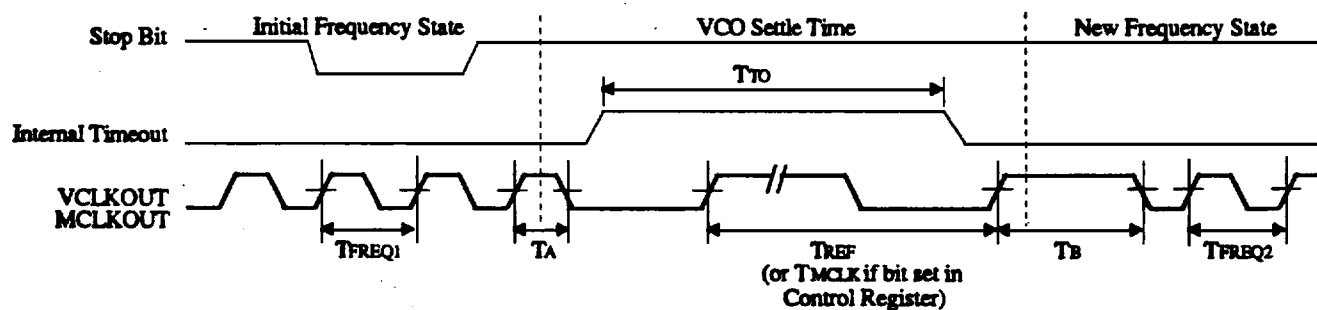


Power-Down Timing

* It takes 2-10 msec after power-down is released to guarantee lock of the VCLK and MCLK PLL's.



Serial Programming Timing



MCLK and Active VCLK Register Programming Timing