TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

1,048,576-WORD BY 18-BIT SYNCHRONOUS NO-TURNAROUND STATIC RAM

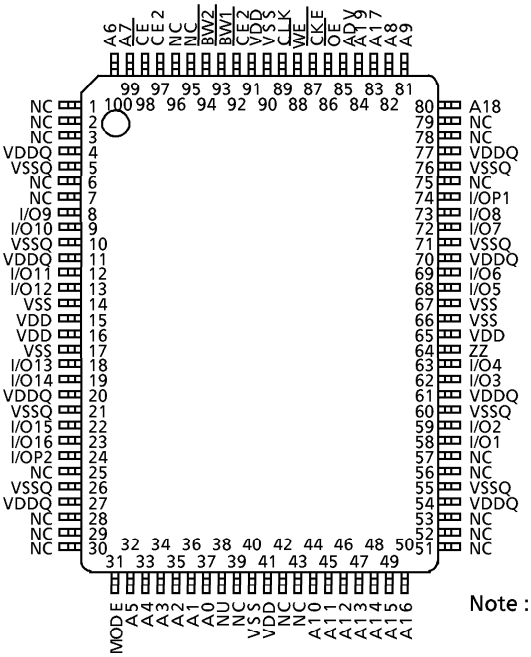
DESCRIPTION

The TC55VL1618FF is a synchronous static random access memory(SRAM) organized as 1,048,576 words by 18 bits. NtRAM™(no-turnaround) SRAM offers high bandwidth by eliminating dead cycles during the transition from a read to a write and vice versa. All inputs except Output Enable $\overline{OE}$ and the Snooze pin ZZ are synchronized with the rising edge of the CLK input. A Read operation is initiated by the ADV Address Advanced Input signal ; the input from the address pins and all control pins except the $\overline{OE}$ and ZZ pins are loaded into the internal registers on the rising edge of CLK in the cycle in which ADV is asserted. The output data is available in the same clock cycle as that in which ADV is asserted. Write operations are internally self-timed and are initiated by the rising edge of CLK in the cycle in which ADV is asserted. The input from the address pins and all control pins except the $\overline{OE}$ and ZZ pins are loaded into the internal registers on the rising edge of CLK in the cycle in which ADV is asserted. Input data is loaded in the cycle following the cycle in which ADV is asserted. Byte Write Enables($\overline{BW1}$ to $\overline{BW2}$) allow from one to four Byte Write operations to be performed. A 2-bit burst address counter and control logic are integrated into this SRAM. The TC55VL1618FF uses a single power supply(3.3V) or dual power supplies(3.3V for core and 2.5V for output buffer) and is available in a 100-pin low-profile plastic QFP(LQFP).

FEATURES

- Organized as 1,048,576 words by 18 bits
- Fast cycle time of 10 ns minimum (100 MHz maximum)
- Fast access time of 8.5 ns maximum (from clock edge to data output)
- No-turnaround operation with flow-through data output
- 2-bit burst address counter (support for interleaved or linear burst sequences)
- Synchronous self-timed Write
- Byte Write control
- Snooze mode pin (ZZ) for power down
- LVTTL-compatible interface
- Single power supply (3.3 V) or Dual power supplies(3.3V for core and 2.5V for output buffer)
- Available in 100-pin LQFP package (LQFP100-P-1420-0.65K ; pitch:0.65 mm, height:1.6 mm, weight: grams(typical))

PIN ASSIGNMENT (TOP VIEW)



PIN NAMES

CLK	Clock Input
A0 to A19	Address Inputs
$\overline{CE}$, $\overline{CE2}$, CE2	Chip Enable Inputs
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable Input
$\overline{BW1}$ to $\overline{BW2}$	Byte Write Enable
ADV	Address Advance Input
$\overline{CKE}$	Clock Enable
ZZ	Snooze Input
I/O1 to I/O16	Data Inputs/Outputs
I/OP1 to I/OP2	Parity Data Inputs/Outputs
MODE	Mode Select Input
NC	Not Connected
NU	Not Usable
V_{DD}	Power Supply for Core
V_{DDQ}	Power Supply for Output Buffer
V_{SS}	Ground for Core
V_{SSQ}	Ground for Output Buffer

Note : NtRAM™ and No-Turnaround Random Access Memory are trademarks of Samsung Electronics Co., Ltd..

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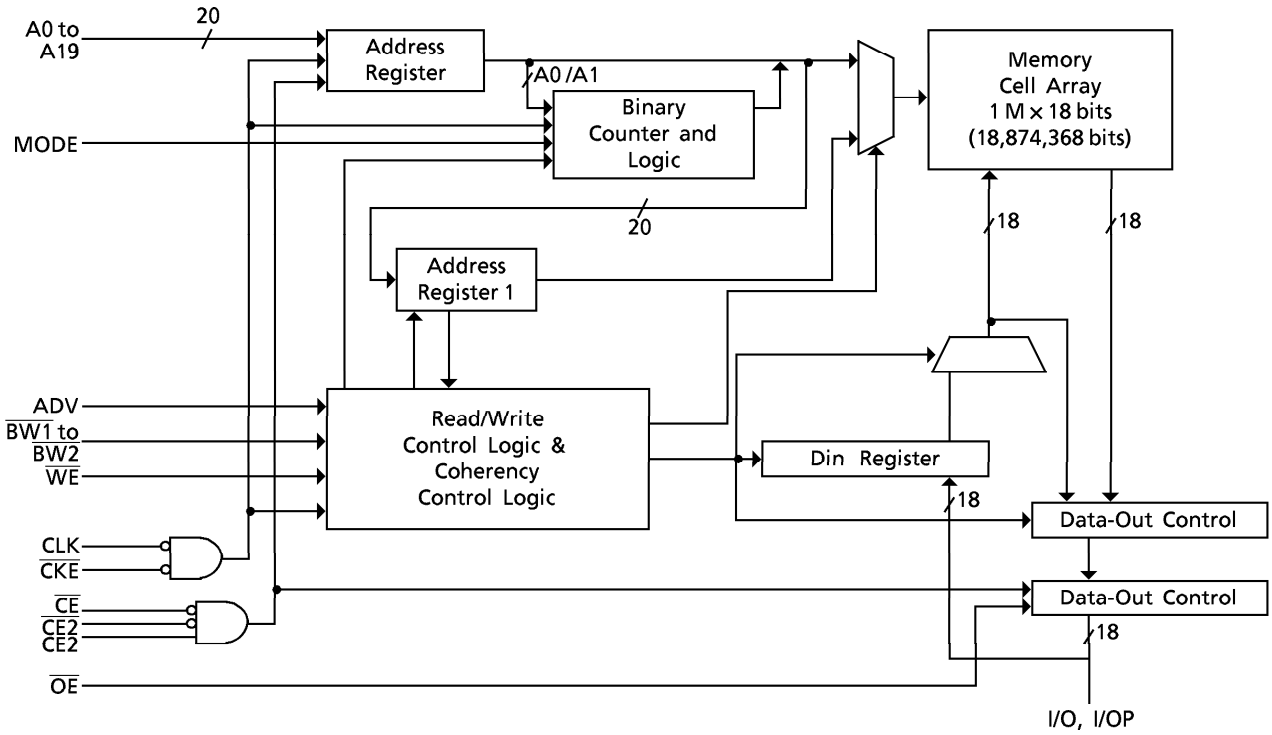
BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NUMBER	SYMBOL	TYPE	DESCRIPTION
89	CLK	Input (NA)	**Clock Input** All synchronous input signals are registered on the rising edge of CLK. When the chip is enabled, address inputs and control pins except for $\overline{OE}$ and ZZ must meet the specified setup and hold times with respect to the CLK rising edge.
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49, 50, 83, 80, 84	A0 to A19	Input (synchronous)	**Address Inputs** These address inputs are registered on the rising edge of CLK. When the chip is enabled, address inputs must meet the specified setup and hold times with respect to the CLK rising edge.
98	$\overline{CE}$	Input (synchronous)	**Chip Enable Input** This active-Low signal controls the chip status (enabled or disabled). It is sampled only when a new external address is loaded.
92	$\overline{CE2}$	Input (synchronous)	**Chip Enable Input** This active-Low signal controls the chip status (enabled or disabled). It is sampled only when a new external address is loaded.
97	CE2	Input (synchronous)	**Chip Enable Input** This active-High signal controls the chip status (enabled or disabled). It is sampled only when a new external address is loaded.
86	$\overline{OE}$	Input (asynchronous)	**Output Enable Input** This active-Low signal control all 36-bits I/O output buffer.
88	$\overline{WE}$	Input (synchronous)	**Write Enable Input** This active-Low input controls Read/Write operations.
93, 94	$\overline{BW1}$ to $\overline{BW2}$	Input (synchronous)	**Byte Write Enable** These active-Low inputs control Byte Write operations when a Write cycle is active. A Byte Write pin controls I/O pins as follows. $\overline{BW1}$:I/O1 to I/O8, I/OP1 $\overline{BW2}$:I/O9 to I/O16, I/OP2
85	ADV	Input (synchronous)	**Address Advance Input** This is used to load the internal registers with the input from the address and control signals when it is Low on the rising edge of CLK. When it is High, the internal burst address counter is incremented. The external address inputs are ignored when this signal is High.
87	$\overline{CKE}$	Input (synchronous)	**Clock Enable** When High, CLK input is ignored and outputs retain the same state.

PIN NUMBER	SYMBOL	TYPE	DESCRIPTION
64	ZZ	Input (asynchronous)	**Snooze Input** This active-High signal is used to place the device into Sleep Mode (Low-Power Standby Mode). When Low, the device remains in the Active state. When High, the device goes into the Sleep state and memory data is retained. After this signal has been deasserted, the device will wake up when a Read or Write operation is initiated by ADV.
58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23	I/O1 to I/O16	I/O (synchronous)	**Data Input/Output**
74, 24	I/OP1 to I/OP2	I/O (synchronous)	**Parity Data Input/Output**
31	MODE	Input (synchronous)	**Mode Select Input** This signal selects the burst sequence. When High, the burst sequence is interleaved. When Low, it is linear sequence.
1, 2, 3, 6, 7, 25, 28, 29, 30, 39, 42, 43, 51, 52, 53, 56, 57, 75, 78, 79, 95, 96	NC	NC	**Not Connected**
38	NU	Input (asynchronous)	**Not Usable**
15, 16, 41, 65, 91	V_{DD}	Supply	**Power Supply for Core**
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	Supply	**Power Supply for Output Buffers**
14, 17, 40, 66, 67, 90	V_{SS}	Ground	**Ground for Core**
5, 10, 21, 26, 55, 60, 71, 76	V_{SSQ}	Ground	**Ground for Output Buffers**

OPERATING MODE

(1) Synchronous Input Truth Table

OPERATION	$\overline{WE}$	ADV	CE	$\overline{BW}$	Addr. Used	$\overline{CKE}$	ZZ	I/O (6)
Read (begin burst)	H	L	Select	×	External	L	L	Output
Read (Continue burst)	×	H	×	×	Internal	L	L	Output
Write (begin burst)	L	L	Select	L	External	L	L	Input
Write (continue burst)	×	H	×	L	Internal	L	L	Input
NOP/Write Abort (begin burst)	L	L	Select	H	×	L	L	Hi-Z
Write Abort (continue burst)	×	H	×	H	Internal	L	L	Hi-Z
Deselected	×	L	Deselect	×	×	L	L	Hi-Z
Deselect Continue (Note 2)	×	H	×	×	×	L	L	Hi-Z
Ignore Clock Edge (Note 3)	×	×	×	×	×	H	L	Previous value
Snooze	×	×	×	×	×	×	H	Hi-Z

Notes: 1. H means logical High and L means logical Low. × means Don't care.
2. A Deselect Continued cycle can only be entered if a Deselect cycle is executed before it.
3. When the Ignore Clock Edge command is asserted during a Read operation, the output data for the previous cycle still appear on the I/O pins. When the command is asserted during a Write operation, the I/O pins remain at Hi-Z, and the Write operation is not executed.
4. All synchronous Inputs must exhibit adequate setup and hold times either side of the rising edge of the CLK pin.
5. The data output appears in the same cycle as that in which the Read command is asserted. Data input is triggered on the rising edge of CLK in the next following the one in which the Write command is asserted.
6. ZZ input is asynchronous, but is included in this table.

(2) Write Enable Truth Table

OPERATION	$\overline{WE}$	$\overline{BW1}$	$\overline{BW2}$	I/O1 to I/O8 I/OP1	I/O9 to I/O16 I/OP2
Read	H	×	×	Output	Output
Write	L	L	L	Input	Input
	L	L	H	Input	Hi-Z
	L	H	L	Hi-Z	Input
	L	H	H	Hi-Z	Hi-Z

Notes: 1. H means logical High and L means logical Low. × means Don't care.

(3) Asynchronous Inputs Truth Table

OPERATION	$\overline{OE}$	ZZ	I/O
Read	L	L	Dout
	H	L	Hi-Z
Write	×	L	Din, Hi-Z
Stop clock (Note 2)	H	L	Hi-Z
	L	L	Dout
Snooze (Note 3)	×	H	Hi-Z

Notes: 1. H means logical High and L means logical Low. × means Don't care.
2. The Stop CLK Mode achieves Low Power Standby by stopping the input clock.
3. The Snooze Mode achieves Low Power Standby by asserting the ZZ pin.
4. The cycle immediately prior to a Snooze brought about by the ZZ pin must be a Read Mode or Deselect Mode cycle.
5. Memory data is retained during Snooze Mode cycles.

(4) Burst Sequence

MODE PIN	BURST OPERATION
L	Linear burst order
H or NC	Interleaved burst order

a) Linear Burst Sequence (MODE input = V_{SS})
Bit Order: A_{19}, ... A_1, A_0

1st Address (external)	2nd Address (internal)	3rd Address (internal)	4th Address (internal)
XX ····· XX00	XX ····· XX01	XX ····· XX10	XX ····· XX11
XX ····· XX01	XX ····· XX10	XX ····· XX11	XX ····· XX00
XX ····· XX10	XX ····· XX11	XX ····· XX00	XX ····· XX01
XX ····· XX11	XX ····· XX00	XX ····· XX01	XX ····· XX10

b) Interleaved Burst Sequence (MODE input = V_{DD} or NC)
Bit Order: A_{19} ..... A_1, A_0

1st Address (external)	2nd Address (internal)	3rd Address (internal)	4th Address (internal)
XX ····· XX00	XX ····· XX01	XX ····· XX10	XX ····· XX11
XX ····· XX01	XX ····· XX00	XX ····· XX11	XX ····· XX10
XX ····· XX10	XX ····· XX11	XX ····· XX00	XX ····· XX01
XX ····· XX11	XX ····· XX10	XX ····· XX01	XX ····· XX00

DEVICE OPERATION

(1) Read Operation

CYCLE	ADDRESS	$\overline{WE}$	$\overline{BW}$	ADV	$\overline{CE}$	$\overline{OE}$	$\overline{CKE}$	I/O	OPERATION
n	A0	H	×	L	L	×	L	×	Address & control valid
n + 1	×	×	×	×	×	L	L	Q0	Read out A0

Note 1: H means logical High and L means logical Low. × means Don't care. Q is data output.

(2) Burst Read Operation

CYCLE	ADDRESS	$\overline{WE}$	$\overline{BW}$	ADV	$\overline{CE}$	$\overline{OE}$	$\overline{CKE}$	I/O	OPERATION
n	A0	H	×	L	L	×	L	×	Address & control valid
n + 1	×	×	×	H	×	L	L	Q0	Read out A0
n + 2	×	×	×	H	×	L	L	Q0 + 1	Read out A0 + 1
n + 3	×	×	×	H	×	L	L	Q0 + 2	Read out A0 + 2
n + 4	×	×	×	H	×	L	L	Q0 + 3	Read out A0 + 3
n + 5	A1	H	×	L	L	L	L	Q0	Read out A0
n + 6	×	×	×	H	×	L	L	Q1	Read out A1
n + 7	A2	H	×	L	L	L	L	Q1 + 1	Read out A1 + 1

Note 1: H means logical High and L means logical Low. × means Don't care. Q is data output.

(3) Write Operation

CYCLE	ADDRESS	$\overline{WE}$	$\overline{BW}$	ADV	$\overline{CE}$	$\overline{OE}$	$\overline{CKE}$	I/O	OPERATION
n	A0	L	L	L	L	×	L	×	Address & control valid
n + 1	×	×	×	×	×	×	L	D0	Write to A0

Note 1: H means logical High and L means logical Low. × means Don't care. D is data input.

(4) Burst Write Operation

CYCLE	ADDRESS	$\overline{WE}$	$\overline{BW}$	ADV	$\overline{CE}$	$\overline{OE}$	$\overline{CKE}$	I/O	OPERATION
n	A0	L	L	L	L	×	L	×	Address & control valid
n + 1	×	×	L	H	×	×	L	D0	Write A0
n + 2	×	×	L	H	×	×	L	D0 + 1	Write A0 + 1
n + 3	×	×	L	H	×	×	L	D0 + 2	Write A0 + 2
n + 4	×	×	L	H	×	×	L	D0 + 3	Write A0 + 3
n + 5	A1	L	L	L	L	×	L	D0	Write A0
n + 6	×	×	L	H	×	×	L	D1	Write A1
n + 7	A2	L	L	L	L	×	L	D1 + 1	Write A1 + 1

Note 1: H means logical High and L means logical Low. × means Don't care. D is data input.

(5) Read Operation with Clock Enable

CYCLE	ADDRESS	$\overline{WE}$	$\overline{BW}$	ADV	$\overline{CE}$	$\overline{OE}$	$\overline{CKE}$	I/O	OPERATION
n	A0	H	×	L	L	×	L	×	Address & control valid
n + 1	×	×	×	×	×	×	H	×	Ignore cycle
n + 2	A1	H	×	L	L	L	L	Q0	A0 read out
n + 3	×	×	×	×	×	L	H	Q0	Ignore clock
n + 4	×	×	×	×	×	L	H	Q0	Ignore clock
n + 5	A2	H	×	L	L	L	L	Q1	Read out A1
n + 6	A3	H	×	L	L	L	L	Q2	Read out A2
n + 7	A4	H	×	L	L	L	L	Q3	Read out A3

Note 1: H means logical High and L means logical Low. × means Don't care. Q is data output.

(6) Write Operation with Clock Enable

CYCLE	ADDRESS	$\overline{WE}$	$\overline{BW}$	ADV	$\overline{CE}$	$\overline{OE}$	$\overline{CKE}$	I/O	OPERATION
n	A0	L	L	L	L	×	L	×	Add. & control valid
n + 1	×	×	×	×	×	×	H	×	Ignore clock
n + 2	A1	L	L	L	L	×	L	D0	Write A0
n + 3	×	×	×	×	×	×	H	×	Ignore clock
n + 4	×	×	×	×	×	×	H	×	Ignore clock
n + 5	A2	L	L	L	L	×	L	D1	Write A1
n + 6	A3	L	L	L	L	×	L	D2	Write A2
n + 7	×	×	×	×	×	×	L	D3	Write A3

Note 1: H means logical High and L means logical Low. × means Don't care. D is data input.

(7) Read Operation with Chip Enable

CYCLE	ADDRESS	$\overline{WE}$	$\overline{BW}$	ADV	$\overline{CE}$	$\overline{OE}$	$\overline{CKE}$	I/O	OPERATION
n	A0	H	×	L	L	×	L	×	Address & control valid
n + 1	×	×	×	L	H	×	L	Q0	Read A0
n + 2	A1	H	×	L	L	L	L	Z	Deselect
n + 3	×	×	×	L	H	×	L	Q1	Read A1
n + 4	×	×	×	L	H	L	L	Z	Deselect
n + 5	A2	H	×	L	L	×	L	Z	Deselect
n + 6	×	×	×	L	H	×	L	Q2	Read A2
n + 7	×	×	×	L	H	L	L	Z	Deselect

Note 1: H means logical High and L means logical Low. × means Don't care. Q is data output.
Z means Hi-Z.

(8) Write Operation with Chip Enable

CYCLE	ADDRESS	$\overline{WE}$	$\overline{BW}$	ADV	$\overline{CE}$	$\overline{OE}$	$\overline{CKE}$	I/O	OPERATION
n	A0	L	L	L	L	×	L	×	Address & control valid
n + 1	×	×	×	L	H	×	L	D0	Write A0
n + 2	A1	L	L	L	L	×	L	Z	Deselect
n + 3	×	×	×	L	H	×	L	D1	Write A1
n + 4	×	×	×	L	H	×	L	Z	Deselect
n + 5	A2	L	L	L	L	×	L	Z	Deselect
n + 6	×	×	×	L	H	×	L	D2	Write A2
n + 7	×	×	×	L	H	×	L	Z	Deselect

Note 1: H means logical High and L means logical Low. × means Don't care. D is data input.
Z means Hi-Z.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	− 0.5 to 4.6	V
V_{DDQ}	Output Buffer Power Supply Voltage	− 0.5 to V_{DD} + 0.5 (≦ 4.6 V max)	V
V_{IN}	Input Terminal Voltage	− 0.5 * to 4.6	V
$V_{I/O}$	Input/Output Terminal Voltage	− 0.5 * to V_{DDQ} + 0.5** (≦ 4.6 V max)	V
P_D	Power Dissipation	1.5	W
T_{solder}	Soldering Temperature (10 s)	260	°C
T_{strg}	Storage Temperature	− 65 to 150	°C
T_{opr}	Operating Temperature	− 10 to 85	°C

*: −1.0 V with a pulse width of 20% of t_{KC}(min) (3 ns max)
**: V_{DDQ} + 1.0 V with a pulse width of 20% of t_{KC}(min) (3 ns max)

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 to 70°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{DD}	Power Supply Voltage	3.135	3.3	3.465	V
V_{DDQ}	Output Buffer Power Supply Voltage	3.135	3.3	3.465	V
V_{IH}	Input High Voltage	2.0	−	V_{DD} + 0.3**	V
V_{IH1}	Input High Voltage for MODE pin	V_{DD} − 0.3	V_{DD}	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	− 0.3 *	−	0.8	V
V_{IL1}	Input Low Voltage for MODE and NU pins	− 0.3	0.0	0.3	V

*: −0.7 V with a pulse width of 20% of t_{KC}(min) (3 ns max)
**: V_{DDQ} + 0.7 V with a pulse width of 20% of t_{KC}(min) (3 ns max)

Note: NU pin must be low or not connected.

DC CHARACTERISTICS (Ta = 0 to 70°C, $V_{DD} = V_{DDQ} = 3.3\ V \pm 5\%$)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0$ to V_{DD}		−1	−	1	μA
I_{NU}	Input Current (NU pin)	$V_{IN} = 0\ V$ to $0.3\ V$		−1	−	1	μA
I_{LO}	Output Leakage Current	Device Deselected or Output Deselected, $V_{OUT} = 0$ to V_{DDQ}		−1	−	1	μA
V_{OH}	Output High Voltage	$I_{OH} = -8\ mA$		2.4	−	−	V
		$I_{OH} = -100\ \mu A$		$V_{DDQ} - 0.2$	−	−	
V_{OL}	Output Low Voltage	$I_{OL} = 8\ mA$		−	−	0.4	
		$I_{OL} = 100\ \mu A$		−	−	0.2	
I_{DDO1}	Operating Current	$I_{OUT} = 0\ mA$, all inputs = $V_{DD} - 0.2\ V/0.2\ V$ Clock ≧ t_{KC}(min)	100MHz	−	−	270	mA
			83MHz	−	−	240	
			75MHz	−	−	220	
I_{DDO2}	Operating Current (idle)	Device Deselected $I_{OUT} = 0\ mA$, all inputs = $V_{DD} - 0.2\ V/0.2\ V$ Clock ≧ t_{KC}(min)	100MHz	−	−	120	mA
			83MHz	−	−	100	
			75MHz	−	−	90	
I_{DDS1}	Standby Current (TTL level)	Clock = V_{SS}, all inputs = V_{IH} or V_{IL}		−	−	65	mA
I_{DDS2}	Standby Current (MOS level)	Clock = V_{SS}, all inputs = $V_{DD} - 0.2\ V$ or $0.2\ V$		−	−	10	mA
I_{DDS3}	Standby Current (Snooze Mode)	ZZ ≧ $V_{DD} - 0.2\ V$ All inputs = $V_{DD} - 0.2\ V$ or $0.2\ V$ Clock ≧ t_{KC}(min)		−	−	10	mA
I_{DDS4}	Standby Current ($\overline{CKE}$ Mode)	$\overline{CKE}$ ≧ V_{IH} All inputs = $V_{DD} - 0.2\ V$ or $0.2\ V$ Clock ≧ t_{KC}(min)		−	−	10	mA

Note: Operating Current(I_{DDO1}) is specified with 50% Read cycles and 50% Write cycles.

CAPACITANCE (Ta = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	5	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	7	pF
C_{NU}	Input Capacitance of NU	V_{IN} = GND	10	pF

Note: This parameter is sampled periodically and is not tested for every device.

AC CHARACTERISTICS (Ta = 0 to 70°C, $V_{DD} = V_{DDQ} = 3.3\ V \pm 5\%$)

SYMBOL	PARAMETER	TC55VL1618FF-100		TC55VL1618FF-83		TC55VL1618FF-75		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{KC}	CLK Cycle Time	10	–	12	–	13	–	ns
t_{KH}	CLK High Pulse Width	3	–	4	–	4	–	
t_{KL}	CLK Low Pulse Width	3	–	4	–	4	–	
t_{KQV}	CLK High to Output Valid	–	8.5	–	9	–	10	
t_{KQX}	CLK High to Output Invalid	3	–	3	–	3	–	
t_{KQLZ}	CLK High to Output Low-Z	4	–	4	–	4	–	
t_{KQHZ}	CLK High to Output High-Z	3	5	3	5	3	5	
t_{GQV}	$\overline{OE}$ Low to Output Valid	–	5	–	5	–	6	
t_{GQLZ}	$\overline{OE}$ Low to Output Low-Z	0	–	0	–	0	–	
t_{GQHZ}	$\overline{OE}$ High to Output High-Z	1.5	5	1.5	5	1.5	6	
t_{AS}	Address Setup Time from CLK	2	–	2	–	2	–	
t_{DS}	Data Setup Time from CLK	2	–	2	–	2	–	
t_{WS}	$\overline{WE}$ Setup Time from CLK	2	–	2	–	2	–	
t_{CES}	CE Setup Time from CLK	2	–	2	–	2	–	
t_{ADVS}	ADV Setup Time from CLK	2	–	2	–	2	–	
t_{BWS}	$\overline{BW}$ Setup Time from CLK	2	–	2	–	2	–	
t_{CKES}	$\overline{CKE}$ Setup Time from CLK	2	–	2	–	2	–	
t_{AH}	Address Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{DH}	Data Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{WH}	$\overline{WE}$ Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{CEH}	CE Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{ADVH}	ADV Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{BWH}	$\overline{BW}$ Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{CKEH}	$\overline{CKE}$ Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{ZS}	ZZ Standby Time	5	–	5	–	5	–	
t_{ZR}	ZZ Recovery Time	5	–	5	–	5	–	
t_{ZHZ}	ZZ to Output in High-Z	–	2	–	2	–	2	cycle

AC TEST CONDITIONS

Input Pulse Level	3.0 V/0.0 V
Input Pulse Rise and Fall Time	1 V/ns(20%/80%)
Input Timing Measurement Reference Level	1.5 V
Output Timing Measurement Reference Level	1.5 V
Output Load	As shown in Fig. 1 and Fig. 2

Fig. 1 : AC test load

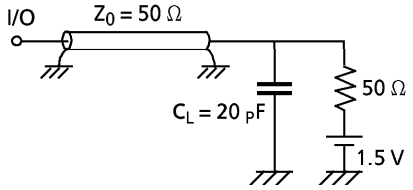
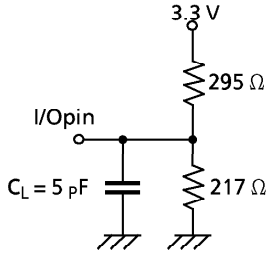
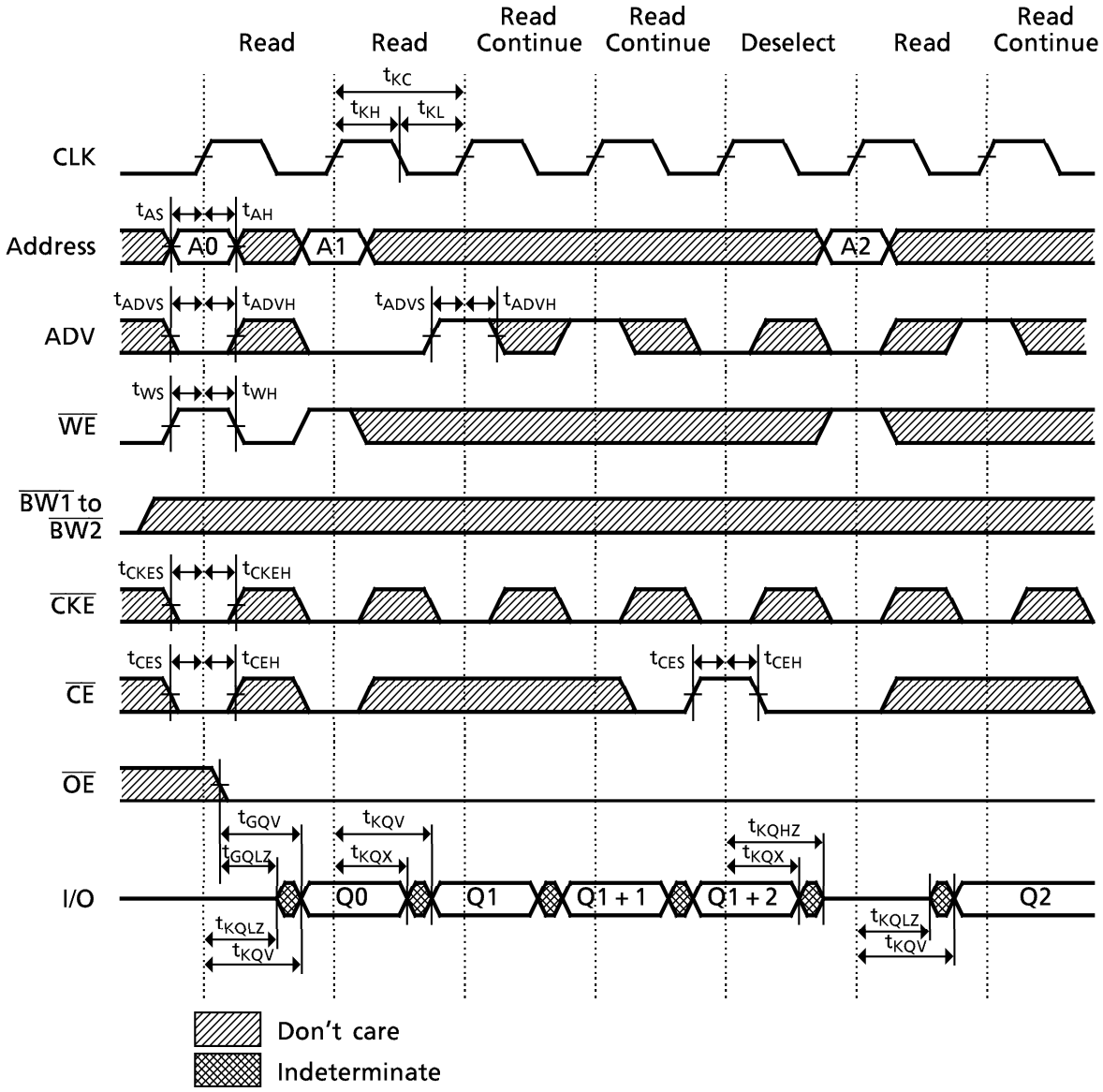


Fig. 2 : AC test load (for Enable/Disable spec)

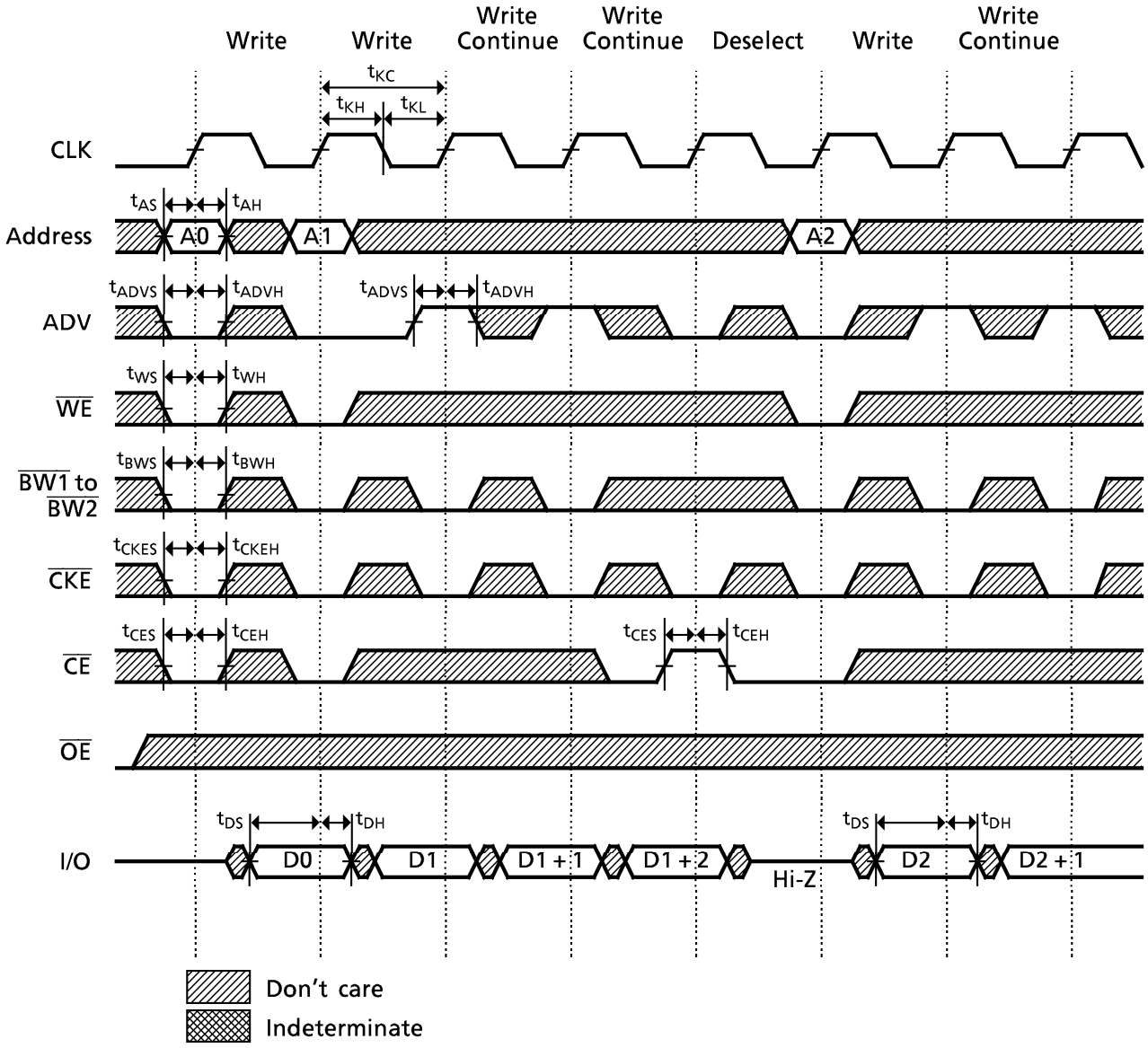


TIMING DIAGRAMS

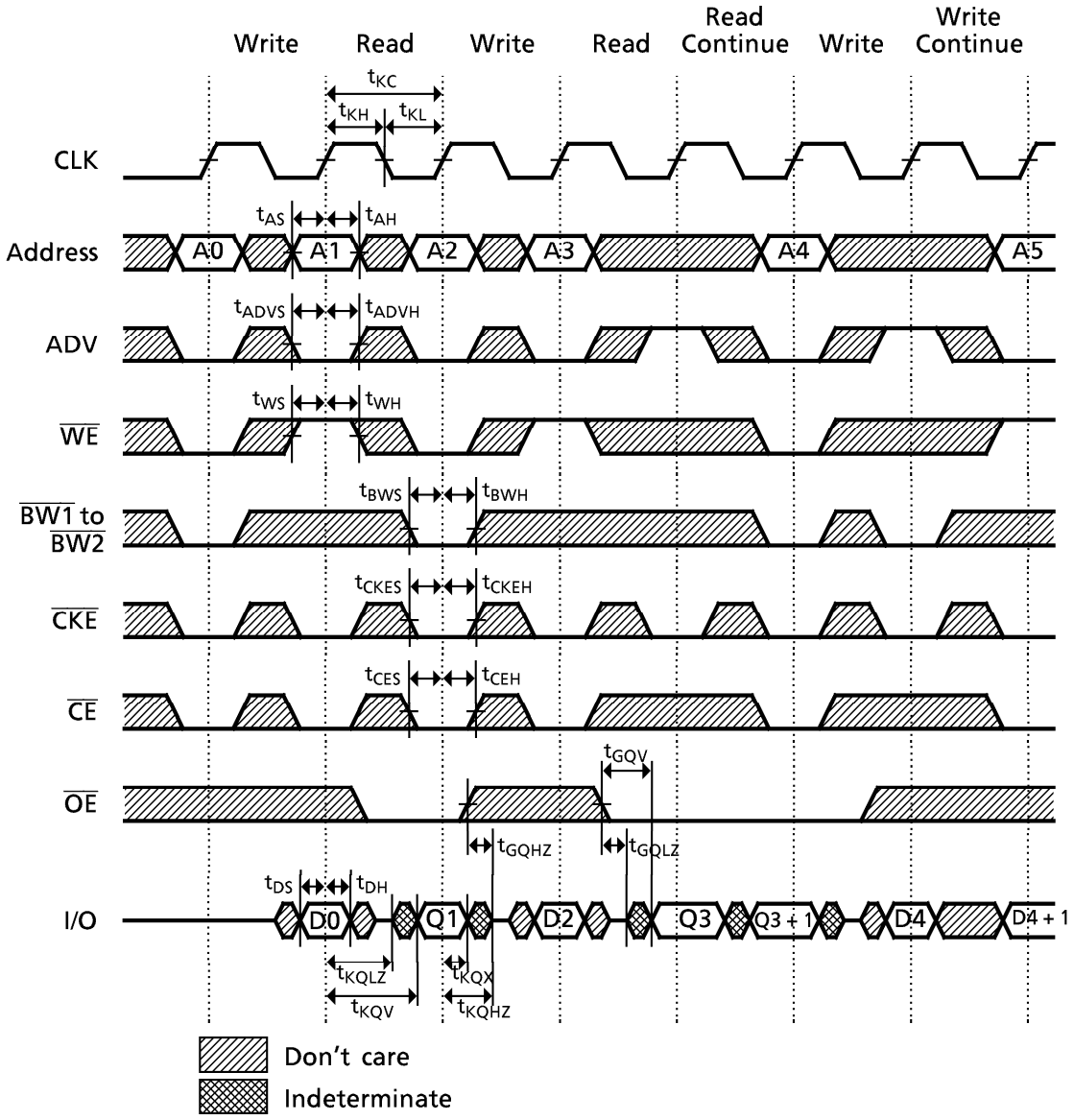
READ CYCLE



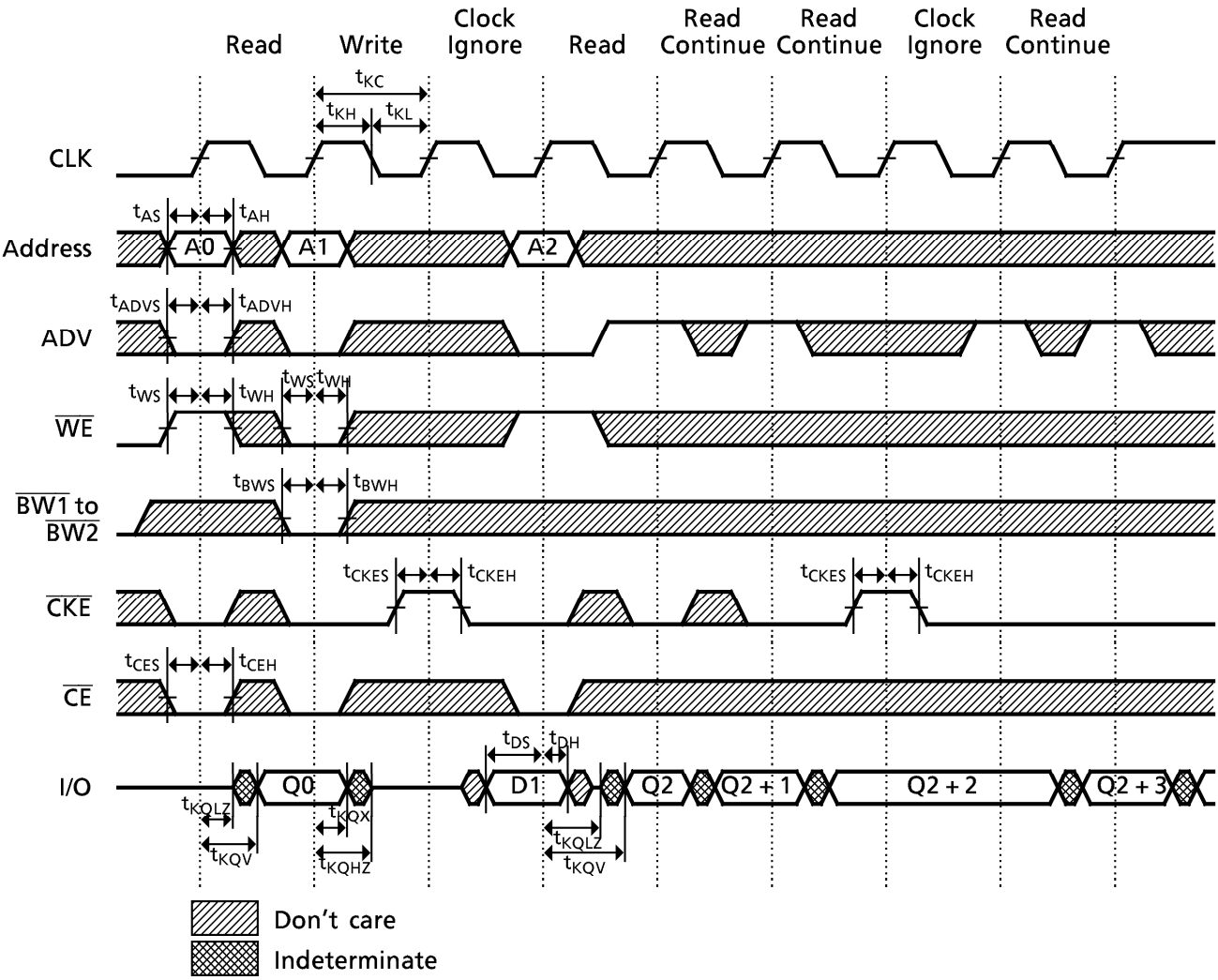
WRITE CYCLE


Write
Write
Write Continue
Write Continue
Deselect
Write
Write Continue
CLK
Address
ADV
WE
BW1 to BW2
CKE
CE
OE
I/O
tKC
tKH
tKL
tAS
tAH
A0
A1
A2
tADVS
tADVH
tWS
tWH
tBWS
tBWH
tCKES
tCKEH
tCES
tCEH
tDS
tDH
D0
D1
D1 + 1
D1 + 2
Hi-Z
D2
D2 + 1
Don't care
Indeterminate

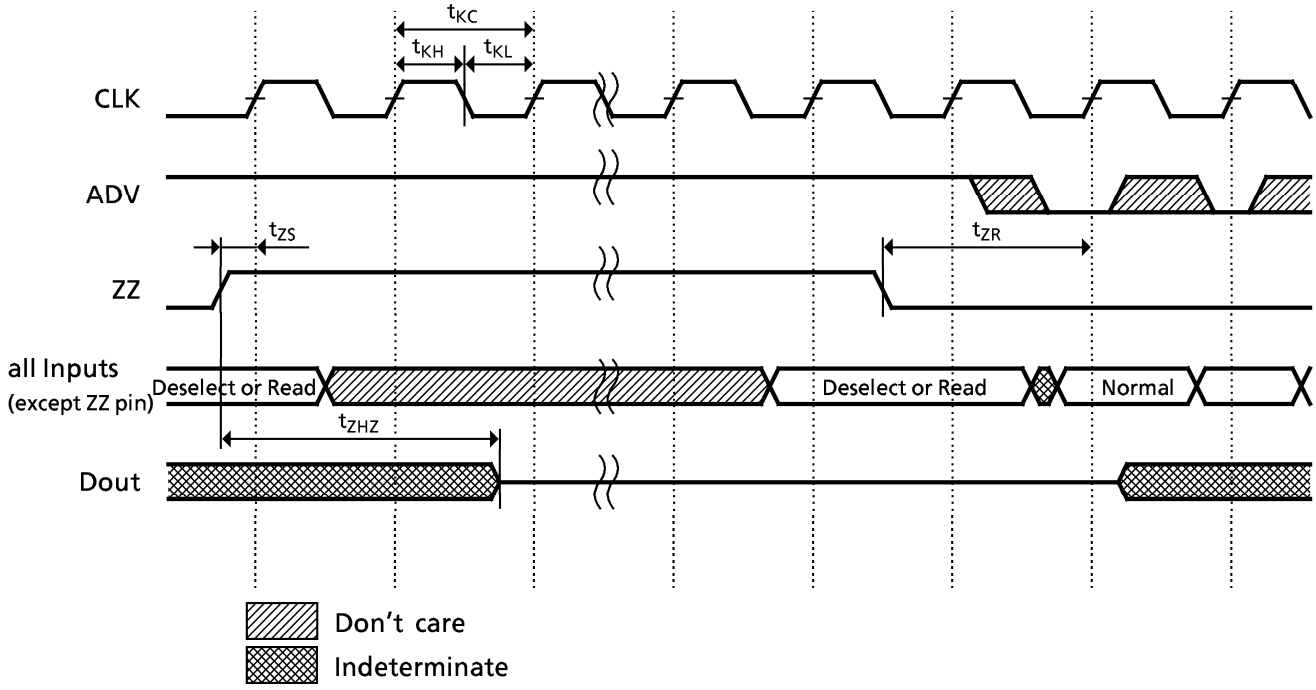
WRITE/READ CYCLE



CLOCK IGNORE CYCLE



SNOOZE CYCLE



Notes: 1. The cycle immediately prior to a Snooze brought about by the ZZ pin must be a Read cycle or Deselect cycle.

2. Memory data is retained during Snooze cycles.

■ V_{DDQ} = 2.5V Interface specification

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 to 70°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{DD}	Power Supply Voltage	3.135	3.3	3.465	V
V_{DDQ}	Output Buffer Power Supply Voltage	2.375	2.5	2.9	V
V_{IH}	Input High Voltage for Address and Control pins	1.7	–	V_{DD} + 0.3**	V
	Input High Voltage for I/O pins	1.7	–	V_{DDQ} + 0.3***	
V_{IH1}	Input High Voltage for MODE pin	V_{DD} – 0.3	V_{DD}	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	– 0.3 *	–	0.7	V
V_{IL1}	Input Low Voltage for MODE and NU pins	– 0.3	0.0	0.3	V

*: −0.7 V with a pulse width of 20% of t_{KC}(min) (3 ns max)
**: V_{DD} + 0.7 V with a pulse width of 20% of t_{KC}(min) (3 ns max)
***: V_{DDQ} + 0.7 V with a pulse width of 20% of t_{KC}(min) (3 ns max)

NOTE: NU pin must be low or not connected.

DC CHARACTERISTICS (Ta = 0 to 70°C, V_{DD} = 3.3 V ± 5%, V_{DDQ} = 2.375 V to 2.9 V)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 to V_{DD}		– 1	–	1	μA
I_{NU}	Input Current (NU pin)	V_{IN} = 0 V to 0.3 V		– 1	–	1	μA
I_{LO}	Output Leakage Current	Device Deselected or Output Deselected, V_{OUT} = 0 to V_{DDQ}		– 1	–	1	μA
V_{OH}	Output High Voltage	I_{OH} = – 2 mA		1.7	–	–	V
		I_{OH} = – 100 μA		V_{DDQ} – 0.2	–	–	
V_{OL}	Output Low Voltage	I_{OL} = 2 mA		–	–	0.7	
		I_{OL} = 100 μA		–	–	0.2	
I_{DDO1}	Operating Current	I_{OUT} = 0 mA, all inputs = V_{DD} – 0.2 V/0.2 V Clock ≧ t_{KC}(min)	100MHz	–	–	270	mA
			83MHz	–	–	240	
			75MHz	–	–	220	
I_{DDO2}	Operating Current (idle)	Device Deselected I_{OUT} = 0 mA, all inputs = V_{DD} – 0.2 V/0.2 V Clock ≧ t_{KC}(min)	100MHz	–	–	120	mA
			83MHz	–	–	100	
			75MHz	–	–	90	
I_{DDS2}	Standby Current (MOS level)	Clock = V_{SS}, all inputs = V_{DD} – 0.2 V or 0.2 V		–	–	10	mA
I_{DDS3}	Standby Current (Snooze Mode)	ZZ ≧ V_{DD} – 0.2 V all inputs = V_{DD} – 0.2 V or 0.2 V Clock ≧ t_{KC}(min)		–	–	10	mA
I_{DDS4}	Standby Current ($\overline{CKE}$ Mode)	$\overline{CKE}$ ≧ V_{IH} All inputs = V_{DD} – 0.2 V or 0.2 V Clock ≧ t_{KC}(min)		–	–	10	mA

AC CHARACTERISTICS (Ta = 0 to 70°C, V_{DD} = 3.3 V ± 5%, V_{DDQ} = 2.375 V to 2.9 V)

SYMBOL	PARAMETER	TC55VL1618FF-100		TC55VL1618FF-83		TC55VL1618FF-75		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{KC}	CLK Cycle Time	10	–	12	–	13	–	ns
t_{KH}	CLK High Pulse Width	3	–	4	–	4	–	
t_{KL}	CLK Low Pulse Width	3	–	4	–	4	–	
t_{KQV}	CLK High to Output Valid	–	8.5	–	9	–	10	
t_{KQX}	CLK High to Output Invalid	3	–	3	–	3	–	
t_{KQLZ}	CLK High to Output Low-Z	4	–	4	–	4	–	
t_{KQHZ}	CLK High to Output High-Z	3	5	3	5	3	5	
t_{GQV}	$\overline{OE}$ Low to Output Valid	–	5	–	5	–	6	
t_{GQLZ}	$\overline{OE}$ Low to Output Low-Z	0	–	0	–	0	–	
t_{GQHZ}	$\overline{OE}$ High to Output High-Z	1.5	5	1.5	5	1.5	6	
t_{AS}	Address Setup Time from CLK	2	–	2	–	2	–	
t_{DS}	Data Setup Time from CLK	2	–	2	–	2	–	
t_{WS}	$\overline{WE}$ Setup Time from CLK	2	–	2	–	2	–	
t_{CES}	CE Setup Time from CLK	2	–	2	–	2	–	
t_{ADVS}	ADV Setup Time from CLK	2	–	2	–	2	–	
t_{BWS}	$\overline{BW}$ Setup Time from CLK	2	–	2	–	2	–	
t_{CKES}	$\overline{CKE}$ Setup Time from CLK	2	–	2	–	2	–	
t_{AH}	Address Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{DH}	Data Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{WH}	$\overline{WE}$ Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{CEH}	CE Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{ADVH}	ADV Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{BWH}	$\overline{BW}$ Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{CKEH}	$\overline{CKE}$ Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{ZS}	ZZ Standby Time	5	–	5	–	5	–	
t_{ZR}	ZZ Recovery Time	5	–	5	–	5	–	
t_{ZHZ}	ZZ to Output in High-Z	–	2	–	2	–	2	cycle

AC TEST CONDITIONS

Input Pulse Level	2.5 V/0.0 V
Input Pulse Rise and Fall Time	1 V/ns(20%/80%)
Input Timing Measurement Reference Level	1.25 V
Output Timing Measurement Reference Level	1.25 V
Output Load	As shown in Fig. 1 and Fig. 2

Fig. 1 : AC test load

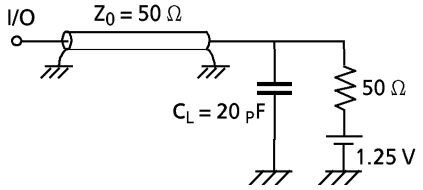
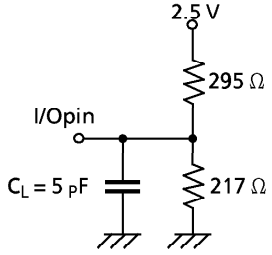


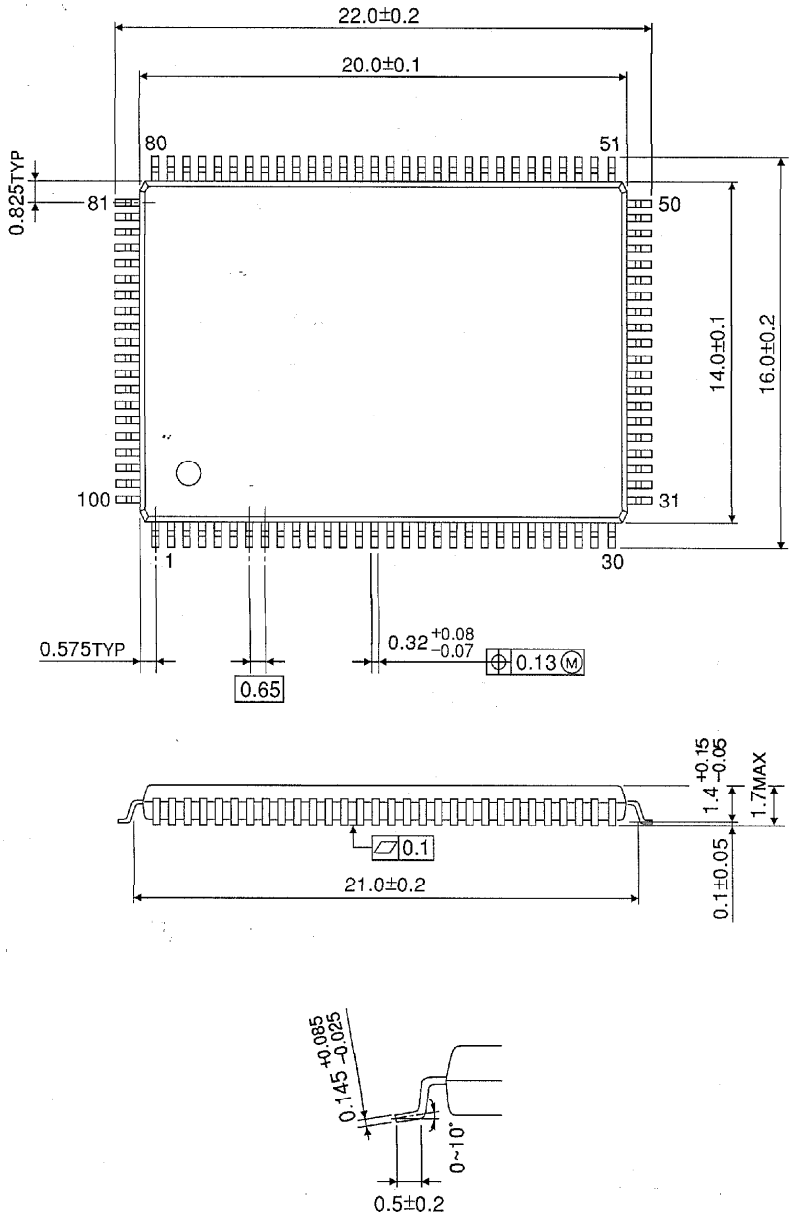
Fig. 2 : AC test load (for Enable/Disable spec)



PACKAGE DIMENSIONS

Plastic LQFP (LQFP100-P-1420-0.65K) TENTATIVE

Unit: mm



Weight: g (typ.)