MOTOROLA

# MC14001UB
Quad 2-Input NOR Gate

# MC14002UB
Dual 4-Input NOR Gate

# MC14011UB
Quad 2-Input NAND Gate

# MC14012UB
Dual 4-Input NAND Gate

# MC14023UB
Triple 3-Input NAND Gate

# MC14025UB
Triple 3-Input NOR Gate

## UB-SUFFIX SERIES CMOS GATES

The UB Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired. The UB set of CMOS gates are inverting non-buffered functions.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linear and Oscillator Applications
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for Corresponding CD4000 Series UB Suffix Devices

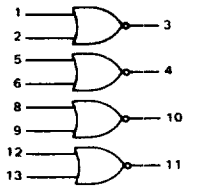
## CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

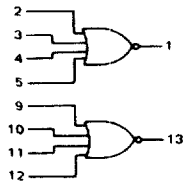
UB-SERIES GATES

## LOGIC DIAGRAMS

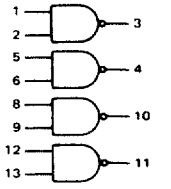
**MC14001UB**
Quad 2-Input NOR Gate



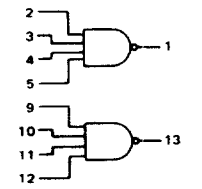

**MC14002UB**
Dual 4-Input NOR Gate



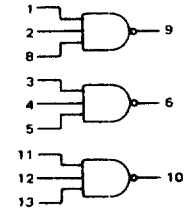

**MC14011UB**
Quad 2-Input NAND Gate



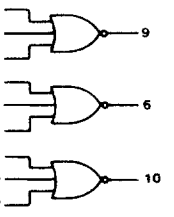

**MC14012UB**
Dual 4-Input NAND Gate



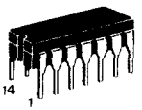

**MC14023UB**
Triple 3-Input NAND Gate



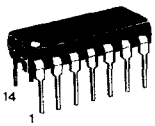

**MC14025UB**
Triple 3-Input NOR Gate




$V_{DD}$ = Pin 14
$V_{SS}$ = Pin 7
for All Devices




**L SUFFIX**
CERAMIC PACKAGE
CASE 632




**P SUFFIX**
PLASTIC PACKAGE
CASE 646

**ORDERING INFORMATION**

A Series: −55°C to +125°C
MC14XXXUBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXUBCP (Plastic Package)
MC14XXXUBCL (Ceramic Package)

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.

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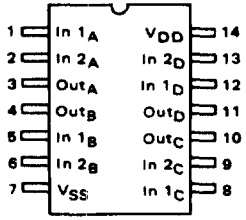
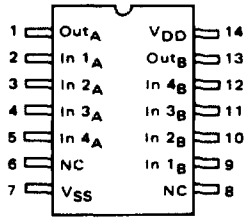
# CMOS UB-SERIES GATES

## PIN ASSIGNMENTS

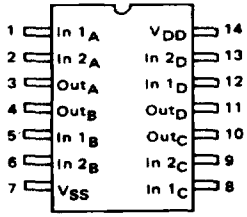
**MC14001UB**
**Quad 2-Input NOR Gate**



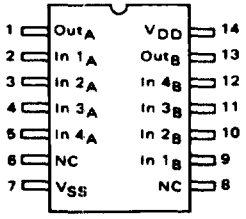

**MC14002UB**
**Dual 4-Input NOR Gate**



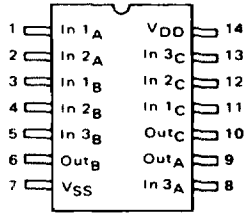

**MC14011UB**
**Quad 2-Input NAND Gate**



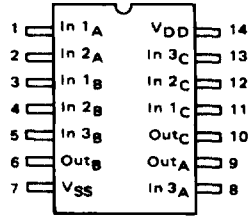

**MC14012UB**
**Dual 4-Input NAND Gate**




**MC14023UB**
**Triple 3-Input NAND Gate**




**MC14025UB**
**Triple 3-Input NOR Gate**




**NC = No Connection**

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**MAXIMUM RATINGS*** (Voltages Referenced to $V_{SS}$)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage | −0.5 to +18.0 | V |
| $V_{in}$, $V_{out}$ | Input or Output Voltage (DC or Transient) | −0.5 to $V_{DD}$ +0.5 | V |
| $I_{in}$, $I_{out}$ | Input or Output Current (DC or Transient), per Pin | ±10 | mA |
| $P_D$ | Power Dissipation, per Package† | 500 | mW |
| $T_{stg}$ | Storage Temperature | −65 to +150 | °C |
| $T_L$ | Lead Temperature (8-Second Soldering) | 260 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur
†Temperature Derating Plastic "P" Package −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to $V_{SS}$)

| Characteristic | Symbol | $V_{DD}$ Vdc | $T_{low}$* Min | $T_{low}$* Max | 25°C Min | 25°C Typ # | 25°C Max | $T_{high}$* Min | $T_{high}$* Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Output Voltage "0" Level | | 5.0 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | |
| $V_{in}$ = $V_{DD}$ or 0 | $V_{OL}$ | 10 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | Vdc |
| | | 15 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | |
| "1" Level | | 5.0 | 4.95 | — | 4.95 | 5.0 | — | 4.95 | — | |
| $V_{in}$ = 0 or $V_{DD}$ | $V_{OH}$ | 10 | 9.95 | — | 9.95 | 10 | — | 9.95 | — | Vdc |
| | | 15 | 14.95 | — | 14.95 | 15 | — | 14.95 | — | |
| Input Voltage "0" Level | | | | | | | | | | |
| ($V_O$ = 4.5 Vdc) | | 5.0 | — | 1.0 | — | 2.25 | 1.0 | — | 1.0 | |
| ($V_O$ = 9.0 Vdc) | $V_{IL}$ | 10 | — | 2.0 | — | 4.50 | 2.0 | — | 2.0 | Vdc |
| ($V_O$ = 13.5 Vdc) | | 15 | — | 2.5 | — | 6.75 | 2.5 | — | 2.5 | |
| "1" Level | | | | | | | | | | |
| ($V_O$ = 0.5 Vdc) | | 5.0 | 4.0 | — | 4.0 | 2.75 | — | 4.0 | — | |
| ($V_O$ = 1.0 Vdc) | $V_{IH}$ | 10 | 8.0 | — | 8.0 | 5.50 | — | 8.0 | — | Vdc |
| ($V_O$ = 1.5 Vdc) | | 15 | 12.5 | — | 12.5 | 8.25 | — | 12.5 | — | |
| Output Drive Current (AL Device) | | | | | | | | | | |
| ($V_{OH}$ = 2.5 Vdc) Source | | 5.0 | 1.2 | — | -1.0 | -1.7 | — | -0.7 | — | |
| ($V_{OH}$ = 4.6 Vdc) | $I_{OH}$ | 5.0 | 0.25 | — | -0.2 | -0.36 | — | -0.14 | — | mAdc |
| ($V_{OH}$ = 9.5 Vdc) | | 10 | -0.62 | — | -0.5 | -0.9 | — | -0.35 | — | |
| ($V_{OH}$ = 13.5 Vdc) | | 15 | -1.8 | — | -1.5 | -3.5 | — | 1.1 | — | |
| ($V_{OL}$ = 0.4 Vdc) Sink | | 5.0 | 0.64 | — | 0.51 | 0.88 | — | 0.36 | — | |
| ($V_{OL}$ = 0.5 Vdc) | $I_{OL}$ | 10 | 1.6 | — | 1.3 | 2.25 | — | 0.9 | — | mAdc |
| ($V_{OL}$ = 1.5 Vdc) | | 15 | 4.2 | — | 3.4 | 8.8 | — | 2.4 | — | |
| Output Drive Current (CL/CP Device) | | | | | | | | | | |
| ($V_{OH}$ = 2.5 Vdc) Source | | 5.0 | -1.0 | — | -0.8 | -1.7 | — | -0.6 | — | |
| ($V_{OH}$ = 4.6 Vdc) | $I_{OH}$ | 5.0 | -0.2 | — | -0.16 | -0.36 | — | -0.12 | — | mAdc |
| ($V_{OH}$ = 9.5 Vdc) | | 10 | 0.5 | — | -0.4 | -0.9 | — | -0.3 | — | |
| ($V_{OH}$ = 13.5 Vdc) | | 15 | -1.4 | — | -1.2 | -3.5 | — | -1.0 | — | |
| ($V_{OL}$ = 0.4 Vdc) Sink | | 5.0 | 0.52 | — | 0.44 | 0.88 | — | 0.36 | — | |
| ($V_{OL}$ = 0.5 Vdc) | $I_{OL}$ | 10 | 1.3 | — | 1.1 | 2.25 | — | 0.9 | — | mAdc |
| ($V_{OL}$ = 1.5 Vdc) | | 15 | 3.6 | — | 3.0 | 8.8 | — | 2.4 | — | |
| Input Current (AL Device) | $I_{in}$ | 15 | — | ±0.1 | — | ±0.00001 | ±0.1 | — | ±1.0 | μAdc |
| Input Current (CL/CP Device) | $I_{in}$ | 15 | — | ±0.3 | — | ±0.00001 | ±0.3 | — | ±1.0 | μAdc |
| Input Capacitance ($V_{in}$ = 0) | $C_{in}$ | — | — | — | — | 5.0 | 7.5 | — | — | pF |
| Quiescent Current (AL Device) | $I_{DD}$ | 5.0 | — | 0.25 | — | 0.0005 | 0.25 | — | 7.5 | μAdc |
| (Per Package) | | 10 | — | 0.5 | — | 0.0010 | 0.5 | — | 15 | |
| | | 15 | — | 1.0 | — | 0.0015 | 1.0 | — | 30 | |
| Quiescent Current (CL/CP Device) | $I_{DD}$ | 5.0 | — | 1.0 | — | 0.0005 | 1.0 | — | 7.5 | μAdc |
| (Per Package) | | 10 | — | 2.0 | — | 0.0010 | 2.0 | — | 15 | |
| | | 15 | — | 4.0 | — | 0.0015 | 4.0 | — | 30 | |
| Total Supply Current**† (Dynamic plus Quiescent, Per Gate, $C_L$ = 50 pF) | $I_T$ | 5.0 | $I_T$ = (0.3 μA/kHz) f + $I_{DD}$/N | | | | | | | μAdc |
| | | 10 | $I_T$ = (0.6 μA/kHz) f + $I_{DD}$/N | | | | | | | |
| | | 15 | $I_T$ = (0.8 μA/kHz) f + $I_{DD}$/N | | | | | | | |

*$T_{low}$ = −55°C for AL Device, −40°C for CL/CP Device.
$T_{high}$ = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: $I_T$ is in μH (per package), $C_L$ in pF, V = ($V_{DD}$ − $V_{SS}$) in volts, f in kHz is input frequency, and k = 0.001 × the number of exercised gates per package.

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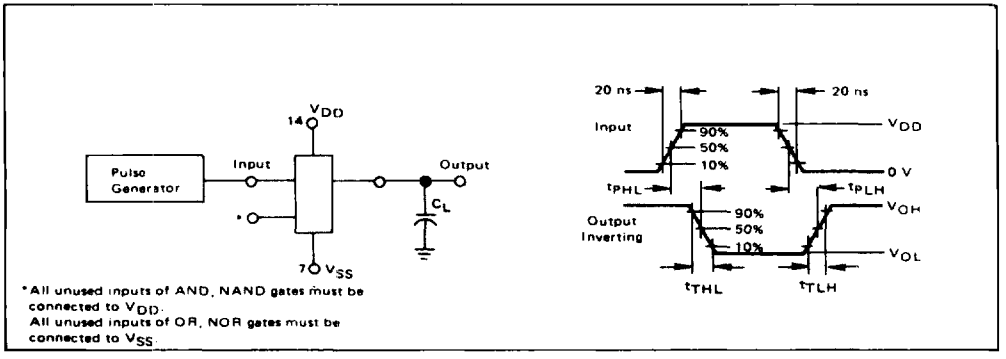
**SWITCHING CHARACTERISTICS*** ($C_L$ = 50 pF, $T_A$ = 25°C)

| Characteristic | Symbol | $V_{DD}$ Vdc | Min | Typ # | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise Time | $t_{TLH}$ | | | | | ns |
| $t_{TLH}$ = (3.0 ns/pF) $C_L$ + 30 ns | | 5.0 | – | 180 | 360 | |
| $t_{TLH}$ = (1.5 ns/pF) $C_L$ + 15 ns | | 10 | – | 90 | 180 | |
| $t_{TLH}$ = (1.1 ns/pF) $C_L$ + 10 ns | | 15 | – | 65 | 130 | |
| Output Fall Time | $t_{THL}$ | | | | | ns |
| $t_{THL}$ = (1.5 ns/pF) $C_L$ + 25 ns | | 5.0 | – | 100 | 200 | |
| $t_{THL}$ = (0.75 ns/pF) $C_L$ + 12.5 ns | | 10 | – | 50 | 100 | |
| $t_{THL}$ = (0.55 ns/pF) $C_L$ + 9.5 ns | | 15 | – | 40 | 80 | |
| Propagation Delay Time | $t_{PLH}$, $t_{PHL}$ | | | | | ns |
| $t_{PLH}$, $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 30 ns | | 5.0 | – | 90 | 180 | |
| $t_{PLH}$, $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 22 ns | | 10 | – | 50 | 100 | |
| $t_{PLH}$, $t_{PHL}$ = (0.50 ns/pF) $C_L$ + 15 ns | | 15 | – | 40 | 80 | |

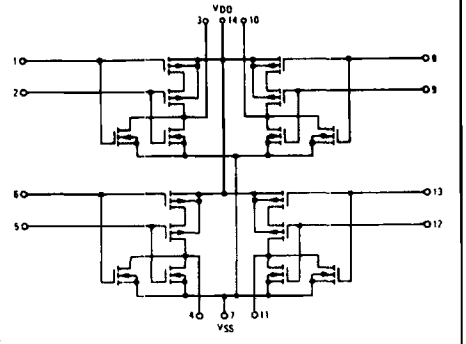
*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

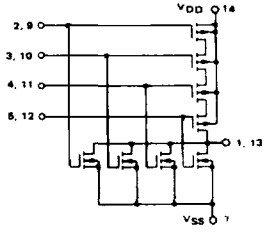
**FIGURE 1 -- SWITCHING TIME TEST CIRCUIT AND WAVEFORMS**




**MC14001UB CIRCUIT SCHEMATIC**




**MC14002UB CIRCUIT SCHEMATIC**
**(1/2 of Device Shown)**

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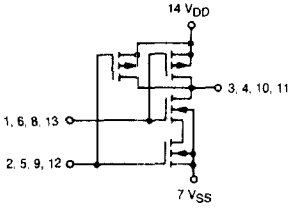
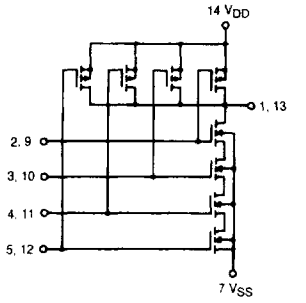
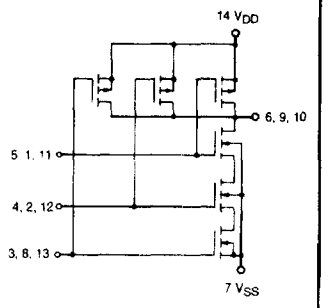
**MC14011UB CIRCUIT SCHEMATIC**
**(1/4 of Device Shown)**




**MC14012UB CIRCUIT SCHEMATIC**
**(1/2 of Device Shown)**




**MC14023UB CIRCUIT SCHEMATIC**
**(1/3 of Device Shown)**




**MC14025UB CIRCUIT SCHEMATIC**
**(1/3 of Device Shown)**

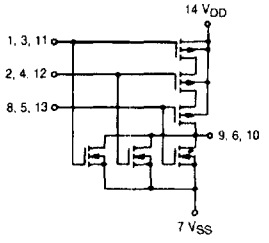



**FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS**

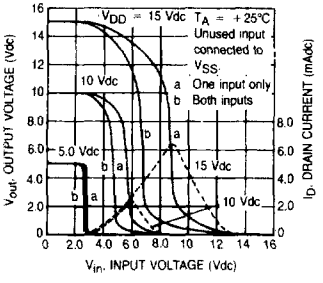



**FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE**

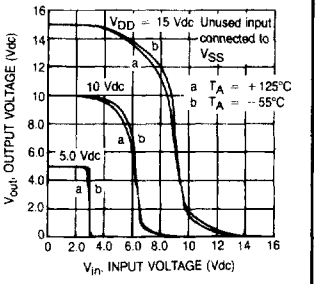



**FIGURE 4 – TYPICAL OUTPUT SOURCE CHARACTERISTICS**

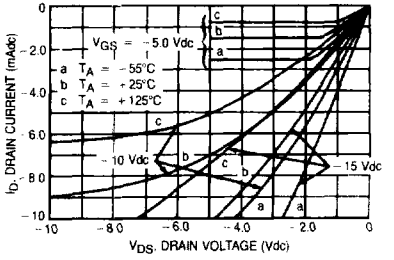
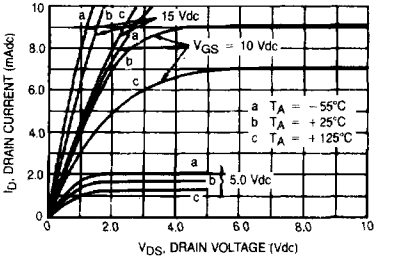



**FIGURE 5 – TYPICAL OUTPUT SINK CHARACTERISTICS**

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