MONOLITHIC CLOCK SYNCHRONIZER (SERIES 3D6701)

RoHS Compliant

data delay devices, inc.

FEATURES

- Synchronizes free-running clock to external gate signal
- **Input frequency range:** 30MHz through 100MHz
- **Phase resolution:** 200ps typical
- **Output frequency:** Programmable from F_{IN} to F_{IN}/256
- **Output period jitter:** Equal to jitter of clock source
- All-silicon, low-power CMOS technology
- TTL/CMOS compatible inputs and outputs
- Vapor phase, IR and wave solderable
- Auto-insertable (DIP pkg.)

For mechanical dimensions, click here.
For package marking details, click here.

PINOUT

3D6701 DIP-14
3D6701D SOIC-14

FUNCTIONAL DESCRIPTION

One major drawback to using a crystal oscillator for frequency generation is that the phase of the generated clock signal cannot be synchronized to an external timing event. A delay-line oscillator (eg, the 3D7701), while supporting this feature, cannot provide the stability and jitter performance of a crystal. The 3D6701 clock synchronizer provides the best of both worlds. The device accepts two inputs – a stable frequency source and a gate signal – and matches the phase of the clock to the gate. It also provides 8 bits of frequency scaling at the device output. The 3D6701 can be operated at 5V or 3.3V, and is offered in both a 16-pin DIP and a space-saving 16-pin SOIC package.

PIN DESCRIPTIONS

F_{IN}	Clock Input
G_{IN}	Gate Input
D0-D7	Divisor Inputs
SEL	VDD Select Input
F_{OUT}	Sync Oscillator Out
VDD	+3.3 or +5 Volts
GND	Ground

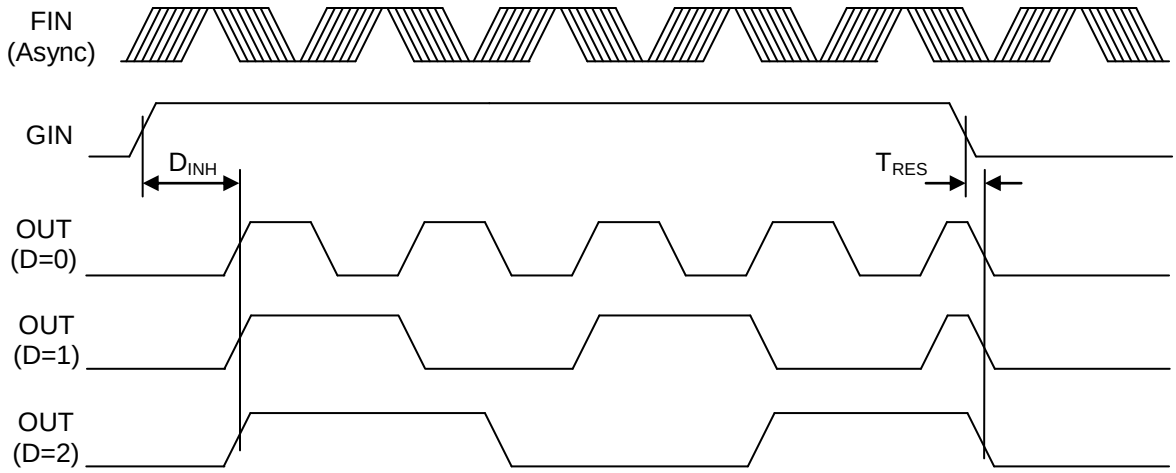


Figure 1: Timing Diagram

THEORY OF OPERATION

The 3D6701 clock synchronizer architecture is shown in Figure 2. The F_{IN} input is assumed to come from a stable clock source, such as a crystal oscillator. A rising edge on the G_{IN} input initiates the phase detection process. Once the phase of the clock with respect to the gate has been resolved, a delay line is adjusted to match the phases of the two signals.

There is a finite resolution to the phase detection process (typically under 500ps), so that, from one gate trigger to the next, there will remain some residual gate-to-output jitter. However, for a given gate, the jitter from one clock cycle to the next is equal to the jitter of the reference clock itself.

The 3D6701 also contains a programmable divider that reduces the output frequency by an amount given by the D7:0 inputs. F_{OUT} is given by F_{IN} / (D+1), so that the output frequency may range from F_{IN} (D=0) to F_{IN} / 256 (D=255). When G_{IN} returns low, the output returns to a low level and remains there until the next rising edge of G_{IN}.

The performance of CMOS integrated circuits is strongly dependent on power supply stability. It is essential that the power supply pins be adequately bypassed and filtered. In addition, the power bus should be of as low an impedance construction as possible. Power planes are preferred.

When operating at 3.3V, tie the SEL input to GND. When operating at 5.0V, tie the SEL input to VDD.

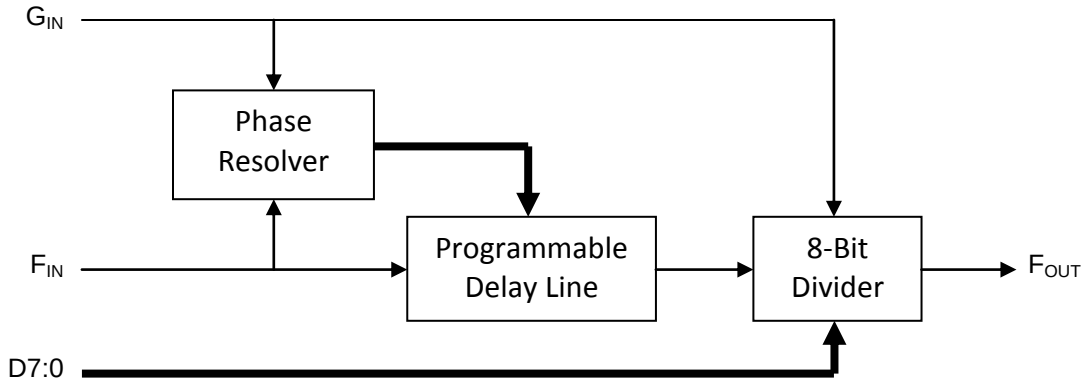


Figure 2: 3D6701 Functional Block Diagram

DEVICE SPECIFICATIONS

TABLE 1: ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{DD}	-0.3	7.0	V	
Input Pin Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Input Pin Current	I_{IN}	-1.0	1.0	mA	25C
Storage Temperature	T_{STRG}	-55	150	C	
Lead Temperature	T_{LEAD}		300	C	10 sec

DEVICE SPECIFICATIONS (Cont'd)

TABLE 2: DC ELECTRICAL CHARACTERISTICS

(-40C to 85C, 3.0V to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Static Supply Current*	I_{DD}		20.0		mA	
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
High Level Input Current	I_{IH}			1.0	µA	$V_{IH} = V_{DD}$
Low Level Input Current	I_{IL}			1.0	µA	$V_{IL} = 0V$
High Level Output Current	I_{OH}		-35.0	-4.0	mA	V_{DD}=4.75V, V_{OH}=2.4V
Low Level Output Current	I_{OL}	4.0	15.0		mA	V_{DD}=4.75V, V_{OL}=0.4V

*I_{DD} will vary slightly for different input clock frequencies

TABLE 3: AC ELECTRICAL CHARACTERISTICS

(-40C to 85C, 3.0V to 3.6V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Frequency	F_{IN}	30		80	MHz	
Duty Cycle	$DC(F_{IN})$	40		60	%	
Gate Frequency	G_{IN}			1	MHz	
Gate Inactive (Low)	$G_{IN,LOW}$	200			ns	
Gate-to-Out Delay	D_{INH}		157		ns	F_{IN}=50MHz
			136		ns	F_{IN}=62MHz
			120		ns	F_{IN}=80MHz
Gate-to-Out Delay Jitter	ΔD_{INH}		420		ps	F_{IN}=50MHz
			460		ps	F_{IN}=62MHz
			780		ps	F_{IN}=80MHz
F_{OUT} Period Jitter				50	ps	
Reset Time	T_{RES}		10		ns	

TABLE 4: AC ELECTRICAL CHARACTERISTICS

(-40C to 85C, 4.75V to 5.25V)

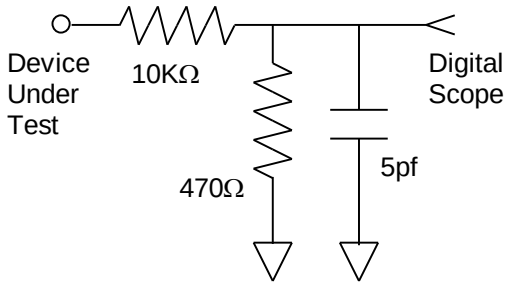
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Frequency	F_{IN}	50		100	MHz	
Duty Cycle	$DC(F_{IN})$	40		60	%	
Gate Frequency	G_{IN}			2	MHz	
Gate Inactive (Low)	$G_{IN,LOW}$	125			ns	
Gate-to-Out Delay	D_{INH}		138		ns	F_{IN}=50MHz
			118		ns	F_{IN}=62MHz
			106		ns	F_{IN}=80MHz
Gate-to-Out Delay Jitter	ΔD_{INH}		640		ps	F_{IN}=50MHz
			700		ps	F_{IN}=62MHz
			520		ps	F_{IN}=80MHz
F_{OUT} Period Jitter				50	ps	
Reset Time	T_{RES}		10		ns	

SILICON DELAY LINE AUTOMATED TESTING

TEST CONDITIONS

INPUT:
Ambient Temperature: 25°C ± 3°C
Supply Voltage (Vcc): 5.0V ± 0.1V
Input Pulse: High = 3.0V ± 0.1V
Low = 0.0V ± 0.1V
Source Impedance: 50Ω Max.
Rise/Fall Time: 3.0 ns Max. (measured between 0.6 and 2.4V)

OUTPUT:
R_{load}: 10KΩ ± 10%
C_{load}: 5pf ± 10%
Threshold: 1.5V (Rising & Falling)



NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.

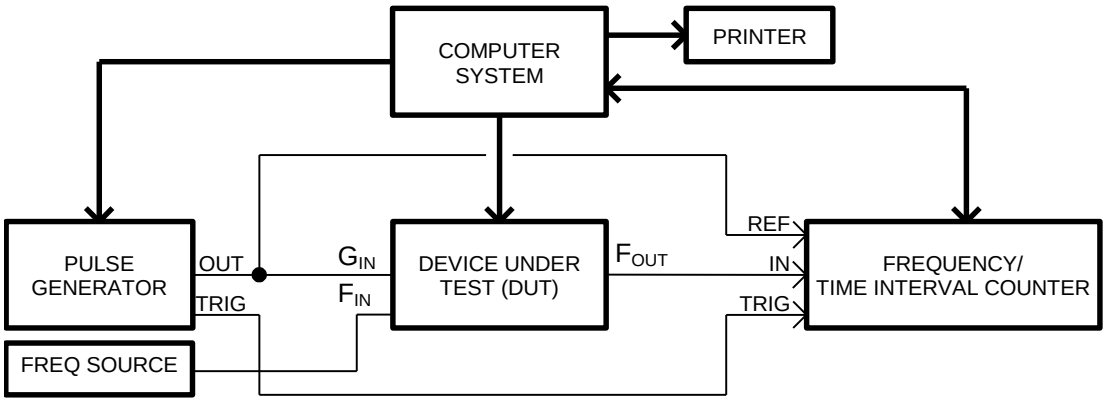


Figure 3: Test Setup

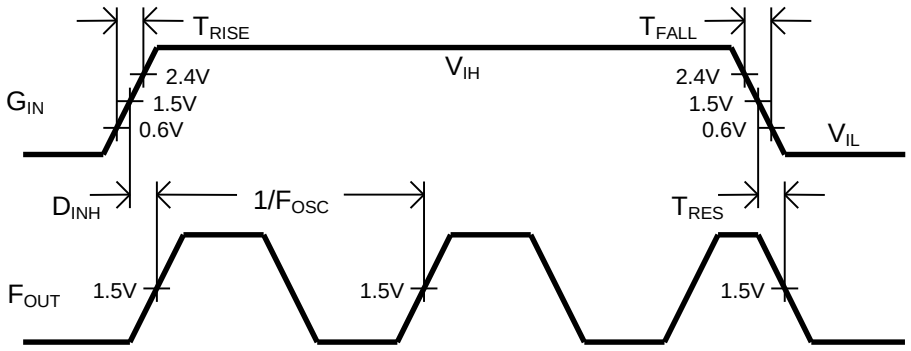


Figure 4: Timing Diagram