FEATURES

- **10-bit SAR ADC**
- **Single supply - Single channel**
- **Fast throughput of 750 kSPS**
- **Analog input range: 0V to 1.2V**
- **Temperature range: –40°C to +85°C**
- **Specified for VDD of 0.9V to 1.32V**
- **Internal power-on reset**
- **Typical power consumption 0.6mW**
- **8-lead TSSOP**

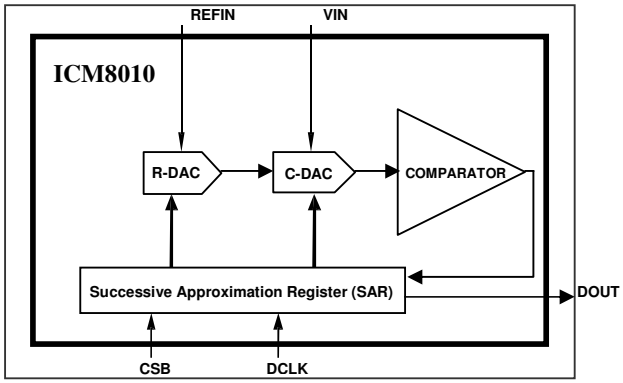
OVERVIEW

The ICM8010 is a 10-bit 750 kSPS through put rate SAR Analog-to-Digital Converter with a uni-polar, single-ended input. It has Successive Approximation Register (SAR) architecture and can sample the analog input. It has a flexible serial interface.

APPLICATIONS

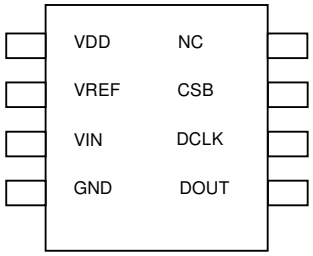
- Battery Powered Systems
- Medical Instrumentation
- Digital Power Supplies
- Touch Screen Controllers
- Data Acquisition Systems
- Automotive

BLOCK DIAGRAM



PACKAGE

8-Pin TSSOP



PIN DESCRIPTION

Pin No	Symbol	Description
1	VDD	Power Supply Input. Range is from 0.9V to 1.32V
2	VREF	Reference input
3	VIN	Analog Input
4	GND	Ground
5	DOUT	Serial Data output, clocked out on falling edge of CLK
6	DCLK	External CLK Input
7	CSB	Chip Select input Active Low. Initiates conversion and enables serial data.
8	NC	No connection

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 1.5	V
I_{IN}	Input Current	+/- 50.0	mA
$V_{IN\_}$	Digital Input Voltage	-0.3 to 1.2	V
V_{IN_REF}	Reference Input Voltage	-0.3 to 1.5	V
T_{STG}	Storage Temperature	-65 to +150	^{o}C
T_{SOL}	Soldering Temperature	300	^{o}C

Note: Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ORDERING INFORMATION

Part	Temperature Range	Package
ICM8010	-40 °C to 85 °C	8-Pin TSSOP

DC ELECTRICAL CHARACTERISTICS

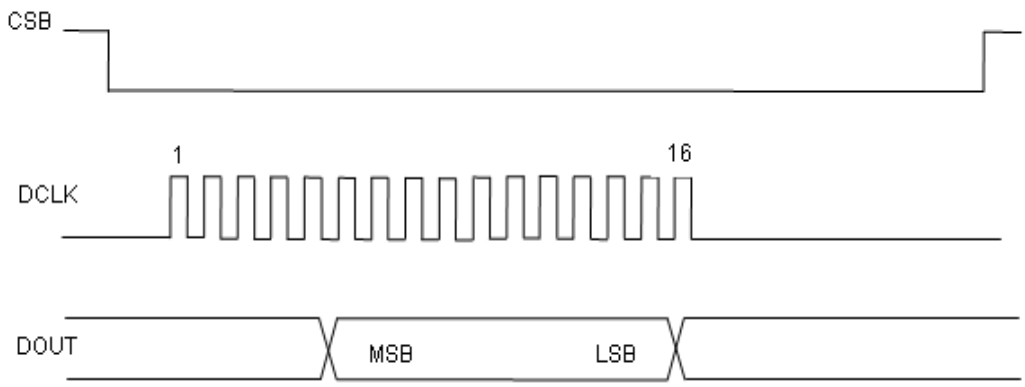
(VDD = 1.2V, Maximum Sample Rate, REF = 1.2V; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DC PERFORMANCE						
N	Resolution	(Note 1)		10		Bits
No Missing Codes		(Note 1)		10		Bits
INL	Integral Nonlinearity	(Note 1)			0.75	% of FSR
GE	Gain Error	(Note 1)			1.1	% of FS
OE	Offset Error	(Note 1)			25	mV
POWER REQUIREMENTS						
VDD	Supply Voltage	(Note 2)	0.9	1.2	1.32	V
I_{VDD}	Supply Current	(Note 1)		500		µA
$I_{SHTDOWN}$	Supply Current	(Note 1)		50		µA

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SWITCHING SPECIFICATIONS (CLK INPUT)						
Fsample	Maximum Conversion Rate	(Note 2)			750	kSPS
	Minimum Conversion Rate	(Note 2)	1			kSPS
TCLK	CLK Period	(Note 2)	82			ns
	Pulse-width High	(Note 2)	41			ns
	Pulse-width Low	(Note 2)	41			ns
T_{Delay}	Data out Delay	(Note 2)		15		ns
REFERENCE						
R_{IN}	Reference Input Resistance	(Note 1)		8.5		kΩ
	Reference Input Span				VDD	V
I_{REF}	Reference Input Current			150		µA

Note 1: 100 % Production Tested at 25 C; guaranteed by design and characterization testing for temperature range.
Note 2: Guaranteed by design & characterization testing.
Note 3: See Applications Information.

TIMING DIAGRAM



DETAILED DESCRIPTION

The ICM8010 is a micropower 1.2V single supply 10-Bit 750 kSPS SAR architecture ADC. It operates on a 0.9V to 1.32V single supply and consumes about 500µA supply current when operating on a 12MHz external clock. The output throughput rate is a maximum of 750 kSPS when the DCLK is running at at the maximum frequency of 12MHz.

The ADC is composed of a high performance capacitive DAC and a comparator along with SAR control logic and resistor string segment. The reference input drives the resistor string directly and has an input resistance of around 8.5 kΩ.

The ICM8010 comes complete with a high performance CMOS sample and hold amplifier made up by the capacitive DAC.

There is shutdown capability which is active between conversions when CSB is high. The converter will shut down to under 50 µA of supply current.

APPLICATIONS INFORMATION

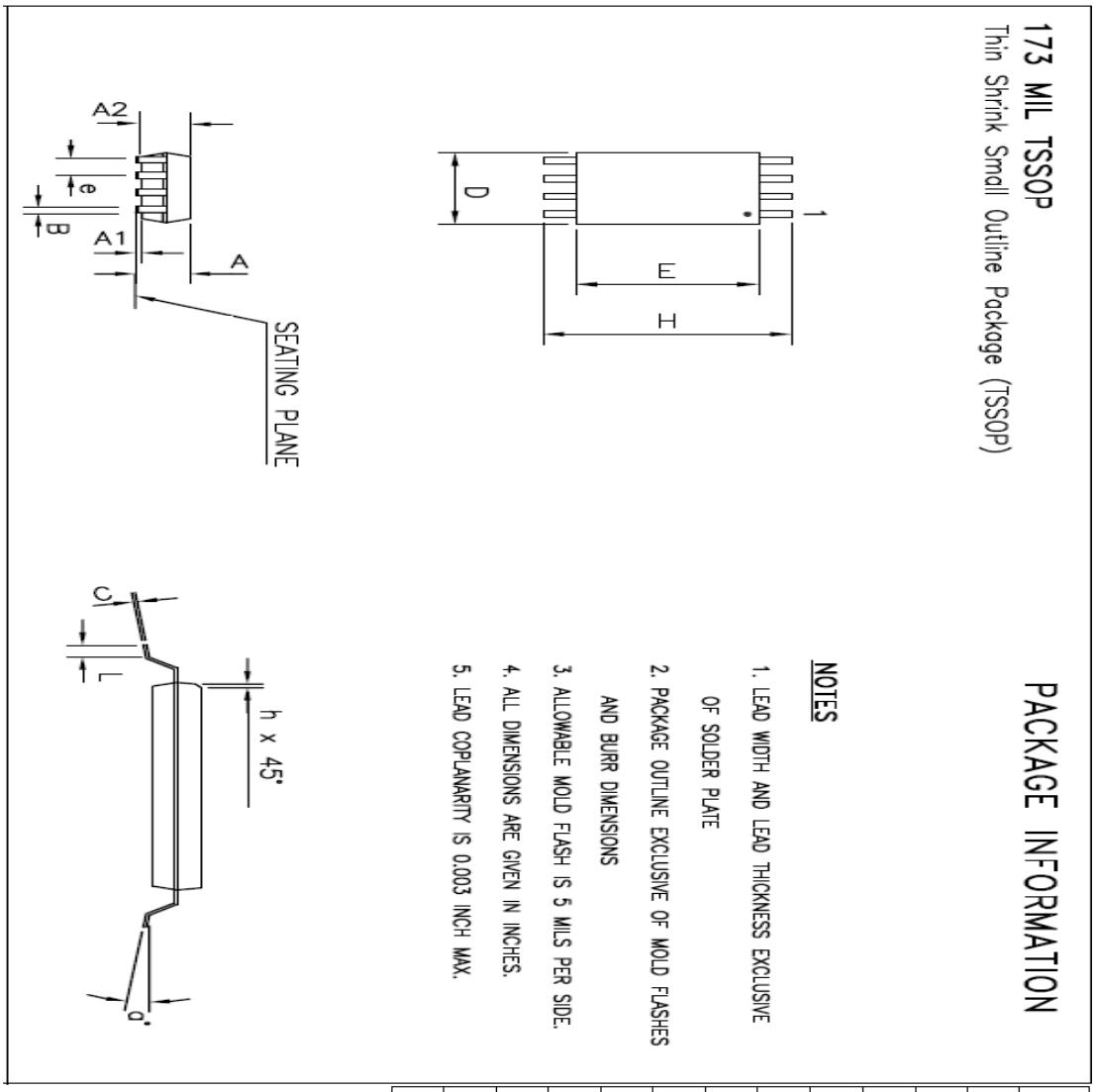
The ICM8010 has a single ended analog input which can swing from GND to VDD. The reference input has a range from GND to VDD and can be tied to VDD for largest input range.

The ICM8010 uses the DCLK as the external clock and this controls all the transfer of information to and from the ADC.

One complete conversion cycle of the ICM8010 will take 16 clock cycles. As CSB is pulled low the ADC powers up and initiates a sampling/conversion cycle. Data is clocked out MSB first on the falling edge of the DCLK input. The analog input is sampled on the first four clock pulses and then conversion process begins. The DOUT is available from the falling edge of the 5th DCLK pulse MSB first and the LSB is available on the falling edge of the 14th DCLK pulse. Since there is some propagation delay the DOUT should be sampled on the rising edge of the following clock pulse.

PACKAGE INFORMATION

8 LEAD TSSOP STANDARD PACKAGE



JEDEC#	MO-153AA		
TYPE	08 LEAD		
SYMBOL	Min	Max	
A	0.034	0.047	
A1	0.002	0.006	
B	0.007	0.012	
C	0.004	0.008	
D	0.114	0.122	
E	0.169	0.177	
e	0.0256 BSC		
H	0.252 BSC		
L	0.020	0.030	
α°	0°	8°	