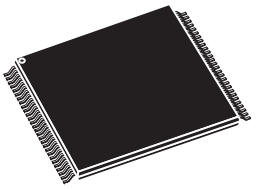
numonyx

M29DW127G

128-Mbit (8 Mbit x16 or 16 Mbit x8 , multiple bank, page, dual boot) 3 V supply flash memory

Features

- Supply voltage
  - V_{CC} = 2.7 to 3.6 V for program, erase and read
  - V_{CCQ} = 1.65 to 3.6 V for I/O buffers
  - V_{PPH} = 12 V for fast program (optional)
- Asynchronous random/page read
  - Page width: 8 words / 16 bytes
  - Page access: 25 ns
  - Random access: 60 or 70, 80 ns
- Enhanced Buffered Program commands
  - 256 words
- Programming time
  - 15 µs per byte/word (typical)
  - 32-word write buffer
  - Chip program time: 5 s with V_{PPH} and 8 s without V_{PPH}
- Erase verify
- Memory blocks
  - Quadruple bank memory array: 16 Mbit+48 Mbit+48 Mbit+16 Mbit
  - Parameter blocks (at top and bottom)
- Dual operation
  - while program or erase in one bank, read in any of the other banks
- Program/erase suspend and resume modes
  - Read from any block during program suspend
  - Read and program another block during erase suspend
- Unlock Bypass/Block Erase/Chip Erase/Write to Buffer/ Enhanced Buffered Program commands
  - Faster production/batch programming
  - Faster block and chip erase
- Common flash interface
  - 64-bit security code



TSOP56 (NF)
14 x 20 mm

TBGA64 (ZA)
10 x 13 mm

- 100,000 program/erase cycles per block
- Low power consumption
  - Standby and automatic standby
- Hardware block protection
  - V_{PP}/$\overline{WP}$ pin for fast program and write protect of the four outermost parameter blocks
- Security features
  - Volatile protection
  - Non-volatile protection
  - Password protection
  - Additional block protection
- Extended memory block
  - Extra block (128-word / 256-byte factory locked and 128-word / 256-byte customer lockable) used as security block or to store additional information
- Electronic signature
  - Manufacturer code: 0020h
  - Device code: 227Eh+2220h+2204h
- ECOPACK® packages available

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1 Description

The M29DW127G is a 128-Mbit (8 Mbit x16 / 16 Mbit x8) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6 V) supply. At power-up the memory defaults to its read mode.

The M29DW127G features an asymmetrical block architecture, with 8 parameter and 62 main blocks, divided into four banks, A, B, C and D, providing multiple bank operations. While programming or erasing in one bank, read operations are possible in any other bank. The bank architecture is summarized in *Table 2*. Four of the parameter blocks are at the top of the memory address space, and four are at the bottom.

Program and erase commands are written to the command interface of the memory. An on-chip program/erase controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

The Chip Enable, Output Enable and Write Enable signals control the bus operations of the memory. They allow simple connection to most microprocessors, often without additional logic.

The device supports asynchronous random read and page read from all blocks of the memory array. The device also features a write to buffer program capability that improves the programming throughput by programming in one shot a buffer of 32 words / 64 bytes. The enhanced buffered program feature is also available to speed up programming throughput, allowing 256 words to be programmed at once (only available in x16 mode). The $V_{PP}/\overline{WP}$ signal can be used to enable faster programming of the device.

The M29DW127G has one extra 256-word block in x16 mode or one extra 512-byte block in x8 mode (extended block, 128 words / 256 bytes factory locked and 128 words / 256 bytes customer lockable) that can be accessed using a dedicated command. The extended block can be protected and so is useful for storing security information. However the protection is irreversible, once protected the protection cannot be undone.

Each block can be erased independently, so it is possible to preserve valid data while old data is erased.

The device features different levels of hardware and software block protection to avoid unwanted program or erase (modify):

- Hardware protection
  - The $V_{PP}/\overline{WP}$ provides a hardware protection of the four outermost parameter blocks (two at the top and two at the bottom of the address space)
- Software protection
  - Volatile protection
  - Non-volatile protection
  - Password protection
- Additional protection features are available upon customer request.

The memory is offered in TSOP56 (14 x 20 mm) and TBGA64 (10 x 13 mm, 1 mm pitch) packages. The memory is delivered with all the bits erased (set to ‘1’).

Table 1. Signal names

Name	Description	Direction
A0-A22	Address inputs	Inputs
DQ0-DQ7	Data inputs/outputs	I/O
DQ8-DQ14	Data inputs/outputs	I/O
DQ15A–1	Data input/output or address input	I/O
$\overline{E}$	Chip enable	Input
$\overline{G}$	Output enable	Input
$\overline{W}$	Write enable	Input
$\overline{RP}$	Reset	Input
$R\overline{B}$	Ready/busy output	Output
$\overline{BYTE}$	Byte/word organization select	Input
V_{CCQ}	Input/output buffer supply voltage	Supply
V_{CC}	Supply voltage	Supply
$V_{PP}/\overline{WP}$(1)	V_{PP}/write protect	Supply/Input
V_{SS}	Ground	–
NC	Not connected	–

1. $V_{PP}/\overline{WP}$ may be left floating as it is internally connected to a pull-up resistor which enables program/erase operations.

Figure 1. Logic diagram

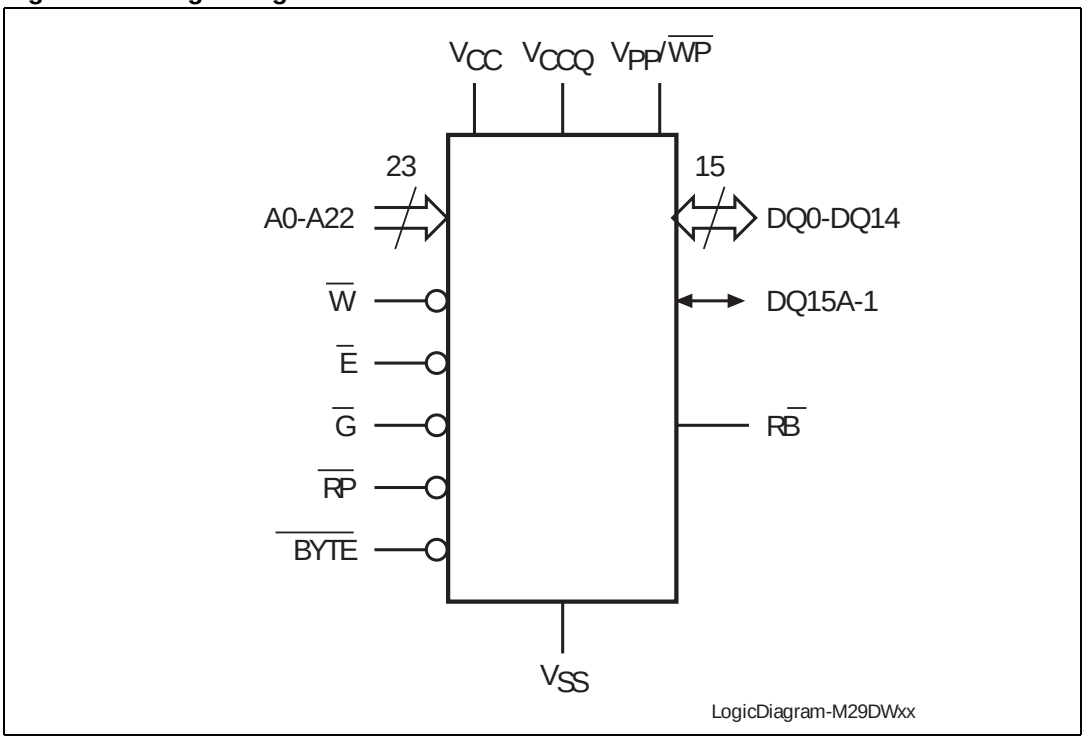


Table 2. Bank architecture

Bank	Bank size	Parameter blocks		Main blocks	
		N. of blocks	Block size	N. of blocks	Block size
A	16 Mbit	4	32 Kwords / 64 Kbytes	7	128 Kwords / 256 Kbytes
B	48 Mbit	—	—	24	128 Kwords / 256 Kbytes
C	48 Mbit	—	—	24	128 Kwords / 256 Kbytes
D	16 Mbit	4	32 Kwords / 64 Kbytes	7	128 Kwords / 256 Kbytes

Figure 2. TSOP connections

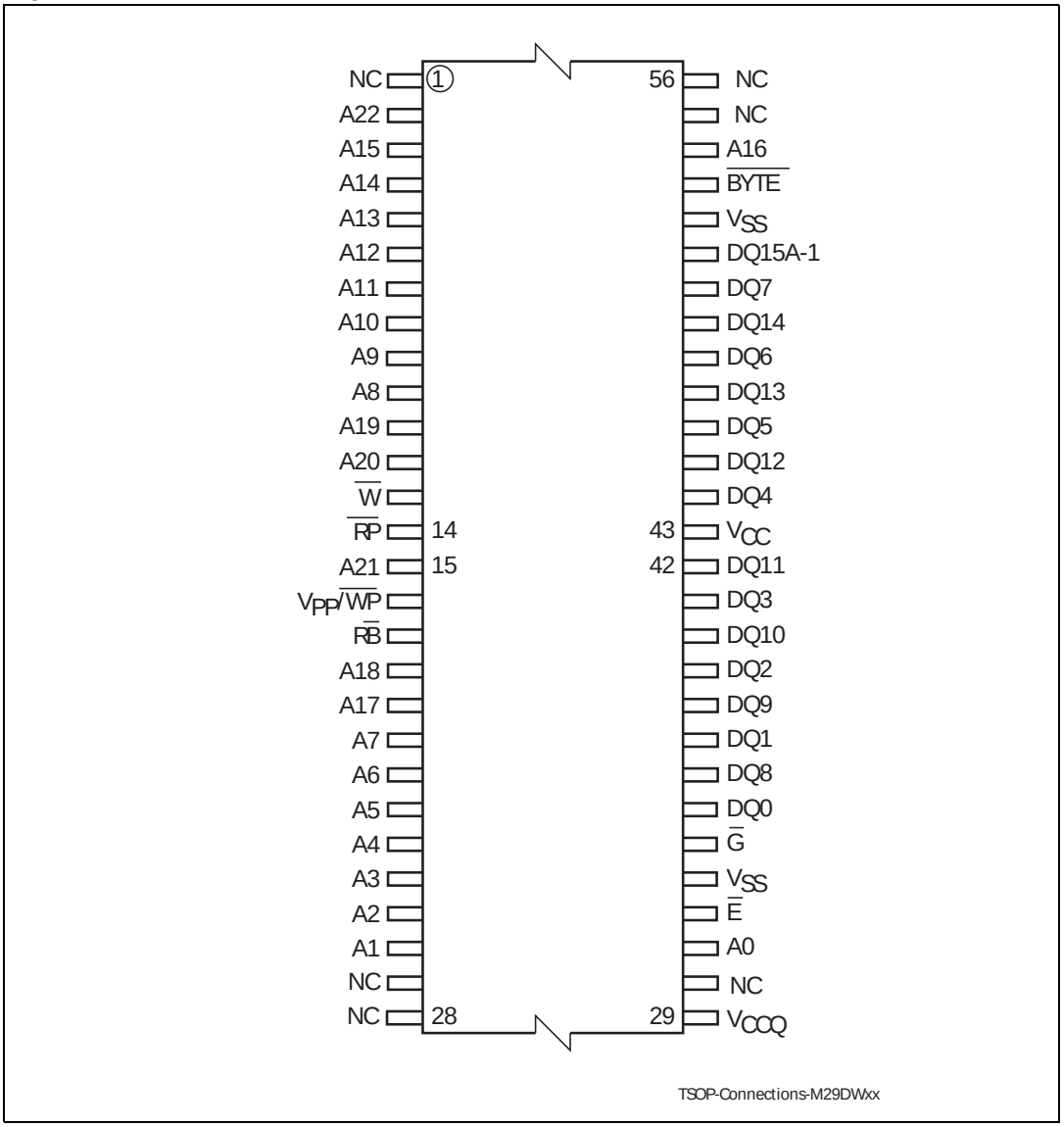


Figure 3. TBGA connections (top view through package)

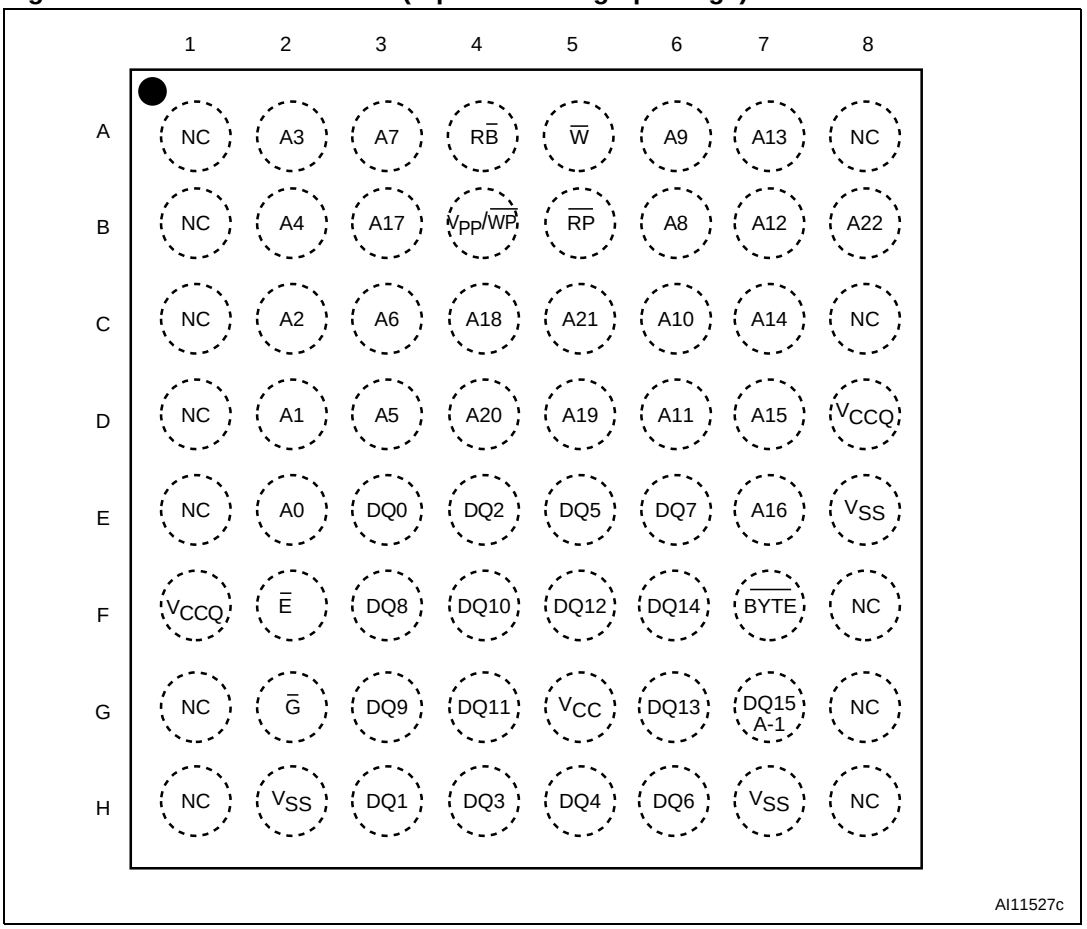


Figure 4. Block addresses (x8 mode)

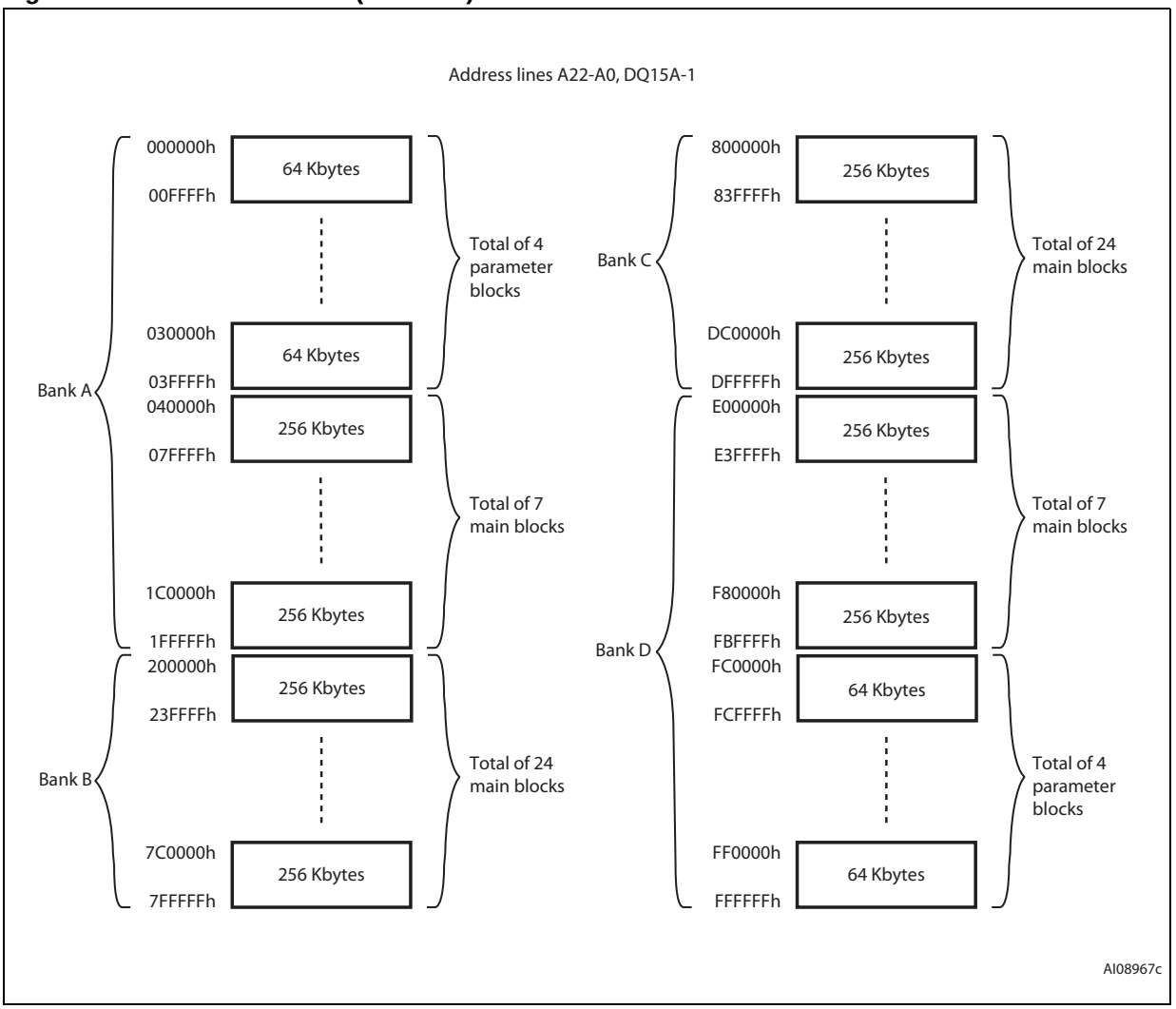
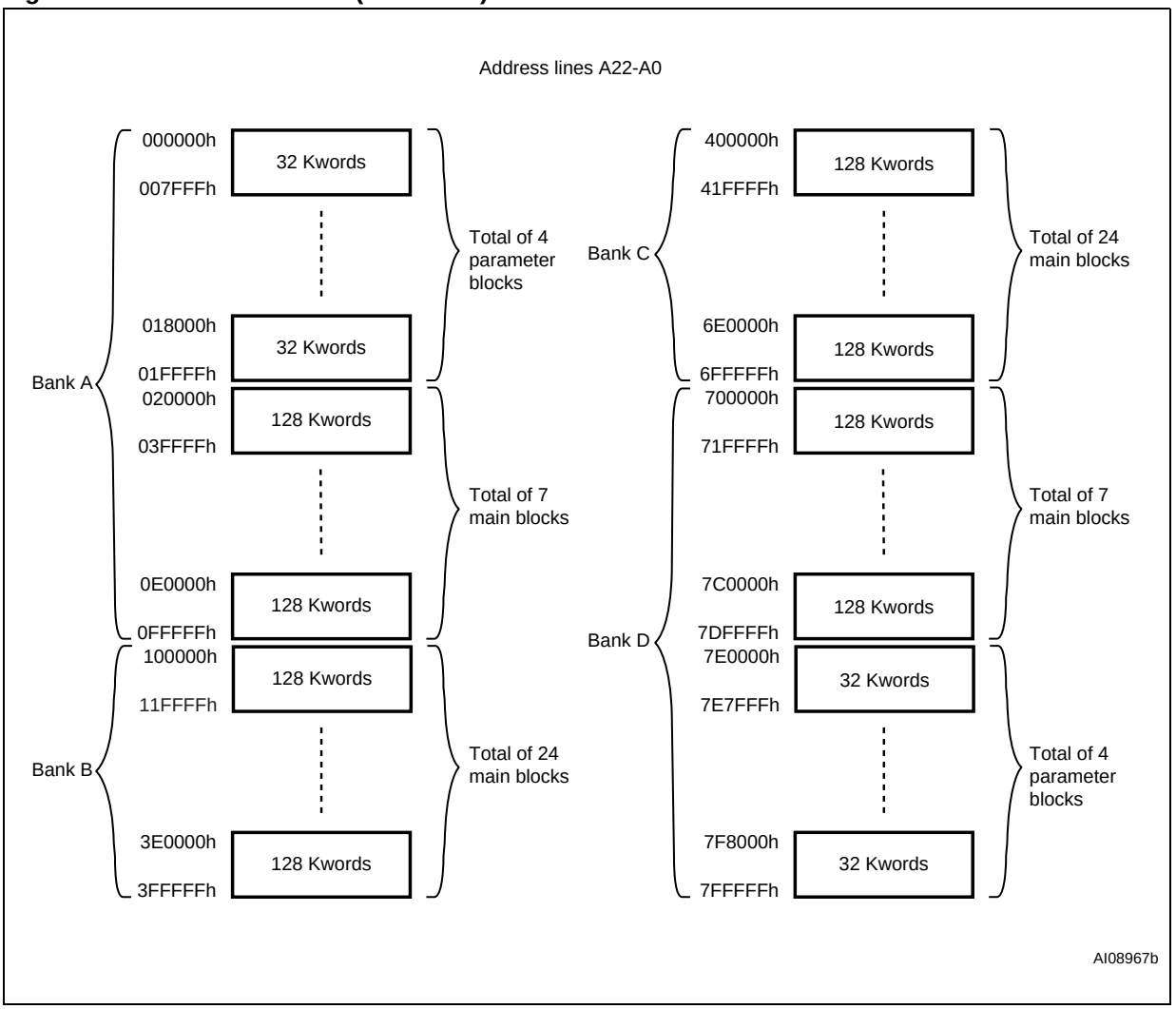


Figure 5. Block addresses (x16 mode)



2 Signal descriptions

See *Figure 1: Logic diagram* and *Table 1: Signal names* for a brief overview of the signals connected to this device.

2.1 Address inputs (A0-A22)

The address inputs select the cells in the memory array to access during bus read operations. During bus write operations they control the commands sent to the command interface of the program/erase controller.

2.2 Data inputs/outputs (DQ0-DQ7)

The data I/O outputs the data stored at the selected address during a bus read operation. During bus write operations they represent the commands sent to the command interface of the internal state machine.

2.3 Data inputs/outputs (DQ8-DQ14)

The data I/O outputs the data stored at the selected address during a bus read operation when $\overline{BYTE}$ is High, V_{IH}. When $\overline{BYTE}$ is Low, V_{IL}, these pins are not used and are high impedance. During bus write operations the command register does not use these bits. When reading the status register these bits should be ignored.

2.4 Data inputs/outputs or address inputs (DQ15A–1)

When the device is in x 16 bus mode, this pin behaves as a data input/output pin (as DQ8-DQ14). When the device operates in x 8 bus mode, this pin behaves as the least significant bit of the address. Throughout the text consider references to the data input/output to include this pin when the device operates in x 16 bus mode and references to the address inputs to include this pin when the device operates in x 8 bus mode except when stated explicitly otherwise.

2.5 Chip Enable ($\overline{E}$)

The Chip Enable pin, $\overline{E}$, activates the memory, allowing bus read and bus write operations to be performed. When chip enable is High, V_{IH}, all other pins are ignored.

2.6 Output Enable ($\overline{G}$)

The Output Enable pin, $\overline{G}$, controls the bus read operation of the memory.

2.7 Write Enable ($\overline{W}$)

The Write Enable pin, $\overline{W}$, controls the bus write operation of the memory's command interface.

2.8 V_{PP}/write protect ($V_{PP}/\overline{WP}$)

The V_{PP}/write protect pin provides two functions. The V_{PPH} function allows the memory to use an external high voltage power supply to reduce the time required for program operations. This is achieved by bypassing the unlock cycles.

The write protect function provides a hardware method of protecting the four outermost blocks, that is the two 32-kword blocks at the top and the two 32-kword blocks at the bottom of the address space (see *Section 1: Description*). When V_{PP}/write protect is Low, V_{IL}, the 4 outermost blocks are protected. Program and erase operations on this block are ignored while V_{PP}/write protect is Low.

When V_{PP}/write protect is High, V_{IH}, the memory reverts to the previous protection status of the four outermost blocks. Program and erase operations can now modify the data in these blocks unless the blocks are protected using block protection.

When V_{PP}/write protect is raised to V_{PPH} the memory automatically enters the unlock bypass mode (see *Section 7.2.6*).

When V_{PP}/write protect is raised to V_{PPH}, the execution time of the command is lower (see *Table 18: Program, erase times and program, erase endurance cycles*).

When V_{PP}/write protect returns to V_{IH} or V_{IL} normal operation resumes. During unlock bypass program operations the memory draws I_{PP} from the pin to supply the programming circuits. See the description of the Unlock Bypass command in the command interface section. The transitions from V_{IH} to V_{PPH} and from V_{PPH} to V_{IH} must be slower than t_{VHVPP} (see *Figure 25: Accelerated program timing waveforms*).

Never raise V_{PP}/write protect to V_{PPH} from any mode except read mode, otherwise the memory may be left in an indeterminate state. A 0.1 µF capacitor should be connected between the VPP/write protect pin and the V_{SS} ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during unlock bypass program (see I_{PP1}, I_{PP2}, I_{PP3}, I_{PP4} in *Table 28: DC characteristics*).

The V_{PP}/write protect pin may be left floating or unconnected because it features an internal pull-up.

Refer to *Table 3* for a summary of $V_{PP}/\overline{WP}$ functions.

Table 3. $V_{PP}/\overline{WP}$ functions

$V_{PP}/\overline{WP}$	Function
V_{IL}	Four outermost blocks(1) protected.
V_{IH}	Four outermost blocks(1) unprotected unless a software protection is activated (see *Section 5: Hardware protection*).
V_{PPH}	Unlock bypass mode. It supplies the current needed to speed up programming.

1. Two at the top and two at the bottom of the address space.

2.9 Reset ($\overline{RP}$)

The reset pin can be used to apply a hardware reset to the memory.

A hardware reset is achieved by holding reset Low, V_{IL}, for at least t_{PLPX}. After reset goes High, V_{IH}, the memory will be ready for bus read and bus write operations after t_{PHEL} or t_{RHEL}, whichever occurs last. See *Section 2.10: Ready/busy output (RB)*, *Table 32: Reset AC characteristics*, *Figure 23* and *Figure 24* for more details.

2.10 Ready/busy output ($\overline{RB}$)

The ready/busy pin is an open-drain output that can be used to identify when the device is performing a program or erase operation. During program or erase operations ready/busy is Low, V_{OL} (see *Table 21: Status register bits*). Ready/busy is high-impedance during read mode, auto select mode and erase suspend mode.

After a hardware reset, bus read and bus write operations cannot begin until ready/busy becomes high-impedance. See *Table 32: Reset AC characteristics*, *Figure 23* and *Figure 24*.

The use of an open-drain output allows the ready/busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

2.11 Byte/word organization select ($\overline{BYTE}$)

It is used to switch between the x8 and x16 bus modes of the memory. When byte/word organization select is Low, V_{IL}, the memory is in x8 mode, when it is High, V_{IH}, the memory is in x16 mode.

2.12 V_{CC} supply voltage

V_{CC} provides the power supply for all operations (read, program and erase).

The command interface is disabled when the V_{CC} supply voltage is less than the lockout voltage, V_{LKO}. This prevents bus write operations from accidentally damaging the data during power-up, power-down and power surges. If the program/erase controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid.

A 0.1 µF capacitor should be connected between the V_{CC} supply voltage pin and the V_{SS} ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations (see I_{CC1}, I_{CC2}, I_{CC3} in *Table 28: DC characteristics*).

2.13 V_{CCQ} input/output supply voltage

V_{CCQ} provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{CC}.

2.14 V_{SS} ground

V_{SS} is the reference for all voltage measurements. The device features two V_{SS} pins both of which must be connected to the system ground.

3 Bus operations

There are five standard bus operations that control the device. These are bus read (random and page modes), bus write, output disable, standby and automatic standby.

Dual operations are possible in the M29DW127G, thanks to its multiple bank architecture. While programming or erasing in one bank, read operations are possible in any of the other banks. Write operations are only allowed in one bank at a time.

See *Table 4: Bus operations, 8-bit mode on page 20* and *Table 5: Bus operations, 16-bit mode on page 20* for a summary. Typical glitches of less than 5 ns on chip enable, write enable, and reset pins are ignored by the memory and do not affect bus operations.

3.1 Bus read

Bus read operations read from the memory cells, or specific registers in the command interface. To speed up the read operation the memory array can be read in page mode where data is internally read and stored in a page buffer. The page has a size of 8 words (or 16 bytes) and is addressed by the address inputs A2-A0 in x16 mode and A2-A0 plus DQ15A-1 in x8 mode.

A valid bus read operation involves setting the desired address on the address inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable High, V_{IH}. The data inputs/outputs will output the value, see *Figure 14: Random read AC waveforms (8-bit mode) on page 65*, *Figure 15: Random read AC waveforms (16-bit mode) on page 65*, and *Table 29: Read AC characteristics on page 69* for details of when the output becomes valid.

3.2 Bus write

Bus write operations write to the command interface. A valid bus write operation begins by setting the desired address on the address inputs. The address inputs are latched by the command interface on the falling edge of Chip Enable or Write Enable, whichever occurs last. The data inputs/outputs are latched by the command interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the whole bus write operation.

For details on AC characteristics (write enabled and chip enabled controlled), see the following figures and tables:

- *Figure 19: Write enable controlled program waveforms (8-bit mode) on page 70*
- *Figure 20: Write enable controlled program waveforms (16-bit mode) on page 71*
- *Table 30: Write AC characteristics, write enable controlled on page 72*
- *Figure 21: Chip enable controlled program waveforms (8-bit mode) on page 73*
- *Figure 22: Chip enable controlled program waveforms (16-bit mode) on page 74*
- *Table 31: Write AC characteristics, chip enable controlled on page 74*

3.3 Output disable

The data inputs/outputs are in the high impedance state when output enable is High, V_{IH}.

3.4 Standby

Driving Chip Enable High, V_{IH}, in read mode, causes the memory to enter standby mode and the data inputs/outputs pins are placed in the high-impedance state. To reduce the supply current to the standby supply current, I_{CC2}, Chip Enable should be held within V_{CC} ± 0.3 V. For the standby current level see *Table 28: DC characteristics*.

During program or erase operations the memory will continue to use the program/erase supply current, I_{CC3}, for program or erase operations until the operation completes.

3.5 Reset

During reset mode the memory is deselected and the outputs are high impedance. The memory is in reset mode when $\overline{RP}$ is at V_{IL}. The power consumption is reduced to the standby level, independently from the Chip Enable, Output Enable or Write Enable inputs.

3.6 Automatic standby

Automatic standby allows the memory to achieve low power consumption during read mode.

After a read operation, if CMOS levels (V_{CC} ± 0.3 V) are used to drive the bus and the bus is inactive for t_{AVQV} + 30 ns or more, the memory enters automatic standby where the internal supply current is reduced to the standby supply current, I_{CC2} (see *Table 28: DC characteristics*). The data inputs/outputs will still output data if a bus read operation is in progress.

The power supplier of data bus, V_{CCQ}, can have a null consumption (depending on load circuits connected with data bus) when the memory enters automatic standby.

Table 4. Bus operations, 8-bit mode

Operation[1]	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$V_{PP}/\overline{WP}$	Address Inputs	Data inputs/outputs	
						A22-A0, DQ15A-1	DQ14-DQ8	DQ7-DQ0
Bus read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Cell address	Hi-Z	Data output
Bus write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X[2]	Command address	Hi-Z	Data input[3]
Standby	V_{IH}	X	X	V_{IH}	X	X	Hi-Z	Hi-Z
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	Hi-Z	Hi-Z
Reset	X	X	X	V_{IL}	X	X	Hi-Z	Hi-Z

1. X = V_{IL} or V_{IH}.
2. To write the four outermost parameter blocks (first two and the last two), VPP/WP must be equal to VIH.
3. Data input as required when issuing a command sequence, performing data polling or block protection.

Table 5. Bus operations, 16-bit mode

Operation[1]	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$V_{PP}/\overline{WP}$	Address inputs	Data inputs/outputs
						A22-A0	DQ15A-1, DQ14-DQ0
Bus read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Cell address	Data output
Bus write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X[2]	Command address	Data input[3]
Standby	V_{IH}	X	X	V_{IH}	X	X	Hi-Z
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	Hi-Z
Reset	X	X	X	V_{IL}	X	X	Hi-Z

1. X = V_{IL} or V_{IH}.
2. To write the four outermost parameter blocks (first two and last two), VPP/WP must be equal to VIH.
3. Data input as required when issuing a command sequence, performing data polling or block protection.

4 Auto select mode

The auto select mode allows the system or the programming equipment to read the electronic signature, verify the protection status of the extended memory block, and apply/remove block protection. For example, this mode can be used by a programming equipment to automatically match a device and the application code to be programmed.

The auto select mode is entered by issuing the Auto Select command (see *Section 7.1.2: Auto Select command*).

At power-up, the device is in read mode, and can then be put in auto select mode by issuing the Auto Select command.

The device cannot enter auto select mode when a program or erase operation is ongoing ($\overline{RB}$ Low). However, auto select mode can be entered if the erase operation has been suspended by issuing an Erase Suspend command (see *Section 7.1.6*).

The auto select mode is exited by performing a reset. The device is returned to read mode, except if the auto select mode was entered after an Erase Suspend or a Program Suspend command. In this case, it returns to the erase or program suspend mode.

4.1 Read electronic signature

The memory has two codes, the manufacturer code and the device code used to identify the memory. These codes can be accessed by performing read operations with control signals and addresses set as shown in *Table 9: Block protection (16-bit mode)* and *Table 6: Read electronic signature, auto select mode method (8-bit mode)* and *Table 7: Read electronic signature, auto select mode method (16-bit mode)*.

4.2 Verify extended memory block protection indicator

The extended memory block is either factory locked or customer lockable.

The protection status of the extended memory block (factory locked or customer lockable) can be accessed by reading the extended memory block protection indicator. See *Table 8: Block protection (8-bit mode)* and *Table 9.: Block protection (16-bit mode)*.

The protection status of the extended memory block is then output on bit DQ7 of the data input/outputs (see *Table 4: Bus operations, 8-bit mode* and *Table 5: Bus operations, 16-bit mode*).

4.3 Verify block protection status

The protection status of a block can be directly accessed by performing a read operation with control signals and addresses set as shown in *Table 8: Block protection (8-bit mode)* and *Table 9: Block protection (16-bit mode)*.

If the block is protected, then 01h is output on data input/outputs DQ0-DQ7, otherwise 00h is output.

Table 6. Read electronic signature, auto select mode method (8-bit mode)

Read cycle[1]	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address inputs									Data inputs/outputs		
				A22-A10	A9-A7	A8	A6	A5-A4	A3	A2	A1	A0	DQ15A-1	DQ14-DQ8	DQ7-DQ0
Manufacturer code	V_{IL}	V_{IL}	V_{IH}	BKA	X	X	V_{IL}	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	X	X	20h
Device code (cycle 1)								V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X	7Eh
Device code (cycle 2)									V_{IH}	V_{IH}	V_{IH}	V_{IL}	X	X	20h
Device code (cycle 3)									V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	X	04h

1. X = V_{IL} or V_{IH}. BKA bank address.

Table 7. Read electronic signature, auto select mode method (16-bit mode)

Read cycle[1]	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address inputs									Data inputs/outputs
				A22-A12	A11-A10	A9	A8	A7-A6	A5-A4	A3	A2	A1	A0	DQ15-DQ0
Manufacturer code	V_{IL}	V_{IL}	V_{IH}	BKA	X	X	X	V_{IL}	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	0020h
Device code (cycle 1)									V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	227Eh
Device code (cycle 2)										V_{IH}	V_{IH}	V_{IH}	V_{IL}	2220h
Device code (cycle 3)										V_{IH}	V_{IH}	V_{IH}	V_{IH}	2204h

1. X = V_{IL} or V_{IH}. BKA bank address.

Table 8. Block protection (8-bit mode)

Operation[1]	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address inputs										Data inputs/outputs	
				A22-A16	A14-A10	A9	A8-A7	A6	A5-A4	A3-A2	A1	A0	DQ15A-1	DQ14-DQ8	DQ7-DQ0
Verify extended memory block protection indicator (bit DQ7)	V_{IL}	V_{IL}	V_{IH}	BKA	X	X	X	V_{IL}	X	V_{IL}	V_{IH}	V_{IH}	X	X	DQ7: 1=factory locked DQ6: 1=customer locked, 0=customer lockable DQ5: 1=reserved, 0=standard DQ4, DQ3-Hardware write protection: 00=WP protects 4 outermost blocks, 11=No WP protection DQ2-DQ0=0
Verify block protection status				BAd								V_{IL}			01h (protected) 00h (unprotected)

1. X = VIL or VIH; BAd = any address in the block; BKA = bank address.

Table 9. Block protection (16-bit mode)

Operation (1)	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$V_{PP}/\overline{WP}$	Address inputs									Data inputs/outputs
						A22-A12	A11-A10	A9	A8	A7	A6	A5-A4	A3-A2	A1	A0	DQ15-DQ0
Verify extended memory block indicator bit	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	BKA	X	X	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	DQ15-DQ8=0 DQ7: 1=factory locked DQ6: 1=customer locked, 0=customer lockable DQ5: 1=reserved, 0=standard DQ4, DQ3-Hardware write protection: 00=$\overline{WP}$ protects 4 outermost blocks, 11=No $\overline{WP}$ protection DQ2-DQ0=0
Verify block protection status						BAd									V_{IL}	0000h (unprotected) 0001h (protected)

1. X = V_{IL} or V_{IH}. BAd any address in the block, BKA bank address.

5 Hardware protection

The M29DW127G features hardware protection/unprotection. Refer to *Table 10: Hardware protection* for details on hardware block protection/unprotection using $V_{PP}/\overline{WP}$ and $\overline{RP}$ pins.

5.1 Write protect

The $V_{PP}/\overline{WP}$ pin can be used to protect the four outermost parameter blocks (refer to *Section 2: Signal descriptions* for a detailed description of the signals). When $V_{PP}/\overline{WP}$ is at V_{IL} the four outermost parameter blocks are protected and remain protected regardless of the block protection status or the reset pin state.

Table 10. Hardware protection

$V_{PP}/\overline{WP}$	Function
V_{IL}	4 outermost parameter blocks (first two and last two) protected from program/erase operations
V_{IH}	4 outermost parameter blocks unprotected unless a software activated (see *Section 5: Hardware protection*)
V_{PPH}	Unlock bypass mode. It supplies the current needed to speed up programming

6 Software protection

The M29DW127G has three different software protection modes:

- Volatile protection
- Non-volatile protection
- Password protection

On first use all parts default to operate in non-volatile protection mode and the customer is free to activate the non-volatile or the password protection mode.

The desired protection mode is activated by setting either the one-time programmable non-volatile protection mode lock bit or the password protection mode lock bit of the lock register (see *Section 8.1: Lock register*). Programming the non-volatile protection mode lock bit or the password protection mode lock bit to '0' will permanently activate the non-volatile or the password protection mode, respectively. These three bits are one-time programmable and non-volatile: once the protection mode has been programmed, it cannot be changed and the device will permanently operate in the selected protection mode. It is recommended to activate the desired software protection mode when first programming the device.

The non-volatile and password protection modes provide non-volatile protection. Volatilely protected blocks and non-volatilely protected blocks can co-exist within the memory array. However, the volatile protection only control the protection scheme for blocks that are not protected using the non-volatile or password protection.

If the user attempts to program or erase a protected block, the device ignores the command and returns to read mode.

The device is shipped with all blocks unprotected. The block protection status can be read either by performing a read electronic signature (see *Table 7: Read electronic signature, auto select mode method (16-bit mode)*) or by issuing an Auto Select command (see *Table 20: Block protection status*).

For the four outermost blocks (that is the two blocks at the top and the two at the bottom of the address space), an even higher level of block protection can be achieved by locking the blocks using the non-volatile protection and then by holding the $V_{PP}/\overline{WP}$ pin Low.

6.1 Volatile protection mode

The volatile protection allows the software application to easily protect blocks against inadvertent change. However, the protection can be easily disabled when changes are needed. Volatile protection bits, VPBs, are volatile and unique for each block and can be individually modified. VPBs only control the protection scheme for unprotected blocks that have their non-volatile protection bits, NVPBs, cleared (erased to '1') (see *Section 6.2: Non-volatile protection mode* and *Section 7.3.5: Non-volatile protection mode command set*).

By issuing the VPB Program or VPB Clear commands, the VPBs are set (programmed to '0') or cleared (erased to '1'), thus placing each block in the protected or unprotected state respectively. The VPBs can be set (programmed to '0') or cleared (erased to '1') as often as needed.

The default values of the volatile protections are set through the VLBB (volatile lock boot bit) of the lock register (see *Table 19: Lock register bits*).

When the parts are first shipped, or after a power-up or hardware reset, the VPBs can be set or cleared depending upon the ordering option chosen:

- If the option to clear the VPBs after power-up is selected, then the blocks can be programmed or erased depending on the NVPBs state (see *Table 20: Block protection status*)
- If the option to set the VPBs after power-up is selected, the blocks default to be protected.

Refer to *Section 7.3.7* for a description of the volatile protection mode command set.

6.2 Non-volatile protection mode

6.2.1 Non-volatile protection bits

A non-volatile protection bit (NVPB) is assigned to each block.

When a NVPB is set to '0', the associated block is protected, preventing any program or erase operations in this block.

The NVPB bits are set individually by issuing a NVPB Program command. They are non-volatile and will remain set through a hardware reset or a power-down/power-up sequence.

The NVPBs cannot be cleared individually, they can only be cleared all at the same time by issuing a Clear all Non-volatile Protection Bits command.

The NVPBs can be protected all at a time by setting a volatile bit, the NVPB lock bit (see *Section 6.2.2: Non-volatile protection bit lock bit*).

If one of the non-volatile protected blocks needs to be unprotected (corresponding NVPB set to '1'), a few more steps are required:

1. First, the NVPB lock bit must be cleared by either putting the device through a power cycle, or hardware reset
2. The NVPBs can then be changed to reflect the desired settings
3. The NVPB lock bit must be set once again to lock the NVPBs. The device operates normally again.

Note: 1 To achieve the best protection, it is recommended to execute the NVPB Lock Bit Program command early in the boot code and to protect the boot code by holding V_{PP}/WP Low, V_{IL}.

2 The NVPBs and VPBs have the same function when V_{PP}/WP pin is High, V_{IH}, as they do when V_{PP} /WP pin is at the voltage for program acceleration (V_{PPH}).

Refer to *Table 20: Block protection status* and *Figure 6: Software protection scheme* for details on the block protection mechanism, and to *Section 7.3.5* for a description of the non-volatile protection mode command set.

6.2.2 Non-volatile protection bit lock bit

The non-volatile protection bit lock bit (NVPB lock bit) is a global volatile bit for all blocks.

When set (programmed to '0'), it prevents changing the state of the NVPBs. When cleared (programmed to '1'), the NVPBs can be set and reset using the NVPB Program command and Clear all NVPBs command, respectively.

There is only one NVPB lock bit per device.

Refer to *Section 7.3.6* for a description of the NVPB lock bit command set.

Note: 1 No software command unlocks this bit unless the device is in password protection mode; it can be cleared only by taking the device through a hardware reset or a power-up.

2 The NVPB lock bit must be set (programmed to '0') only after all NVPBs are configured to the desired settings.

6.3 Password protection mode

The password protection mode provides an even higher level of security than the non-volatile protection mode by requiring a 64-bit password for unlocking the device NVPB lock bit.

In addition to this password requirement, the NVPB lock bit is set '0' after power-up and reset to maintain the device in password protection mode. Successful execution of the Password Unlock command by entering the correct password clears the NVPB lock bit, allowing for block NVPBs to be modified.

If the password provided is not correct, the NVPL Lock bit remains locked and the state of the NVPBs cannot be modified.

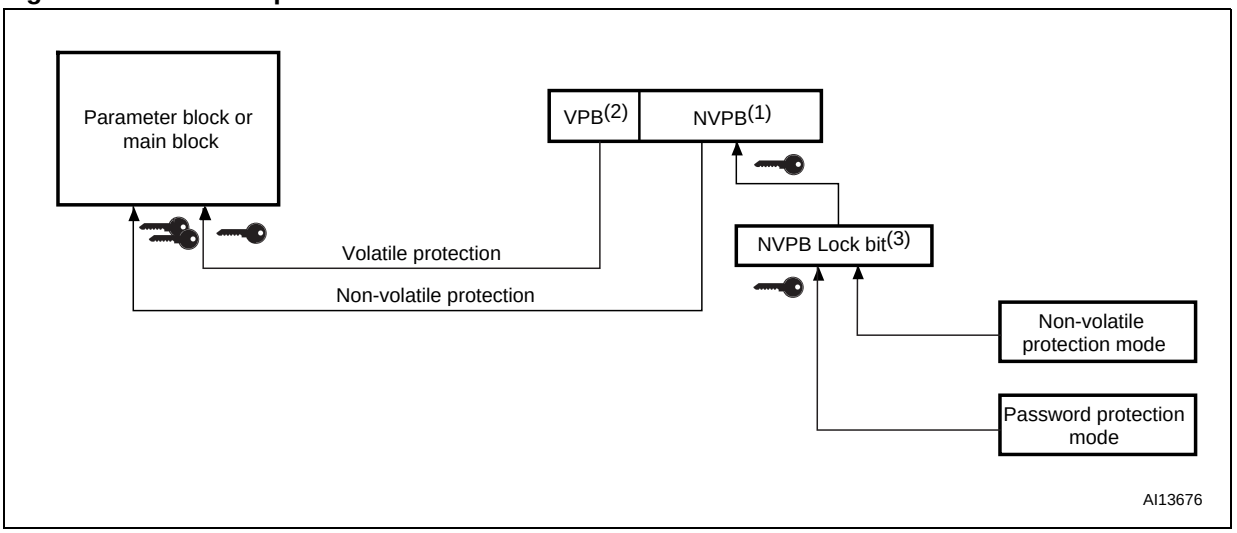
To place the device in password protection mode, the following steps are required:

1. Prior to entering the password protection mode, it is necessary to set a 64-bit password and to verify it (see *Password Program command* and *Password Read command*). Password verification is only allowed during the password programming operation
2. The password protection mode is then activated by programming the password protection mode lock bit to '0'. This operation is not reversible and once the bit is programmed it cannot be erased, the device permanently remains in password protection mode, and the 64-bit password can neither be retrieved nor reprogrammed. Moreover, all commands to the address where the password is stored, are disabled. Refer to *Table 20: Block protection status* and *Figure 6: Software protection scheme* for details on the block protection scheme.

Refer to *Section 7.3.4* for a description of the password protection mode command set.

Note: There is no means to verify the password after it is set. If the password is lost after setting the password mode lock bit, there is no way to clear the NVPB lock bit.

Figure 6. Software protection scheme



1. NVPBs default to ‘1’ (block unprotected) after power-up and hardware reset. A block is protected or unprotected when its NVPB is set to ‘0’ and ‘1’, respectively. NVPBs are programmed individually and cleared collectively.
2. VPB default status depends on ordering option. A block is protected or unprotected when its VPB is set to ‘0’ and ‘1’, respectively. VPBs are programmed and cleared individually. For the volatile protection to be effective, the NVPB lock bit must be set to ‘0’ (NVPB bits unlocked) and the block NVPB must be set to ‘1’ (block unprotected).
3. The NVPB Lock bit is volatile and default to ‘1’ (NVPB bits unlocked) after power-up and hardware reset. NVPB bits are locked by setting the NVPB lock bit to ‘0’. Once programmed to ‘0’, the NVPB lock bit can be reset to ‘1’ only be taking the device through a power-up or hardware reset.

7 Command interface

All bus write operations to the memory are interpreted by the command interface. Commands consist of one or more sequential bus write operations. Failure to observe a valid sequence of bus write operations will result in the memory returning to read mode. The long command sequences are imposed to maximize data security.

7.1 Standard commands

See *Table 12: Standard commands (16-bit mode)* for a summary of the standard commands.

7.1.1 Read/Reset command

The device is in read mode after reset or after power-up.

The Read/Reset command returns the memory to read mode. It also resets the errors in the status register. Either one or three bus write operations can be used to issue the Read/Reset command.

The Read/Reset command can be issued, between bus write cycles before the start of a program or erase operation, to return the device to read mode. If the Read/Reset command is issued during the timeout of a block erase operation, the memory will take up to 10 µs to abort. During the abort period no valid data can be read from the memory.

The Read/Reset command will not abort an erase operation when issued while in erase suspend.

7.1.2 Auto Select command

The Auto Select command puts the device in auto select mode (see *Section 4: Auto select mode*). When in auto select mode, the system can read the manufacturer code, the device code, the protection status of each block (block protection status) and the extended memory block protection indicator.

Three consecutive bus write operations are required to issue the Auto Select command. Once the Auto Select command is issued bus read operations to specific addresses output the manufacturer code, the device code, the extended memory block protection indicator and a block protection status (see *Table 12: Standard commands (16-bit mode)* in conjunction with *Table 7: Read electronic signature, auto select mode method (16-bit mode)*, and *Table 9: Block protection (16-bit mode)*). The memory remains in auto select mode until a Read/Reset or CFI Query command is issued.

7.1.3 Read CFI Query command

The memory contains an information area, named CFI data structure, which contains a description of various electrical and timing parameters, density information and functions supported by the memory. See *Appendix B*, *Table 38*, *Table 39*, *Table 40, Table 41, Table 42* and *Table 43* for details on the information contained in the common flash interface (CFI) memory area.

The Read CFI Query command is used to put the memory in read CFI query mode. Once in read CFI query mode, bus read operations to the memory will output data from the common flash interface (CFI) memory area. One bus write cycle is required to issue the Read CFI Query command. This command is valid only when the device is in the read array or auto select mode.

The Read/Reset command must be issued to return the device to the previous mode (the read array mode or auto select mode). A second Read/Reset command is required to put the device in read array mode from auto select mode.

7.1.4 Chip Erase command

The Chip Erase command can be used to erase the entire chip. Six bus write operations are required to issue the Chip Erase command and start the program/erase controller.

If some block are protected, then these are ignored and all the other blocks are erased. If all of the blocks are protected the chip erase operation appears to start but will terminate within about 100 µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the erase operation the memory will ignore all commands, including the Erase Suspend command. It is not possible to issue any command to abort the operation. Typical chip erase times are given in *Table 18*. All bus read operations during the chip erase operation will output the status register on the data inputs/outputs. See *Section 8.2: Status register* for more details.

After the chip erase operation has completed the memory will return to the read mode, unless an error has occurred. When an error occurs the memory will continue to output the status register. A Read/Reset command must be issued to reset the error condition and return to read mode.

The Chip Erase command sets all of the bits in unprotected blocks of the memory to ’1’. All previous data is lost.

The chip erase operation is aborted by performing a reset or powering down the device. In this case, data integrity cannot be ensured, and it is recommended to erase again the entire chip.

7.1.5 Block Erase command

The Block Erase command can be used to erase a list of one or more blocks. It sets all of the bits in the unprotected selected blocks to ’1’. All previous data in the selected blocks is lost.

Six bus write operations are required to select the first block in the list. Each additional block in the list can be selected by repeating the sixth bus write operation using the address of the additional block. After the command sequence is written, a block erase timeout occurs. During the timeout period, additional sector addresses and sector erase commands may be written. Once the program/erase controller has started, it is not possible to select any more

blocks. Each additional block must therefore be selected within the timeout period of the last block. The timeout timer restarts when an additional block is selected. After the sixth bus write operation, a bus read operation outputs the status register (bus reading operations from banks different from those including the blocks being erased, output the memory array content). See *Figure 19: Write enable controlled program waveforms (8-bit mode)* and *Figure 20: Write enable controlled program waveforms (16-bit mode)* for details on how to identify if the program/erase controller has started the block erase operation.

After the block erase operation has completed, the memory returns to the read mode, unless an error has occurred. When an error occurs, bus read operations will continue to output the status register. A Read/Reset command must be issued to reset the error condition and return to read mode.

If any selected blocks are protected then these are ignored and all the other selected blocks are erased. If all of the selected blocks are protected the block erase operation appears to start but will terminate within about 100 µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the block erase operation the memory ignores all commands except the Erase Suspend command and the Read/Reset command which is only accepted during the timeout period. Typical block erase time and block erase timeout are given in *Table 18*.

The block erase operation is aborted by performing a reset or powering down the device. In this case, data integrity cannot be ensured, and it is recommended to erase again the blocks aborted.

7.1.6 Erase Suspend command

The Erase Suspend command can be used to temporarily suspend a block erase operation. One bus write operation is required to issue the command together with the block address.

The program/erase controller suspends the erase operation within the erase suspend latency time of the Erase Suspend command being issued. However, when the Erase Suspend command is written during the block erase timeout, the device immediately terminates the timeout period and suspends the erase operation.

Once the program/erase controller has stopped, the memory operates in read mode and the erase is suspended.

During erase suspend it is possible to read and execute program or write to buffer program operations in blocks that are not suspended; both read and program operations behave as normal on these blocks. Reading from blocks that are suspended will output the status register. If any attempt is made to program in a protected block or in the suspended block then the Program command is ignored and the data remains unchanged. In this case the status register is not read and no error condition is given.

It is also possible to issue the Auto Select (after entering Autoselect mode), Read CFI Query, and Unlock Bypass commands during an erase suspend. The Read/Reset command must be issued to return the device to read array mode before the Resume command will be accepted.

During erase suspend a bus read operation to the extended memory block will output the extended memory block data. Once in the extended block mode, the Exit Extended Block command must be issued before the erase operation can be resumed.

The Erase Suspend command is ignored if written during chip erase operations.

Refer to *Table 18: Program, erase times and program, erase endurance cycles* for the values of block erase timeout and block erase suspend latency time.

If the erase suspend operation is aborted by performing a reset or powering down the device, data integrity cannot be ensured, and it is recommended to erase again the blocks suspended.

7.1.7 Erase Resume command

The Erase Resume command is used to restart the program/erase controller after an erase suspend.

The device must be in read array mode before the Resume command will be accepted. An erase can be suspended and resumed more than once.

7.1.8 Program Suspend command

The Program Suspend command allows the system to interrupt a program operation so that data can be read from any block. When the Program Suspend command is issued during a program operation, the device suspends the program operation within the program suspend latency time (see *Table 18: Program, erase times and program, erase endurance cycles*) and updates the status register bits.

After the program operation has been suspended, the system can read array data from any address. However, data read from program-suspended addresses is not valid.

The Program Suspend command may also be issued during a program operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the extended memory block area (one-time program area), the user must use the proper command sequences to enter and exit this region.

The system may also issue the Auto Select command sequence when the device is in the program suspend mode. The system can read as many auto select codes as required. When the device exits the auto select mode, the device reverts to the program suspend mode, and is ready for another valid operation. See Auto Select command sequence for more information.

If the program suspend operation is aborted by performing a reset or powering down the device, data integrity cannot be ensured, and it is recommended to program again the words or bytes aborted.

7.1.9 Program Resume command

After the Program Resume command is issued, the device reverts to programming. The controller can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. Refer to *Figure 19: Write enable controlled program waveforms (8-bit mode)* and *Figure 20: Write enable controlled program waveforms (16-bit mode)* for details.

The system must issue a Program Resume command, to exit the program suspend mode and to continue the programming operation.

Further issuing of the Resume command is ignored. Another Program Suspend command can be written after the device has resumed programming.

7.1.10 Program command

The Program command can be used to program a value in the memory array one address at a time. The command requires four bus write operations, the final write operation latches the address and data in the internal state machine and starts the program/erase controller.

Programming can be suspended and then resumed by issuing a Program Suspend command and a Program Resume command, respectively. If the address falls in a protected block, the Program command is ignored and the data remains unchanged. The status register is never read and no error condition is given.

After programming has started, bus read operations output the status register content (bus reading operations from banks different from those including the block being programmed, output the memory array content). See *Figure 19: Write enable controlled program waveforms (8-bit mode)* and *Figure 20: Write enable controlled program waveforms (16-bit mode)* for more details. Typical program times are given in *Table 18: Program, erase times and program, erase endurance cycles*.

After the program operation has completed the memory will return to the read mode, unless an error has occurred. When an error occurs, bus read operations to the memory continue to output the status register. A Read/Reset command must be issued to reset the error condition and return to read mode.

One of the erase commands must be used to set all the bits in a block or in the whole memory from ’0’ to ’1’.

The program operation is aborted by performing a reset or powering-down the device. In this case data integrity cannot be ensured, and it is recommended to reprogram the word or byte aborted.

Table 11. Standard commands (8-bit mode)

Command[1]		Length	Bus operations[2]											
			1st		2nd		3rd		4th		5th		6th	
			Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Read/Reset		1	X	F0										
		3	AAA	AA	555	55	X	F0						
Auto Select	Manufacturer code	3	AAA	AA	555	55	(BKA) AAA	90	(3)(4)	(3)(4)				
	Device code													
	Extended memory block protection indicator													
	Block protection status													
Program[5]		4	AAA	AA	555	55	AAA	A0	PA	PD				
Chip Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Block Erase		6+	AAA	AA	555	55	AAA	80	AAA	AA	555	55	BAd	30
Erase/Program Suspend		1	BKA	B0										
Erase/Program Resume		1	BKA	30										
Read CFI Query		1	BKA AAA	98										

1. The device doesn't tolerate FFh as a valid command, and once FFh is issued to the device, the M29DW127G will enter unexpected state. Adding a F0h command systematically after FFh command is necessary.
2. X don't care, PA program address, PD program data, BAd any address in block, BKA bank address, values hexadecimal.
3. These cells represent read cycles. All the other cells are write cycles.
4. The auto select addresses and data are given in *Table 7: Read electronic signature, auto select mode method (16-bit mode)*, and *Table 9: Block protection (16-bit mode)*, except for A9 that is 'don't care'.
5. In unlock bypass, the first two unlock cycles are no more needed (see *Table 14: Fast program commands (16-bit mode)*).

Table 12. Standard commands (16-bit mode)

Command[1]		Length	Bus operations[2]											
			1st		2nd		3rd		4th		5th		6th	
			Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Read/Reset		1	X	F0										
		3	555	AA	2AA	55	X	F0						
Auto Select	Manufacturer code	3	555	AA	2AA	55	(BKA) 555	90	(3)(4)	(3)(4)				
	Device code													
	Extended memory block protection indicator													
	Block protection status													
Program[5]		4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Block Erase		6+	555	AA	2AA	55	555	80	555	AA	2AA	55	BAd	30
Erase/Program Suspend		1	BKA	B0										
Erase/Program Resume		1	BKA	30										
Read CFI Query		1	BKA (555)	98										

1. The device doesn't tolerate FFh as a valid command, and once FFh is issued to the device, the M29DW127G will enter unexpected state. Adding a F0h command systematically after FFh command is necessary.
2. X don't care, PA program address, PD program data, BAd any address in block, BKA bank address, values hexadecimal.
3. These cells represent read cycles. All the other cells are write cycles.
4. The auto select addresses and data are given in *Table 7: Read electronic signature, auto select mode method (16-bit mode)*, and *Table 9: Block protection (16-bit mode)*, except for A9 that is 'don't care'.
5. In unlock bypass, the first two unlock cycles are no more needed (see *Table 14: Fast program commands (16-bit mode)*).

7.2 Fast program commands

The M29DW127G offers a set of fast program commands to improve the programming throughput:

- Write to Buffer Program
- Enhanced Buffered Program
- Unlock Bypass.

See *Table 14: Fast program commands (16-bit mode)* for a summary of the fast program commands.

When V_{PPH} is applied to the V_{PP}/write protect pin the memory automatically enters unlock bypass mode (see *Section 7.2.6: Unlock Bypass command*).

After programming has started, bus read operations in the memory output the status register content (bus reading operations from banks different from those including the block being programmed, output the memory array content). Write to Buffer Program command can be

suspended and then resumed by issuing a Program Suspend command and a Program Resume command, respectively (see *Section 7.1.8: Program Suspend command* and *Section 7.1.9: Program Resume command*).

After the fast program operation has completed, the memory will return to the read mode, unless an error has occurred. When an error occurs bus read operations to the memory will continue to output the status register. A Read/Reset command must be issued to reset the error condition and return to read mode. One of the erase commands must be used to set all the bits in a block or in the whole memory from ’0’ to ’1’.

Typical program times are given in *Table 18: Program, erase times and program, erase endurance cycles*.

7.2.1 Write to Buffer Program command

The Write to Buffer Program command makes use of the device’s 32-word / 64 byte write buffer to speed up programming. 32 words / 64 bytes can be loaded into the write buffer. Each write buffer has the same A22-A5 addresses.The Write to Buffer Program command dramatically reduces system programming time compared to the standard non-buffered Program command.

When issuing a Write to Buffer Program command, the $V_{PP}/\overline{WP}$ pin can be either held High, V_{IH}, or raised to V_{PPH}.

See *Table 18* for details on typical write to buffer program times in both cases.

The following successive steps are required to issue the Write to Buffer Program command:

1. The Write to Buffer Program command starts with two unlock cycles
2. The third bus write cycle sets up the Write to Buffer Program command. The setup code can be addressed to any location within the targeted block
3. The fourth bus write cycle sets up the number of words/bytes to be programmed. Value N is written to the same block address, where N+1 is the number of words/bytes to be programmed. N+1 must not exceed the size of the write buffer or the operation will abort
4. The fifth cycle loads the first address and data to be programmed
5. Use N bus write cycles to load the address and data for each word/byte into the write buffer. Addresses must lie within the range from the start address+1 to the start address + N-1.

All the addresses used in the write to buffer program operation must lie within the same page.

To program the content of the write buffer, this command must be followed by a Write to Buffer Program Confirm command.

If an address is written several times during a write to buffer program operation, the address/data counter will be decremented at each data load operation and the data will be programmed to the last word loaded into the buffer.

Invalid address combinations or failing to follow the correct sequence of bus write cycles will abort the Write to Buffer Program.

The status register bits DQ1, DQ5, DQ6, DQ7 can be used to monitor the device status during a write to buffer program operation.

It is possible to detect program operation fails when changing programmed data from ‘0’ to ‘1’, that is when reprogramming data in a portion of memory already programmed.

See *Appendix D*, *Figure 29: Write to buffer program flowchart and pseudocode*, for a suggested flowchart on using the Write to Buffer Program command.

7.2.2 Enhanced Buffered Program command

The Enhanced Buffered Program command makes use of the device's 256-word write buffer to speed up programming. 256 words can be loaded into the write buffer. Each write buffer has the same A22-A8 addresses. The Enhanced Buffered Program command dramatically reduces system programming time compared to both the standard non-buffered Program command and the Write to Buffer command.

When issuing an Enhanced Buffered Program command, the $V_{PP}/\overline{WP}$ pin can be either held High, V_{IH}, or raised to V_{PPH}.

See *Table 18: Program, erase times and program, erase endurance cycles* for details on typical enhanced buffered program times in both cases.

Three successive steps are required to issue the Enhanced Buffered Program command:

- The Enhanced Buffered Program command starts with two unlock cycles
- The third bus write cycle sets up the Enhanced Buffered Program command. The setup code can be addressed to any location within the targeted block
- The fourth bus write cycle loads the first address and data to be programmed. There a total of 256 address and data loading cycles.

To program the content of the write buffer, the Enhanced Buffered Program command must be followed by an Enhanced Buffered Program Confirm command. The command ends with an internal enhanced buffered program confirm cycle.

Note that address/data cycles must be loaded in an increasing address order (from ADD[7:0]=00000000 to ADD[7:0]=11111111) and completely (all 256 words). Invalid address combinations or failing to follow the correct sequence of bus write cycles will abort the enhanced buffered program.

The status register bits DQ1, DQ5, DQ6, and DQ7 can be used to monitor the device status during an enhanced buffered program operation.

An external supply (12 V) can be used to improve programming efficiency.

It is possible to detect program operation fails when changing programmed data from '0' to '1', that is when reprogramming data in a portion of memory already programmed. The resulting data will be the logical OR between the previous and the current value.

See *Appendix D* and *Figure 30: Enhanced buffered program flowchart and pseudocode*, for a suggested flowchart on using the Enhanced Buffered Program command.

7.2.3 Buffered Program Abort and Reset command

A Buffered Program Abort and Reset command must be issued to abort the write to buffer program and enhanced buffered program operation and reset the device in read mode.

The write to buffer and enhanced buffered programming sequence can be aborted in the following ways:

- Load a value that is greater than the page buffer size during the number of locations to program step in the Write to Buffer Program command
- Write to an address in a block different than the one specified during the write-buffer-load command
- Write an address/data pair to a different write-buffer-page than the one selected by the starting address during the write buffer data loading stage of the operation
- Write data other than the Confirm command after the specified number of data load cycles
- Load address/data pairs in an incorrect sequence during the enhanced buffered program.

The abort condition is indicated by DQ1 = 1, DQ7 = $\overline{DQ7}$ (for the last address location loaded), DQ6 = toggle, and DQ5 = 0 (all of which are status register bits). A Buffered Program Abort and Reset command sequence must be written to reset the device for the next operation. Note that the full 3-cycle Buffered Program Abort and Reset command sequence is required when using write to buffer and enhanced buffered programming features in unlock bypass mode.

7.2.4 Write to Buffer Program Confirm command

The Write to Buffer Program Confirm command is used to confirm a Write to Buffer Program command and to program the N+1 words/bytes loaded in the write buffer by this command.

7.2.5 Enhanced Buffered Program Confirm command

The Enhanced Buffered Program Confirm command is used to confirm an Enhanced Buffered Program command and to program the 256 words loaded in the buffer.

7.2.6 Unlock Bypass command

The Unlock Bypass command is used to place the device in unlock bypass mode. When the device enters the unlock bypass mode, the two initial unlock cycles required in the standard program command sequence are no more needed, and only two write cycles are required to program data, instead of the normal four cycles (see *Note 5* below *Table 12: Standard commands (16-bit mode)*). This results in a faster total programming time.

Unlock Bypass command is consequently used in conjunction with the Unlock Bypass Program command to program the memory faster than with the standard program commands. When the cycle time to the device is long, considerable time saving can be made by using these commands. Three bus write operations are required to issue the Unlock Bypass command.

When in unlock bypass mode, only the following commands are valid:

- The Unlock Bypass Program command can be issued to program addresses within the memory
- The Unlock Bypass Block Erase command can then be issued to erase one or more memory blocks
- The Unlock Bypass Chip Erase command can be issued to erase the whole memory array
- The Unlock Bypass Write to Buffer Program command can be issued to speed up programming operation
- The Unlock Bypass Enhanced Buffered Program command can be issued to speed up programming operation
- The Unlock Bypass CFI command can be issued to read the CFI when the memory is in the unlock bypass mode
- The Unlock Bypass Reset command can be issued to return the memory to read mode.

In unlock bypass mode the memory can be read as if in read mode.

7.2.7 Unlock Bypass Program command

The Unlock Bypass Program command can be used to program one address in the memory array at a time. The command requires two bus write operations, the final write operation latches the address and data and starts the program/erase controller.

The program operation using the Unlock Bypass Program command behaves identically to the program operation using the Program command. The operation cannot be aborted, a bus read operation to the memory outputs the status register (bus reading operations from a bank different from the one including the block being programmed, output the memory array content). See the Program command for details on the behavior.

7.2.8 Unlock Bypass Block Erase command

The Unlock Bypass Block Erase command can be used to erase one or more memory blocks at a time. The command requires two bus write operations instead of six using the standard Block Erase command. The final bus write operation latches the address of the block and starts the program/erase controller.

To erase multiple block (after the first two bus write operations have selected the first block in the list), each additional block in the list can be selected by repeating the second bus write operation using the address of the additional block.

The Unlock Bypass Block Erase command behaves in the same way as the Block Erase command: the operation cannot be aborted, and a bus read operation to the memory outputs the status register (bus reading operations from banks different from those including the blocks being erased, output the memory array content). See *Section 7.1.5: Block Erase command* for details.

7.2.9 Unlock Bypass Chip Erase command

The Unlock Bypass Chip Erase command can be used to erase all memory blocks at a time. The command requires two bus write operations only instead of six using the standard Chip Erase command. The final bus write operation starts the program/erase controller.

The Unlock Bypass Chip Erase command behaves in the same way as the Chip Erase command: the operation cannot be aborted, and a bus read operation to the memory outputs the status register (see *Section 7.1.4: Chip Erase command* for details).

7.2.10 Unlock Bypass Write to Buffer Program command

The Unlock Bypass Write to Buffer command can be used to program the memory in fast program mode. The command requires two bus write operations less than the standard Write to Buffer Program command.

The Unlock Bypass Write to Buffer Program command behaves in the same way as the Write to Buffer Program command: the operation cannot be aborted and a bus read operation to the memory outputs the status register (bus reading operations from a bank different from the one including the block being programmed, output the memory array content). See *Section 7.2.1: Write to Buffer Program command* for details.

The Write to Buffer Program Confirm command is used to confirm an Unlock Bypass Write to Buffer Program command and to program the N+1 words/bytes loaded in the write buffer by this command.

7.2.11 Unlock Bypass Enhanced Buffered Program command

The Unlock Bypass Enhanced Buffered Program command can be used to program the memory in fast program mode. The command requires two address/data loading cycles less than the standard Enhanced Buffered Program command (see *Table 15: Enhanced buffered program commands*).

The Unlock Bypass Enhanced Buffered Program command behaves identically to the enhanced buffered program operation using the Enhanced Buffered Program command. The operation cannot be aborted and a bus read operation to the memory outputs the status register (bus reading operations from a bank different from the one including the block being programmed, output the memory array content). See *Section 7.2.2: Enhanced Buffered Program command* for details on the behavior.

The Enhanced Buffered Program Confirm command is used to confirm an Unlock Bypass Enhanced Buffered Program command and to program the 256 words loaded in the buffer.

7.2.12 Unlock Bypass CFI command

The Unlock Bypass CFI command allows to use any address in the bank to perform a CFI query when the memory is in the unlock bypass mode.

7.2.13 Unlock Bypass Reset command

The Unlock Bypass Reset command can be used to return to read/reset mode from unlock bypass mode. Two bus write operations are required to issue the Unlock Bypass Reset command. Read/Reset command does not exit from unlock bypass mode.

Table 13. Fast program commands (8-bit mode)

Command	Length	Bus write operations[1]											
		1st		2nd		3rd		4th		5th		6th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Write to Buffer Program	N+5	AAA	AA	555	55	BAd	25	BAd	N[2]	PA[3]	PD	WBL[4]	PD
Write to Buffer Program Confirm	1	BAd[5]	29										
Buffered Program Abort and Reset	3	AAA	AA	555	55	AAA	F0						
Unlock Bypass	3	AAA	AA	555	55	AAA	20						
Unlock Bypass Program	2	X	A0	PA	PD								
Unlock Bypass Block Erase	2+	X	80	BAd	30								
Unlock Bypass Chip Erase	2	X	80	X	10								
Unlock Bypass Write to Buffer Program	N+3	BAd	25	BAd	N[2]	PA[3]	PD	WBL[4]	PD				
Unlock Bypass CFI	1	BKA	98										
Unlock Bypass Reset	2	X	90	X	00								

1. X don't care, PA program address, PD program data, BAd any address in the block, BKA bank address, WBL write buffer location. All values in the table are in hexadecimal.
2. The maximum number of cycles in the command sequence is 36. N+1 is the number of words to be programmed during the write to buffer program operation.
3. Each buffer has the same A22-A5 addresses. A0-A4 are used to select a word within the N+1 word page.
4. The 6th cycle has to be issued N time. WBL scans the word inside the page.
5. BAd must be identical to the address loaded during the write to buffer program 3rd and 4th cycles.

Table 14. Fast program commands (16-bit mode)

Command	Length	Bus write operations[1]											
		1st		2nd		3rd		4th		5th		6th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Write to Buffer Program	N+5	555	AA	2AA	55	BAd	25	BAd	N[2]	PA[3]	PD	WBL[4]	PD
Write to Buffer Program Confirm	1	BAd[5]	29										
Buffered Program Abort and Reset	3	555	AA	2AA	55	555	F0						
Unlock Bypass	3	555	AA	2AA	55	555	20						

Table 14. Fast program commands (16-bit mode)

Command	Length	Bus write operations[1]											
		1st		2nd		3rd		4th		5th		6th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Unlock Bypass Program	2	X	A0	PA	PD								
Unlock Bypass Block Erase	2+	X	80	BAd	30								
Unlock Bypass Chip Erase	2	X	80	X	10								
Unlock Bypass Write to Buffer Program	N+3	BAd	25	BAd	N[2]	PA (3)	PD	WBL (4)	PD				
Unlock Bypass CFI	1	BKA	98										
Unlock Bypass Reset	2	X	90	X	00								

1. X don't care, PA program address, PD program data, BAd any address in the block, BKA bank address, WBL write buffer location. All values in the table are in hexadecimal.
2. The maximum number of cycles in the command sequence is 36. N+1 is the number of words to be programmed during the write to buffer program operation.
3. Each buffer has the same A22-A5 addresses. A0-A4 are used to select a word within the N+1 word page.
4. The 6th cycle has to be issued N time. WBL scans the word inside the page.
5. BAd must be identical to the address loaded during the write to buffer program 3rd and 4th cycles.

Table 15. Enhanced buffered program commands[1][2]

Command	Length	Bus write operations																	
		1st		2nd		3rd		4th		...		257th		258th		259th		260th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Enhanced Buffered Program	259	555	AA	2AA	55	BAd	33	BAd (00)	Data	...	...					BAd (FF)	Data		
Enhanced Buffered Program Confirm	1	BAd (00)	29																
Unlock Bypass Enhanced Buffered Program	257	BAd	33	BAd (00)	Data							BAd (FF)	Data						

1. Only available from week 8 of 2008.
2. BAd any address in the block.

7.3 Protection commands

Blocks can be protected individually against accidental program, erase or read operations. The device block protection scheme is shown in *Figure 6: Software protection scheme*. See *Table 17: Block protection commands (16-bit mode)* for a summary of the block protection commands.

The memory block and extended memory block protection is configured through the Lock register (see *Section 8.1: Lock register*).

7.3.1 Enter Extended Memory Block command

The M29DW127G has one extra 256-word block (extended memory block) that can only be accessed using the Enter Extended Memory Block command.

The extended memory block is divided in two memory areas of 128 words each: the first one is factory locked and the second one is customer lockable.

Three Bus Write cycles are required to issue the Extended Memory Block command. Once the command has been issued the device enters the extended memory block mode where all bus read or program operations are conducted on the extended memory block. Once the device is in the extended block mode, the extended memory block is addressed by using the addresses occupied by the first boot block in the other operating modes (see *Table 37: Block addresses*).

The device remains in extended memory block mode until the Exit Extended Memory Block command is issued or power is removed from the device. After power-up or hardware reset, the device reverts to read mode where the commands issued to the first boot block address space will address the first boot block.

The extended memory block cannot be erased, and can be treated as one-time programmable (OTP) memory.

In extended block mode only array cell locations (bank A) with the same addresses as the extended block are not accessible. In extended block mode dual operations are allowed and the extended block physically belongs to bank A. In extended block mode, Erase, Chip Erase, Erase Suspend and Erase Resume commands are not allowed.

To exit from the extended memory block mode the Exit Extended Memory Block command must be issued.

The extended memory block can be protected by setting the extended memory block protection bit to ‘1’ (see *Section 8.1: Lock register*); however once protected the protection cannot be undone.

Note: When the device is in the extended memory block mode, the $V_{PP}/\overline{WP}$ pin cannot be used for fast programming and the unlock bypass mode is not available (see Section 2.8: VPP/write protect (VPP/WP)).

7.3.2 Exit Extended Memory Block command

The Exit Extended Memory Block command is used to exit from the extended memory block mode and return the device to read mode. Four bus write operations are required to issue the command.

7.3.3 Lock register command set

The M29DW127G offers a set of commands to access the lock register and to configure and verify its content. See the following sections in conjunction with *Section 8.1: Lock register* and *Table 17: Block protection commands (16-bit mode)*.

Enter Lock Register Command Set command

Three bus write cycles are required to issue the Enter Lock Register Command set command. Once the command has been issued, all bus read or program operations are issued to the lock register.

Lock Register Program and Lock Register Read command

The Lock Register Program command allows to configure the lock register. The programmed data can then be checked by issuing a Lock Register Read command.

An Exit Protection Command set command must then be issued to return the device to read mode (see *Section 7.3.8: Exit protection command set command*).

7.3.4 Password protection mode command set

Enter Password Protection Command Set command

Three bus write cycles are required to issue the Enter Password Protection Command Set command. Once the command has been issued, the commands related to the password protection mode can be issued to the device.

Password Program command

The Password Program command is used to program the 64-bit password used in the password protection mode.

To program the 64-bit password, the complete command sequence must be entered four times at four consecutive addresses selected by A1-A0.

The password can be checked by issuing a Password Read command.

Once password program operation has completed, an Exit Protection Command Set command must be issued to return the device to read mode. The password protection mode can then be selected.

By default, all password bits are set to ‘1’.

Password Read command

The Password Read command is used to verify the password used in password protection mode.

To verify the 64-bit password, the complete command sequence must be entered four times at four consecutive addresses selected by A1-A0.

If the password mode lock bit is programmed and the user attempts to read the password, the device will output FFh onto the I/O data bus.

An Exit Protection Command Set command must be issued to return the device to read mode.

Password Unlock command

The Password Unlock command is used to clear the NVPB lock bit allowing to modify the NVPBs.

The Password Unlock command must be issued along with the correct password.

There must be a 1 µs delay between successive password unlock commands in order to prevent hackers from cracking the password by trying all possible 64-bit combinations. If this delay is not respected, the latest command will be ignored.

Approximately 1 µs is required for unlocking the device after the valid 64-bit password has been provided.

7.3.5 Non-volatile protection mode command set

Enter Non-volatile Protection Command Set command

Three bus write cycles are required to issue the Enter Non-volatile Protection Command Set command. Once the command has been issued, the commands related to the non-volatile protection mode can be issued to the device.

Non-volatile Protection Bit Program command (NVPB Program)

A block can be protected from program or erase by issuing a Non-volatile Protection Bit command along with the block address. This command sets the NVPB to ‘1’ for a given block.

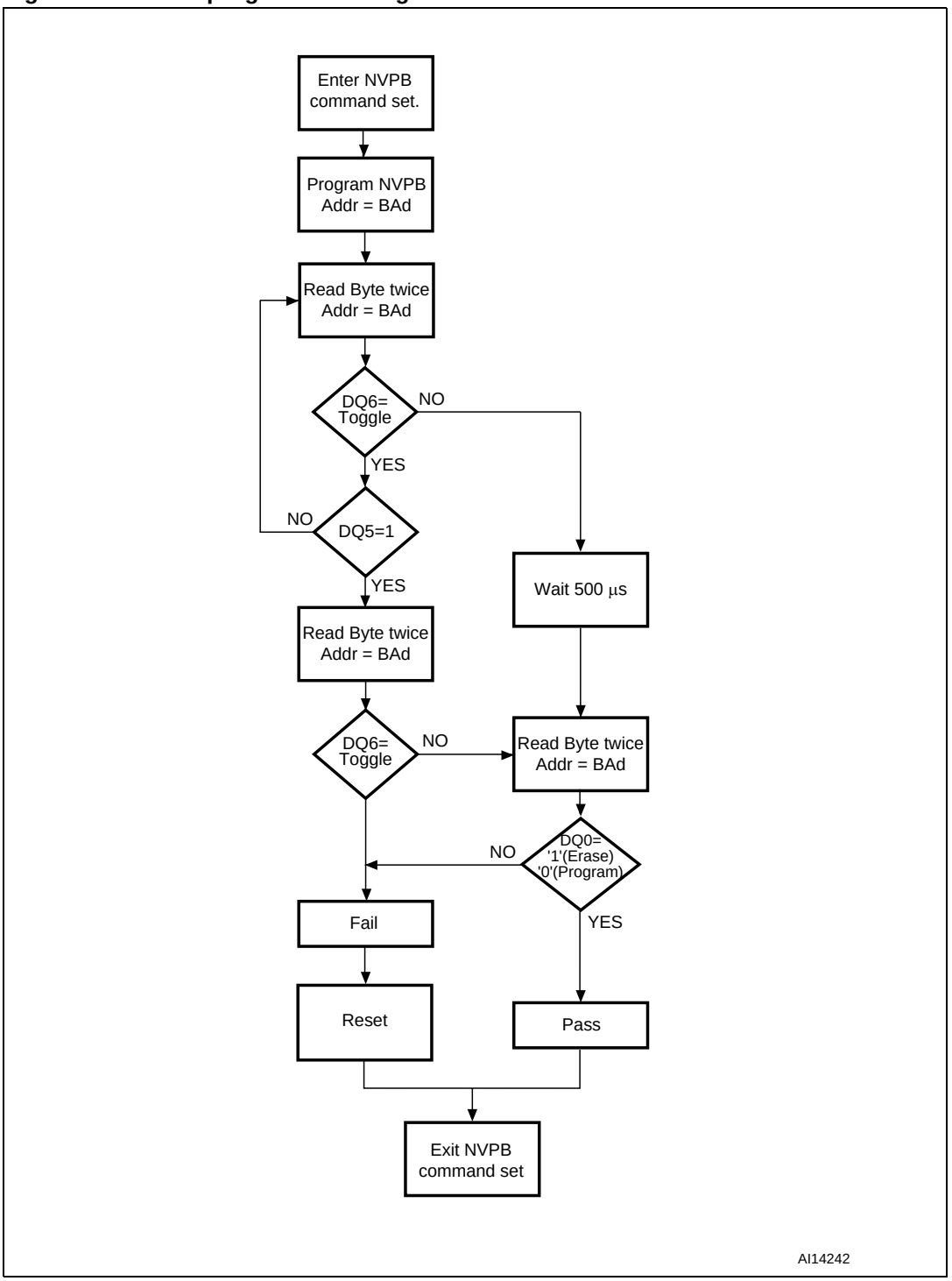
Read Non-volatile Protection Bit Status command (Read NVPB Status)

The status of a NVPB for a given block or group of blocks can be read by issuing a Read Non-Volatile Modify Protection Bit command along with the block address.

Clear all Non-volatile Protection Bits command (Clear all NVPBs)

The NVPBs are erased simultaneously by issuing a Clear all Non-volatile Protection Bits command. No specific block address is required. If the NVPB lock bit is set to ‘0’, the command fails.

Figure 7. NVPB program/erase algorithm



7.3.6 NVPB lock bit command set

Enter NVPB Lock Bit Command Set command

Three bus write cycles are required to issue the Enter NVPB Lock Bit Command Set command. Once the command has been issued, the commands allowing to set the NVPB lock bit can be issued to the device.

NVPB Lock Bit Program command

This command is used to set the NVPB Lock bit to ‘0’ thus locking the NVPBs, and preventing them from being modified.

Read NVPB Lock Bit Status command

This command is used to read the status of the NVPB lock bit.

7.3.7 Volatile protection mode command set

Enter Volatile Protection Command Set command

Three bus write cycles are required to issue the Enter Volatile Protection Command Set command. Once the command has been issued, the commands related to the volatile protection mode can be issued to the device.

Volatile Protection Bit Program command (VPB Program)

The VPB Program command individually sets a VPB to ‘0’ for a given block.

If the NVPB for the same block is set, the block is locked regardless of the value of the VPB bit (see *Table 20: Block protection status*).

Read VPB Status command

The status of a VPB for a given block can be read by issuing a Read VPB Status command along with the block address.

VPB Clear command

The VPB Clear command individually clears (sets to ‘1’) the VPB for a given block.

If the NVPB for the same block is set, the block is locked regardless of the value of the VPB bit. (see *Table 20: Block protection status*).

7.3.8 Exit protection command set command

The Exit Protection Command Set command is used to exit from the Lock register, password protection, non-volatile protection, volatile protection, and NVPB lock bit command set mode. It returns the device to read mode.

Table 16. Block protection commands (8-bit mode)(1)(2)(3)

	Command	Length	Bus operations													
			1st		2nd		3rd		4th		5th		6th		7th	
			Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data
Lock register	Enter Lock Register Command Set(4)	3	AAA	AA	555	55	AAA	40								
	Lock Register Program	2	X	A0	00	DATA(5)										
	Lock Register Read	1	X	DATA(5)												
Password protection	Enter Password Protection Command Set(4)	3	AAA	AA	555	55	AAA	60								
	Password Program (6)(7)	2	X	A0	PWAn	PWDn										
	Password Read	4	00	PWD0	01	PWD1	02	PWD2	03	PWD3						
	Password Unlock(7)	7	00	25	00	03	00	PWD0	01	PWD1	02	PWD2	03	PWD3	00	29
Non-volatile protection	Enter Non-volatile Protection Command Set(4)	3	AAA	AA	555	55	(BKA) AAA	C0								
	NVPB Program(8)	2	X	A0	(BKA) BAd	00										
	Clear all NVPBs(9)	2	X	80	00	30										
	Read NVPB Status	1	(BKA) BAd	RD(0)												
NVPB lock bit	Enter NVPB Lock Bit Command Set	3	AAA	AA	555	55	AAA	50								
	NVPB Lock Bit Program	2	X	A0	X	00										
	Read NVPB Lock Bit Status	1	BKA	RD(0)												
Volatile protection	Enter Volatile Protection Command Set	3	AAA	AA	555	55	(BKA) AAA	E0								
	VPB Program	2	X	A0	(BKA) BAd	00										
	Read VPB Status	1	(BKA) BAd	RD(0)												
	VPB Clear	2	X	A0	(BKA) BAd	01										
Extended block sector	Enter Extended Block	3	AAA	AA	555	55	AAA	88								
	Extended Block Program(4)	2	X	A0	PA	DATA(5)										
	Extended Block Read(4)	1	Ad	DATA(5)												
	Exit Extended Block	4	AAA	AA	555	55	AAA	90	X	00						
Exit Protection Command Set(10)		2	X	90	X	00										

1. PA program address, Ad address, BAd any address in the block, BKA bank address, RD read data, PWDn password word (n = 0 to 3), PWAn password address (n = 0 to 3), X don't care. All values in the table are in hexadecimal.
2. Grey cells represent read cycles. The other cells are write cycles.
3. DQ15 to DQ8 are 'don't care' during unlock and command cycles. A22 to A16 are 'don't care' during unlock and command cycles unless an address is required.
4. An enter command sequence must be issued prior to any operation. It disables read and write operations from and to block 0. Read and write operations from any other block are allowed.
5. DATA = Extended block content.
6. Only one portion of password can be programmed or read by each Password Program command.
7. The password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.
8. Protected and unprotected states correspond to 00 and 01, respectively.
9. The Clear all NVPBs command programs all NVPBs before erasure in order to prevent the over-erasure of previously cleared non-volatile modify protection bits.
10. If an Entry Command Set command is issued, an Exit Protection Command Set command must be issued to return the device to read mode.

Table 17. Block protection commands (16-bit mode)(1)(2)(3)

	Command	Length	Bus operations													
			1st		2nd		3rd		4th		5th		6th		7th	
			Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data
Lock register	Enter Lock Register Command Set(4)	3	555	AA	2AA	55	555	40								
	Lock Register Program	2	X	A0	00	DATA(5)										
	Lock Register Read	1	X	DATA(5)												
Password protection	Enter Password Protection Command Set(4)	3	555	AA	2AA	55	555	60								
	Password Program (6)(7)	2	X	A0	PWAn	PWDn										
	Password Read	4	00	PWD0	01	PWD1	02	PWD2	03	PWD3						
	Password Unlock(7)	7	00	25	00	03	00	PWD0	01	PWD1	02	PWD2	03	PWD3	00	29
Non-volatile protection	Enter Non-volatile Protection Command Set(4)	3	555	AA	2AA	55	(BKA) 555	C0								
	NVPB Program(8)	2	X	A0	(BKA) BAd	00										
	Clear all NVPBs(9)	2	X	80	00	30										
	Read NVPB Status	1	(BKA) BAd	RD(0)												
NVPB lock bit	Enter NVPB Lock Bit Command Set	3	555	AA	2AA	55	555	50								
	NVPB Lock Bit Program	2	X	A0	X	00										
	Read NVPB Lock Bit Status	1	BKA	RD(0)												
Volatile protection	Enter Volatile Protection Command Set	3	555	AA	2AA	55	(BKA) 555	E0								
	VPB Program	2	X	A0	(BKA) BAd	00										
	Read VPB Status	1	(BKA) BAd	RD(0)												
	VPB Clear	2	X	A0	(BKA) BAd	01										
Extended block sector	Enter Extended Block	3	555	AA	2AA	55	555	88								
	Extended Block Program(4)	2	X	A0	PA	DATA(5)										
	Extended Block Read(4)	1	Ad	DATA(5)												
	Exit Extended Block	4	555	AA	2AA	55	555	90	X	00						
Exit Protection Command Set(10)		2	X	90	X	00										

1. PA program address, Ad address, BAd any address in the block, BKA bank address, RD read data, PWDn password word (n = 0 to 3), PWAn password address (n = 0 to 3), X don't care. All values in the table are in hexadecimal.
2. Grey cells represent read cycles. The other cells are write cycles.
3. DQ15 to DQ8 are 'don't care' during unlock and command cycles. A22 to A16 are 'don't care' during unlock and command cycles unless an address is required.
4. An enter command sequence must be issued prior to any operation. It disables read and write operations from and to block 0. Read and write operations from any other block are allowed.
5. DATA = Extended block content.
6. Only one portion of password can be programmed or read by each Password Program command.
7. The password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.
8. Protected and unprotected states correspond to 00 and 01, respectively.
9. The Clear all NVPBs command programs all NVPBs before erasure in order to prevent the over-erasure of previously cleared non-volatile modify protection bits.
10. If an Entry Command Set command is issued, an Exit Protection Command Set command must be issued to return the device to read mode.

Table 18. Program, erase times and program, erase endurance cycles

Parameter			Min	Typ(1)(2)	Max(2)	Unit
Chip Erase				40	400(3)	s
Block Erase (128 Kwords/256 Kbytes)(4)				1		s
Erase Suspend latency time				25	35	µs
Block Erase timeout			50			µs
Byte Program	Single Byte Program			16	200(3)	µs
	Write to Buffer Program (64 bytes at-a-time)	$V_{PP}/\overline{WP} = V_{PPH}$		51		µs
		$V_{PP}/\overline{WP} = V_{IH}$		78		
Word Program	Single Word Program			16	200(3)	µs
	Write to Buffer Program (32 words at-a-time)	$V_{PP}/\overline{WP} = V_{PPH}$		51		µs
		$V_{PP}/\overline{WP} = V_{IH}$		78		
Chip Program (byte by byte)				270	800(3)	s
Chip Program (word by word)				135	400(3)	s
Chip Program (Write to Buffer Program)(5)				20	200(3)	s
Chip Program (Write to Buffer Program with $V_{PP}/\overline{WP} = V_{PPH}$)(5)				13	50(3)	s
Chip Program (Enhanced Buffered Program)(5)				8	40	s
Chip Program (Enhanced Buffered Program with $V_{PP}/\overline{WP} = V_{PP}$)(5)				5	25	s
Program Suspend latency time				5	15	µs
Program/Erase cycles (per block)			100,000			Cycles
Data retention			20			Years

1. Typical values measured at room temperature and nominal voltages and for not cycled devices.
2. Sampled, but not 100% tested.
3. Maximum value measured at worst case conditions for both temperature and V_{CC} after 100,000 program/erase cycles.
4. Block Erase polling cycle time (see *Figure 26: Data polling AC waveforms*).
5. Intrinsic program timing, that means without the time required to execute the bus cycles to load the program commands.

8 Registers

The device feature two registers:

- A lock register that allows to configure the memory blocks and extended memory block protection (see *Table 20: Block protection status*)
- A status register that provides information on the current or previous program or erase operations.

8.1 Lock register

The lock register is a 16-bit one-time programmable register. The bits in the lock register are summarized in *Table 19: Lock register bits*.
See *Section 7.3.3: Lock register command set* for a description of the commands allowing to read and program the lock register.

8.1.1 Volatile lock boot bit (DQ4)

DQ4 sets the default values for volatile block protection: when programmed, the blocks are protected at power-up.

8.1.2 Password protection mode lock bit (DQ2)

The password protection mode lock bit, DQ2, is one-time programmable. Programming (setting to ‘0’) this bit permanently places the device in password protection mode.

Any attempt to program the password protection mode lock bit when the non-volatile protection mode bit is programmed causes the operation to abort and the device to return to read mode.

8.1.3 Non-volatile protection mode lock bit (DQ1)

The non-volatile protection mode lock bit, DQ1, is one-time programmable. Programming (setting to ‘0’) this bit permanently places the device in non-volatile protection mode.

When shipped from the factory, all parts default to operate in non-volatile protection mode. The memory blocks can be either unprotected (NVPBs set to ‘1’) or protected (NVPBs set to ‘0’), according to the ordering option that has been chosen.

Any attempt to program the non-volatile protection mode lock bit when the password protection mode bit is programmed causes the operation to abort and the device to return to read mode.

8.1.4 Extended block protection bit (DQ0)

If the device has not been shipped with the extended memory block factory locked, the block can be protected by setting the extended memory block protection bit, DQ0, to ‘0’. However, this bit is one-time programmable and once protected the extended memory block cannot be unprotected.

The extended memory block protection status can be read in auto select mode by issuing an Auto Select command (see *Table 12: Standard commands (16-bit mode)*).

8.1.5 DQ15 to DQ5 and DQ3 reserved

They are ‘don’t care’.

Table 19. Lock register bits(1)

DQ15-5	DQ4	DQ3	DQ2	DQ1	DQ0
Don’t care	Volatile lock boot bit	Don’t care	Password protection mode lock bit	Non-volatile protection mode lock bit	Extended block protection bit

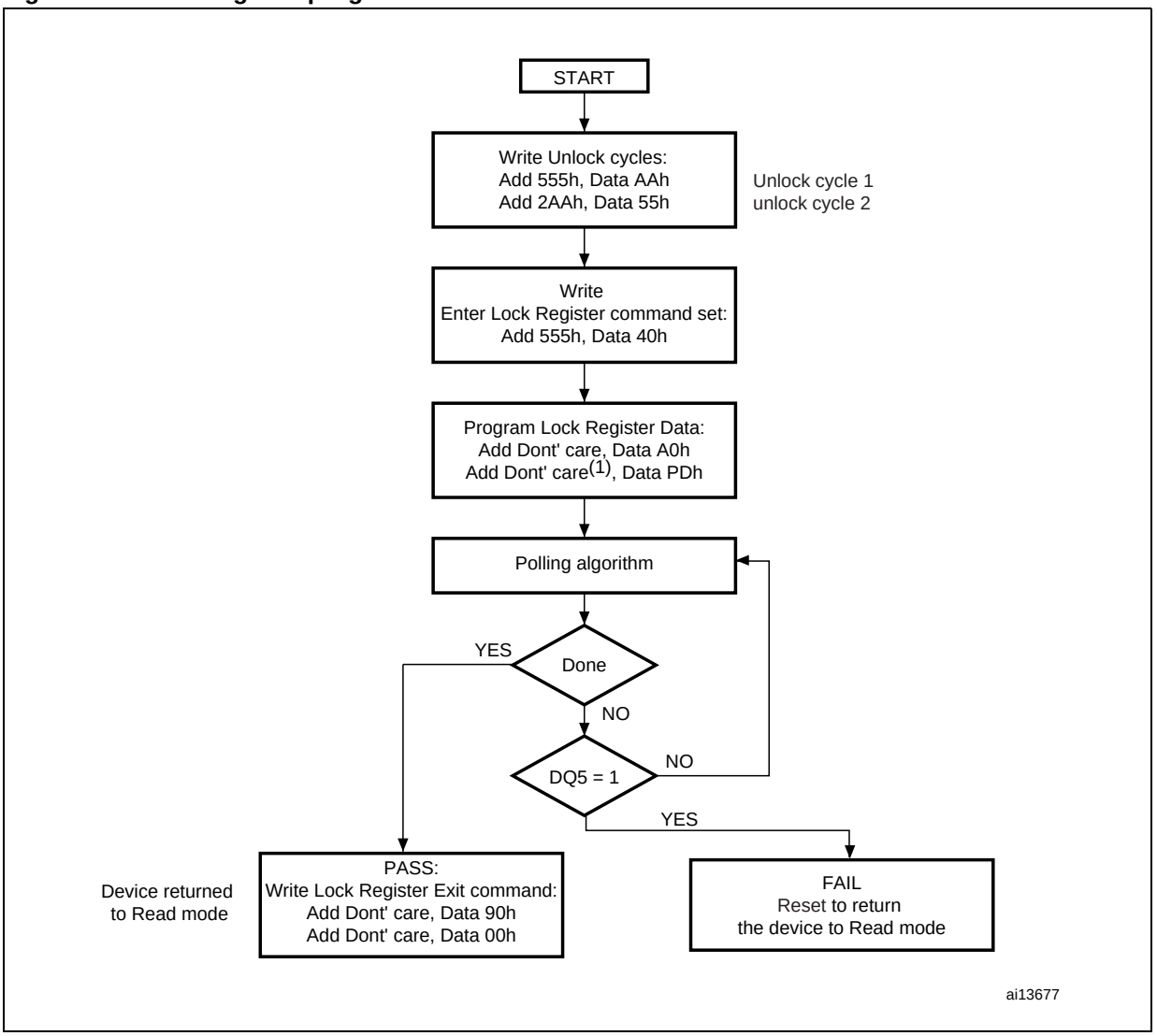
1. DQ0, DQ1, DQ2 and DQ4 are set to ‘1’ when shipped from the factory.

Table 20. Block protection status

NVPB lock bit(1)	Block NVPB(2)	Block VPB(3)	Block protection status	Block protection status
0	0	x	01h	Block protected (non-volatile protection through NVPB)
0	1	1	00h	Block unprotected
0	1	0	00h	Block protected (volatile protection through VPB)
1	0	x	01h	Block protected (non-volatile protection through NVPB)
1	1	0	01h	Block protected (volatile protection through VPB)
1	1	1	00h	Block unprotected

1. If the NVPB lock bit is set to ‘0’, all NVPBs are locked. If the NVPB lock bit is set to ‘1’, all NVPBs are unlocked.
2. If the block NVPB is set to ‘0’, the block is protected, if set to ‘1’, it is unprotected.
3. If the block VPB is set to ‘0’, the block is protected, if set to ‘1’, it is unprotected.

Figure 8. Lock register program flowchart



1. PD is the programmed data (see *Table 19: Lock register bits*).
2. The lock register can only be programmed once.

8.2 Status register

The M29DW127G has one status register. The various bits convey information and errors on the current and previous program/erase operation. Bus read operations from any address within the memory, always read the status register during program and erase operations. It is also read during erase suspend when an address within a block being erased is accessed.

The bits in the status register are summarized in *Table 21: Status register bits*.

8.2.1 Data polling bit (DQ7)

The data polling bit can be used to identify whether the program/erase controller has successfully completed its operation or if it has responded to an erase suspend. The data polling bit is output on DQ7 when the status register is read.

During program operations the data polling bit outputs the complement of the bit being programmed to DQ7. After successful completion of the program operation the memory returns to read mode and bus read operations, from the address just programmed, output DQ7, not its complement.

During erase operations the data polling bit outputs ’0’, the complement of the erased state of DQ7. After successful completion of the erase operation the memory returns to read mode.

In erase suspend mode the data polling bit will output a ’1’ during a bus read operation within a block being erased. The data polling bit will change from ’0’ to ’1’ when the program/erase controller has suspended the erase operation.

Figure 9: Data polling flowchart, gives an example of how to use the data polling bit. A valid address is the address being programmed or an address within the block being erased.

8.2.2 Toggle bit (DQ6)

The toggle bit can be used to identify whether the program/erase controller has successfully completed its operation or if it has responded to an erase suspend. The toggle bit is output on DQ6 when the status register is read.

During a program/erase operation the toggle bit changes from ’0’ to ’1’ to ’0’, etc., with successive bus read operations at any address. After successful completion of the operation the memory returns to read mode.

During erase suspend mode the toggle bit will output when addressing a cell within a block being erased. The toggle bit will stop toggling when the program/erase controller has suspended the erase operation.

Figure 10: Data toggle flowchart, gives an example of how to use the data toggle bit.

8.2.3 Error bit (DQ5)

The error bit can be used to identify errors detected by the program/erase controller. The error bit is set to ’1’ when a program, block erase or chip erase operation fails to write the correct data to the memory. If the error bit is set a Read/Reset command must be issued

before other commands are issued. The error bit is output on DQ5 when the status register is read.

Note that the Program command cannot change a bit set to ’0’ back to ’1’ and attempting to do so will set DQ5 to ‘1’. A bus read operation to that address will show the bit is still ‘0’. One of the erase commands must be used to set all the bits in a block or in the whole memory from ’0’ to ’1’.

8.2.4 Erase timer bit (DQ3)

The erase timer bit can be used to identify the start of program/erase controller operation during a Block Erase command. Once the program/erase controller starts erasing the erase timer bit is set to ’1’. Before the program/erase controller starts the erase timer bit is set to ’0’ and additional blocks to be erased may be written to the command interface. The erase timer bit is output on DQ3 when the status register is read.

8.2.5 Alternative toggle bit (DQ2)

The alternative toggle bit can be used to monitor the program/erase controller during erase operations. The alternative toggle bit is output on DQ2 when the status register is read.

During chip erase and block erase operations the toggle bit changes from ’0’ to ’1’ to ’0’, etc., with successive bus read operations from addresses within the blocks being erased. A protected block is treated the same as a block not being erased. Once the operation completes the memory returns to read mode.

During erase suspend the alternative toggle bit changes from ’0’ to ’1’ to ’0’, etc. with successive bus read operations from addresses within the blocks being erased. Bus read operations to addresses within blocks not being erased will output the memory array data as if in read mode.

After an erase operation that causes the error bit to be set, the alternative toggle bit can be used to identify which block or blocks have caused the error. The alternative toggle bit changes from ’0’ to ’1’ to ’0’, etc. with successive bus read operations from addresses within blocks that have not erased correctly. The alternative toggle bit does not change if the addressed block has erased correctly.

8.3 Buffered program abort bit (DQ1)

The Buffered program abort bit, DQ1, is set to ‘1’ when a write to buffer program or enhanced buffered program operation aborts. The Buffered Program Abort and Reset command must be issued to return the device to read mode (see write to buffer program in *Section 7.1: Standard commands*).

Table 21. Status register bits(1)

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	$\overline{RB}$
Program(2)	Bank address	$\overline{DQ7}$	Toggle	0	–	–	0	0
Program During Erase Suspend	Bank address	$\overline{DQ7}$	Toggle	0	–	–	–	0
Buffered Program Abort(2)	Bank address	$\overline{DQ7}$	Toggle	0	–	–	1	0
Program Error	Bank address	$\overline{DQ7}$	Toggle	1	–	–	–	Hi-Z
Chip Erase	Any address	0	Toggle	0	1	Toggle	–	0
Block Erase before timeout	Erasing block	0	Toggle	0	0	Toggle	–	0
	Non-erasing block	0	Toggle	0	0	No toggle	–	0
Block Erase	Erasing block	0	Toggle	0	1	Toggle	–	0
	Non-erasing block	0	Toggle	0	1	No toggle	–	0
Erase Suspend	Erasing block	1	No Toggle	0	–	Toggle	–	Hi-Z
	Non-erasing block	Data read as normal					–	Hi-Z
Erase Error	Good block address	0	Toggle	1	1	No toggle	–	Hi-Z
	Faulty block address	0	Toggle	1	1	Toggle	–	Hi-Z

1. Unspecified data bits should be ignored.
2. $\overline{DQ7}$ for write to buffer program and enhanced buffered program is related to the last address location loaded.

Figure 9. Data polling flowchart

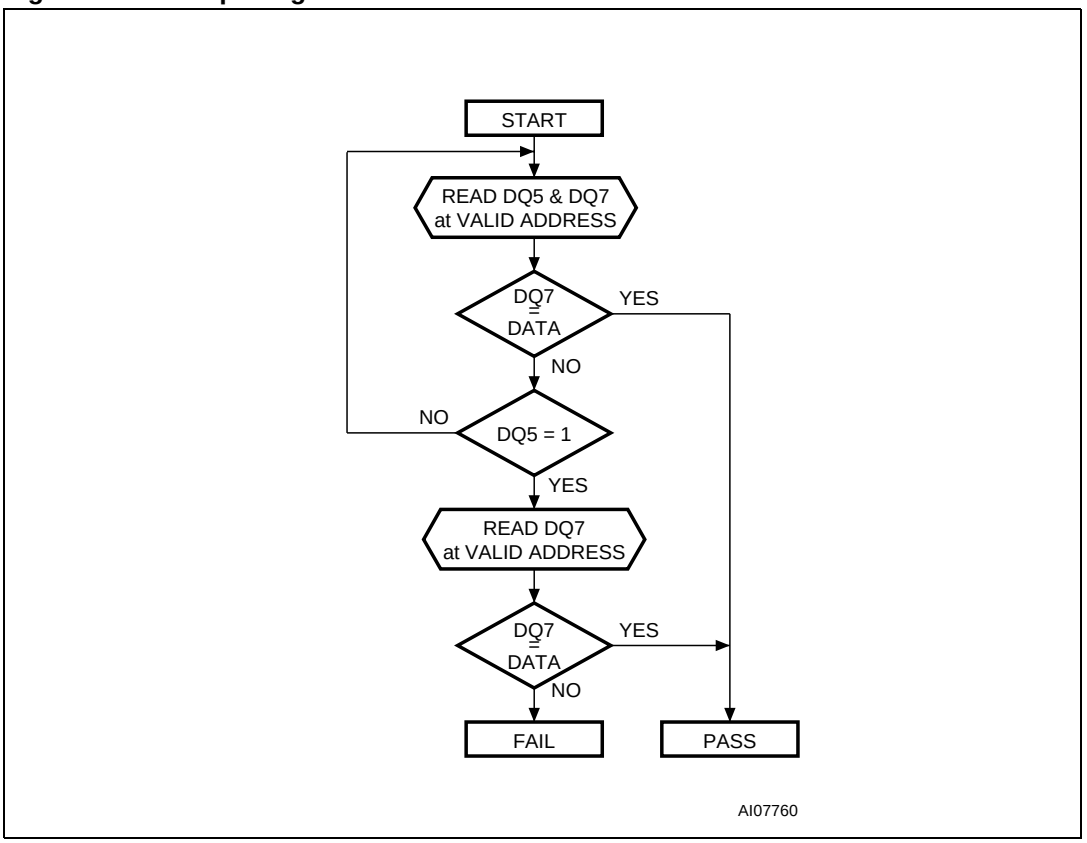
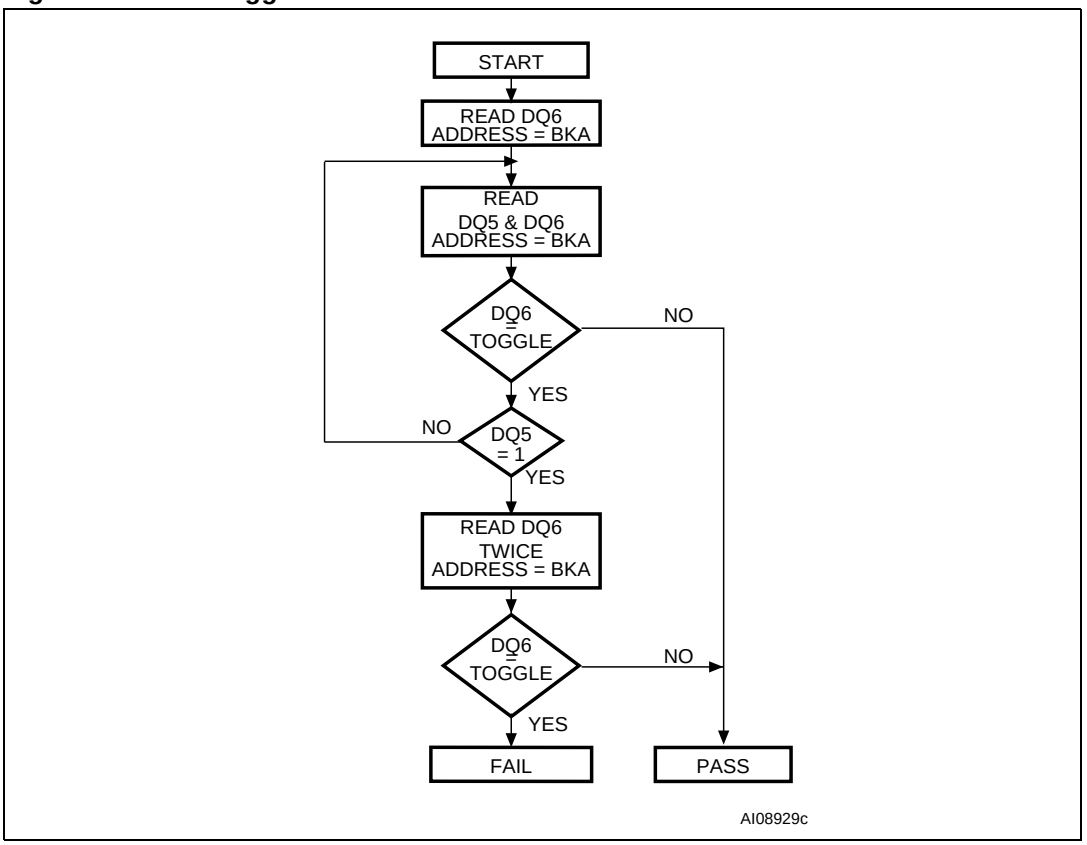


Figure 10. Data toggle flowchart



1. BKA=bank address being programmed or erased.

9 Dual operations and multiple bank architecture

The multiple bank architecture of the M29DW127G gives greater flexibility for software developers to split the code and data spaces within the memory array. The dual operations feature simplifies the software management of the device by allowing code to be executed from one bank while another bank is being programmed or erased.

The dual operations feature means that while programming or erasing in one bank, read operations are possible in another bank with zero latency.

Only one bank at a time is allowed to be in program or erase mode. However, certain commands can cross bank boundaries, which means that during an operation only the banks that are not concerned with the cross bank operation are available for dual operations. For example, if a Block Erase command is issued to erase blocks in both bank A and bank B, then only banks C or D are available for read operations while the erase is being executed.

If a read operation is required in a bank, which is programming or erasing, the program or erase operation can be suspended.

Also if the suspended operation was erase then a program command can be issued to another block, so the device can have one block in erase suspend mode, one programming and other banks in read mode.

By using a combination of these features, read operations are possible at any moment.

Table 22 and *Table 23* show the dual operations possible in other banks and in the same bank. Note that only the commonly used commands are represented in these tables.

Table 22. Dual operations allowed in other banks(1)

Status of bank	Commands allowed in another bank							
	Read	Read Status Register (2)	Read CFI Query	Auto Select	Program	Erase	Program/Erase Suspend	Program/Erase Resume
Idle	Yes	Yes(3)	Yes	Yes	Yes	Yes	Yes(3)	Yes(4)
Programming	Yes	No	No	No	–	–	No	No
Erasing	Yes	No	No	No	–	–	No	No
Program suspended	Yes	No	Yes	Yes	No	No	–	No
Erase suspended	Yes	No	Yes	Yes	Yes	No	–	Yes(5)

1. If several banks are involved in a program or erase operation, then only the banks that are not concerned with the operation are available for dual operations.
2. Read Status Register is not a command. The status register can be read during a block program or erase operation.
3. Only after a program or erase operation in that bank.
4. Only after a Program or Erase Suspend command in that bank.
5. Only an erase resume is allowed if the bank was previously in erase suspend mode.

Table 23. Dual operations allowed in same bank

Status of bank	Commands allowed in another bank							
	Read	Read Status Register (1)	Read CFI Query	Auto Select	Program	Erase	Program/ Erase Suspend	Program/Erase Resume
Idle	Yes	Yes	Yes	Yes	Yes	Yes	Yes(2)	Yes(3)
Programming	No	Yes	No	No	–	–	Yes(4)	–
Erasing	No	Yes	No	No	–	No	Yes(5)	–
Program suspended	Yes	No	Yes	Yes	No	–	–	Yes
Erase suspended	Yes(6)	Yes(7)	Yes	Yes	Yes(6)	No	–	Yes

1. Read status register is not a command. The status register can be read during a block program or erase operation.
2. Only after a program or erase operation in that bank.
3. Only after a Program or Erase Suspend command in that bank.
4. Only a program suspend.
5. Only an erase suspend.
6. Not allowed in the block or word that is being erased or programmed.
7. The status register can be read by addressing the block being erase suspended.

10 Maximum ratings

Stressing the device above the rating listed in *Table 24: Absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied.

Table 24. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
T_{BIAS}	Temperature under bias	–50	125	°C
T_{STG}	Storage temperature	–65	150	°C
V_{IO}	Input or output voltage(1)(2)	–0.6	V_{CC} + 0.6	V
V_{CC}	Supply voltage	–0.6	4	V
V_{CCQ}	Input/output supply voltage	–0.6	4	V
V_{ID}	Identification voltage	–0.6	10.5	V
V_{PPH}(3)	Program voltage	–0.6	10.5	V

1. Minimum voltage may undershoot to –2 V during transition and for less than 20 ns during transitions.
2. Maximum voltage may overshoot to V_{CC} + 2 V during transition and for less than 20 ns during transitions.
3. V_{PPH} must not remain at 9 V for more than a total of 80 hrs.

11 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in *Table 25: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 25. Operating and AC measurement conditions

Parameter	M29DW127G				Unit
	70 or 60 ns		80 ns		
	Min	Max	Min	Max	
V_{CC} supply voltage	2.7	3.6	2.7	3.6	V
V_{CCQ} supply voltage ($V_{CCQ} \leq V_{CC}$)	2.7	3.6	1.65	3.6	V
Ambient operating temperature	– 40	85	– 40	85	°C
Load capacitance (C_L)	30		30		pF
Input rise and fall times		10		10	ns
Input pulse voltages	0 to V_{CCQ}		0 to V_{CCQ}		V
Input and output timing ref. voltages	$V_{CCQ}/2$		$V_{CCQ}/2$		V

Figure 11. AC measurement load circuit

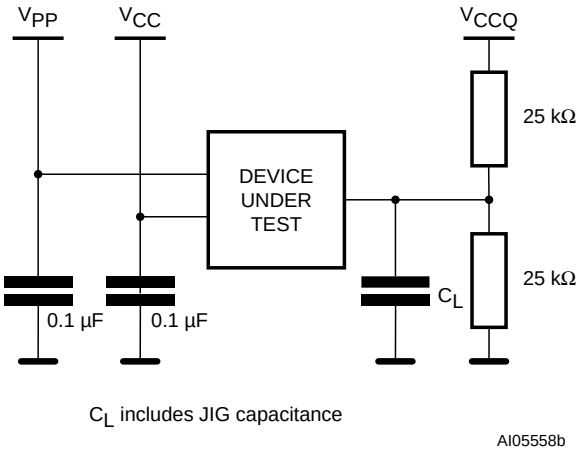


Figure 12. AC measurement I/O waveform

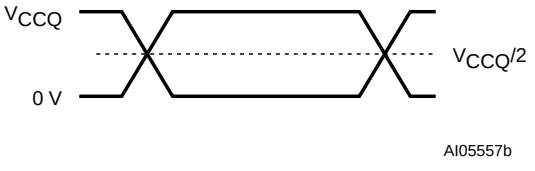


Table 26. Power-up waiting timings

Symbol	Parameter		M29DW127G		Unit
			70 or 60 ns	80 ns	
t_{VCHEL}	V_{CC}(1) High to Chip Enable Low	Min	55		µs
t_{VCQHEL}	V_{CCQ}(1) High to Chip Enable Low	Min	55		µs
t_{VCHWL}	V_{CC} High to Write Enable Low	Min	500		µs
t_{VCQHWL}	V_{CCQ} High to Write Enable Low	Min	500		µs

1. V_{CC} and V_{CCQ} ramps must be synchronized during power-up.

Figure 13. Power-up waiting timings

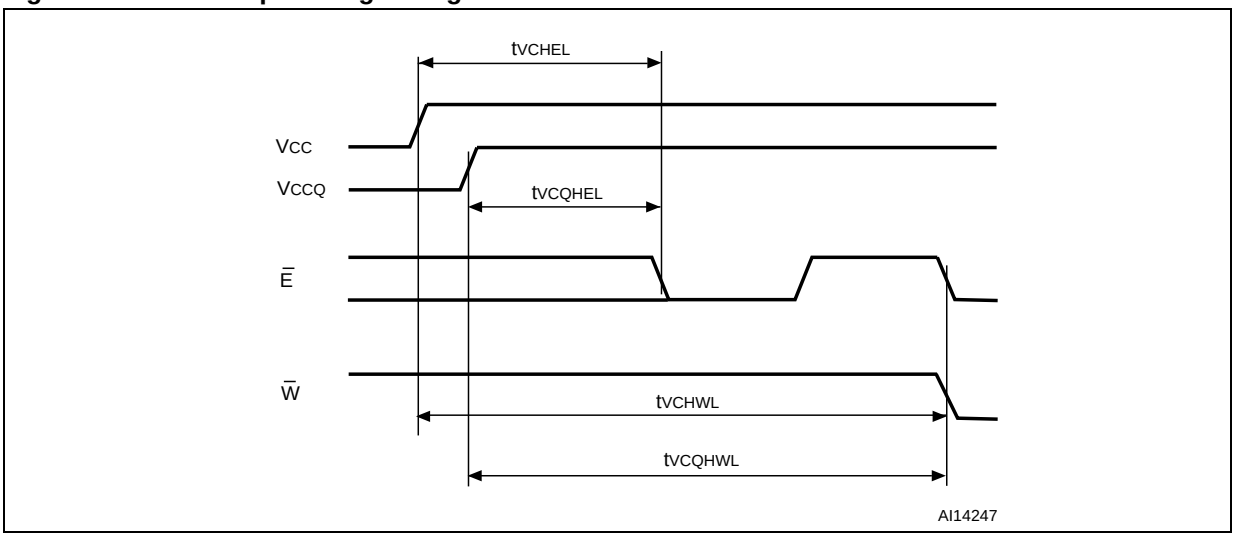


Table 27. Device capacitance(1)

Symbol	Parameter	Test condition	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V		6	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V		12	pF

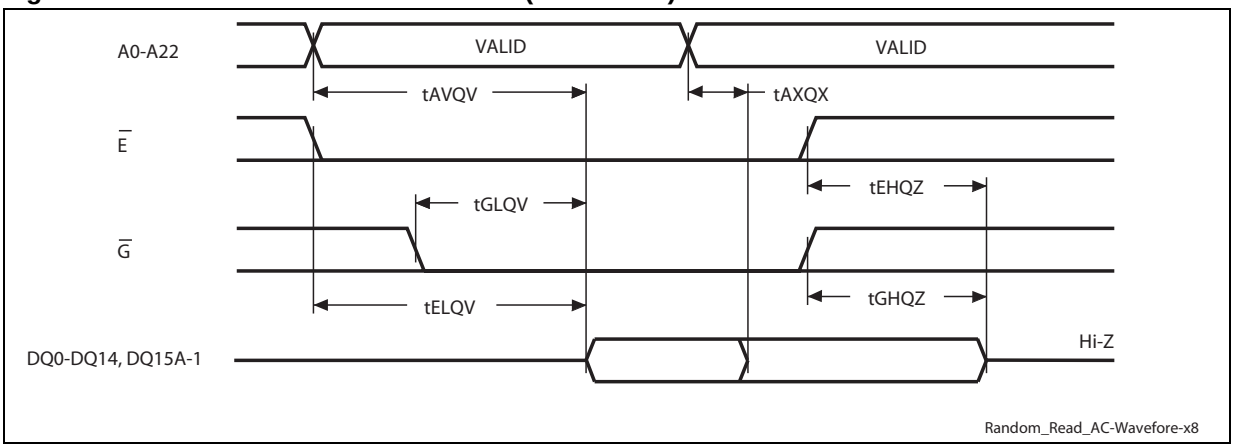
1. Sampled only, not 100% tested.

Table 28. DC characteristics

Symbol	Parameter		Test condition		Min	Typ	Max	Unit
I_{LI}(1)	Input leakage current		0 V ≤ V_{IN} ≤ V_{CC}				±1	µA
I_{LO}	Output leakage current		0 V ≤ V_{OUT} ≤ V_{CC}				±1	µA
I_{CC1}	Read current	Random read	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}, f = 6 MHz				10	mA
		Page read	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}, f = 10 MHz				15	mA
I_{CC2}	Supply current (standby)		$\overline{E}$ = V_{CCQ} ± 0.2 V, $\overline{RP}$ = V_{CCQ} ± 0.2 V				100	µA
I_{CC3}(2)	Supply current (program/erase)		Program/Erase controller active	$V_{PP}/\overline{WP}$ = V_{IL} or V_{IH}			20	mA
				$V_{PP}/\overline{WP}$ = V_{PPH}			20	mA
I_{PP1}	Program current (Program)	Read or standby	$V_{PP}/\overline{WP}$ ≤ V_{CC}			1	5	µA
I_{PP2}		Reset	$\overline{RP}$ = V_{SS} ± 0.2 V			1	5	µA
I_{PP3}		Program operation ongoing	$V_{PP}/\overline{WP}$ = 12 V ± 5%			1	10	mA
			$V_{PP}/\overline{WP}$ = V_{CC}			1	5	µA
I_{PP4}	Program current (Erase)	Erase operation ongoing	$V_{PP}/\overline{WP}$ = 12 V ± 5%			3	10	mA
			$V_{PP}/\overline{WP}$ = V_{CC}			1	5	µA
V_{IL}	Input Low voltage		V_{CC} ≥ 2.7 V		–0.5		0.3V_{CCQ}	V
V_{IH}	Input High voltage		V_{CC} ≥ 2.7 V		0.7V_{CCQ}		V_{CCQ}+0.4	V
V_{OL}	Output Low voltage		I_{OL} = 100 µA, V_{CC} = $V_{CC(min)}$, V_{CCQ} = $V_{CCQ(min)}$				0.15V_{CCQ}	V
V_{OH}	Output High voltage		I_{OH} = 100 µA, V_{CC} = $V_{CC(min)}$, V_{CCQ} = $V_{CCQ(min)}$		0.85V_{CCQ}			V
V_{ID}	Identification voltage				8.5		9.5	V
V_{PPH}	Voltage for $V_{PP}/\overline{WP}$ program acceleration				8.5		9.5	V
V_{LKO}(2)	Program/Erase lockout supply voltage				1.8		2.5	V

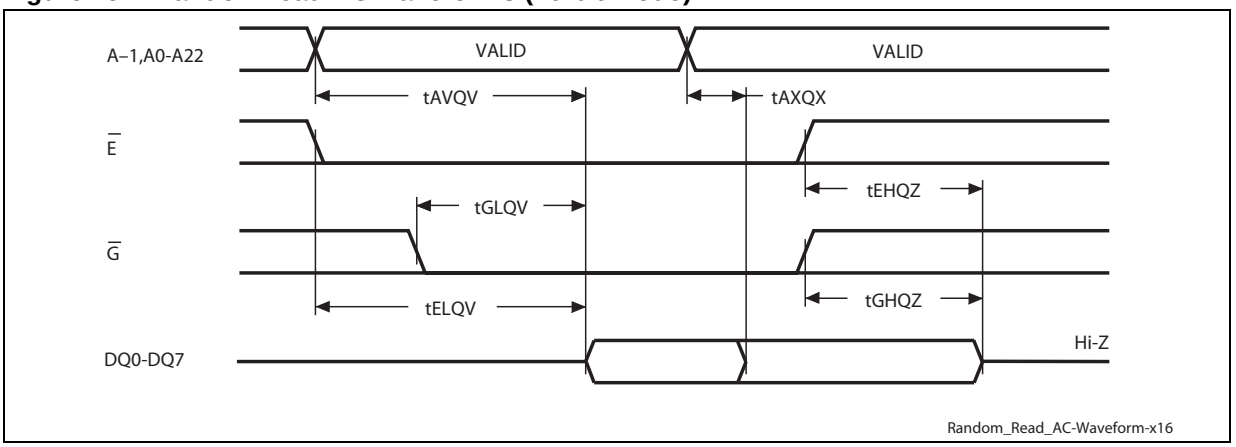
1. The maximum input leakage current is ±5 µA on the $V_{PP}/\overline{WP}$ pin.
2. Sampled only, not 100% tested.

Figure 14. Random read AC waveforms (8-bit mode)



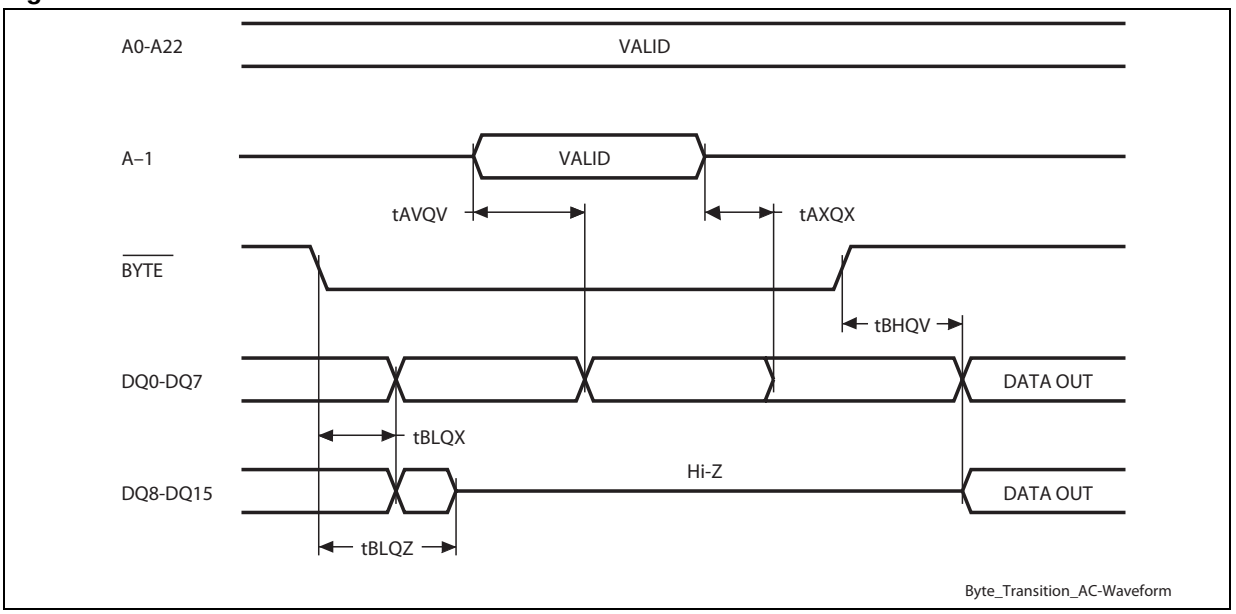
Note: $\overline{BYTE} = V_{IL}$

Figure 15. Random read AC waveforms (16-bit mode)



Note: $\overline{BYTE} = V_{IH}$

Figure 16. BYTE transition AC waveforms



Note: Chip Enable $\overline{(E)}$ and Output Enable $\overline{(G)}$ = V_{IL}

Figure 17. Page read AC waveforms (8-bit mode)

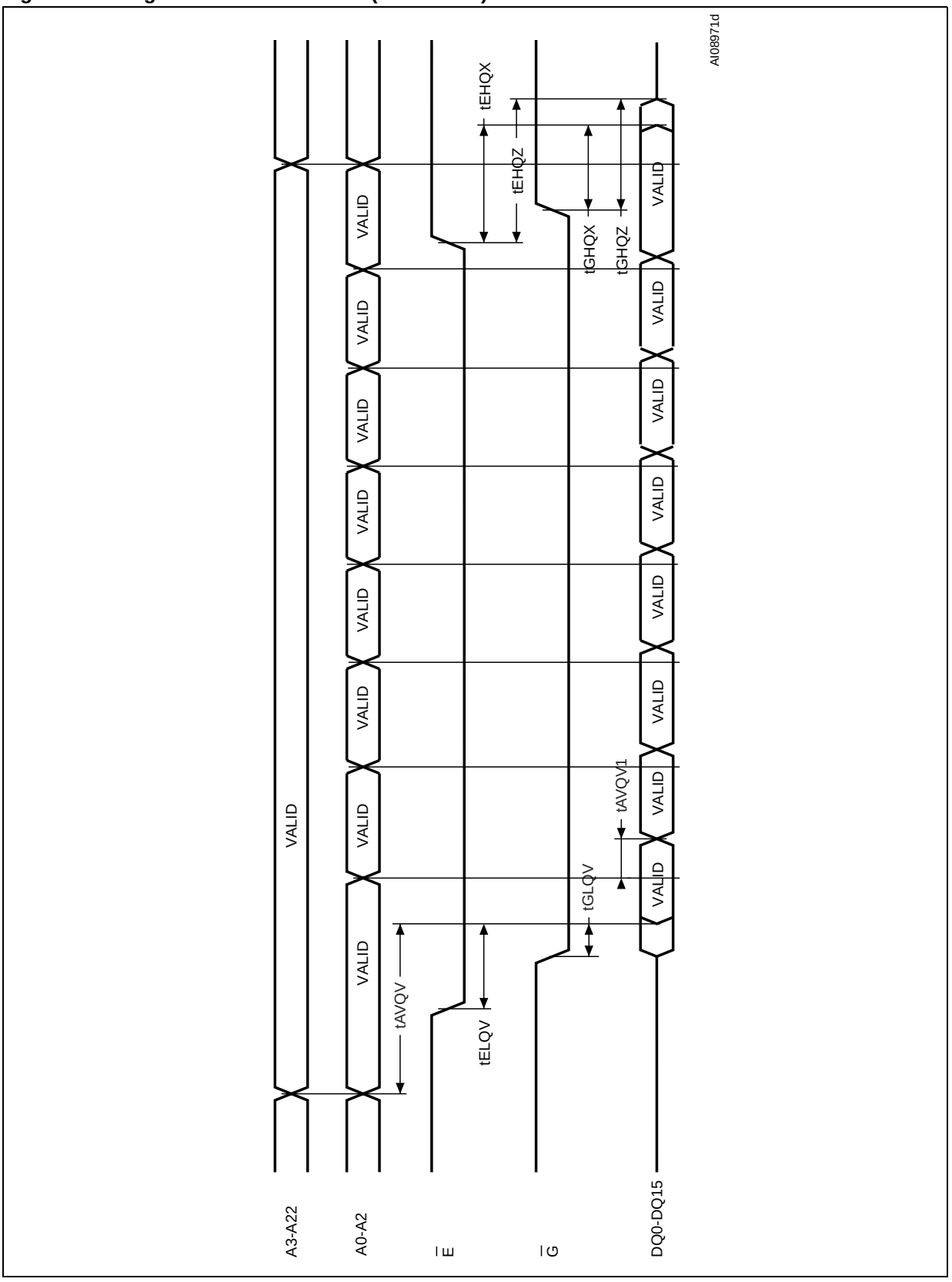


Figure 18. Page read AC waveforms (16-bit mode)

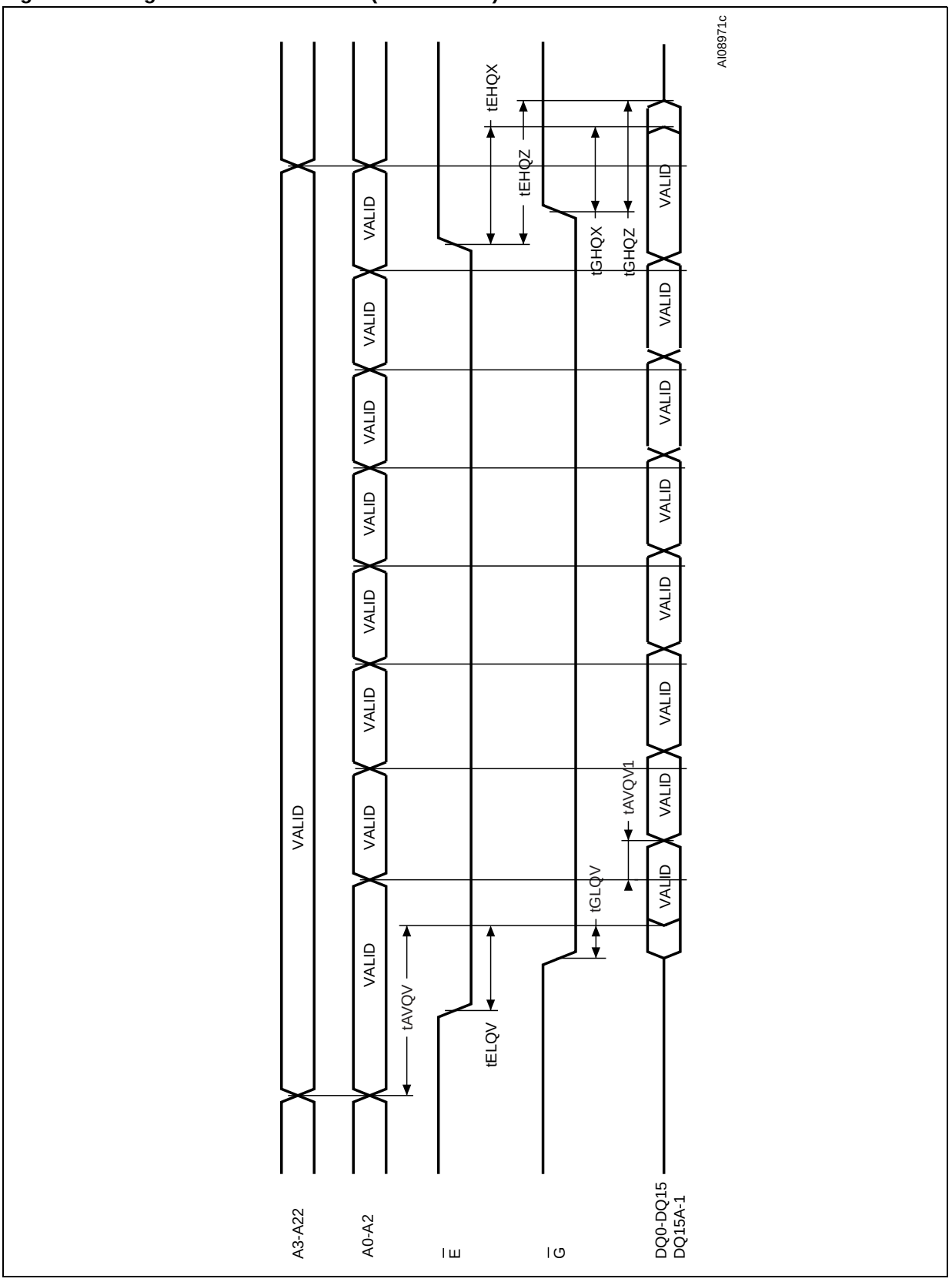
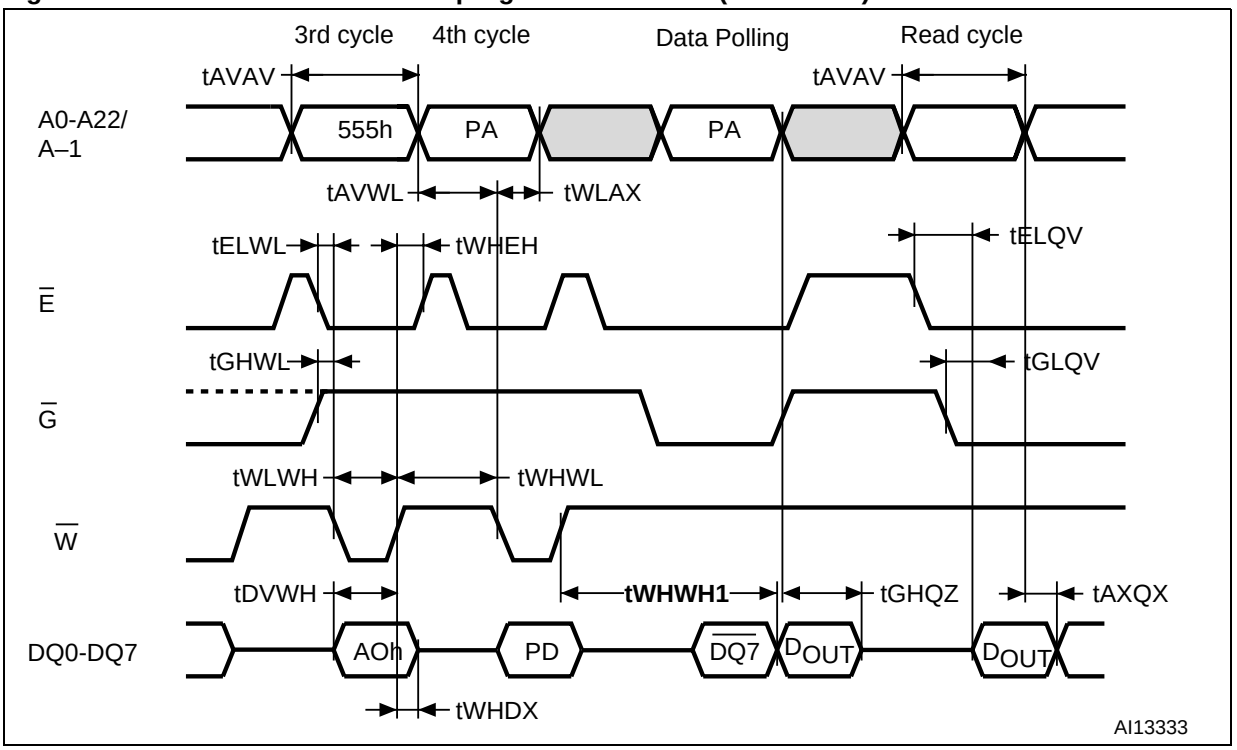


Table 29. Read AC characteristics

Symbol	Alt.	Parameter	Test condition		M29DW127G			Unit
					60 ns(1) $V_{CCQ}=V_{CC}$	70 ns $V_{CCQ}=V_{CC}$	80 ns V_{CCQ}=1.65 V to V_{CC}	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}=V_{IL}$ $\overline{G}=V_{IL}$	Min	60	70	80	ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}=V_{IL}$ $\overline{G}=V_{IL}$	Max	60	70	80	ns
t_{AVQV1}	t_{PAGE}	Address Valid to Output Valid (Page)	$\overline{E}=V_{IL}$ $\overline{G}=V_{IL}$	Max	25	25	30	ns
t_{ELQX}(2)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}=V_{IL}$	Min	0	0	0	ns
t_{ELQV}	$t_{\overline{E}}$	Chip Enable Low to Output Valid	$\overline{G}=V_{IL}$	Max	60	70	80	ns
t_{GLQX}(2)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}=V_{IL}$	Min	0	0	0	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}=V_{IL}$	Max	25	25	30	ns
t_{EHQZ}(2)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}=V_{IL}$	Max	20	20	30	ns
t_{GHQZ}(2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}=V_{IL}$	Max	20	20	20	ns
t_{EHQX} t_{GHQX} t_{AXQX}	t_{OH}	Chip Enable, Output Enable or Address Transition to Output Transition		Min	0	0	0	ns
t_{ELBL} t_{ELBH}	t_{ELFL} t_{ELFH}	Chip Enable to $\overline{BYTE}$ Low or High		Max	5	5	5	ns
t_{BLQZ}	t_{FLQZ}	$\overline{BYTE}$ Low to Output Hi-Z		Max	25	25	25	ns
t_{BHQV}	t_{FHQV}	$\overline{BYTE}$ High to Output Valid		Max	30	30	30	ns

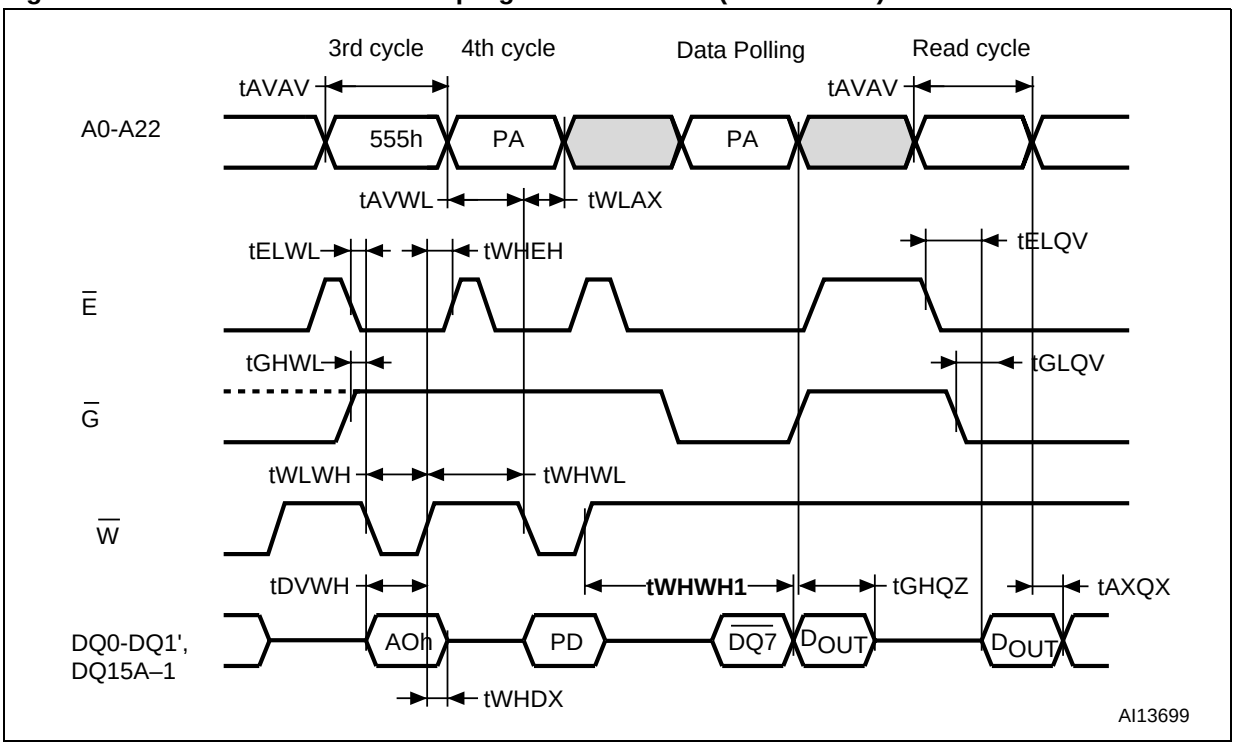
1. Only available upon customer request.
2. Sampled only, not 100% tested.

Figure 19. Write enable controlled program waveforms (8-bit mode)



1. Only the third and fourth cycles of the Program command are represented. The Program command is followed by the check of status register data polling bit and by a read operation that outputs the data, DOUT, programmed by the previous Program command.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (see *Section 8.2.1: Data polling bit (DQ7)*).
4. See*Table 30: Write AC characteristics, write enable controlled*, *Table 31: Write AC characteristics, chip enable controlled* and *Table 29: Read AC characteristics* for details on the timings.

Figure 20. Write enable controlled program waveforms (16-bit mode)



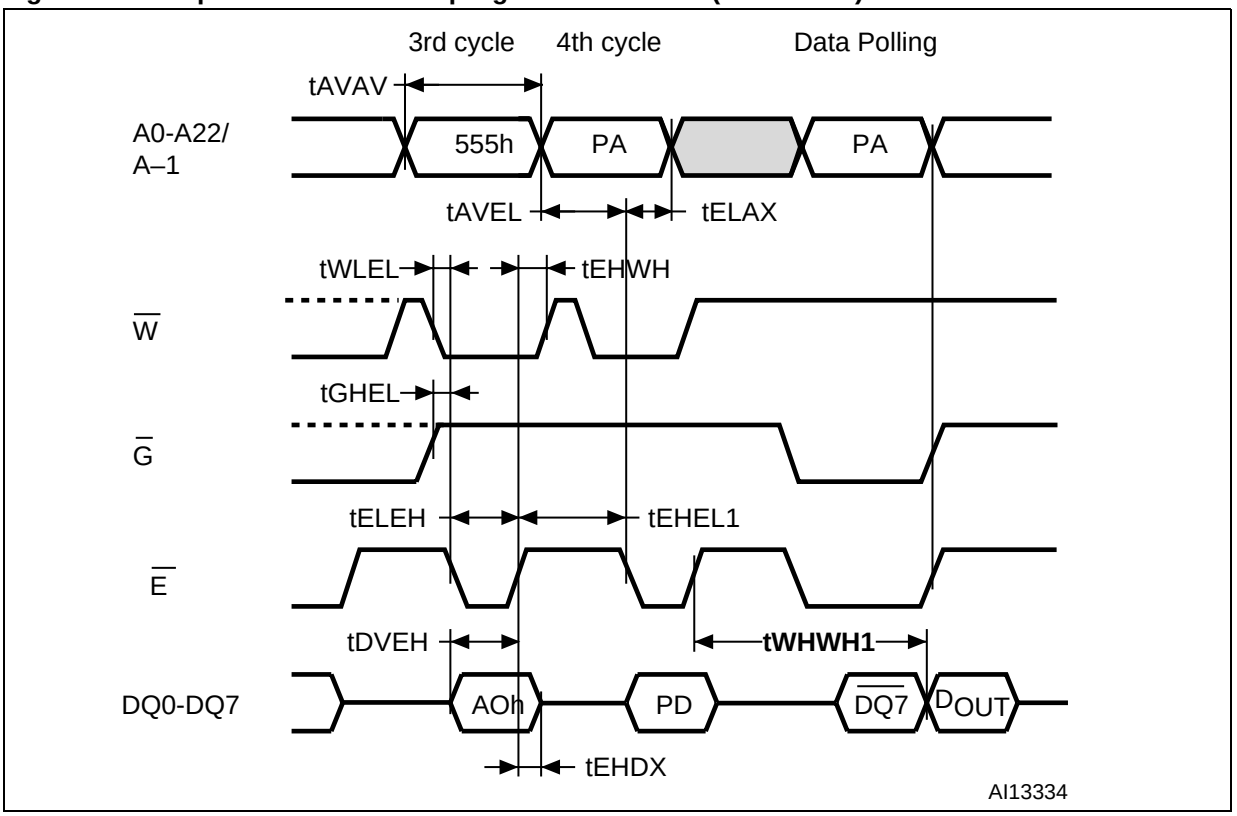
1. Only the third and fourth cycles of the Program command are represented. The Program command is followed by the check of status register data polling bit and by a read operation that outputs the data, DOUT, programmed by the previous Program command.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (see *Section 8.2.1: Data polling bit (DQ7)*).
4. See*Table 30: Write AC characteristics, write enable controlled*, *Table 31: Write AC characteristics, chip enable controlled* and *Table 29: Read AC characteristics* for details on the timings.

Table 30. Write AC characteristics, write enable controlled

Symbol	Alt	Parameter		M29DW127G			Unit
				60 ns(1)	70 ns	80 ns	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	65	70	80	ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	Min	0	0	0	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	Min	35	35	35	ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	Min	45	45	45	ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	Min	0	0	0	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	Min	0	0	0	ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	Min	30	30	30	ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	Min	0	0	0	ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	Min	45	45	45	ns
t_{GHWL}		Output Enable High to Write Enable Low	Min	0	0	0	ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	Min	0	0	0	ns
t_{WHRL}(2)	t_{BUSY}	Program/Erase Valid to $\overline{RB}$ Low	Max	30	30	30	ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	Min	50	50	50	µs

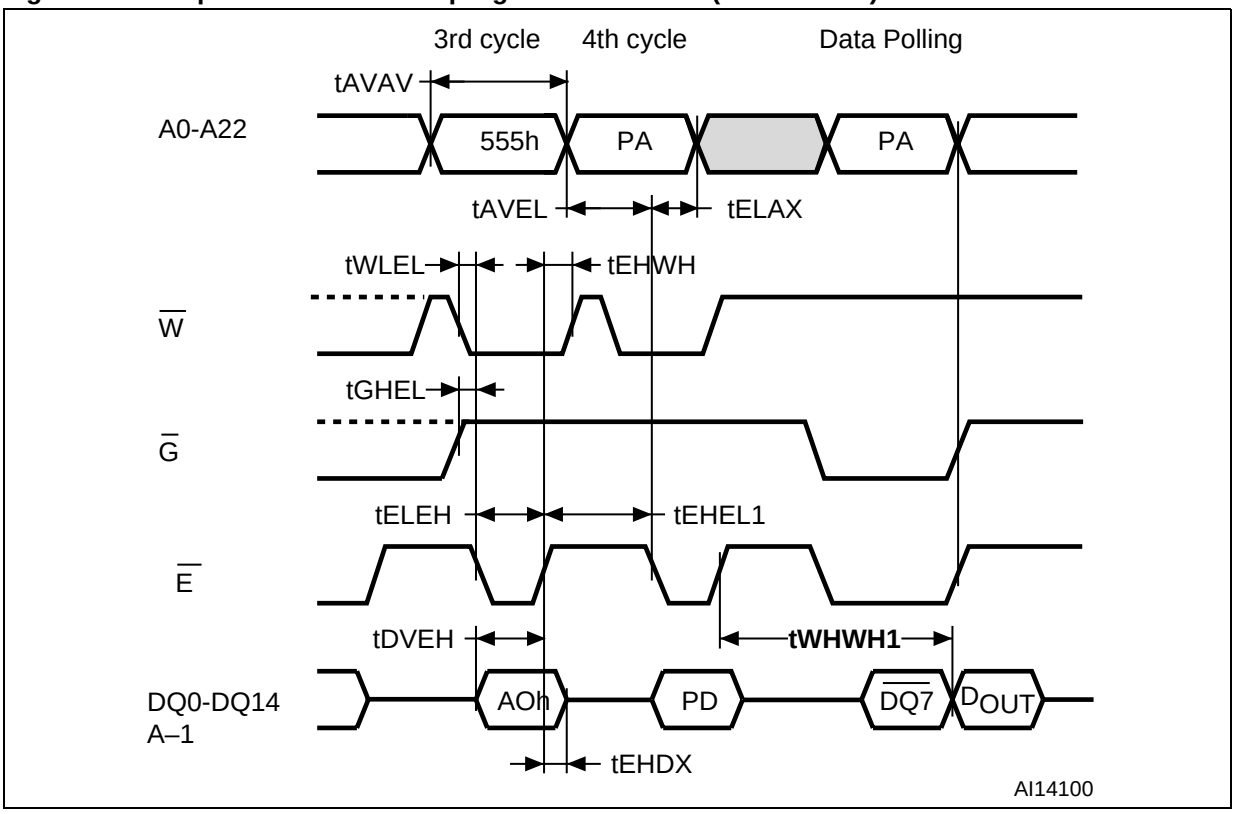
1. Only available upon customer request.
2. Sampled only, not 100% tested.

Figure 21. Chip enable controlled program waveforms (8-bit mode)



1. Only the third and fourth cycles of the Program command are represented. The Program command is followed by the check of status register data polling bit.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (see *Section 8.2.1: Data polling bit (DQ7)*).
4. See *Table 30: Write AC characteristics, write enable controlled*, *Table 31: Write AC characteristics, chip enable controlled* and *Table 29: Read AC characteristics* for details on the timings.

Figure 22. Chip enable controlled program waveforms (16-bit mode)



1. Only the third and fourth cycles of the Program command are represented. The Program command is followed by the check of status register data polling bit.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (see *Section 8.2.1: Data polling bit (DQ7)*).
4. See *Table 30: Write AC characteristics, write enable controlled*, *Table 31: Write AC characteristics, chip enable controlled* and *Table 29: Read AC characteristics* for details on the timings.

Table 31. Write AC characteristics, chip enable controlled

Symbol	Alt.	Parameter		M29DW127G			Unit
				60 ns(1)	70 ns	80 ns	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	65	70	80	ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	Min	0	0	0	ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	Min	35	35	35	ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	Min	45	45	45	ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	Min	0	0	0	ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	Min	0	0	0	ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	Min	30	30	30	ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	Min	0	0	0	ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	Min	45	45	45	ns
t_{GHEL}		Output Enable High Chip Enable Low	Min	0	0	0	ns

1. Only available upon customer request.

Figure 23. Reset AC waveforms (no program/erase ongoing)

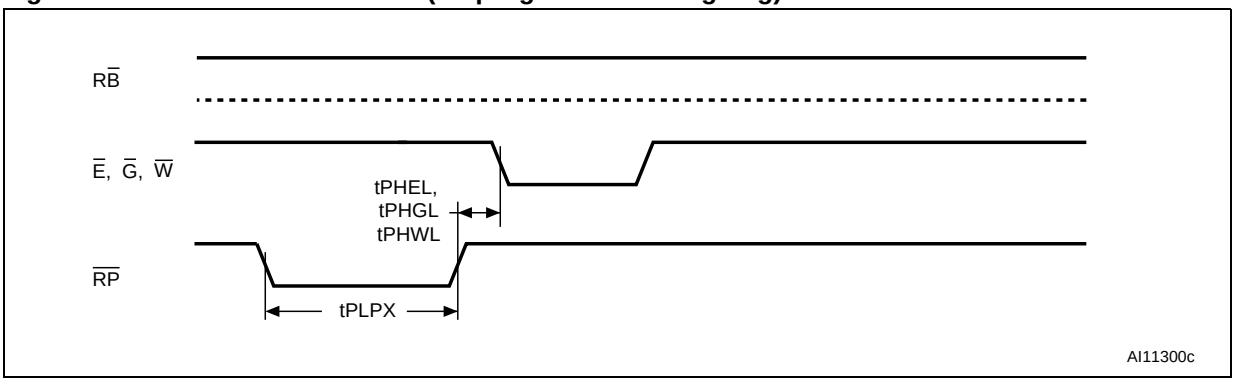


Figure 24. Reset during program/erase operation AC waveforms

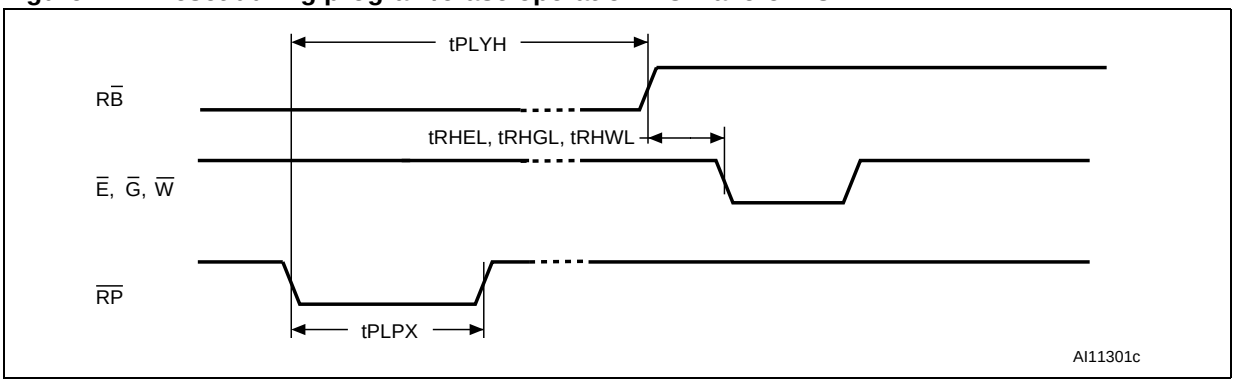


Table 32. Reset AC characteristics

Symbol	Alt.	Parameter		M29DW127G			Unit
				60 ns	70 ns	80 ns	
t_{PLYH} (1)	t_{READY}	$\overline{RP}$ Low to read mode, during program or erase	Max	50	50	50	µs
t_{PLPX}	t_{RP}	$\overline{RP}$ pulse width	Min	10	10	10	µs
t_{PHEL}, t_{PHGL}, t_{PHWL} (1)	t_{RH}	$\overline{RP}$ High to Write Enable Low, Chip Enable Low, Output Enable Low	Min	50	50	50	ns
	t_{RPD}	$\overline{RP}$ Low to standby mode, during read mode	Min	10	10	10	µs
		$\overline{RP}$ Low to standby mode, during program or erase	Min	50	50	50	µs
t_{RHEL}, t_{RHGL}, t_{RHWL} (1)	t_{RB}	$\overline{RB}$ High to Write Enable Low, Chip Enable Low, Output Enable Low	Min	0	0	0	ns

1. Sampled only, not 100% tested.

Figure 25. Accelerated program timing waveforms

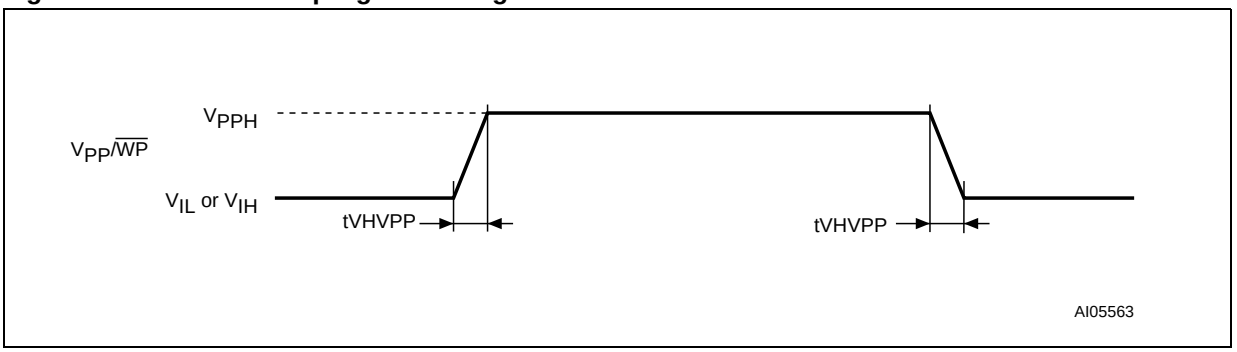
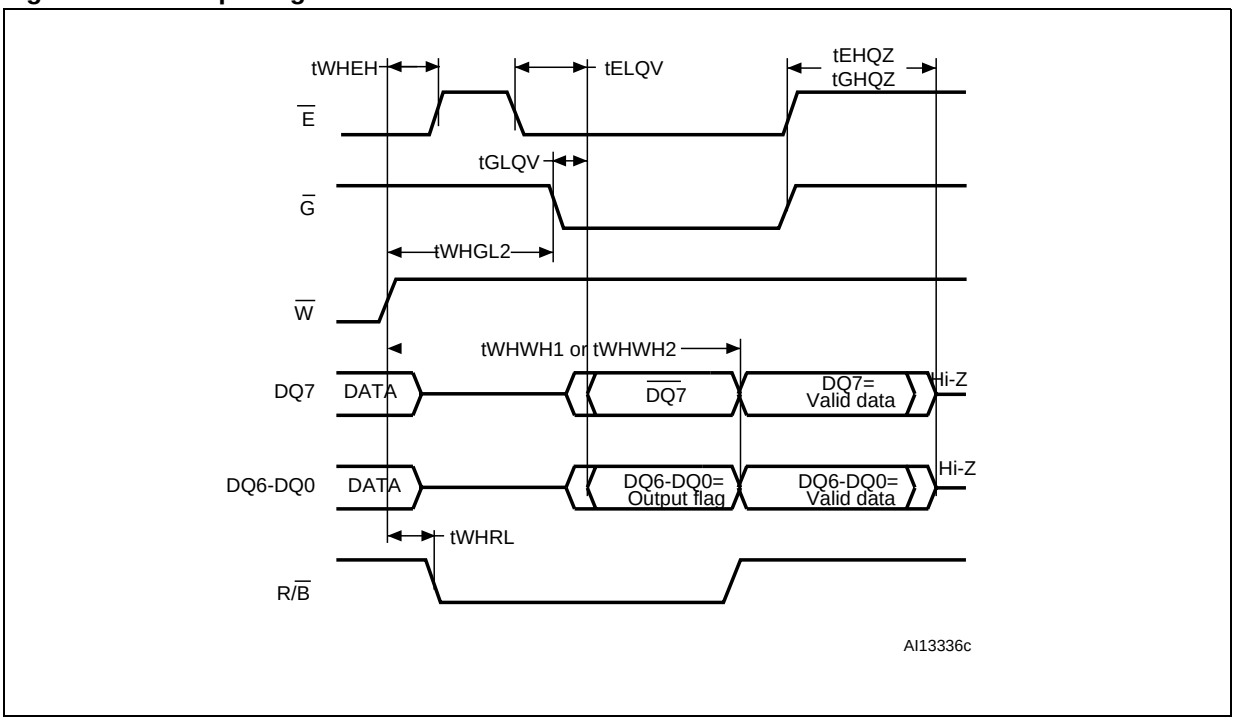


Figure 26. Data polling AC waveforms



1. DQ7 returns valid data bit when the ongoing Program or Erase command is completed.
2. See *Table 33: Accelerated program and data polling/data toggle AC characteristics* and *Table 29: Read AC characteristics* for details on the timings.

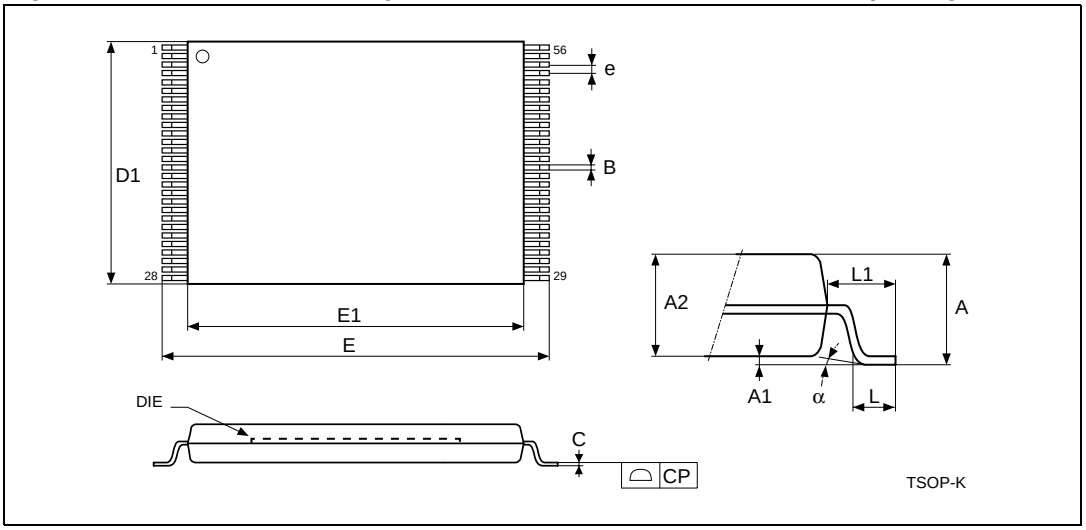
Table 33. Accelerated program and data polling/data toggle AC characteristics

Symbol	Alt.	Parameter		M29DW127G			Unit
				60 ns	70 ns	80 ns	
t_{VHVPP}		$V_{PP}/\overline{WP}$ raising and falling time	Min	250	250	250	ns
t_{AXGL}	t_{ASO}	Address setup time to Output Enable Low during toggle bit polling	Min	10	10	10	ns
t_{GHAX}, t_{EHAX}	t_{AHT}	Address hold time from Output Enable during toggle bit polling	Min	10	10	10	ns
t_{EHEL2}	t_{EPH}	Chip Enable High during toggle bit polling	Min	10	10	10	ns
t_{WHGL2}, t_{GHGL2}	t_{OEH}	Output hold time during data and toggle bit polling	Min	20	20	20	ns
t_{WHRL}	t_{BUSY}	Program/Erase Valid to $\overline{RB}$ Low	Max	30	30	30	ns

12 Package mechanical

To meet environmental requirements, Numonyx offers the M29DW127G in ECOPACK® packages. ECOPACK packages are lead-free. The category of second level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 27. TSOP56 – 56 lead plastic thin small outline, 14 x 20 mm, package outline

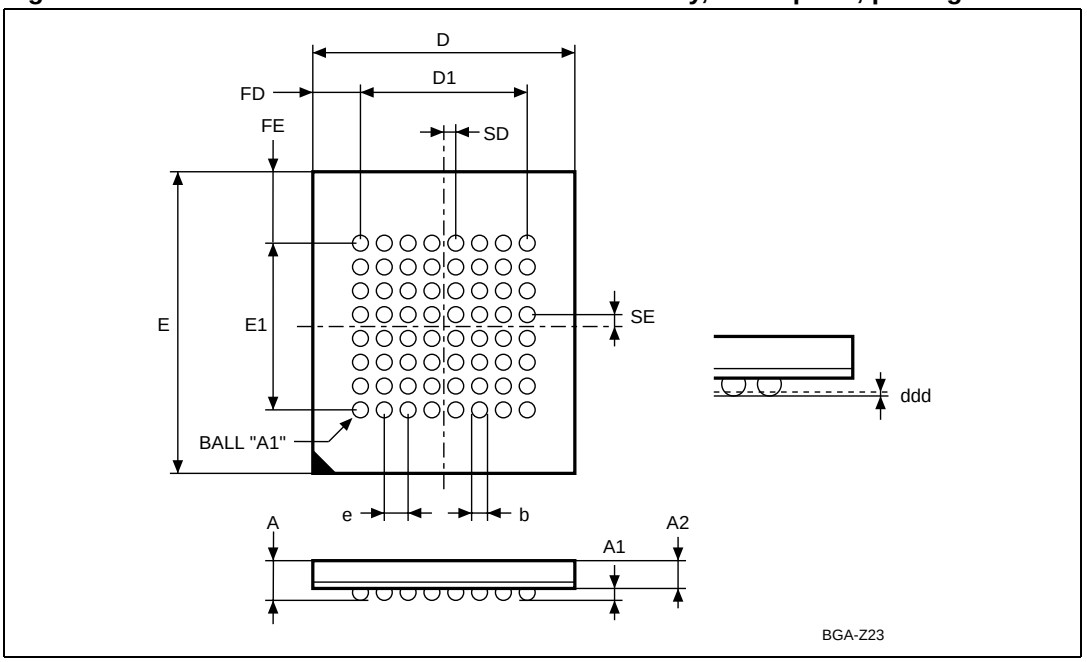


1. Drawing is not to scale.

Table 34. TSOP56 – 56 lead plastic thin small outline, 14 x 20 mm, package mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1	0.10	0.05	0.15	0.004	0.002	0.006
A2	1.00	0.95	1.05	0.039	0.037	0.041
B	0.22	0.17	0.27	0.009	0.007	0.011
C		0.10	0.21		0.004	0.008
CP			0.10			0.004
D1	14.00	13.90	14.10	0.551	0.547	0.555
E	20.00	19.80	20.20	0.787	0.780	0.795
E1	18.40	18.30	18.50	0.724	0.720	0.728
e	0.50	–	–	0.020	–	–
L	0.60	0.50	0.70	0.024	0.020	0.028
α	3	0	5	3	0	5

Figure 28. TBGA64 10 x 13 mm - 8 x 8 active ball array, 1 mm pitch, package outline



1. Drawing is not to scale.

Table 35. TBGA64 10 x 13 mm - 8 x 8 active ball array, 1 mm pitch, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1	0.30	0.20	0.35	0.012	0.008	0.014
A2	0.80			0.031		
b		0.35	0.50		0.014	0.020
D	10.00	9.90	10.10	0.394	0.390	0.398
D1	7.000	–	–	0.276	–	–
ddd			0.10			0.004
e	1.00	–	–	0.039	–	–
E	13.00	12.90	13.10	0.512	0.508	0.516
E1	7.00	–	–	0.276	–	–
FD	1.50	–	–	0.059	–	–
FE	3.00	–	–	0.118	–	–
SD	0.50	–	–	0.020	–	–
SE	0.50	–	–	0.020	–	–

13 Ordering information

Table 36. Ordering information scheme

Example: M29 D W 127G 60 NF 6 E

Device type

M29

Architecture

D = Dual operation

Operating voltage

W = V_{CC} = 2.7 to 3.6 V

Device function

127G = 128 Mbit (8-Mbit x16 or 16-Mbit x8), page, dual boot

Speed

60= 60 ns (80 ns if V_{CCQ}=1.65 V to V_{CC})(1)

70=70 ns (80 ns if V_{CCQ}=1.65 V to V_{CC})

Package

NF = TSOP56: 14 x 20 mm

ZA = TBGA64: 10 x 13 mm - 1 mm pitch

Temperature range

6 = -40 to 85 °C

Option

E = ECOPACK package, standard packing

F = ECOPACK package, tape & reel packing

1. Only available upon customer request.

Note: This product is also available with the extended block factory locked.

Devices are shipped from the factory with the memory content bits erased to ’1’.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest Numonyx sales office.

Appendix A Block addresses and read/modify protection groups

Table 37. Block addresses

Bank	Block	Protection group	Block size (Kbytes/Kwords)	16-bit address range (in hexadecimal)
Bank A	0	Protection group	64/32	0000000–0007FFF
	1	Protection group	64/32	0008000–000FFFF
	2	Protection group	64/32	0010000–0017FFF
	3	Protection group	64/32	0018000–001FFFF
	4	Protection group	256/128	0020000–003FFFF
	5	Protection group	256/128	0040000–005FFFF
	6	Protection group	256/128	0060000–007FFFF
	7	Protection group	256/128	0080000–009FFFF
	8	Protection group	256/128	00A0000–00BFFFF
	9	Protection group	256/128	00C0000–00DFFFF
	10	Protection group	256/128	00E0000–00FFFFF

Table 37. Block addresses (continued)

Bank	Block	Protection group	Block size (Kbytes/Kwords)	16-bit address range (in hexadecimal)
Bank B	11	Protection group	256/128	0100000–011FFFF
	12	Protection group	256/128	0120000–013FFFF
	13	Protection group	256/128	0140000–015FFFF
	14	Protection group	256/128	0160000–017FFFF
	15	Protection group	256/128	0180000–019FFFF
	16	Protection group	256/128	01A0000–01BFFFF
	17	Protection group	256/128	01C0000–01DFFFF
	18	Protection group	256/128	01E0000–01FFFFF
	19	Protection group	256/128	0200000–021FFFF
	20	Protection group	256/128	0220000–023FFFF
	21	Protection group	256/128	0240000–025FFFF
	22	Protection group	256/128	0260000–027FFFF
	23	Protection group	256/128	0280000–029FFFF
	24	Protection group	256/128	02A0000–02BFFFF
	25	Protection group	256/128	02C0000–02DFFFF
	26	Protection group	256/128	02E0000–02FFFFF
	27	Protection group	256/128	0300000–031FFFF
	28	Protection group	256/128	0320000–033FFFF
	29	Protection group	256/128	0340000–035FFFF
	30	Protection group	256/128	0360000–037FFFF
	31	Protection group	256/128	0380000–039FFFF
	32	Protection group	256/128	03A0000–03BFFFF
	33	Protection group	256/128	03C0000–03DFFFF
	34	Protection group	256/128	03E0000–03FFFFF

Table 37. Block addresses (continued)

Bank	Block	Protection group	Block size (Kbytes/Kwords)	16-bit address range (in hexadecimal)
Bank C	35	Protection group	256/128	0400000–041FFFF
	36	Protection group	256/128	0420000–043FFFF
	37	Protection group	256/128	0440000–045FFFF
	38	Protection group	256/128	0460000–047FFFF
	39	Protection group	256/128	0480000–049FFFF
	40	Protection group	256/128	04A0000–04BFFFF
	41	Protection group	256/128	04C0000–04DFFFF
	42	Protection group	256/128	04E0000–04FFFFF
	43	Protection group	256/128	0500000–051FFFF
	44	Protection group	256/128	0520000–053FFFF
	45	Protection group	256/128	0540000–055FFFF
	46	Protection group	256/128	0560000–057FFFF
	47	Protection group	256/128	0580000–059FFFF
	48	Protection group	256/128	05A0000–05BFFFF
	49	Protection group	256/128	05C0000–05DFFFF
	50	Protection group	256/128	05E0000–05FFFFF
	51	Protection group	256/128	0600000–061FFFF
	52	Protection group	256/128	0620000–063FFFF
	53	Protection group	256/128	0640000–065FFFF
	54	Protection group	256/128	0660000–067FFFF
	55	Protection group	256/128	0680000–069FFFF
	56	Protection group	256/128	06A0000–06BFFFF
	57	Protection group	256/128	06C0000–06DFFFF
	58	Protection group	256/128	06E0000–06FFFFF

Table 37. Block addresses (continued)

Bank	Block	Protection group	Block size (Kbytes/Kwords)	16-bit address range (in hexadecimal)
Bank D	59	Protection group	256/128	0700000–071FFFF
	60	Protection group	256/128	0720000–073FFFF
	61	Protection group	256/128	0740000–075FFFF
	62	Protection group	256/128	0760000–077FFFF
	63	Protection group	256/128	0780000–079FFFF
	64	Protection group	256/128	07A0000–07BFFFF
	65	Protection group	256/128	07C0000–07DFFFF
	66	Protection group	64/32	07E0000–07E7FFF
	67	Protection group	64/32	07E8000–07EFFFF
	68	Protection group	64/32	07F0000–07F7FFF
	69	Protection group	64/32	07F8000–07FFFFF

Appendix B Common flash interface (CFI)

The common flash interface is a JEDEC approved, standardized data structure that can be read from the flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the Read CFI Query command is issued, the memory enters read CFI query mode and read operations output the CFI data. *Table 38*, *Table 39*, *Table 40*, *Table 41*, *Table 42* and *Table 43* show the addresses (A0-A7) used to retrieve the data. The CFI data structure also contains a security area where a 64-bit unique security number is written (see *Table 43: Security code area*). This area can be accessed only in read mode by the final user. It is impossible to change the security number after it has been written by Numonyx.

Table 38. Query structure overview(1)

Address		Sub-section name	Description
x16	x8		
10h	20h	CFI query identification string	Command set ID and algorithm data offset
1Bh	36h	System interface information	Device timing & voltage information
27h	4Eh	Device geometry definition	Flash device layout
40h	80h	Primary algorithm-specific extended query table	Additional information specific to the primary algorithm (optional)
61h	C2h	Security code area	64-bit unique device number

1. Query data are always presented on the lowest order data outputs.

Table 39. CFI query identification string(1)

Address		Data	Description	Value
x16	x8			
10h	20h	0051h	Query unique ASCII string ‘QRY’	‘Q’
11h	22h	0052h		‘R’
12h	24h	0059h		‘Y’
13h	26h	0002h	Primary algorithm command set and control interface ID code 16 bit ID code defining a specific algorithm	Spansion compatible
14h	28h	0000h		
15h	2Ah	0040h	Address for primary algorithm extended query table (see *Table 42*)	P = 40h
16h	2Ch	0000h		
17h	2Eh	0000h	Alternate vendor command set and control interface ID code second vendor - specified algorithm supported	NA
18h	30h	0000h		
19h	32h	0000h	Address for alternate algorithm extended query table	NA
1Ah	34h	0000h		

1. Query data are always presented on the lowest order data outputs (DQ7-DQ0) only. DQ8-DQ15 are ‘0’.

Table 40. CFI query system interface information(1)

Address		Data	Description	Value
x16	x8			
1Bh	36h	0027h	V_{CC} logic supply minimum program/erase voltage bit 7 to 4 value in volts bit 3 to 0 value in 100 mV	2.7 V
1Ch	38h	0036h	V_{CC} logic supply maximum program/erase voltage bit 7 to 4BCD value in volts bit 3 to 0BCD value in 100 mV	3.6 V
1Dh	3Ah	00B5h	V_{PPH} [programming] supply minimum program/erase voltage bit 7 to 4 value in volts bit 3 to 0 value in 100 mV	11.5 V
1Eh	3Ch	00C5h	V_{PPH} [programming] supply maximum program/erase voltage bit 7 to 4 value in volts bit 3 to 0 value in 100 mV	12.5 V
1Fh	3Eh	0004h	1Fh 3Eh 0004h typical timeout for single byte/word program = 2^n µs	16 µs
20h	40h	0004h	20h 40h 0004h typical timeout for minimum size write buffer program = 2^n µs	16 µs
21h	42h	000Ah	Typical timeout for individual block erase = 2^n ms	1 s
22h	44h	0010h	Typical timeout for full Chip Erase = 2^n ms	40 s
23h	46h	0004h	Maximum timeout for word program = 2^n times typical	200 µs
24h	48h	0004h	Maximum timeout for write buffer program = 2^n times typical	200 µs
25h	4Ah	0004h	Maximum timeout per individual block erase = 2^n times typical	4.6 s
26h	4Ch	0004h	Maximum timeout for Chip Erase = 2^n times typical	400 s

1. The values given in the above table are valid for both packages.

Table 41. Device geometry definition

Address		Data	Description	Value
x16	x8			
27h	4Eh	0018h	Device size = 2^n in number of bytes	16 Mbytes
28h 29h	50h 52h	0002h 0000h	Flash device interface code description	x8, x16 async.
2Ah 2Bh	54h 56h	0006h 0000h	Maximum number of bytes in multiple-byte program or page= 2^n	64
2Ch	58h	0003h	Number of erase block regions. It specifies the number of regions containing contiguous erase blocks of the same size.	3
2Dh 2Eh	5Ah 5Ch	0003h 0000h	Erase block region 1 information 2Dh-2Eh: number of erase blocks of identical size.	4 blocks 64 Kbytes
2Fh 30h	5Eh 60h	0000h 0001h	Erase block region 1 information 2Fh-30h: block size (n*256 bytes)	4 blocks 64 Kbytes
31h 32h 33h 34h	62h 64h 66h 68h	003Dh 0000h 0000h 0004h	Erase block region 2 information	62 blocks 256 Kbytes
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0003h 0000h 0000h 0001h	Erase block region 3 information	4 blocks 64 Kbytes
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase block region 4 information	NA

Table 42. Primary algorithm-specific extended query table (1)

Address		Data	Description	Value
x16	x8			
40h	80h	0050h	Primary algorithm extended query table unique ASCII string ‘PRI’	‘P’
41h	82h	0052h		‘R’
42h	84h	0049h		‘I’
43h	86h	0031h	Major version number, ASCII	‘1’
44h	88h	0033h	Minor version number, ASCII	‘3’
45h	8Ah	000Dh	Address sensitive unlock (bits 1 to 0) 00 = required, 01= not required Silicon revision number (bits 7 to 2)	Yes, 90 nm
46h	8Ch	0002h	Erase Suspend 00 = not supported, 01 = read only, 02 = read and write	2
47h	8Eh	0001h	Block protection 00 = not supported, x = number of blocks per group	1
48h	90h	0000h	Temporary block unprotect 00 = not supported, 01 = supported	Not supported
49h	92h	0008h	Block protect /unprotect 08 = M29DW127G	8
4Ah	94h	003Bh	Simultaneous operations: x= block number (excluding bank A)	59
4Bh	96h	0000h	Burst mode, 00 = not supported, 01 = supported	Not supported
4Ch	98h	0002h	Page mode, 00 = not supported, 02 = 8-word page	Yes
4Dh	9Ah	00B5h	V_{PPH} [programming/erasing] supply minimum program/erase voltage bit 7 to 4 value in volts bit 3 to 0 value in 100 mV	11.5 V
4Eh	9Ch	00C5h	V_{PPH} [programming/erasing] supply maximum program/erase voltage bit 7 to 4 value in volts bit 3 to 0 value in 100 mV	12.5 V
4Fh	9Eh	0001h	01 = dual boot	Dual boot
50h	A0h	0001h	Program suspend, 00 = not supported, 01 = supported	Supported
51h	A2h	0001h	Unlock bypass: 00 = not supported, 01 = supported	Supported
52h	A4h	0008h	Extended memory block size (customer lockable), 2^n bytes	256
57h	AEh	0004h	Bank organization, 00 = data at 4Ah is 0, x= bank number	4
58h	B0h	000Bh	Bank A information, x = number of blocks in bank A	11
59h	B2h	0018h	Bank B information, x = number of blocks in bank B	24
5Ah	B4h	0018h	Bank C information, x = number of blocks in bank C	24
5Bh	B6h	000Bh	Bank D information, x = number of blocks in bank D	11

1. The values given in the above table are valid for both packages.

Table 43. Security code area

Address		Data	Description	Value
x16	x8			
61h	C3h, C2h	XXXX	XXXX	64 bit: unique device number
62h	C5h, C4h	XXXX	XXXX	
63h	C7h, C6h	XXXX	XXXX	
64h	C9h, C8h	XXXX	XXXX	

Appendix C Extended memory block

The M29DW127G has an extra block, the extended memory block, that can be accessed using a dedicated command. This extended memory block is 256 words (x16 mode) and 512 bytes (x8 mode). It is used as a security block (to provide a permanent security identification number) or to store additional information.

The extended memory block is divided into two memory areas of 256 bytes / 128 words each:

- The first one is factory locked.
- The second one is customer lockable. It is up to the customer to protect it from program operations. Its status is indicated by bit DQ6 and DQ7. When DQ7 is set to '1' and DQ6 to '0', it indicates that this second memory area is customer lockable. When DQ7 and DQ6 are both set to '1', it indicates that the second part of the extended memory block is customer locked and protected from program operations.

Bits DQ6 and DQ7 are the most significant bits in the extended block protection indicator and a specific procedure must be followed to read it. See *Section 4.2: Verify extended memory block protection indicator* and *Table 9: Block protection (16-bit mode)* for details of how to read bit DQ7.

The extended memory block can only be accessed when the device is in extended block mode. For details of how the extended block mode is entered and exited, refer to the *Section 7.1.10: Program command* and *Section 7.3.2: Exit Extended Memory Block command*, and to *Table 17: Block protection commands (16-bit mode)*.

C.1 Factory locked section of extended memory block

The first section of the extended memory block is permanently protected from program operations and cannot be unprotected. The random number, electronic serial number (ESN) and security identification number (see *Table 44: Extended memory block address and data*) are written in this section in the factory.

C.2 Customer lockable section of extended memory block

The device is delivered with the second section of the extended memory block ‘customer lockable’: bits DQ7 and DQ6 are set to '1' and '0' respectively. It is up to the customer to program and protect this section of the extended memory block but care must be taken because the protection is not reversible.

This section can be protected by setting the extended memory block protection bit, DQ0, to ‘0’.

Bit DQ6 of the extended block protection indicator is automatically set to '1' to indicate that the second section of the extended memory block is customer locked.

Once the extended memory block is programmed and protected, the Exit Extended Block command must be issued to exit the extended block mode and return the device to read mode.

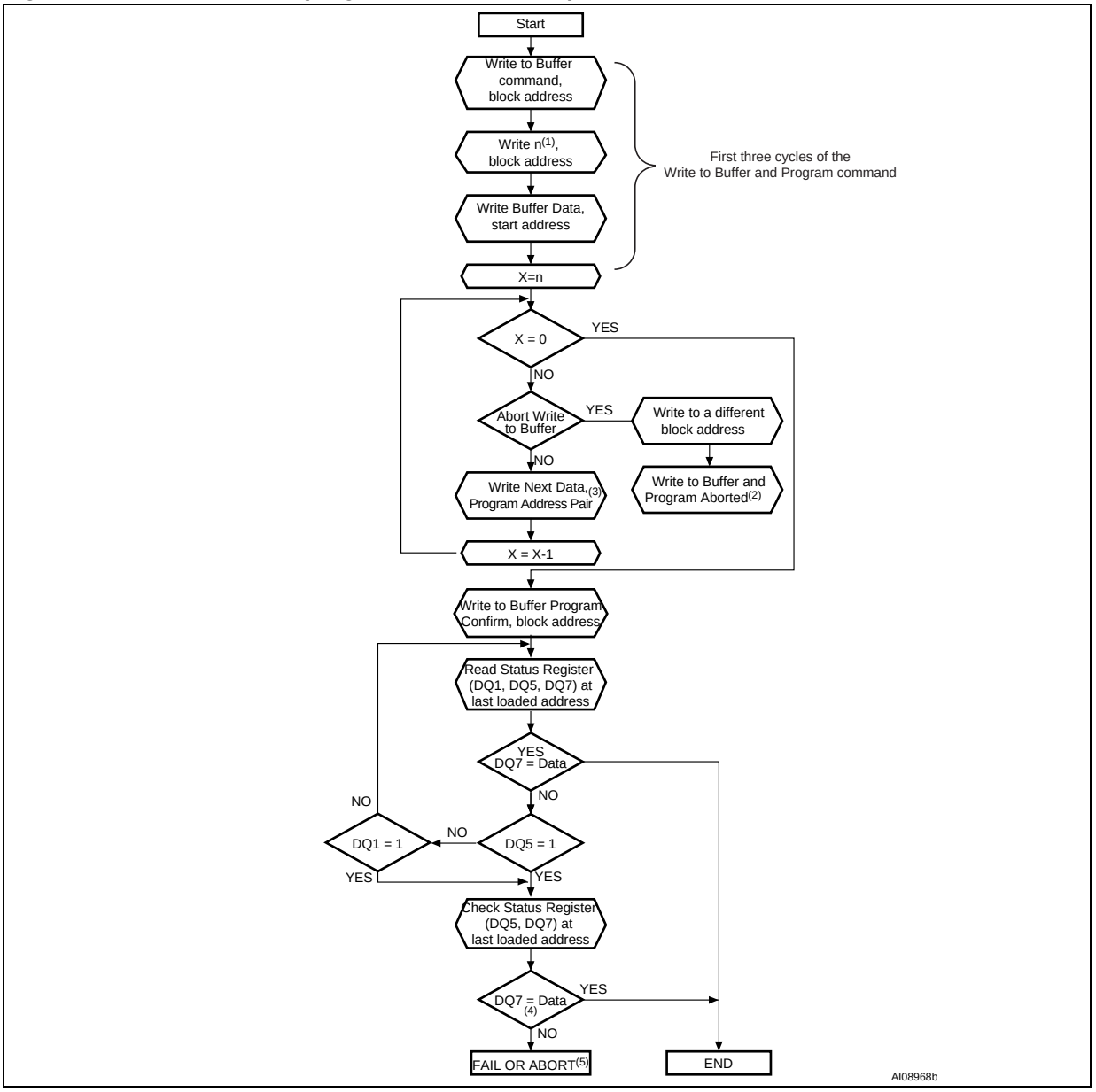
Table 44. Extended memory block address and data

Device	Address(1)	Data	
		Factory locked	Customer lockable
M29DW127G	000000h-00007Fh	Random number, ESN(2), security identification number	Unavailable
	000080h-0000FFh	Unavailable	Determined by customer

1. See *Table 37: Block addresses*.
2. ESN = electronic serial number.

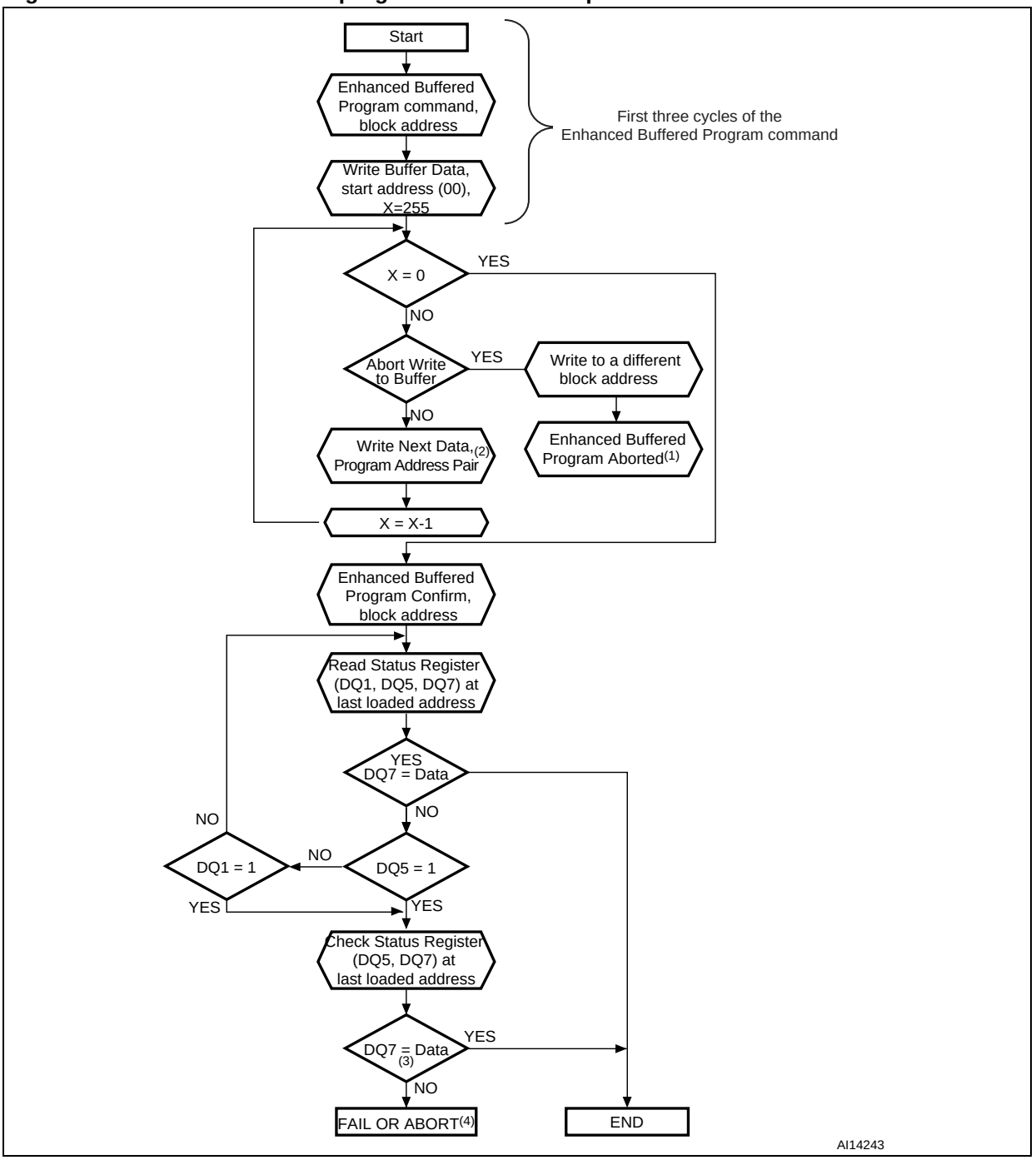
Appendix D Flowcharts

Figure 29. Write to buffer program flowchart and pseudocode



1. n+1 is the number of addresses to be programmed.
2. A write to buffer program abort and reset must be issued to return the device in read mode.
3. When the block address is specified, any address in the selected block address space is acceptable. However when loading write buffer address with data, all addresses must fall within the selected write buffer page.
4. DQ7 must be checked since DQ5 and DQ7 may change simultaneously.
5. If this flowchart location is reached because DQ5='1', then the Write to Buffer Program command failed. If this flowchart location is reached because DQ1='1', then the Write to Buffer Program command aborted. In both cases, the appropriate Reset command must be issued to return the device in read mode: a Reset command if the operation failed, a Write to Buffer Program Abort and Reset command if the operation aborted.
6. See *Table 12: Standard commands (16-bit mode)*, for details on Write to Buffer Program command sequence.

Figure 30. Enhanced buffered program flowchart and pseudocode



1. A buffered program abort and reset must be issued to return the device in read mode.
2. When the block address is specified, all the addresses in the selected block address space must be issued starting from (00). Furthermore, when loading write buffer address with data, data program addresses must be consecutive.
3. DQ7 must be checked since DQ5 and DQ7 may change simultaneously.
4. If this flowchart location is reached because DQ5='1', then the Enhanced Buffered Program command failed. If this flowchart location is reached because DQ1='1', then the Enhanced Buffered Program command aborted. In both cases, the appropriate reset command must be issued to return the device in read mode: a Reset command if the operation failed, a Buffered Program Abort and Reset command if the operation aborted.
5. See *Table 15: Enhanced buffered program commands*, for details on Enhanced Buffered Program command sequence.

14 Revision history

Table 45. Document revision history

Date	Version	Revision details
20-Oct-2008	1	Initial release.
28-Oct-2008	2	Revised the *Appendix B: Common flash interface (CFI)* to include both x16 and x8 information. Revised the following data in *Table 40: CFI query system interface information*: – at address 1Dh changed data column from 0085h to 00B5h and value column from 8.5 V to 11.5 V. – at address 1Eh changed data column 0095h to 00C5h and value column from 9.5 V to 12.5 V. Revised the following data in In *Table 42: Primary algorithm-specific extended query table*: – at address 4Dh changed data column from 0085h to 00B5h and value column from 8.5 V to 11.5 V. – at address 4Eh changed data column 0095h to 00C5h and value column from 9.5 V to 12.5 V.
5-May-2009	3	Corrected order information table.

Please Read Carefully:

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