Data Sheet

Rev. 2.00 / December 2012

ZSC31150

Fast Automotive Sensor Signal Conditioner

Precise and Deliberate

ZSC31150

Fast Automotive Sensor Signal Conditioner

Brief Description

The ZSC31150 is a CMOS integrated circuit for highly accurate amplification and sensor-specific correction of bridge sensor signals. Digital compensation of sensor offset, sensitivity, temperature drift, and non-linearity is accomplished via an internal 16-bit RISC microcontroller running a correction algorithm, with calibration coefficients stored in an EEPROM.

The ZSC31150 is adjustable to nearly all bridge sensor types. Measured values are provided at the analog voltage output or at the digital ZACwire™ and I²C™* interface. The digital interface can be used for a simple PC-controlled calibration procedure in order to program a set of calibration coefficients into an on-chip EEPROM. A specific sensor and a ZSC31150 can be mated digitally: fast, precise, and without the cost overhead associated with trimming by external devices or a laser.

Features

- Digital compensation of sensor offset, sensitivity, temperature drift, and non-linearity
- Adjustable to nearly all bridge sensor types
- Analog gain of 420, overall gain up to 2000
- Output options: ratiometric analog voltage output (5% to 95% maximum, 12.4-bit resolution) or ZACwire™ (digital one-wire-interface)
- Temperature compensation: internal or external diode, bridge resistance, thermistor
- Sensor biasing by voltage or constant current
- Sample rate: up to 7.8 kHz
- High voltage protection up to 33 V
- Supply current: max. 5.5mA
- Reverse polarity and short-circuit protection
- Wide operation temperature depending on part number: up to -40 to +150°C
- Traceability by user-defined EEPROM entries
- Safety and diagnostic functions

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* I²C™ is a trademark of NXP.

Benefits

- No external trimming components required
- Only a few external protection devices needed
- PC-controlled configuration and single pass calibration via I²C™ or ZACwire™ interface: Simple, cost efficient, quick, and precise
- End-of-line calibration via I²C™ or ZACwire™ interface
- High accuracy (0.25% FSO @ -25 to 85°C; 0.5% FSO @ -40 to 125°C)
- The ZSC31150 is optimized for automotive environments by its special protection circuitry and excellent electromagnetic compatibility
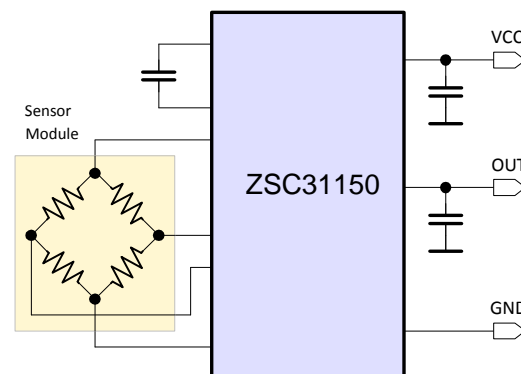
Available Support

- Evaluation Kits
- Application Notes
- Mass calibration setup

Physical Characteristics

- Supply voltage: 4.5 to 5.5 V
- Operation temperature: -40°C to 125°C (-40°C to +150°C de-rated, depending on product version)
- Available in SSOP14 or as die

ZSC31150 Application Circuit

For more information, contact ZMDI via SSC@zmdi.com.

ZSC31150 Block Diagram
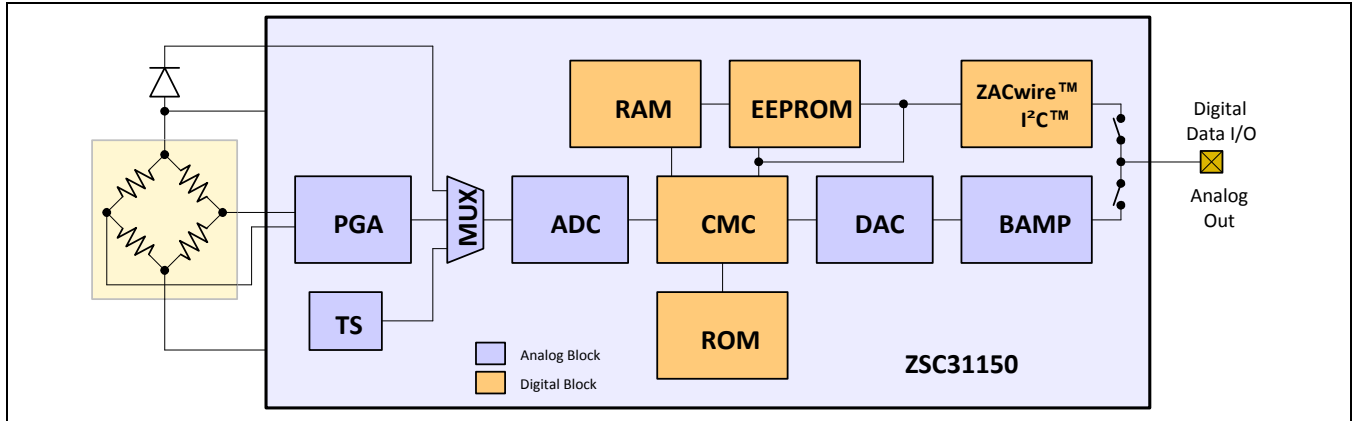
Ordering Information *(Please refer to section 8 in the data sheet for additional options.)*

Product Sales Code	Description	Package
ZSC31150GEB	ZSC31150 Die — Temperature range: -40°C to +150°C	Unsawn on Wafer
ZSC31150GEC	ZSC31150 Die — Temperature range: -40°C to +150°C	Sawn on Wafer Frame
ZSC31150GED	ZSC31150 Die — Temperature range: -40°C to +150°C	Waffle Pack
ZSC31150GEG1	ZSC31150 SSOP-14— Temperature range: -40°C to +150°C	Tube: add "-T" to sales code Reel: add "-R"
ZSC31150KIT Evaluation Kit V1.0	ZSC31150 SSC Evaluation Kit: 3 interconnecting boards, 5 ZSC31150 SSOP-14 samples, USB cable, software/documentation DVD	Kit
ZSC31150 Mass Calibration System V1.1	Modular Mass Calibration System (MSC) for ZSC31150: MCS boards, cable, connectors, DVD with software and documentation	Kit

Sales and Further Information   www.zmdi.com   SSC@zmdi.com

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1 Electrical Characteristics

1.1. Absolute Maximum Ratings

Parameters apply in operation temperature range and without time limitations.

Table 1.1 Absolute Maximum Ratings

No.	Parameter	Symbol	Conditions	Min	Max	Unit
1.1.1	Supply voltage [1]	$VDDE_{AMR}$	To VSSE. Refer to section 3 for application circuits.	-33	33	VDC
1.1.2	Potential at pin AOUT [1]	V_{OUT}	Relative to VSSE	-33	33	VDC
1.1.3	Analog supply voltage [1]	$VDDA_{AMR}$	Relative to VSSA, VDDE - VDDA < 0.35 V	-0.3	6.5	VDC
1.1.4	Voltage at all analog and digital IO pins	V_{A_IO} V_{D_IO}	Relative to VSSA	-0.3	VDDA + 0.3	VDC
1.1.5	Storage temperature	T_{STG}		-55	150	°C

1.2. Operating Conditions

All voltages are related to VSSA.

Table 1.2 Operating Conditions

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.2.1	Ambient temperature [2]	T_{AMB}	TQE	-40		150	°C
1.2.2.1	Ambient temperature advanced performance [3]	T_{AMB_TQA}	TQA	-40		125	°C
1.2.2.2	Ambient temperature advanced performance [3]	T_{AMB_TQI}	TQI	-25		85	°C
1.2.3	Supply voltage	VDDE		4.5	5.0	5.5	VDC
1.2.4	Bridge resistance [3, 4]	R_{BR_V}	Bridge Voltage Mode	2		25	kΩ
1.2.5	Bridge resistance [3, 4]	R_{BR_C}	Bridge Current Excitation; note I_{BR_MAX}			10	kΩ
1.2.6	Resistor R_{IBR} [3]	R_{IBR}	$I_{BR} = VDDA / (16 * R_{IBR})$	$0.07 * R_{BR}$			kΩ
1.2.7	Maximum bridge current	I_{BR_MAX}				2	mA
1.2.8	Maximum bridge top voltage	V_{BR_TOP}				$(^{15}/_{16} * VDDA) - 0.3$	V
1.2.9	TC current reference resistor [3]	TC R_{IBR}	Behavior influences current generated.		50		ppm/K

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1 Refer to the *ZSC31150 High Voltage Protection Description* for specification and detailed conditions.
2 Note: Refer to the temperature profile description in the *ZSC31150 Dice Package Document* for operation in temperature range > 125 °C.
3 No measurement in mass production, parameter is guaranteed by design and/or quality observation.
4 Symmetric behavior and identical electrical properties (especially with regard to the low pass characteristic) of both sensor inputs of the ZSC31150 are required. Unsymmetrical conditions of the sensor and/or external components connected to the sensor input pins of ZSC31150 can generate a failure in signal operation.

1.3. Electrical Parameters

All parameter values are valid for operating conditions specified in section 1.2 (special definitions excluded). All voltages related to VSSA.

Table 1.3   Electrical Parameters

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.1. Supply Current and System Operation Conditions							
1.3.1.1	Supply current	T_{ADV}	Without bridge and load current, $f_{CLK} \leq 3$ MHz			5.5	mA
1.3.1.2	Clock frequency [5]	T_{AMB_TQA}	Guaranteed adjustment range	2	3	4	MHz
1.3.2. Analog Front-End (AFE) Characteristics							
1.3.2.1	Input span	V_{IN_SP}	Analog gain: 420 to 2.8	1		275	mV/V
1.3.2.2	Analog offset compensation range		Depends on gain adjust; refer to section 2.3.2	-300		300	% V_{IN_SP}
1.3.2.3	Parasitic differential input offset current [5]	I_{IN_OFF}	Within T_{AMB}	-10		10	nA
			Within T_{AMB_TQI}	-2		2	nA
1.3.2.4	Common mode input range	V_{IN_CM}	Depends on gain adjustment; no XZC; refer to section 2.3.1	0.29 * VDDA		0.65 * VDDA	V
1.3.3. Temperature Measurement [6]							
1.3.3.1	External temperature diode channel gain	A_{TSED}		300		1300	ppm FS / (mV/V)
1.3.3.2	External temperature diode bias current	I_{TSE}		6	10	20	μA
1.3.3.3	External temperature diode input range [5]			0		1.5	V
1.3.3.4	External temperature resistor channel gain	A_{TSER}		1200		3500	ppm FS / (mV/V)
1.3.3.5	External temperature resistor / input voltage range [5]	V_{TSER}		0		600	mV/V
1.3.3.6	Internal temperature diode sensitivity	ST_{TSI}	Raw values – without conditioning	700		2700	ppm FS / K
1.3.4. A-D Conversion							
1.3.4.1	A/D resolution [5]	r_{ADC}		13		16	Bit
1.3.4.2	DNL [5]	DNL_{ADC}	r_{ADC} =13-Bit, f_{CLK}=3MHz, best fit, 2nd order, complete AFE, 1.3.4.5			0.95	LSB
1.3.4.3	INL TQA [5]	INL_{ADC}				4	LSB
1.3.4.4	INL TQE	INL_{ADC}				5	LSB
1.3.4.5	ADC input range	Range		10		90	%VDDA

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5   No measurement in mass production, parameter is guaranteed by design and/or quality observation.
6   Refer to section 2.4.

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
			1.3.5. Sensor Connection Check				
1.3.5.1	Sensor connection loss	R_{SCC_min}	Detection threshold	100			kΩ
1.3.5.2	Sensor input short	R_{SSC_short}	Short detection guaranteed	0		50	Ω
1.3.5.3	Sensor input no short	R_{SSC_pass}	Short is never detected	1000			Ω
			1.3.6. DAC & Analog Output (AOUT Pin)				
1.3.6.1	D/A resolution	r_{DAC}	Analog output, 10-90%		12		Bit
1.3.6.2	Output current sink and source for VDDE=5V	$I_{SRC/SINK\_OUT}$	V_{OUT}: 5-95%, R_{LOAD}>=2kΩ			2.5	mA
			V_{OUT}: 10-90%, R_{LOAD}>=1kΩ			5	mA
1.3.6.3	Short circuit current	I_{OUT_max}	To VSSE or VDDE [7]	-25		25	mA
1.3.6.4	Addressable output signal range	V_{SR_OUT95}	@ R_{LOAD}>=2kΩ	0.05		0.95	VDDE
		V_{SR_OUT90}	@ R_{LOAD}>=1kΩ	0.1		0.9	VDDE
1.3.6.5	Output slew rate [8]	SR_{OUT}	C_{LOAD} < 50nF	0.1			V/µs
1.3.6.6	Output resistance in diagnostic mode	R_{OUT_DIA}	Diagnostic Range: <4|96>%, R_{LOAD}>=2kΩ <8|92>%, R_{LOAD}>=1kΩ			82	Ω
1.3.6.7	Load capacitance [8]	C_{LOAD}	C3 + CL (see section 3)			150	nF
1.3.6.8	DNL	DNL_{OUT}		-1.5		1.5	LSB
1.3.6.9	INL TQA [8]	INL_{OUT}	Best fit, r_{DAC} =12-Bit	-5		5	LSB
1.3.6.10	INL TQE	INL_{OUT}	Best fit, r_{DAC} =12-Bit	-8		8	LSB
1.3.6.11	Output leakage current @ 150grd	I_{LEAK_OUT}	In case of power or ground loss	-25		25	µA
			1.3.7. System Response				
1.3.7.1	Startup time [9]	t_{STA}	To 1st output, f_{CLK}=3MHz, no ROM check, ADC: 14_bit & 2nd order			5	ms
1.3.7.2	Response time (100% jump) [8]	t_{RESP}	f_{CLK}=4MHz, 13-Bit, 2nd order, refer to Table 2.3	256		512	µs
1.3.7.3	Bandwidth [8]		Comparable to analog SSCs		5		kHz
1.3.7.4	Analog output noise peak-to-peak [8]	$V_{NOISE,PP}$	Shorted inputs, gain= bandwidth $\leq$ 10kHz			10	mV
1.3.7.5	Analog output noise RMS [8]	$V_{NOISE,RMS}$	Shorted inputs, gain= bandwidth $\leq$ 10kHz			3	mV
1.3.7.6	Ratiometricity error	RE_{OUT_5}	Maximum error of VDDE=5V to 4.5/5.5V			1000	ppm

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7   Minimum output voltage to VDDE or maximum output voltage to VSSE.
8   No measurement in mass production, parameter is guaranteed by design and/or quality observation.
9   Depends on resolution and configuration - start routine begins approximately 0.8ms after power on.

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.7.7	Overall failure (deviation from ideal line including INL, gain, offset & temp errors) [10]	F_{ALL} TQI	13-Bit 2nd order ADC, f_{CLK}<=3MHz, XZC=0 No sensor caused effects; value in parentheses is the digital readout.		0.25 (0.1)		% FS
		F_{ALL} TQA			0.5 (0.25)		% FS
		F_{ALL} TQE			1.0 (0.5)		% FS

1.4. Interface Characteristics & EEPROM

Table 1.4 *Interface and EEPROM Characteristics*

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.4.1. I²C^{TM} Interface [11]							
1.4.1.1	Input-high level [12]	$V_{I2C\_IN\_H}$		0.8			VDDA
1.4.1.2	Input-low level [12]	$V_{I2C\_IN\_L}$				0.2	VDDA
1.4.1.3	Output-low level [12]	$V_{I2C\_OUT\_L}$	Open Drain, I_{OL}<2mA			0.15	VDDA
1.4.1.4	SDA load capacitance [12]	C_{SDA}				400	pF
1.4.1.5	SCL clock frequency [12]	f_{SCL}				400	kHz
1.4.1.6	Internal pull-up resistor [12]	R_{I2C}		25		100	kΩ
1.4.2. ZACwire™ One Wire Interface (OWI)							
1.4.2.1	Input-low level [12]	$V_{OWI\_IN\_L}$				0.2	VDDA
1.4.2.2	Input-high level [12]	$V_{OWI\_IN\_H}$		0.75			VDDA
1.4.2.3	Output-low level [12]	$V_{OWI\_OUT\_L}$	Open Drain, I_{OL}<2mA			t.b.d.	VDDA
1.4.2.4	Start window [12]		Typ: @ f_{CLK}=3MHz	96	175	455	ms
1.4.3. EEPROM							
1.4.3.1	Ambient temperature EEPROM programming [12]	T_{AMB_EEP}		-40		150	°C
1.4.3.2	Write cycles [12]	n_{WRI_EEP}	Write temperature: <= 85°C			100k	
			Write temperature: up to 150°C			100	
1.4.3.3	Read cycles [12, 13]	n_{READ_EEP}	Read temperature: <=175°C			$8 * 10^8$	
1.4.3.4	Data retention [12, 14]	t_{RET_EEP}	1300h at 175°C =100000h at 55°C; 27000h at 125°C; 3000h at 150°C)			15	a
1.4.3.5	Programming time [12]	t_{WRI_EEP}	Per written word, f_{CLK}=3MHz		12		ms

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10 XZC is active: additional overall failure of 25ppm/K for XZC=31 at maximum; failure decreases linearly for XZC adjustments lower than 31.
11 Refer to *ZSC31150 Functional Description* for timing details.
12 No measurement in mass production, parameter is guaranteed by design and/or quality observation.
13 Valid for the dice; note that additional package and temperature version cause restrictions.
14 Over lifetime and valid for the dice; use calculation sheet *ZMDI Temperature Profile Calculation Sheet* for temperature stress calculation; note additional restrictions are caused by different package and temperature versions.

2 Circuit Description

2.1. Signal Flow

The ZSC31150's signal path is partly analog and partly digital. The analog part is realized differentially – this means the differential bridge sensor signal is internally handled via two signal lines, which are rejected symmetrically around an internal common mode potential (analog ground = VDDA/2).

Consequently, it is possible to amplify positive and negative input signals, which are located within the common mode range of the signal input.

Figure 2.1   Block Diagram of the ZSC31150
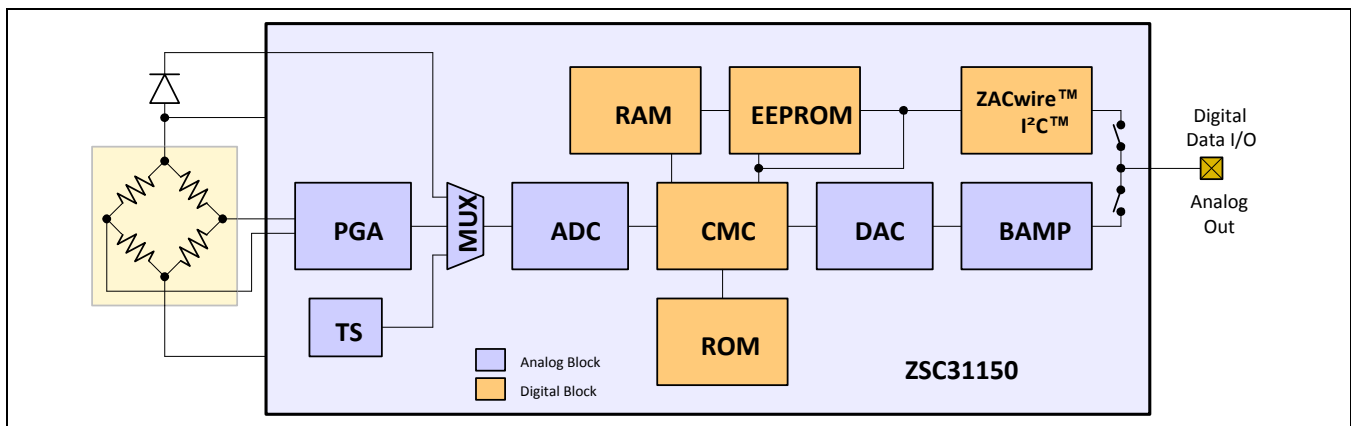
PGA	Programmable Gain Amplifier
MUX	Multiplexer
ADC	Analog-to-Digital Converter
CMC	Calibration Microcontroller
DAC	Digital-to-Analog Converter
BAMP	Buffer Amplifier – output buffer OPAMP
EEPROM	Non Volatile Memory for Calibration Parameters and Configuration
TS	On-chip Temperature Sensor (pn-junction)
ROM	Memory for Correction Formula and –Algorithm
RAM	Volatile Memory for Calibration Parameters and Configuration

The differential signal from the bridge sensor is pre-amplified by the Programmable Gain Amplifier (PGA). The Multiplexer (MUX) transmits the signals from either the bridge sensor, the external diode, or the separate temperature sensor, to the Analog-to-Digital Converter (ADC) in a certain sequence (instead of the temperature diode, the internal pn-junction (TS) can be used optionally). Afterwards, the ADC converts these signals into digital values.

The digital signal correction takes place in the calibration microcontroller (CMC). It is based on a correction formula located in the ROM and on sensor-specific coefficients stored in the EEPROM during calibration. Dependent on the programmed output configuration, the corrected sensor signal is output as an analog value or in a digital format (I²C™ or ZACwire™). The configuration data and the correction parameters can be programmed into the EEPROM via the digital interfaces.

2.2. Application Modes

For each application, a configuration set has to be established (generally prior to calibration) by programming the on-chip EEPROM regarding to the following modes:

- Sensor Channel
  - Sensor Mode: Ratiometric bridge excitation in voltage or current supply mode.
  - Input Range: The gain adjustment of the AFE with respect to the maximum sensor signal span and the zero point of the ADC have to be chosen.
  - Additional Offset Compensation (XZC): The extended analog offset compensation has to be enabled, if required; e.g., if the sensor offset voltage is near to or larger than the sensor span.
  - Resolution/Response Time: The A/D converter has to be configured for resolution and converting scheme or ADC order (first or second order). These settings influence the sampling rate and the signal integration time, and thus, the noise immunity.
- Temperature
  - Temperature Measurement: The source for the temperature correction has to be chosen.

2.3. Analog Front End (AFE)

The Analog Front End (AFE) consists of the Programmable Gain Amplifier (PGA), the Multiplexer (MUX), and the Analog-to-Digital Converter (ADC).

2.3.1. Programmable Gain Amplifier (PGA)

Table 2.1 shows the adjustable gains, the sensor signal spans, and the allowed common mode range.

Table 2.1 Adjustable Gains, Resulting Sensor Signal Spans and Common Mode Ranges

No.	Overall Gain a_{IN}	Max. Span V_{IN_SP} [mV/V] [15]	Gain Amp1	Gain Amp2	Gain Amp3	Input common mode range V_{IN_CM} as % of VDDA [16]	
						XZC = Off	XZC = On
1	420	1.8	30	7	2	29 to 65	45 to 55
2	280	2.7	30	4.66	2	29 to 65	45 to 55
3	210	3.6	15	7	2	29 to 65	45 to 55
4	140	5.4	15	4.66	2	29 to 65	45 to 55
5	105	7.1	7.5	7	2	29 to 65	45 to 55
6	70	10.7	7.5	4.66	2	29 to 65	45 to 55
7	52.5	14.3	3.75	7	2	29 to 65	45 to 55
8	35	21.4	3.75	4.66	2	29 to 65	45 to 55
9	26.3	28.5	3.75	3.5	2	29 to 65	45 to 55
10	14	53.75	1	7	2	29 to 65	45 to 55
11	9.3	80	1	4.66	2	29 to 65	45 to 55
12	7	107	1	3.5	2	29 to 65	45 to 55
13	2.8	267	1	1.4	2	32 to 57	not applicable

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[15] Recommended internal signal range is 75% of supply voltage in maximum.
Span is calculated by the following formula: Span = 75% / gain.

[16] Bridge in voltage mode, containing maximum input signal (with XZC: +300% Offset), 14-bit accuracy. Refer to the *ZSC31150 Functional Description* for usable input signal/common mode range at bridge in current mode.

2.3.2. Offset Compensation

The ZSC31150 supports two methods of sensor offset compensation (zero shift):

- Digital offset correction
- XZC - Analog compensation for large offset values (up to in maximum approximately 300% of span, depending on gain adjustment)

Digital sensor offset correction will be processed during the digital signal correction/conditioning by the calibration microcontroller (CMC). Analog sensor offset pre-compensation will be needed for compensation of large offset values, which would overdrive the analog signal path by uncompensated gaining. For analog sensor offset pre-compensation, a compensation voltage will be added in the analog pre-gaining signal path (coarse offset removal). The analog offset compensation in the AFE can be adjusted by 6 EEPROM bits.

Table 2.2   Analog Zero Point Shift Ranges (XZC)

PGA gain a_{IN}	Max. Span V_{IN_SP} [mV/V]	Offset shift per step in % of full span	Approx. maximum offset shift [mV/V]	Approx. maximum shift [% V_{IN_SP}] (@ ± 31)
420	1.8	12.5 %	7.8	388 %
280	2.7	7.6 %	7.1	237 %
210	3.6	12.5 %	15.5	388 %
140	5.4	7.6 %	14.2	237 %
105	7.1	12.5 %	31	388 %
70	10.7	7.6 %	28	237 %
52.5	14.3	12.5 %	32	388 %
35	21.4	7.6 %	57	237 %
26.3	28.5	5.2 %	52	161 %
14	53.75	12.5 %	194	388 %
9.3	80	7.6 %	189	237 %
7	107	5.2 %	161	161 %
2.8	267	0.83 %	72	26 %

2.3.3. Measurement Cycle

The Multiplexer selects, depending on EEPROM settings, the following inputs in a certain sequence.

- Temperature measured by external diode or thermistor, internal pn-junction or bridge
- Internal offset of the input channel (V_{OFF})
- Pre-amplified bridge sensor signal

The complete measurement cycle is controlled by the CMC. The cycle diagram at Figure 2.2 shows its principle structure.

The EEPROM adjustable parameters are:

   n=<1,31>: Bridge sensor measurement count

After power on the start routine is called, that contains all needed measurements once.

Remark: The tasks "CMV," "SSC/SCC+" and "SSC/SCC-" are always contained independently from EEPROM configuration in every cycle.

Figure 2.2   Measurement Cycle

```
                              Start routine

                    1         Temperature auto-zero
              →     n         Bridge sensor measurement
              →     1         Temp measurement
              →     n         Bridge sensor measurement
              →     1         Bridge sensor auto-zero
              →     n         Bridge sensor measurement
              →     1         CMV
              →     n         Bridge sensor measurement
              →     1         SSC/SCC+
              →     n         Bridge sensor measurement
              →     1         SSC/SCC-
              →     n         Bridge sensor measurement
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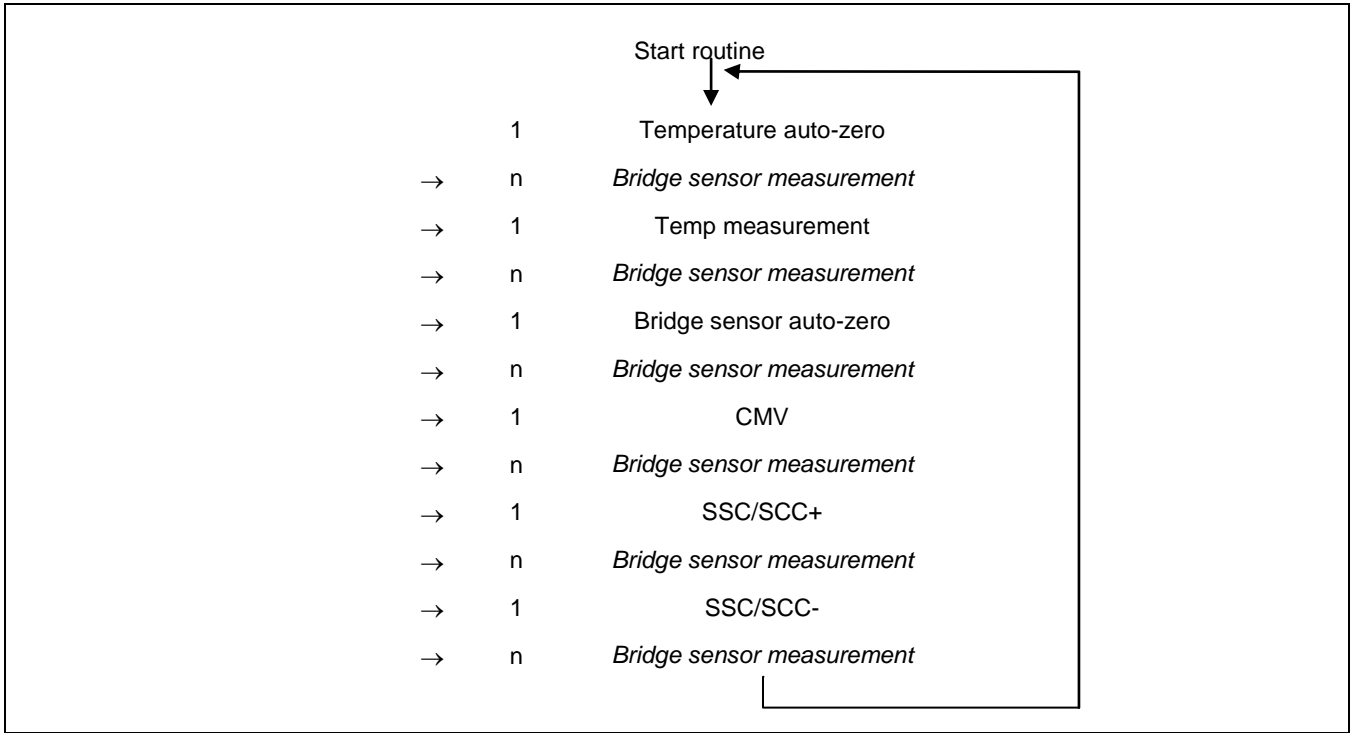
2.3.4.   Analog-to-Digital Converter

The ADC is an integrating analog-to-digital converter in full differential switched capacitor technique.

Programmable ADC resolutions are r_{ADC}=<13, 14> and with segmentation <15, 16> bit.

It can be used as first or second order converter. In the **first order** mode it is inherently monotone and insensitive against short and long-term instability of the clock frequency. The conversion cycle time depends on the desired resolution and can be roughly calculated by the following equation:

$$t_{CYC\_1} = 2^r / 2 / f_{CLK}$$

In the **second order** mode two conversions are stacked with the advantage of much shorter conversion cycle time and the drawback of a lower noise immunity caused by the shorter signal integration period. The conversion cycle time at this mode is roughly calculated by the following equation:

$$t_{CYC\_2} = 2^{(r+3)/2} / 2 / f_{CLK}$$

The calculation formulas give an overview about conversion time for one AD-conversion. Refer to the calculation worksheet *ZSC31150 Bandwidth Calculation Sheet* for detailed calculation of sampling time and bandwidth.

The result of the AD conversion is a relative counter result corresponding to the following equation:

$$Z_{ADC} = 2^r * (V_{ADC\_DIFF} / V_{ADC\_REF} - RS_{ADC})$$

Where

Z_{ADC}:   number of counts (result of the conversion)

r: adjusted resolution in bit

V_{ADC/REF_DIFF}: differential input/reference voltage of ADC

RS_{ADC}:   digital ADC Range Shift ($RS_{ADC} = {}^1/_{16}, {}^1/_8, {}^1/_4, {}^1/_2$, controlled by the EEPROM content)

With the RS_{ADC} value a sensor input signal can be shifted in the optimal input range of the ADC.

Table 2.3   Analog Output Resolution Versus Sample Rate

ADC Adjustment		Approximated Output Resolution [17]		Sample Rate f_{CON} [18]		Averaged Bandwidth @	
Order	r_{ADC}	Digital	Analog	f_{CLK}=3MHz	f_{CLK}=4MHz	f_{CLK}=3MHz	f_{CLK}=4MHz
O_{ADC}	[Bit]	[Bit]	[Bit]	[Hz]	[Hz]	[Hz]	[Hz]
1	13	13	12	345	460	130	172
	14	14	12	178	237	67	89
	15	14	12	90	120	34	45
	16	14	12	45	61	17	23
2	13	13	12	5859	7813	2203	2937
	14	14	12	3906	5208	1469	1958
	15	14	12	2930	3906	1101	1468
	16	14	12	1953	2604	734	979

Note: ADCs reference voltage ADC_{VREF} is defined by the potential between <VBR_T> and <VBR_B> (or <VDDA> to <VSSA>, if CFGAPP:BREF=1). The theoretically input range ADC_{RANGE_INP} of the ADC is equivalent to ADCs reference voltage.

In practice ADCs input range should be used in maximum from 10% to 90% of ADC_{RANGE_INP} - a necessary condition for abiding specified accuracy, stability, and nonlinearity parameters of AFE. This condition is also valid for whole temperature range and all applicable sensor tolerances. Inside of ZSC31150 is no failsafe task implemented, which verifies abiding of this condition.

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17 ADC resolution should be one bit higher then applied output resolution, if AFE gain is adjusted in such manner, that input range is used more than 50%. Otherwise ADC resolution should be more than one bit higher than applied output resolution.
18 The sampling rate (AD conversion time) is only a part of the whole cycle, refer to *ZSC31150 Bandwidth Calculation Sheet* for detailed information

2.4. Temperature Measurement

The ZSC31150 supports four different methods for temperature data acquiring needed for calibration of the sensor signal in temperature range.

Temperature data can be acquired using

- an internal pn-junction temperature sensor,
- an external pn-junction temperature sensor connected to sensor top potential (V_{BRTOP}),
- an external resistive half bridge temperature sensor and
- the temperature coefficient of the sensor bridge at bridge current excitation.

Refer to *ZSC31150 Functional Description* for a detailed explanation of temperature sensor adaptation and adjustment.

2.5. System Control and Conditioning Calculation

The system control supports the following tasks/features:

- control the measurement cycle regarding to the EEPROM-stored configuration data
- 16 bit correction calculation for each measurement signal using the EEPROM stored calibration coefficients and ROM-based algorithms = signal conditioning
- manage start up sequence and start signal conditioning
- handle communication requests received by the digital interface
- failsafe tasks for the functions of ZSC31150 and message detected errors with diagnostic states

Refer to *ZSC31150 Functional Description* for a detailed description.

2.5.1. Operation Modes

The internal state machine represents three main states:

- the continuous running signal conditioning mode – called Normal Operation Mode: NOM
- the calibration mode with access to all internal registers and states – called Command Mode: CM
- the failure messaging mode – called Diagnostic Mode: DM

2.5.2. Start Up Phase[19]

The start-up phase consists of following parts:

1. internal supply voltage settling phase (=potential VDDA-VSSA) – finished by disabling the reset signal through the power on clear block (POC). Refer to *ZSC31150 High Voltage Protection Description,* section 4 for power on/off thresholds.
   Time (for beginning with VDDA-VSSA=0V): 500µs to 2000µs, AOUT: tristate
2. system start, EEPROM read out and signature check (and ROM-check, if CFGAPP:CHKROM=1).
   Time: ~200µs (~9000µs with ROM-check – 28180clocks), AOUT: LOW (DM)
3. processing the start routine of signal conditioning (all measures & conditioning calculation).
   Time: 5x AD conversion time, AOUT behavior depending on adjusted OWI mode (refer to 2.6):
   - OWIANA & OWIDIS => AOUT: LOW (DM)
   - OWIWIN & OWIENA => AOUT: tristate

The analog output AOUT will be activated at the end of start-up phase depending on adjusted output and communication mode (refer to section 2.6). In case of detected errors Diagnostic Mode (DM) is activated and diagnostic output signal is driven at the output.

After the start-up phase the continuous running measurement and calibration cycle is started. Refer to *ZSC31150 Bandwidth Calculation Sheet* for detailed information about output update rate.

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19 All timings described are roughly estimated values and correlates with internal clock frequency. Timings estimated for fclk=3MHz.

2.5.3. Conditioning Calculation

The digitalized value for bridge sensor measurement (acquired raw data) is processed with the correction formula to remove offset and temperature dependency and to compensate non-linearity up to 3rd order. The result of the correction calculation is a non-negative 15-bit value for bridge sensor (P) in the range [0; 1]. This value P is clipped with programmed limitation coefficients and continuously written to the output register of the digital serial interface and the output DAC.

Note: The conditioning includes up to third order nonlinearity sensor input correction. The available adjustment ranges depend on the specific calibration parameters, for a detailed description, refer to *ZSC31150 Functional Description.* To give a rough idea: Offset compensation and linear correction are only limited by the loose of resolution it will cause, the second order correction is possible up to about 30% full scale difference to straight line, third order up to about 20% (ADC resolution = 13bit). The used calibration principle is able to reduce present nonlinearity errors of the sensor up to 90%. The temperature calibration includes first and second order correction and should be fairly sufficient in all relevant cases. ADC resolution influences also calibration possibilities – 1 bit more resolution reduces calibration range by approximately 50%. Calculation input data width is in maximum 14bit. 15 & 16bit ADC resolution mode uses only a 14 bit segment of ADC range.

2.6. Analog Output AOUT

The analog output is used for output the analog signal conditioning result and for "End of Line" communication via the ZACwire^{TM} interface (one wire communication interface - OWI). The ZSC31150 supports four different modes of the analog output in combination with OWI behavior:

- OWIENA: analog output is deactivated, OWI communication is enabled
- OWIDIS: analog output is active (~2ms after power on), OWI communication is disabled
- OWIWIN: analog output will be activated after time window,
  OWI communication is enabled in time window of ~500ms in maximum,
  transmission of "START_CM" command has to be finished during time window
- OWIANA: analog output will be activated after ~2ms power on time,
  OWI communication is enabled in time window of ~500ms in maximum,
  transmission of "START_CM" command has to be finished during time window,
  to communicate the internal driven potential at AOUT has to be overwritten
  by the external communication master (AOUT drive capability is current limited)

The analog output potential is driven by a unity gain output buffer, those input signal is generated by a 12.4-bit resistor string DAC. The output buffer (BAMP) – a rail-to-rail OPAMP - is offset compensated and current limited. So a short-circuit of analog output to ground or power supply does not damage the ZSC31150.

2.7. Serial Digital Interface

The ZSC31150 includes a serial digital interface (SIF), which is used for communication with the circuit to realize calibration of the sensor module. The serial interface is able to communicate with two communication protocols – I²C™ and ZACwire™ (a one-wire communication interface – also called OWI). The OWI can be used to realize an "End of Line" calibration via the analog output AOUT of the complete assembled sensor module.

Refer to *ZSC31150 Functional Description* for a detailed description of the serial interfaces and communication protocols.

2.8.   Failsafe Features, Watchdog and Error Detection

The ZSC31150 detects various possible errors. A detected error is signalized by changing the internal status in diagnostic mode (DM). In this case the analog output is set to LOW (minimum possible output value = lower diagnostic range – LDR) and the output registers of the digital serial interface are set to a significant error code.

A watchdog oversees the continuous working of the CMC and the running measurement loop. The operation of the internal clock oscillator is verified continuously by oscillator fail detection.

A check of the sensor bridge for broken wires is done permanently by two comparators watching the input voltage of each input (sensor connection and short check). Additionally the common mode voltage of the sensor and sensor input short is watched permanently (sensor aging).

Different functions and blocks in digital part - like RAM-, ROM-, EEPROM- and register content - are watched continuously. Refer to *ZSC31150 Functional Description* for a detailed description of safety features and methods of error messaging.

2.9.   High Voltage, Reverse Polarity and Short Circuit Protection

The ZSC31150 is designed for 5V power supply operation.

The ZSC31150 and the connected sensor are protected from overvoltage and reverse polarity damage by an internal supply voltage limiter. The analog output AOUT can be connected (short circuit, overvoltage and reverse) with all potentials in protection range under all potential conditions at the pins VDDE and VSSE.

All external components – explained in application circuit in section 3 – are required to guarantee this operation. The protection is no time limited. Refer to *ZSC31150 High Voltage Protection Description* for a detailed description of protection cases and conditions.

3 Application Circuit Examples

The application circuits contain external components, which are needed for overvoltage, reverse polarity, and short circuit protection.

Note: Check also the available ZSC31150 Application Notes for application examples and board layout.

Table 3.1   Application Circuit Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
C1	C	100		470	nF	
C2	C	100			nF	
C3 [20, 21]	C	4	47	160	nF	The value of C3 is the sum of the load capacitor and the cable capacitance
C4, C5 [21]	C	0		10	nF	Recommended to increase EMC immunity. The value of C4, C5 is the sum of the load capacitor and the cable capacitance
R1			10		kΩ	
R_{IBR}	R		Refer to section 1.2.		Ω	

Figure 3.1   Bridge in Voltage Mode, External Diode Temperature Sensor

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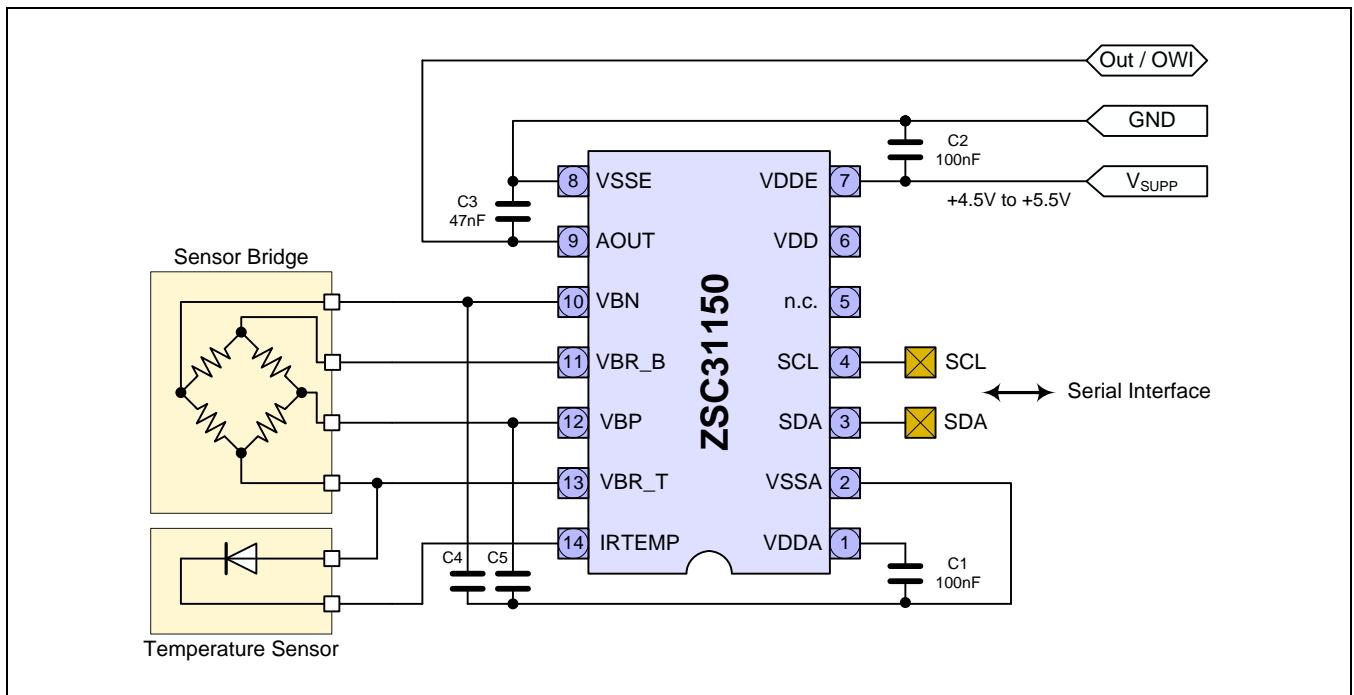
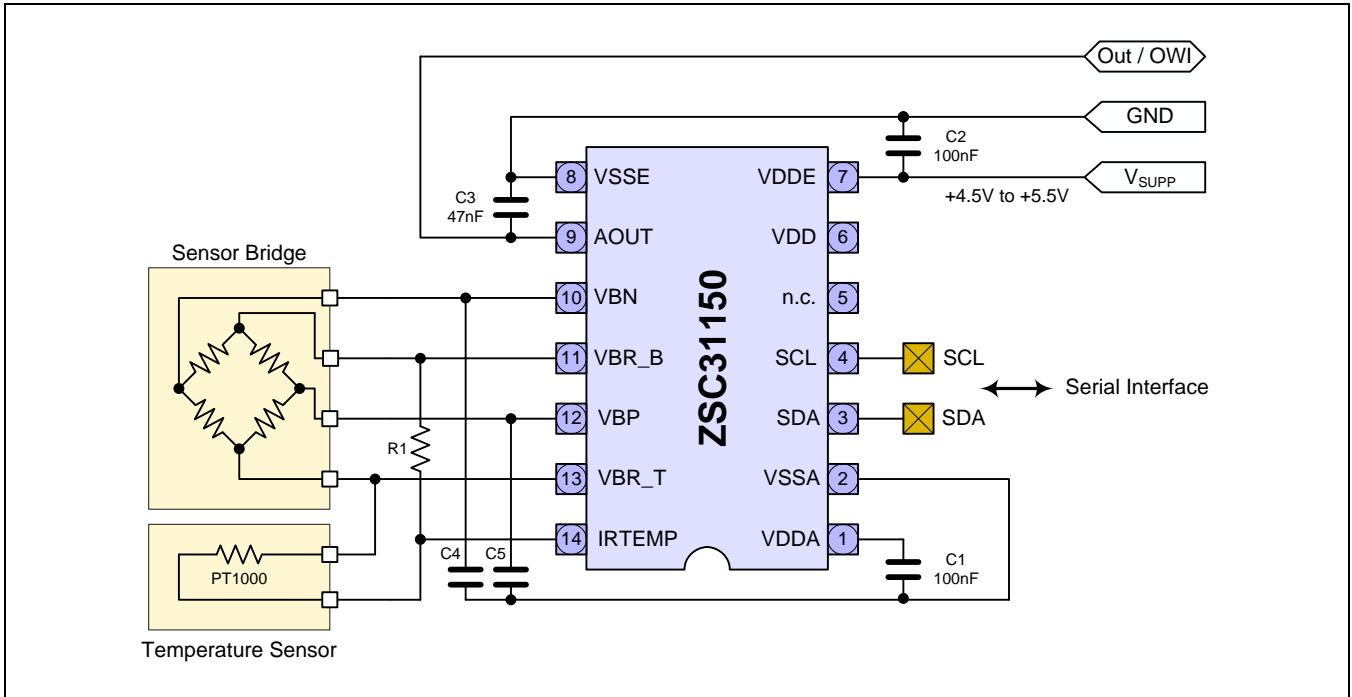[20] Value of C3 summarizes load capacitor and cable capacity.
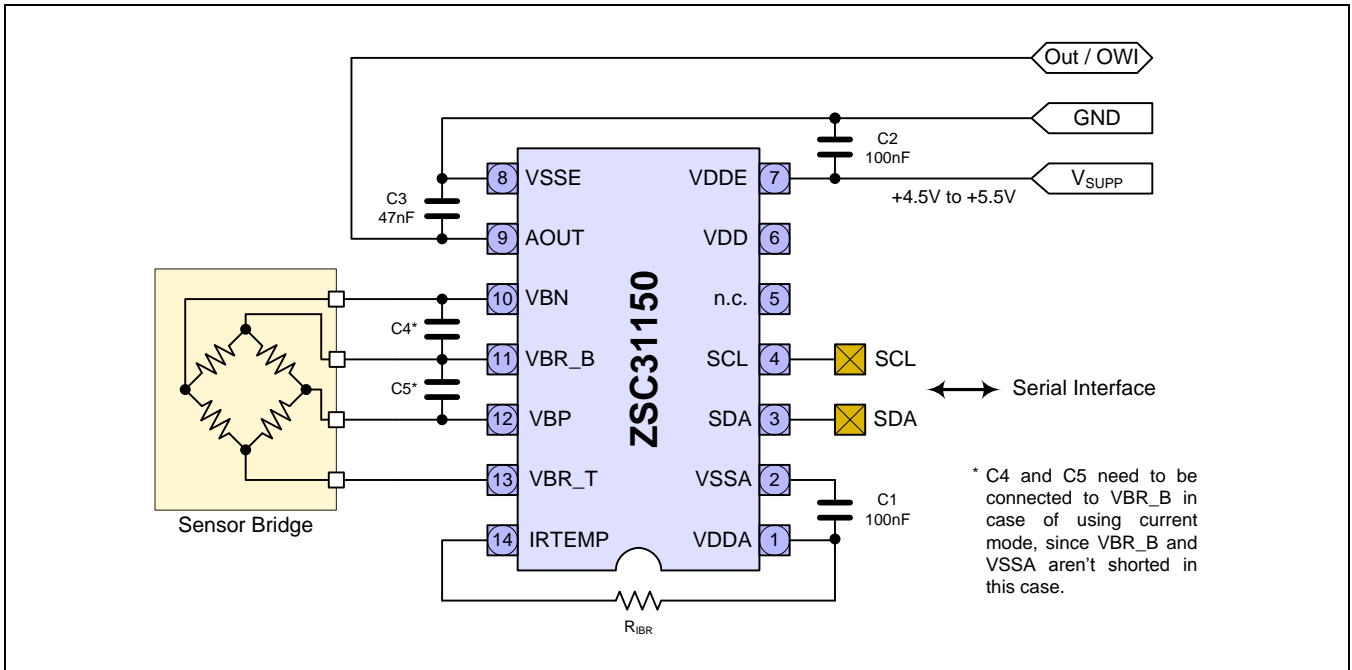[21] Higher values for C3, C4 and C5 increase EMC immunity.

Figure 3.2   Bridge in Voltage Mode, External Thermistor

Figure 3.3   Bridge in Current Mode, Temperature Measurement via Bridge TC

* C4 and C5 need to be connected to VBR_B in case of using current mode, since VBR_B and VSSA aren't shorted in this case.

4 Pin Configuration, Latch-Up and ESD Protection

4.1. Pin Configuration and Latch-up Conditions

Table 4.1   Pin Configuration and Latch-Up Conditions

Pin	Name	Description	Remarks	Usage/ Connection [22]	Latch-up Related Application Circuit Restrictions and/or Remarks
1	VDDA	Positive analog supply voltage	Analog IO	Required/-	
2	VSSA	Negative analog supply voltage	Analog IO	Required/-	
3	SDA	I²C™ data IO	Digital IO, pull-up	-/VDDA	Trigger Current/Voltage to VDDA/VSSA: +/-100mA or 8/-4V
4	SCL	I²C™ clock	Digital IN, pull-up	-/VDDA	
5	N.C.	No connection			
6	VDD	Positive digital supply voltage	Analog IO	Required or open/-	only capacitor to VSSA is allowed, otherwise no application access
7	VDDE	Positive external supply voltage	Supply	Required/-	Trigger Current/Voltage: -100mA/33V
8	VSSE	Negative external supply voltage	Ground	Required/-	
9	AOUT	Analog output & one wire IF IO	IO	Required/-	Trigger Current/Voltage: -100mA/33V
10	VBN	Negative input sensor bridge	Analog IN	Required/-	
11	VBR_B	Bridge bottom potential	Analog IO	Required/VSSA	Depending on application circuit, short to VDDA/VSSA possible
12	VBP	Positive input sensor bridge	Analog IN	Required/-	
13	VBR_T	Bridge top potential	Analog IO	Required/VDDA	
14	IRTEMP	Temp sensor & current source resistor	Analog IO	-/VDDA, VSSA	Depending on application circuit

4.2. ESD Protection

All pins have an ESD Protection of >2000V. Additionally the pins VDDE, VSSE and AOUT have an ESD Protection of >4000V.

ESD protection referred to the Human Body Model is tested with devices in SSOP14 packages during product qualification. The ESD test follows the human body model with 1.5kOhm/100pF based on MIL 883, Method 3015.7.

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22 Usage: If "Required" is specified, an electrical connection is necessary – refer to the application circuits.
   Connection: To be connected to this potential, if not used or no application/configuration related constraints are given.
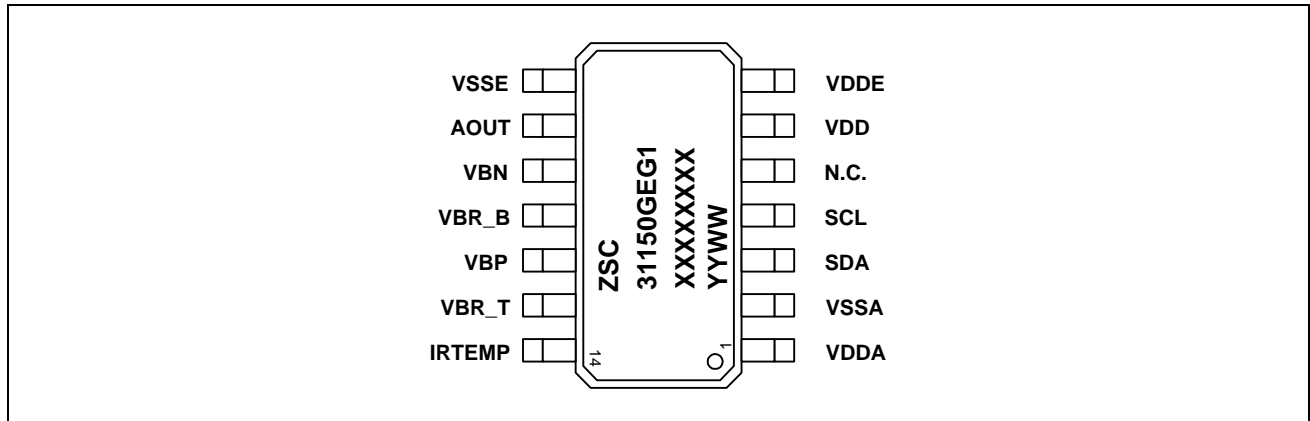
5 Package

The standard package of the ZSC31150 is an SSOP14 green package (5.3mm body width) with a lead pitch of 0.65 mm. For the package markings shown in Figure 5.1, YYWW refers to the last two digits of the year (YY) and two digits for the work-week designation (WW). XXXXXXXX refers to the lot number.

Figure 5.1   ZSC31150 Pin Diagram

6 Quality and Reliability

The ZSC31150 is qualified according to the AEC-Q100 standard, operating temperature grade 0. A fit rate <5fit (temp=55°C, S=60%) is guaranteed. A typical fit rate of the C7D-technologie, which is used for ZSC31150, is 2.5fit.

7 Customization

For high-volume applications, which require an up- or downgraded functionality compared to the ZSC31150, ZMDI can customize the circuit design by adding or removing certain functional blocks.

For it ZMDI has a considerable library of sensor-dedicated circuitry blocks.

Thus ZMDI can provide a custom solution quickly. Please contact ZMDI for further information.

8   Ordering Information

Product Code	Description	Package
ZSC31150GEB	ZSC31150 Die — Temperature range: -40°C to +150°C	Unsawn on Wafer
ZSC31150GEC	ZSC31150 Die — Temperature range: -40°C to +150°C	Sawn on Wafer Frame
ZSC31150GED	ZSC31150 Die — Temperature range: -40°C to +150°C	Waffle Pack
ZSC31150GEG1	ZSC31150 SSOP-14 — Temperature range: -40°C to +150°C	Tube: add "-T" to sales code Reel: add "-R"
ZSC31150GAB	ZSC31150 Die — Temperature range: -40°C to +125°C	Unsawn on Wafer
ZSC31150GAC	ZSC31150 Die — Temperature range: -40°C to +125°C	Sawn on Wafer Frame
ZSC31150GAD	ZSC31150 Die — Temperature range: -40°C to +125°C	Waffle Pack
ZSC31150GAG1	ZSC31150 SSOP-14 — Temperature range: -40°C to +125°C	Tube: add "-T" to sales code Reel: add "-R"
ZSC31150GLB	ZSC31150 Die — Temperature range: -40°C to +150°C (long life 5000h @150°C)	Unsawn on Wafer
ZSC31150GLC	ZSC31150 Die — Temperature range: -40°C to +150°C (long life 5000h @150°C)	Sawn on Wafer Frame
ZSC31150GLD	ZSC31150 Die — Temperature range: -40°C to +150°C (long life 5000h @150°C)	Waffle Pack
ZSC31150GLG1	ZSC31150 SSOP-14 — Temperature range: -40°C to +150°C (long life 5000h @150°C)	Tube: add "-T" to sales code Reel: add "-R"
ZSC31150KIT Evaluation Kit V1.0	ZSC31150 SSC Evaluation Kit: 3 interconnecting boards, 5 ZSC31150 SSOP-14 samples, USB cable, software/documentation DVD	Kit
ZSC31150 Mass Calibration System V1.1	Modular Mass Calibration System (MSC) for ZSC31150: MCS boards, cable, connectors, DVD with software and documentation	Kit

9   Additional Documents

Document	File Name
ZSC31150 Feature Sheet	*ZSC31150_FeatureSheet_Rev_*.PDF*
ZSC31150 Functional Description	*ZSC31150_FunctionalDescription_Rev_*.PDF*
ZSC31150 High Voltage Protection Description	*ZSC31150_HV_PROT_Rev_*.PDF*
ZSC31150 Dice Package	*ZSC31150_DicePackagePin_Rev_*.PDF*
ZSC31150 Bandwidth Calculation Sheet	*ZSC31150_Bandwidth_Calculation_Rev*.xls*
ZMDI Temperature Profile Calculation Sheet	*ZMDI_Temperature_Profile_Rev_*.xls*
ZSC31150 Application Kit Description	*ZSC31150_APPLKIT_Rev_*.pdf*
ZSC31150 Application Notes	*ZSC31150_AN*.pdf*

Visit ZMDI's website www.zmdi.com or contact your nearest sales office for the latest version of these documents.

10   Glossary

Term	Description
ADC	Analog-to-Digital Converter
AEC	Automotive Electronics Council
AFE	Analog Front End
AOUT	Analog Output
BAMP	Buffer Amplifier
CM	Command Mode
CMC	Calibration Microcontroller
CMV	Common Mode Voltage
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
DM	Diagnostic Mode
EEPROM	Electrically Erasable Programmable Read Only Memory
ESD	Electrostatic Device
LDR	Lower Diagnostic Range
MUX	Multiplexer
NOM	Normal Operation Mode
OWI	One Wire Interface
P	Bridge Sensor Measurement; e.g., Pressure Sensor

Term	Description
PGA	Programmable Gain Amplifier
POC	Power on Clear
RAM	Random-Access Memory
RISC	Reduced Instruction Set Computer
ROM	Read Only Memory
SCC	Sensor Connection Check
SIF	Serial Interface
SSC+	Positive-biased Sensor Short Check
SSC-	Negative-biased Sensor Short Check
TS	Temperature Sensor
XZC	eXtended Zero Compensation

11 Document Revision History

Revision	Date	Description
0.46	June 12, 2008	First release after format update
0.47	July 20, 2008	Update after review
1.01	September 20, 2008	"6." – fit rate added "1.5.2" – ROM check time revised/corrected "5.3.4.3" – SSC – no detection limit added
1.02	September 20, 2009	adjust to new ZMDI template
1.03	October 2, 2009	change to ZMDI denotation
1.04	October 22, 2009	formatting and linking issues solved
1.05	February 26, 2010	adjust to new ZMDI template include ZSC31150 Feature Sheet at page 2&3 add ordering codes for ZSC31150 and evaluation kits extend glossary add new phone number for ZMD FAR EAST, Ltd. and ZMDA America Office Madison
1.06	July 29, 2010	correct "Offset shift per step" and "Approx. maximum offset shift" in Table 2.2 for PGA gain = 105 and 52.5 move 1.4.1.6 "Internal pull-up resistor" into section 1.4.1 in Table 1.2 redrawing of Sensor Bridge in Figure 3.1, Figure 3.2 and Figure 3.3 add comment for C4 and C5 in Figure 3.3 rename ZMD31150 to ZSC31150
1.07	August 31, 2010	Connection of R_{IBR} in Figure 3.3 corrected
1.08	August 15, 2011	Update ordering information with "Long Life Automotive" in "Ordering Information" on page 3 and section 8)
2.00	December 15, 2012	Update for part numbers and ZMDI contact information. Minor edits.

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