



## U74AHCT374

CMOS IC

### OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

#### DESCRIPTION

The **U74AHCT374** is a octal edge-triggered D-type flip-flops with 3-state outputs and 8 channels.

When the  $\overline{OE}$  input is low, on the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

When the  $\overline{OE}$  input is high, the outputs are in the high-impedance.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

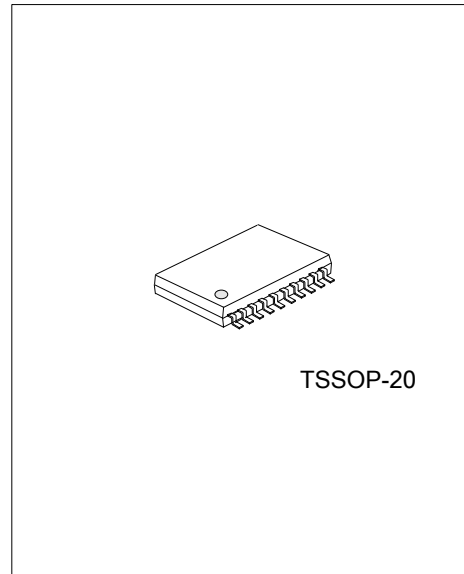
#### FEATURES

- \* Inputs are TTL-Voltage Compatible
- \* Operate from 4.5V to 5.5V
- \* Inputs Accept Voltages to 5.5V
- \* Max  $t_{PD}$  of 9.4ns at  $V_{CC}=5V$ ,  $C_L=15pF$
- \* Typical  $V_{OL} < 0.36V$  at  $V_{CC}=4.5V$ ,  $I_{OL}=8mA$ ,  $T_A=25^\circ C$
- \* Typical  $V_{OH} > 3.94V$  at  $V_{CC}=4.5V$ ,  $I_{OH}=-8mA$ ,  $T_A=25^\circ C$

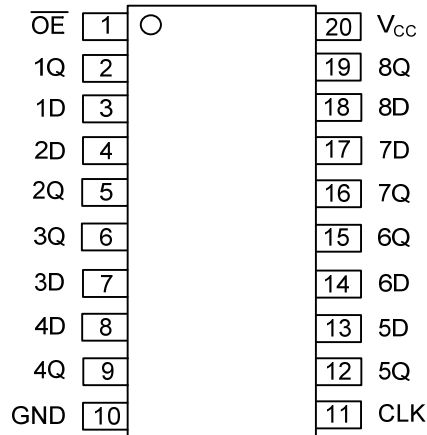
#### ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHCT374L-P20-R	U74AHCT374G-P20-R	TSSOP-20	Tape Reel
U74AHCT374L-P20-T	U74AHCT374G-P20-T	TSSOP-20	Tube

<p>U74AHCT374L-P20-R</p> <p>(1)Packing Type (2)Package Type (3)Lead Free</p>	<p>(1) R: Tape Reel, T: Tube (2) P20: TSSOP-20 (3) G: Halogen Free, L: Lead Free</p>
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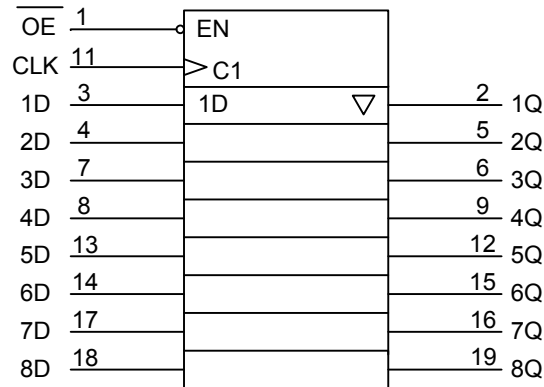
■ PIN CONFIGURATION



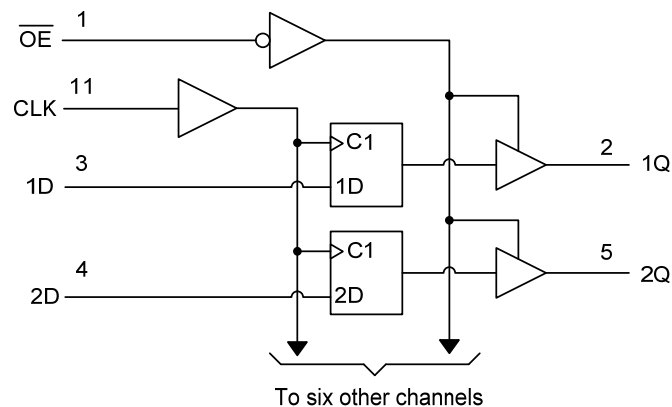
■ FUNCTION TABLE

INPUTS( $\overline{OE}$ )	INPUTS(CLK)	INPUTS(D)	OUTPUT(Q)
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	H or L	X	$Q_0$
H	X	X	Z

■ LOGIC SYMBOL



■ LOGIC DIAGRAM



### ■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{CC}$	-0.5 ~ 7	V
Input Voltage	$V_{IN}$	-0.5 ~ 7	V
Output Voltage	$V_{OUT}$	-0.5 ~ $V_{CC} + 0.5$	V
$V_{CC}$ or GND Current	$I_{CC}$	±70	mA
Output Current	$I_{OUT}$	±35	mA
Input Clamp Current	$I_{IK}$	-20	mA
Output Clamp Current	$I_{OK}$	±20	mA
Operating Temperature	$T_{OPR}$	-40 ~ + 85	°C
Storage Temperature	$T_{STG}$	-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.  
 Absolute maximum ratings are stress ratings only and functional device operation is not implied.

### ■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	$V_{CC}$	4.5		5.5	V
High-level Input Voltage	$V_{IH}$	2			V
Low-level Input Voltage	$V_{IL}$			0.8	V
Input Voltage	$V_{IN}$	0		5.5	V
Output Voltage	$V_{OUT}$	0		$V_{CC}$	V
High-Level Output Current	$I_{OH}$			-8	mA
Low-Level Output Current	$I_{OL}$			8	mA
Input Rise or Fall Times	$t_{R}, t_{F}$			20	ns/V
Operating free-Air Temperature	$T_A$	-40		85	°C

### ■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage High-Level	$V_{OH}$	$V_{CC}=4.5V, I_{OH}=-50\mu A$	4.4	4.5		V
		$V_{CC}=4.5V, I_{OH}=-8mA$	3.94			
Output Voltage Low-Level	$V_{OL}$	$V_{CC}=4.5V, I_{OL}=50\mu A$			0.1	V
		$V_{CC}=4.5V, I_{OL}=8mA$			0.36	
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=0V$ to 5.5V, $V_{IN}=0$ or 5.5V			±0.1	μA
Leakage Current (For Output in High-Impedance State)	$I_{OZ}$	$V_{CC}=5.5V, V_{IN}=V_{IH}$ or $V_{IH}, V_{OUT}=0$ or 5.5V			±0.25	μA
Quiescent Supply Current	$I_{CC}$	$V_{CC}=5.5V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$			4	μA
Additional Quiescent Supply Current	$\Delta I_{CC}$	$V_{CC}=5.5V$ , one input at 3.4V, Other inputs at $V_{CC}$ or GND			1.35	mA
Input Capacitance	$C_I$	$V_{CC}=5V, V_{IN}=V_{CC}$ or GND		4	10	pF
Output Capacitance	$C_O$	$V_{CC}=5V, V_{OUT}=V_{CC}$ or GND		9		pF

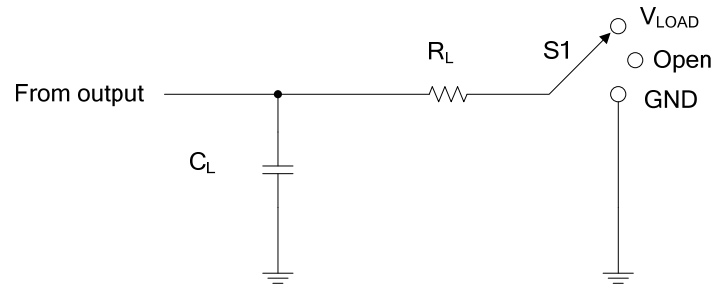
■ SWITCHING CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , See TEST CIRCUIT AND WAVEFORMS)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
From CLK to Q	$t_{PLH}/t_{PHL}$	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	$C_L = 15\text{pF}$	5.6	9.4	ns
			$C_L = 50\text{pF}$	6.4	10.4	
From $\overline{\text{OE}}$ to Q	$t_{PZL}/t_{PZH}$	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	$C_L = 15\text{pF}$	6.5	10.2	ns
			$C_L = 50\text{pF}$	7.3	11.2	
From $\overline{\text{OE}}$ to Q	$t_{PLZ}/t_{PHZ}$	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	$C_L = 15\text{pF}$	6.2	10.2	ns
			$C_L = 50\text{pF}$	7	11.2	
Maximum Clock Frequency	$f_{MAX}$	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	$C_L = 15\text{pF}$	90	140	MHz
			$C_L = 50\text{pF}$	85	130	
Pulse Width	$t_W$	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		6.5		ns
Setup Time	$t_{SU}$	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		2.5		ns
Hold Time	$t_H$	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		2.5		ns

■ OPERATING CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	$C_{PD}$	No load, $V_{CC} = 5\text{ V}$ , $f = 1\text{MHz}$		27		pF

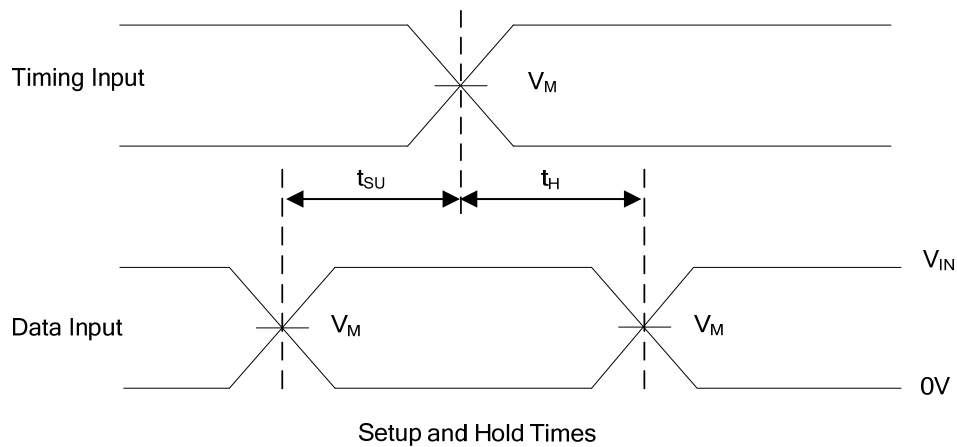
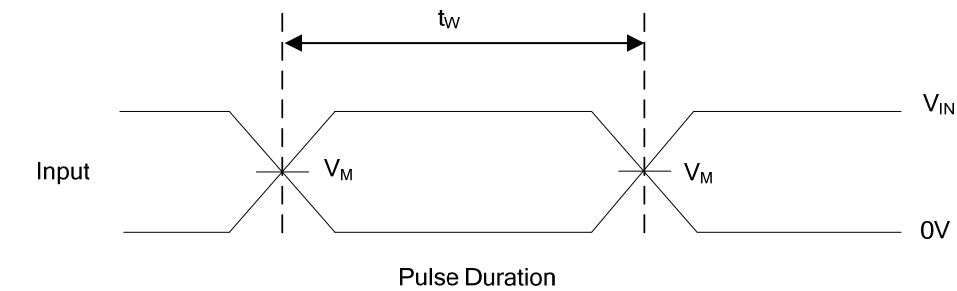
## ■ TEST CIRCUIT AND WAVEFORMS



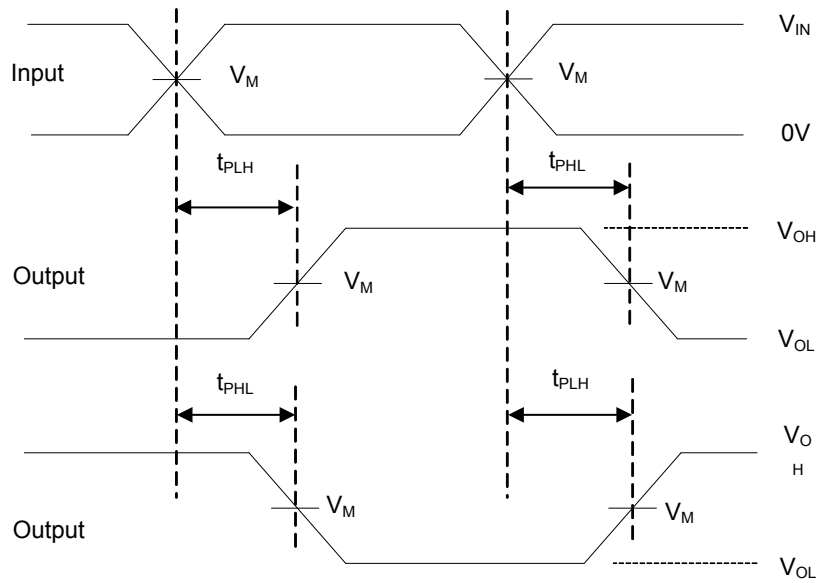
Test Circuit

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

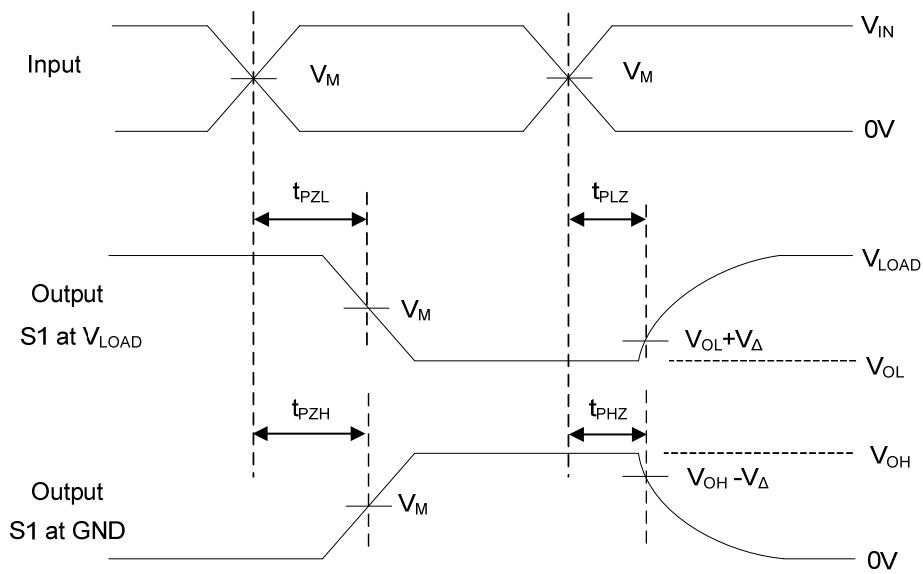
$V_{CC}$	Input		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_{IN}$	$t_R, t_F$					
$5V \pm 0.5V$	$V_{CC}$	$\leq 3ns$	$V_{CC}/2$	$V_{CC}$	15pF	$1k\Omega$	0.5V
					50pF		



## ■ TEST CIRCUIT AND WAVEFORMS(Cont.)



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enable and Disable Times

Note: A.  $C_L$  includes probe and jig capacitance.

B.  $P_{RR} \leq 1\text{MHz}$ ,  $Z_O = 50\Omega$ ,  $t_R \leq 3\text{ns}$ ,  $t_F \leq 3\text{ns}$ .

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