ML7202-001

2-Channel Echo Canceler with Multifunction ADPCM Transcoder

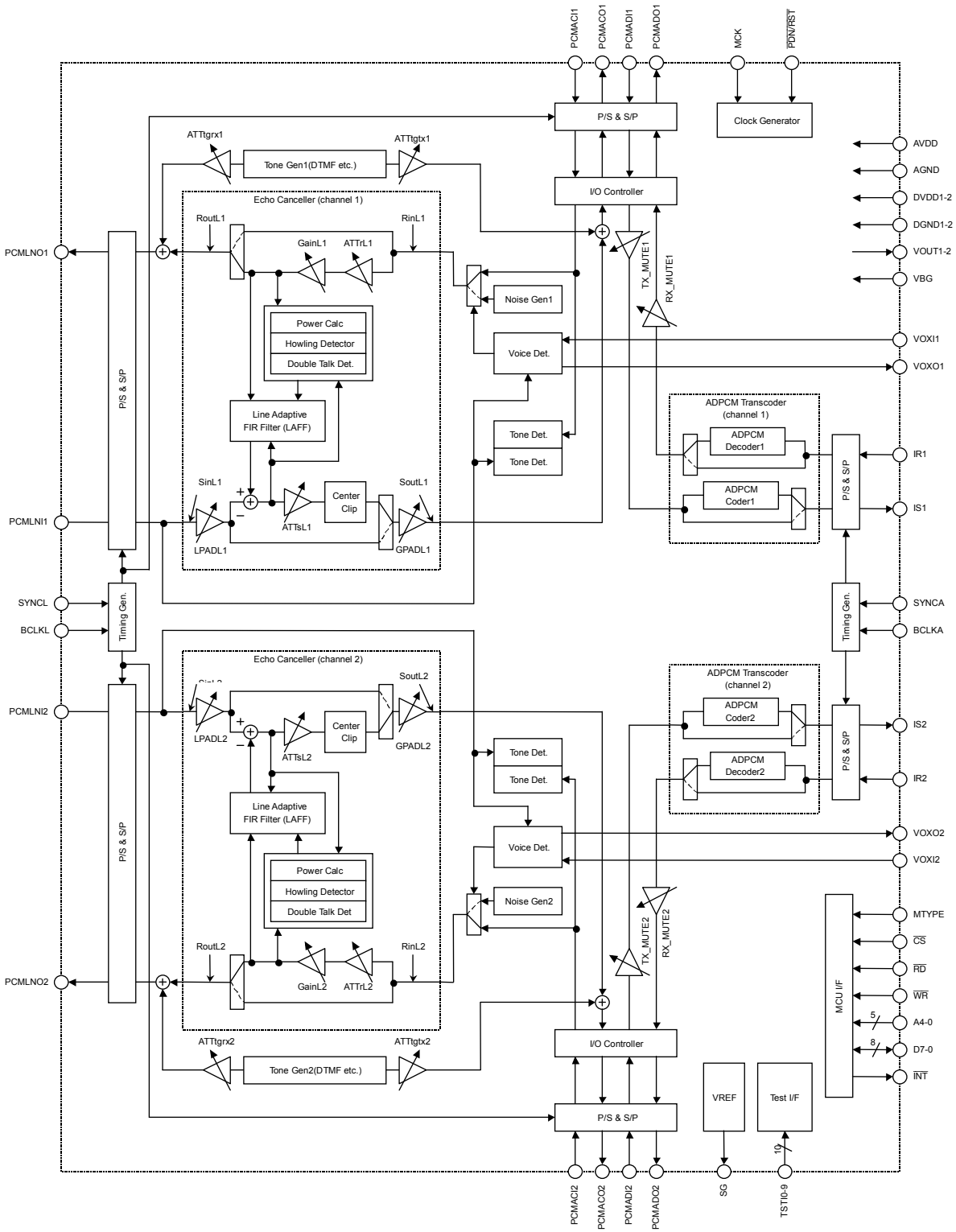
GENERAL DESCRIPTION

The ML7202-001 is an LSI supporting 2-channel transmit/receive. Each channel of transmit/receive has a built-in line echo canceler and full-duplex ADPCM transcoder. The ML7202-001, which performs functions such as the DTMF tone and single tone generation, and tone detection, transmit/receive data mute, gain control, and VOX, is ideally suited to applications such as basestations of ADPCM-based cordless telephone systems like Asian-prevailing PHS (Personal Handyphone System).

FEATURES

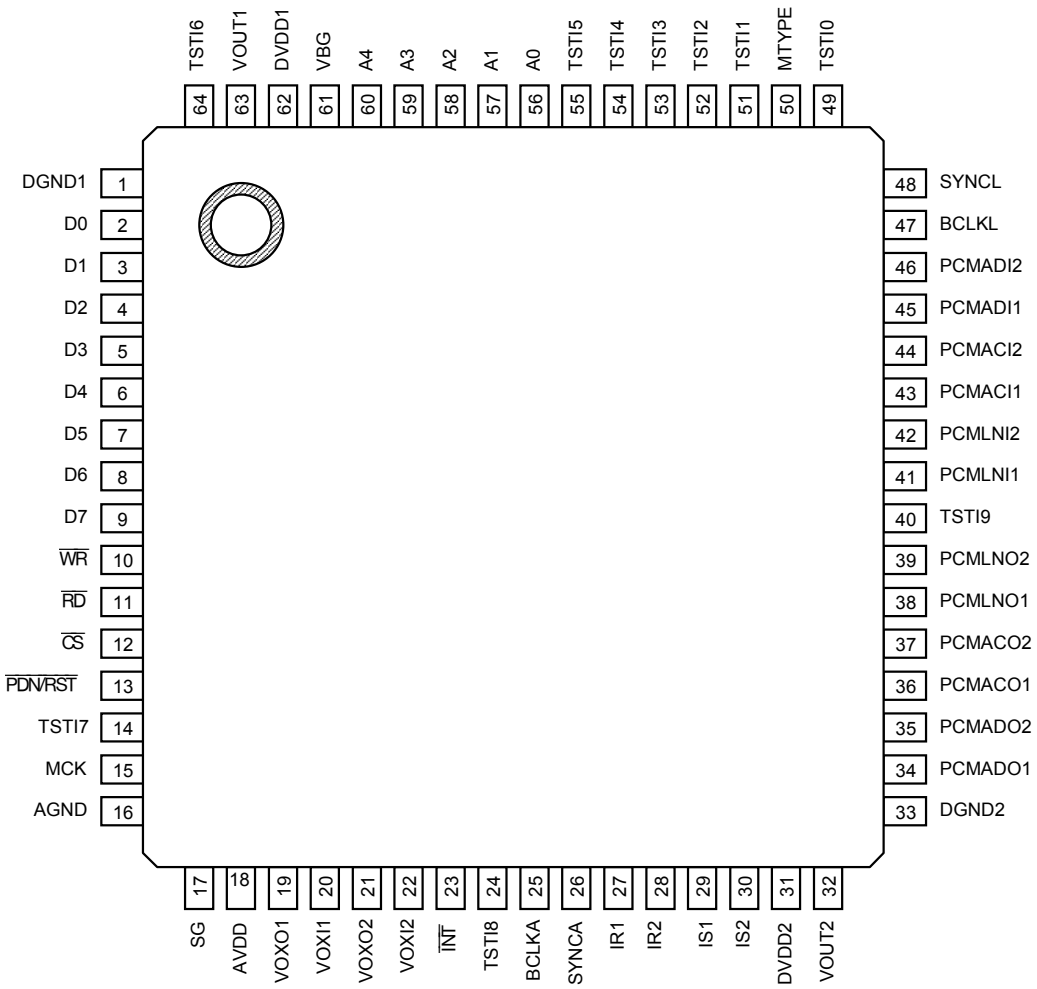
- Single 3.3 V power supply (DVDD1, 2, AVDD: 3.0 to 3.6 V)
- ADPCM: ITU-T Recommendation G.726 (32 kbps)
- PCM interface code format: ITU-T Recommendation G.711 (64 kbps), μ-law or A-law selectable
- Built-in echo canceler
  Echo attenuation: 30 dB（typ.）white noise
  Cancelable echo delay time: 64ms（max）
- Serial ADPCM and PCM transmission rate: 64 to 2048 kbps
- Digital interface synchronization mode: Long Frame Sync
- Time slot assignment
  μ-law/A-law setting: Supports 32 slots (BCLK setting: 2.048 MHz external input)
- Transmit/receive mute function and transmit/receive programmable gain setting
- Built-in DTMF tone and single tone generators
- Single tone detector
  2100 Hz (default)
- Built-in VOX functions
  Transmit side : Voice/silence detection
  Receive side : Background noise generation during silence
- Parallel microcontroller interface
- Master clock frequency: 19.2 MHz
- Hardware and software power-down mode
- Operating temperature range: –40°C to +85°C
- Package:
  64-pin plastic TQFP (TQFP64-P-1010-0.50-K) (ML7202-001TB)

BLOCK DIAGRAM



* Transmit side : Direction from the PCMLNI1-pin (or the PCMLNI2-pin) toward the IS1-pin (or the IS2-pin)
Receive side : Direction from the IR1-pin (or the IR2-pin) toward the PCMLNO1-pin (or the PCMLNO2-pin)

PIN CONFIGURATION (TOP VIEW)



64-Pin Plastic TQFP

PIN DESCRIPTIONS

Pin	Symbol	I/O	State when $\overline{\text{PDN/RST}}$ ="0"	Description
1	DGND1	—	—	Digital ground pin
2	D0	I/O	I	Data I/O pins for accessing control registers. This LSI contains 32-byte control registers and reads/writes by an external microcontroller are via the $\overline{\text{WR}}$, $\overline{\text{RD}}$, and $\overline{\text{CS}}$ pins. See "Microcontroller Interface Write/Read Timing" in the "ELECTRICAL CHARACTERISTICS" Section.
3	D1	I/O	I	
4	D2	I/O	I	
5	D3	I/O	I	
6	D4	I/O	I	
7	D5	I/O	I	
8	D6	I/O	I	
9	D7	I/O	I	
10	$\overline{\text{WR}}$	I	I	Write enable input pin for accessing the control registers
11	$\overline{\text{RD}}$	I	I	Read enable input pin for accessing the control registers. This pin is enabled when the MTYPE pin is set to "0" and is disabled when the MTYPE pin is set to "1". When this pin is disabled, fix this pin to "1".
12	$\overline{\text{CS}}$	I	I	Chip select input pin for the control registers
13	$\overline{\text{PDN/RST}}$	I	"0"	Power-down and reset control input pin. When this pin is set to "0", the LSI is powered down. In power down mode, all of the control registers, internal data memories, coefficients in the echo canceler and the ADPCM transcoder are reset. For normal operation, set this pin to "1". Since the power-down reset function is determined by the OR'ed value of a negative logic of this pin and the CR0-B7 (SPDN), set the CR0-B7 (SPDN) to "0" when using the pin. When applying power, hold the pin in "0" for 250 μS or longer from the master clock input (20 clocks minimum) after the digital supply (DVDD1 and DVDD2) voltage and the analog supply (AVDD) voltage reach 90% of their nominal value. See "Reset Function" in the "TIMING DIAGRAM" Section. Note that the specifications prescribed in this data sheet may not be satisfied until the requirements of inputting a minimum of 20 master clock pulses and holding the pin in "0" for 250 μS or more are met.
14	TSTI7	I	I	Input pin for LSI manufacturer's tests. Fix this pin to "0".
15	MCK	I	I	Master clock input pin. The input frequency shall be 19.2 MHz. The master clock can be asynchronized to SYNCL, SYNCA, BCLKL, and BCLKA.
16	AGND	—	—	Analog ground pin
17	SG	O	"0"	Output pin for analog signal ground in the LSI. The output voltage is about 1.4 V. Connect 10 μF and 0.1 μF (ceramic type) bypass capacitors between this pin and the AGND pin. This output cannot be directly used as analog signal ground. A buffer should be placed when this output is used.
18	AVDD	—	—	+3.3 V analog power supply pin

Pin	Symbol	I/O	$\overline{\text{PDN/RST}}$ ="0"	Description
19	VOXO1	O	"0"	Output pin for the VOX function on the transmit side of channel 1. This pin is enabled when CR21-B7 (VOX_ON1) is set to "1". This pin is used for identifying the voice/silence state by detecting the power of the transmit signal. At detection of voice, a logic "1" is output to this pin and at detection of silence, logic "0" is output. CR21-B6 and B5 (VOX_ON_LVL11 and_ VOX_ON_LVL01) are used for setting the threshold to be identified. This signal is also output to CR5-B2 (VOX_OUT1). Figure 4 shows the timing diagram for the VOX function. The transmit signal refers to the PCMLNI1 pin input signal.
20	VOXI1	I	I	Input pin for the VOX function on the receive side (line echo canceler RinL1 side) of channel 1. This pin is enabled when CR21-B7 (VOX_ON1) is set to "1". When this pin is a logic "1", receive side speech signals are fed to the RinL1. When this pin is a logic "0", the background noise generator's output is fed to the RinL1 instead of the receive side speech signals. Use CR21-B1 and B0 (RX_NOISE_LVL11 and RX_NOISE_LVL01) for setting the level of the background noise. Set CR21-B2 (VOX_IN1) to "0" when using this pin, since this pin is OR'ed with CR21-B2 (VOX_IN1) internally. When the application has a means to detect silence with the receive side speech signals, this function could be made use of as comfort noise generator.
21	VOXO2	O	"0"	Output pin for the VOX function on the transmit side of channel 2. This pin is enabled when CR22-B7 (VOX_ON2) is set to "1". This pin is used for identifying the voice/silence state by detecting the power of the transmit signal. At detection of voice, a logic "1" is output to this pin and at detection of silence, logic "0" is output. CR22-B6 and B5 (VOX_ON_LVL12 and_ VOX_ON_LVL02) are used for setting the threshold to be identified. This signal is also output to CR5-B6 (VOX_OUT2). Figure 4 shows the timing diagram for the VOX function. The transmit signal refers to the PCMLNI2 pin input signal.
22	VOXI2	I	I	Input pin for the VOX function on the receive side (line echo canceler RinL2 side) of channel 2. This pin is enabled when CR22-B7 (VOX_ON2) is set to "1". When this pin is a logic "1", receive side speech signals are fed to the RinL2. When this pin is a logic "0", the background noise generator's output is fed to the RinL2 instead of the receive side speech signals. Use CR22-B1 and B0 (RX_NOISE_LVL12 and RX_NOISE_LVL02) for setting the level of the background noise. Set CR22-B2 (VOX_IN2) to "0" when using this pin, since this pin is OR'ed with CR22-B2 (VOX_IN2) internally. When the application has a means to detect silence with the receive side speech signals, this function could be made use of as comfort noise generator.
23	$\overline{\text{INT}}$	O	"1"	Interrupt request output pin. An interrupt is generated when the transmit/receive tone detector in each channel detects a tone signal of 2100 Hz (default). An interrupt also is generated when the state changes from tone detection to non-detection of 2100 Hz (default). When an interrupt event occurs, the pin outputs a logic "0" for 0.7 μs. When the interrupt event remains unchanged, the pin outputs a logic "1". By reading CR4-B3 to B0, it is possible to identify the detected channel and the path (on the transmit side/receive side).

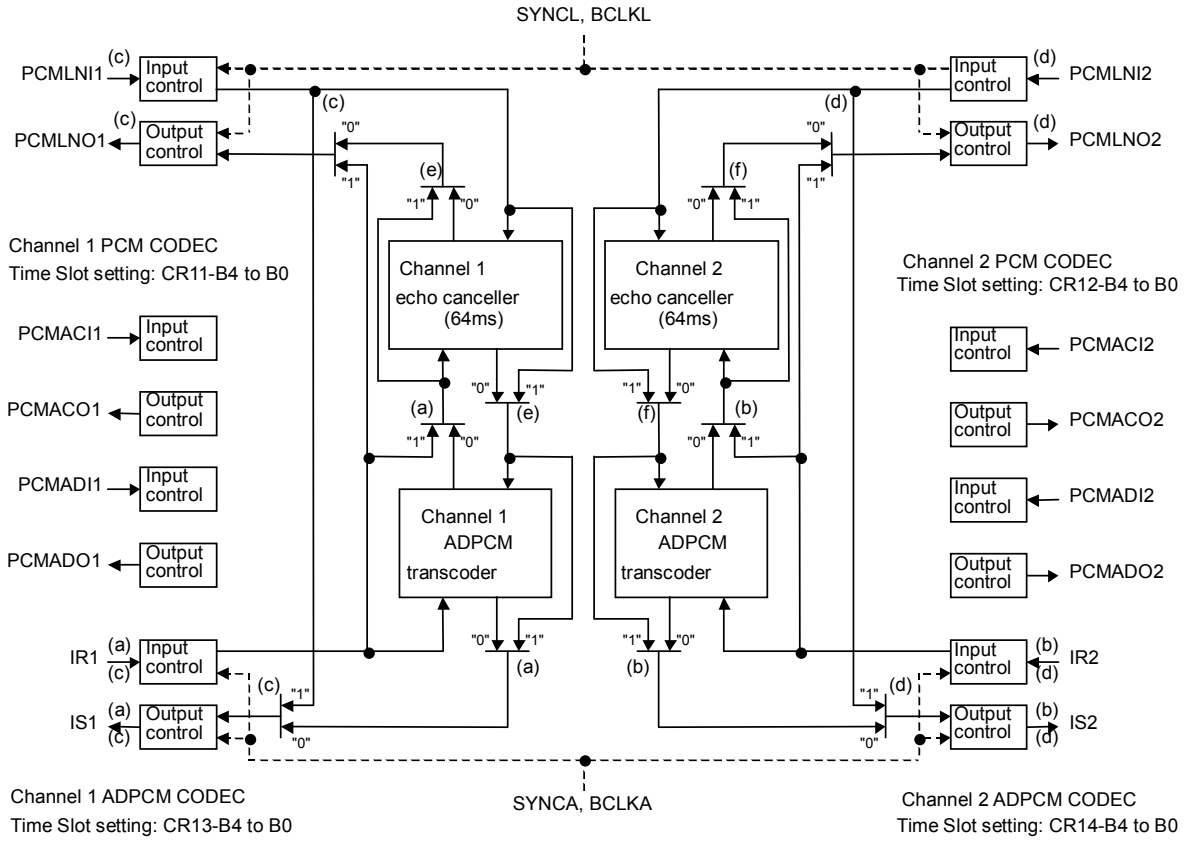
Pin	Symbol	I/O	$\overline{\text{PDN/RST}}$ ="0"	Description
24	TSTI8	I	I	Input pin for testing. Fix this pin to "0".
25	BCLKA	I	I	Shift clock input pin for ADPCM data (IS1, IS2, IR1, and IR2). The frequency is within the range of 64 to 2048 kHz.
26	SYNCA	I	I	8 kHz synchronous signal input pin for ADPCM data. This signal must be synchronized with the BCLKA signal. This signal indicates the location of MSB of ADPCM data.
27	IR1	I	I	4-bit ADPCM data input pin on the receive side of channel 1. The signal that is input to this pin is output to the PCMADO1 pin when CR0-B3 (IOSEL) is set to "1" and the signal is output to the PCMLNO1 pin when CR0-B3 is set to "0". This ADPCM data is shifted on the falling edge of BCLKA, synchronized to SYNCA and input serially starting from MSB. When CR2-B7 (CONTA1) is set to "1", this pin is configured as an 8-bit PCM data input and the data is processed skipping the ADPCM transcoder. When CR2-B5 (DTHR1) is set to "1", the output pin set by CR0-B3（IOSEL）is configured as a 4-bit ADPCM data output and the 4-bit ADPCM input data is output as it is. When CR2-B5 (DTHR1) is set to "1", the MUTE function is disabled and, even if CR2-B7 (CONTA1) is set to "1", the pin is not configured as an 8-bit PCM data input.
28	IR2	I	I	4-bit ADPCM data input pin on the receive side of channel 2. The signal that is input to this pin is output to the PCMADO2 pin when CR0-B3 (IOSEL) is set to "1" and the signal is output to the PCMLNO2 pin when CR0-B3 is set to "0". This ADPCM data is shifted on the falling edge of BCLKA, synchronized to SYNCA and input serially starting from MSB. When CR3-B7 (CONTA2) is set to "1", this pin is configured as an 8-bit PCM data input and the data is processed skipping the ADPCM transcoder. When CR3-B5 (DTHR2) is set to "1", the output pin set by CR0-B3（IOSEL）is configured as a 4-bit ADPCM data output and the 4-bit ADPCM input data is output as it is. When CR3-B5 (DTHR2) is set to "1", the MUTE function is disabled, and even if CR3-B7 (CONTA2) is set to "1", the pin is not configured as an 8-bit PCM data input.
29	IS1	O	Hi-Z	ADPCM data output pin on the transmit side of channel 1. When CR0-B3 (IOSEL) is set to "1", the signal that is input from the PCMADI1 pin is output from this pin. When CR0-B3 is set to "0", the signal that is input from the PCMLNII1 pin is output. ADPCM data is output serially starting from MSB, synchronized to the rising edges of BCLKA and SYNCA, and this pin gets in a high impedance state except when the 4-bit ADPCM data is being output. Also during power-down/reset and initial mode, this pin is put in a high impedance state. When CR2-B7 (CONTA1) is set to "1", this pin is configured as an 8-bit PCM data output skipping the ADPCM transcoder. This pin gets in a high impedance state except when the 8-bit PCM data is being output. When CR2-B5 (DTHR1) is set to "1", the 4-bit ADPCM input data from the input pin set by CR0-B3 (IOSEL) is output from this pin as it is. This pin gets in a high impedance state except when the 4-bit ADPCM data is being output. When CR2-B5 (DTHR1) is set to "1", the MUTE function is disabled, and the pin is not configured as an 8-bit PCM data output even if CR2-B7 (CONTA1) is set to "1".

Pin	Symbol	I/O	$\overline{\text{PDN/RST}}$ ="0"	Description
30	IS2	O	Hi-Z	ADPCM data output pin on the transmit side of channel 2. When CR0-B3 (IOSEL) is set to "1", the signal that is input from the PCMADI2 pin is output from this pin. When CR0-B3 is set to "0", the signal that is input from the PCMLNII2 pin is output. ADPCM data is output serially starting from MSB, synchronized to the rising edges of BCLKA and SYNCA, and this pin gets in a high impedance state except when the 4-bit ADPCM data is being output. Also during power-down/reset and initial mode, this pin is put in a high impedance state. When CR3-B7 (CONTA2) is set to "1", this pin is configured as an 8-bit PCM data output skipping the ADPCM transcoder. This pin gets in a high impedance state except when the 8-bit PCM data is being output. When CR3-B5 (DTHR2) is set to "1", the 4-bit ADPCM input data from the input pin set by CR0-B3 (IOSEL) is output from this pin as it is. This pin gets in a high impedance state except when the 4-bit ADPCM data is being output. When CR3-B5 (DTHR2) is set to "1", the MUTE function is disabled, and the pin is not configured as an 8-bit PCM data output even if CR3-B7 (CONTA2) is set to "1".
31	DVDD2	—	—	+3.3 V digital power supply pin
32	VOUT2	O	About 2.6 V	Regulator output pin. The output voltage is about 2.6 V. Connect 10 μF and 0.1 μF bypass capacitors between this pin and the DGND2 pin.
33	DGND2	—	—	Digital Ground pin
34	PCMADO1	O	Hi-Z	PCM data output pin of channel 1. This pin is enabled when CR0-B3 (IOSEL) is set to "1" and is put in a high impedance state when CR0-B3 is set to "0". The PCM data is output serially starting from MSB, synchronized to the rising edges of BCLKL and SYNCL, and the pin gets in a high impedance state except when the 8-bit PCM data is being output. Also during power-down reset and initial mode, the pin is also put in a high impedance. When CR2-B5 (DTHR1) is set to "1", this pin is configured as a 4-bit ADPCM data output and 4-bit ADPCM input data from the IR1 pin is output as it is. This pin gets in a high impedance state except when the 4-bit ADPCM data is being output. When CR2-B7 (CONTA1) is set to "1", the ADPCM transcoder goes into a through mode and 8-bit PCM input data from the IR1 pin is output as it is from this pin. The pin gets in a high impedance state except when the 8-bit PCM data is being output. When CR2-B5 (DTHR1) is set to "1", the MUTE function is disabled and the pin is not configured as an 8-bit PCM data output even if CR2-B7 (CONTA1) is set to "1".

Pin	Symbol	I/O	$\overline{\text{PDN/RST}}$ ="0"	Description
35	PCMADO2	O	Hi-Z	PCM data output pin of channel 2. This pin is enabled when CR0-B3 (IOSEL) is set to "1" and is put in a high impedance state when CR0-B3 is set to "0". The PCM data is output serially starting from MSB, synchronized to the rising edges of BCLKL and SYNCL, and the pin gets in a high impedance state except when the 8-bit PCM data is being output. Also during power-down reset and initial mode, the pin is also put in a high impedance. When CR3-B5 (DTHR2) is set to "1", this pin is configured as a 4-bit ADPCM data output and 4-bit ADPCM input data itself from the IR2 pin is output. This pin gets in a high impedance state except when the 4-bit ADPCM data is being output. When CR3-B7 (CONTA2) is set to "1", the ADPCM transcoder goes into a through mode and 8-bit PCM input data from the IR2 pin is output as it is from this pin. The pin gets in a high impedance state except when the 8-bit PCM data is being output. When CR3-B5 (DTHR2) is set to "1", the MUTE function is disabled and the pin is not configured as an 8-bit PCM data output even if CR3-B7 (CONTA2) is set to "1".
36	PCMACO1	O	Hi-Z	PCM data output pin of channel 1 line echo canceler. This pin is enabled when CR0-B3 (IOSEL) is set to "1". When CR0-B3 is set to "0", the pin is put in a high impedance. PCM data is output serially starting from MSB, synchronized to the rising edges of BCLKL and SYNCL, and the pin gets in a high impedance state except when the 8-bit PCM data is being output. Also during power-down reset and initial mode, the pin is put in a high impedance. During an end-to-end 4-bit ADPCM transparent mode defined by CR2-B5 (DTHR1) set to "1", this pin is configured as 4-bit ADPCM data output, and the line echo canceler, the VOX function, and the tone detector are disabled. The 4-bit ADPCM input data from the PCMLNI1 pin is output as it is, and the pin gets in a high impedance state except when the 4-bit ADPCM data is being output. Note that the pin is not configured as an 8-bit PCM data output when CR2-B5 (DTHR1) is set to "1" even if CR2-B7 (CONTA1) is set to "1".
37	PCMACO2	O	Hi-Z	PCM data output pin of channel 2 line echo canceler. This pin is enabled when CR0-B3 (IOSEL) is set to "1". When CR0-B3 is set to "0", the pin is put in a high impedance. PCM data is output serially starting from MSB, synchronized to the rising edges of BCLKL and SYNCL, and the pin gets in a high impedance state except when the 8-bit PCM data is being output. Also during power-down reset and initial mode, the pin is put in a high impedance. During an end-to-end 4-bit ADPCM transparent mode defined by CR3-B5 (DTHR2) set to "1", this pin is configured as 4-bit ADPCM data output, the VOX function, and the tone detector are disabled. The 4-bit ADPCM input data from the PCMLNI2 pin is output as it is, and the pin gets in a high impedance state except when the 4-bit ADPCM data is being output. Note that the pin is not configured as an 8-bit PCM data output when CR3-B5 (DTHR2) is set to "1" even if CR3-B7 (CONTA2) is set to "1".

Pin	Symbol	I/O	$\overline{\text{PDN/RST}}$ ="0"	Description
38	PCMLNO1	O	Hi-Z	PCM data output pin of line echo canceler of channel 1. The PCM data is output serially starting from MSB, synchronized to the rising edges of BCLKL and SYNCL. The pin gets in a high impedance state except when the 8-bit PCM data is being output. Also during power-down reset and initial mode, the pin is put in a high impedance. During an end-to-end 4-bit ADPCM transparent mode defined by CR2-B5 (DTHR1) set to "1", this pin is configured as 4-bit ADPCM data output, and the line echo canceler, the VOX function, and the tone detector are disabled. The 4-bit ADPCM input data from the input pin set by CR0-B3 (IOSEL) is output as it is from this pin. The pin gets in a high impedance state except when the 4-bit ADPCM data is being output. Note that the pin is not configured as an 8-bit PCM data output when CR2-B5 (DTHR1) is set to "1" even if CR2-B7 (CONTA1) is set to "1".
39	PCMLNO2	O	Hi-Z	PCM data output pin of line echo canceler of channel 2. The PCM data is output serially starting from MSB, synchronized to the rising edges of BCLKL and SYNCL. The pin gets in a high impedance state except when the 8-bit PCM data is being output. Also during power-down reset and initial mode, the pin is put in a high impedance. During an end-to-end 4-bit ADPCM transparent mode defined by CR3-B5 (DTHR2) set to "1", this pin is configured as 4-bit ADPCM data output, and the line echo canceler, the VOX function, and the tone detector are disabled. The 4-bit ADPCM input data from the input pin set by CR0-B3 (IOSEL) is output as it is from this pin. The pin gets in a high impedance state except when the 4-bit ADPCM data is being output. Note that the pin is not configured as an 8-bit PCM data output when CR3-B5 (DTHR2) is set to "1" even if CR3-B7 (CONTA2) is set to "1".
40	TSTI9	I	I	Input pin for testing. Fix this pin to "0".
41	PCMLNI1	I	I	PCM data input pin of line echo canceler of channel 1. This PCM input signal is shifted on the falling edge of BCLKL and is input starting from MSB. The start of PCM data (MSB) is identified by the rising edge of SYNCL. When CR2-B5 (DTHR1) is set to "1", the pin is configured as a 4-bit ADPCM data input and the input data from this pin is output as it is to the output pin set by CR0-B3 (IOSEL).
42	PCMLNI2	I	I	PCM data input pin of line echo canceler of channel 2. This PCM input signal is shifted on the falling edge of BCLKL and is input starting from MSB. The start of PCM data (MSB) is identified by the rising edge of SYNCL. When CR3-B5 (DTHR2) is set to "1", the pin is configured as a 4-bit ADPCM data input and the input data from this pin is output as it is to the output pin set by CR0-B3 (IOSEL).
43	PCMACI1	I	I	PCM data input pin of line echo canceler of channel 1. This pin is enabled when CR0-B3 (IOSEL) is set to "1" and when CR0-B3 is set to "0", input to the pin is disabled. When the input is disabled, fix the pin to "0" or "1". The PCM input signal is shifted on the rising edge of BCLKL and is input starting from MSB. The start of PCM data (MSB) is identified by the rising edge of SYNCL. When CR2-B5 (DTHR1) is set to "1", the pin is configured as a 4-bit ADPCM data input and 4-bit ADPCM data input from the PCMLNO1 is output from this pin as it is.
44	PCMACI2	I	I	PCM data input pin of line echo canceler of channel 2. This pin is enabled when CR0-B3 (IOSEL) is set to "1" and when CR0-B3 is set to "0", input to the pin is disabled. When the input is disabled, fix the pin to "0" or "1". The PCM input signal is shifted on the rising edge of BCLKL and is input starting from MSB. The start of PCM data (MSB) is identified by the rising edge of SYNCL. When CR3-B5 (DTHR2) is set to "1", the pin is configured as a 4-bit ADPCM data input and 4-bit ADPCM data input from the PCMLNO2 is output from this pin as it is.

Pin	Symbol	I/O	$\overline{\text{PDN/RST}}$ ="0"	Description
45	PCMADI1	I	I	PCM data input pin of channel 1. When CR0-B3 (IOSEL) is set to "1", input to this pin is enabled; and when CR0-B3 is set to "0", input to the pin is disabled. When the pin input is disabled, fix the pin to "0" or "1". The PCM input signal is shifted on the falling edge of BCLKL and is input starting from MSB. The beginning of PCM data (MSB) is identified by the rising edge of SYNCL. When CR2-B5 (DTHR1) is set to "1", the pin is configured as a 4-bit ADPCM data input and the 4-bit ADPCM data input from this pin is output to the IS1 pin as it is. When CR2-B7 (CONTA1) is set to "1", the ADPCM transcoder goes into a through mode and 8-bit PCM data input from this pin is output to the IS1 pin as it is.
46	PCMADI2	I	I	PCM data input pin of channel 2. When CR0-B3 (IOSEL) is set to "1", input to this pin is enabled; and when CR0-B3 is set to "0", input to the pin is disabled. When the pin input is disabled, fix the pin to "0" or "1". The PCM input signal is shifted on the falling edge of BCLKL and is input starting from MSB. The beginning of PCM data (MSB) is identified by the rising edge of SYNCL. When CR3-B5 (DTHR2) is set to "1", the pin is configured as a 4-bit ADPCM data input and the 4-bit ADPCM data input from this pin is output to the IS2 pin as it is. When CR3-B7 (CONTA2) is set to "1", the ADPCM transcoder goes into a through mode and 8-bit PCM data input from this pin is output to the IS2 pin as it is.
47	BCLKL	I	I	Shift clock input pin for PCM data (PCMLNO1/PCMLNI1, PCMACO1 /PCMACI1, PCMADO1/PCMADI1, PCMLNO2/PCMLNI2, PCMACO2 /PCMACI2, and PCMADO2/PCMADI2). The input frequency is 64 to 2048 kHz.
48	SYNCL	I	I	8 kHz synchronous signal input pin for PCM data. This signal must be synchronized to the BCLKL signal.
49	TSTI0	I	I	Input pin for testing. Fix this pin to "0".
50	MTYPE	I	I	Microcontroller interface select pin. When the pin is set to "0", the pin is in read/write independent control mode; and when it is set to "1", the pin is in read/write shared (R/W) control mode. When this pin is set to "1", fix the $\overline{\text{RD}}$ pin to "1".
51	TSTI1	I	I	Input pins for LSI manufacturer's testing. Fix these pins to "0".
52	TSTI2	I	I	
53	TSTI3	I	I	
54	TSTI4	I	I	
55	TSTI5	I	I	
56	A0	I	I	Address input pins for accessing the control register
57	A1	I	I	
58	A2	I	I	
59	A3	I	I	
60	A4	I	I	
61	VBG	O	About 1.2 V	Regulator reference voltage output pin. The output voltage is about 1.2 V. Connect a 150 pF bypass capacitor between this pin and the DGND1 pin.
62	DVDD1	—	—	+3.3 V digital power supply pin
63	VOUT1	O	About 2.6 V	Regulator output pin. The output voltage is about 2.6 V. Connect 10 μF and 0.1 μF bypass capacitors between this pin and the DGND1 pin.
64	TSTI6	I	I	Input pin for LSI manufacturer's testing. Fix this pin to "0".

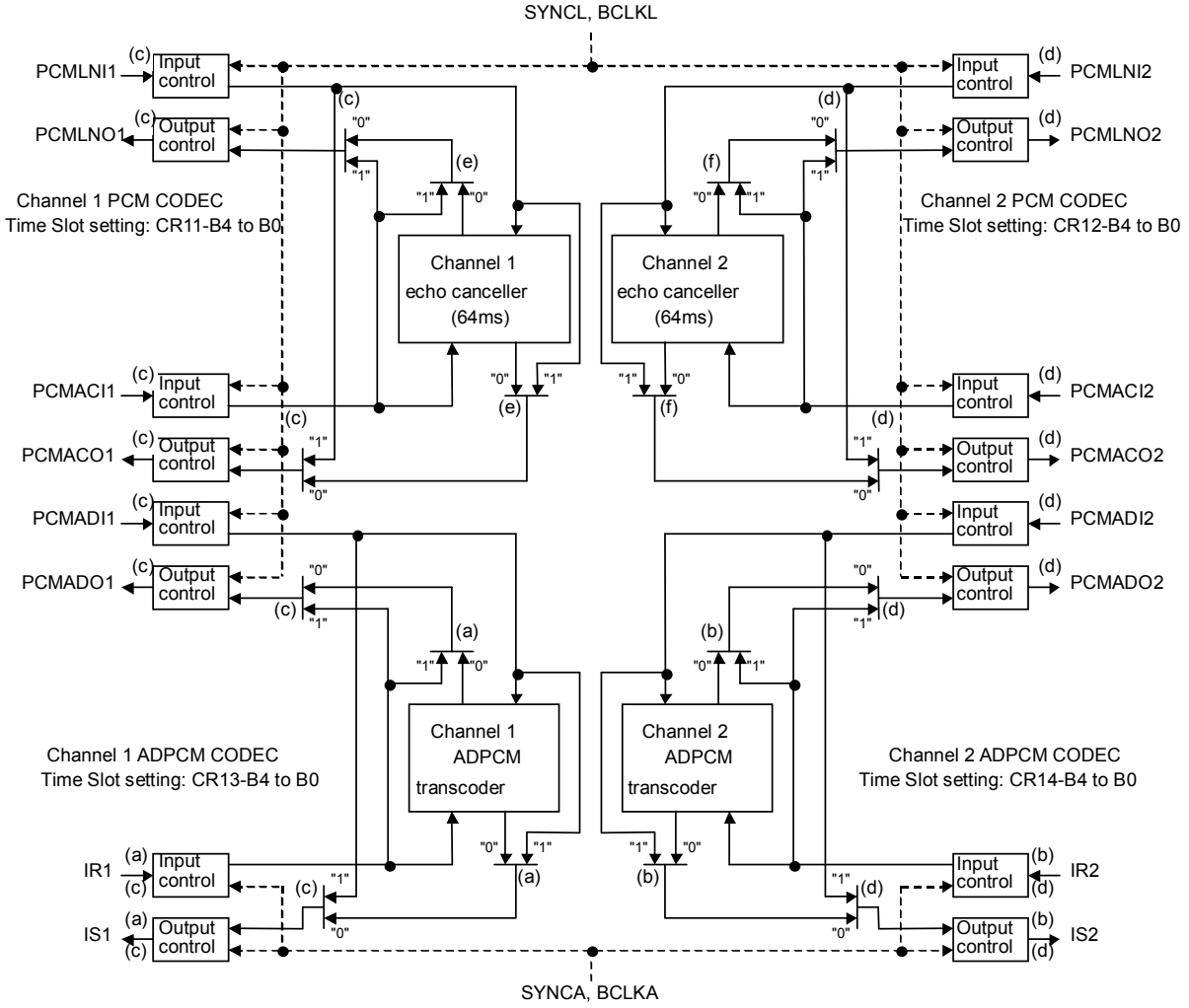


IOSEL(CR0-B3)=0

Control (a): CONTA1 (channel 1 ADPCM through control)...CR2-B7
Control (b): CONTA2 (channel 2 ADPCM through control)...CR3-B7
Control (c): DTHR1 (channel 1 end-to-end 4-bit ADPCM transparent control)...CR2-B5
Control (d): DTHR2 (channel 2 end-to-end 4-bit ADPCM transparent control)...CR3-B5
Control (e): LTHR1 (channel 1 echo canceller through control)...CR27-B7
Control (f): LTHR2 (channel 2 echo canceller through control)...CR28-B7

Note: Fix the input pins, PCMACI1, PCMADI1, PCMACI2, and PCMADI2 to “1” or “0”.
The outputs of PCMACO1, PCMADO1, PCMACO2 and PCMADO2 are all in high impedance.

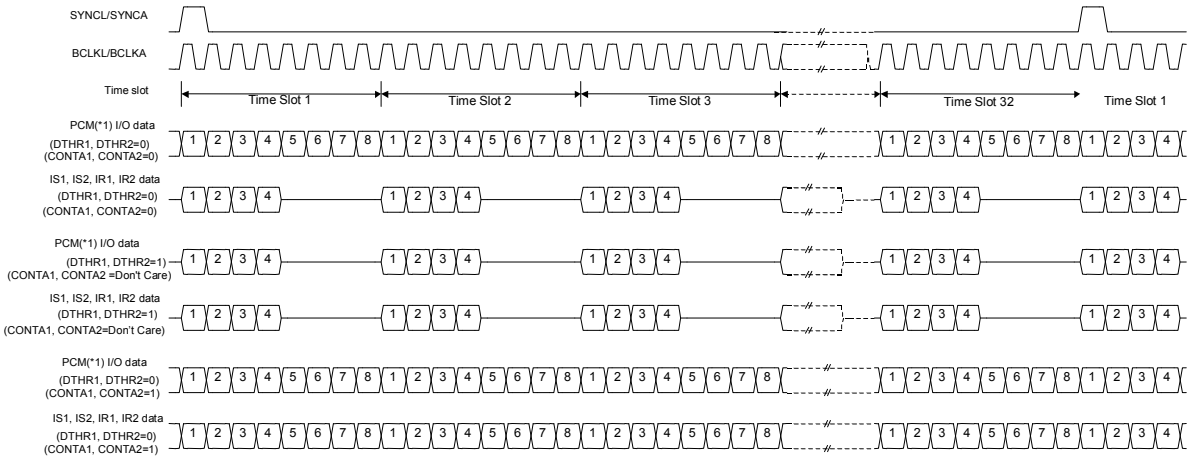
Figure 1 Signal Input/Output Control 1



IOSEL(CR0-B3)=1

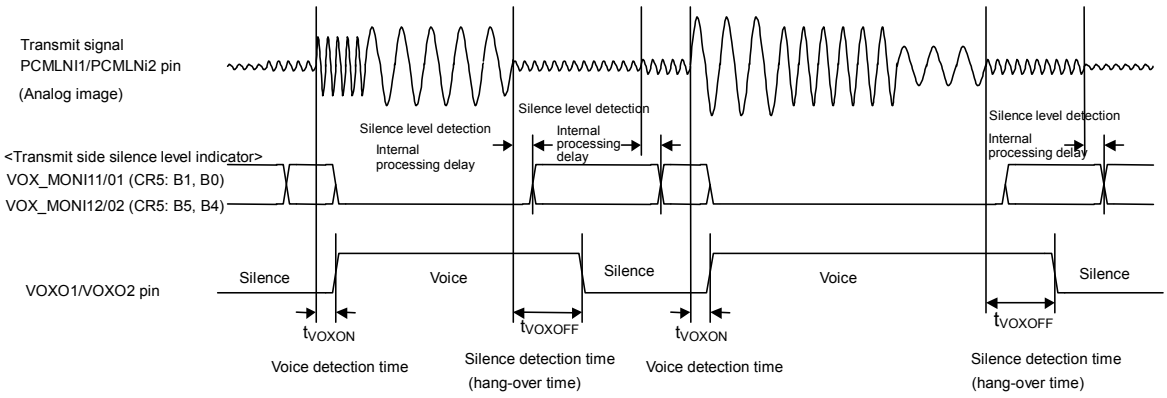
Control (a): CONTA1 (channel 1 ADPCM transcoder enable/through control)...CR2-B7
Control (b): CONTA2 (channel 2 ADPCM transcoder enable/through control)...CR3-B7
Control (c): DTHR1 (channel 1 end-to-end 4-bit ADPCM transparent control)...CR2-B5
Control (d): DTHR2 (channel 2 end-to-end 4-bit ADPCM transparent control)...CR3-B5
Control (e): LTHR1 (channel 1 echo canceller through control)...CR27-B7
Control (f): LTHR2 (channel 2 echo canceller through control)...CR28-B7

Figure 2 Signal Input/Output Control 2

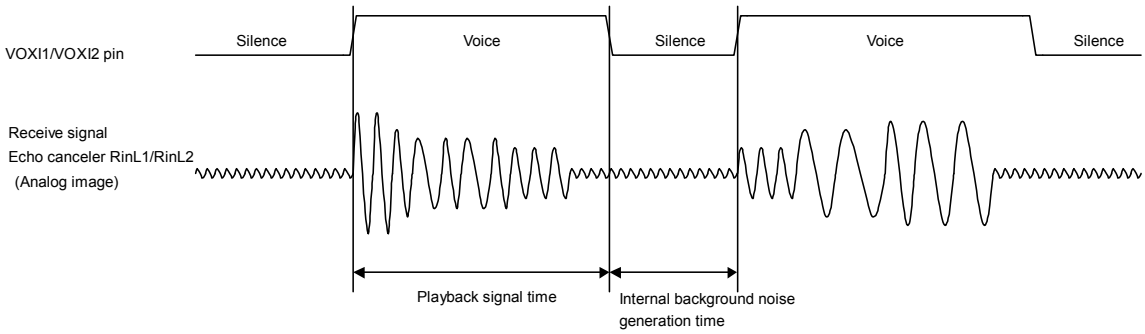


*1: PCMLNI1, PCMLNO1, PCMACI1, PCMACO1, PCMADI1, PCMADO1, PCMLNI2, PCMLNO2, PCMACI2, PCMACO2, PCMADI2, PCMADO2

Figure 3 PCM-ADPCM Time Slot Assignment

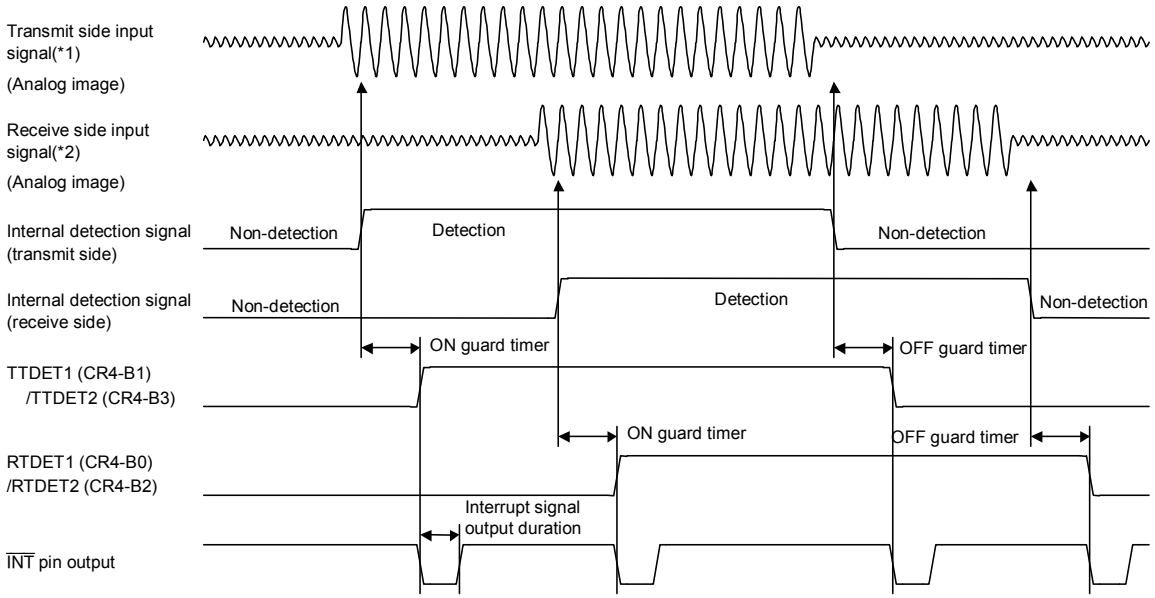


(a) VOX function timing on the transmission side



(b) VOX function timing on the reception side.

Figure 4 VOX Function



*1: Transmit side input pin: PCMLNI1, PCMLNI2

*2: Receive side input pin: PCMACI1, PCMACI2, IR1, IR2

Figure 5 Tone Detector Function

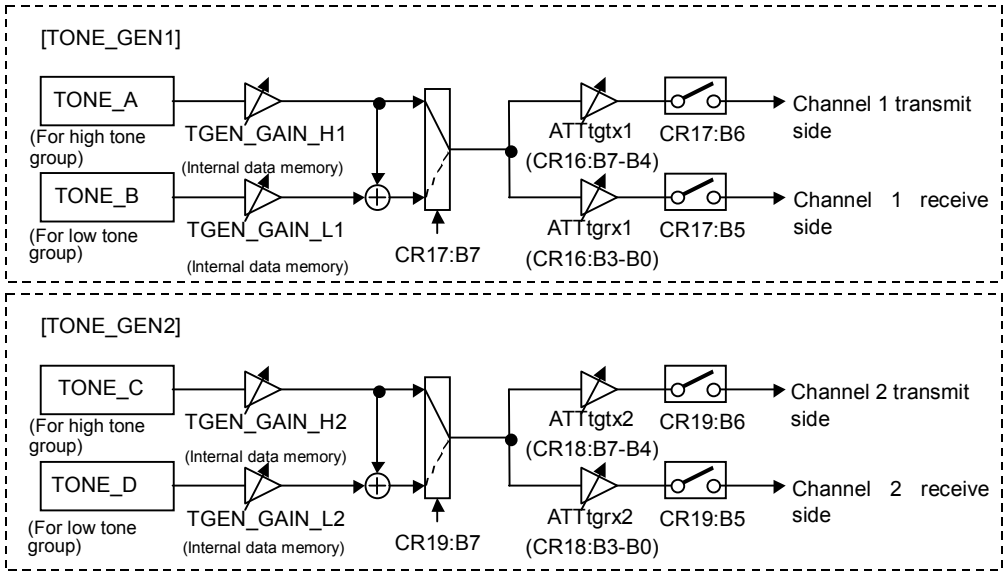
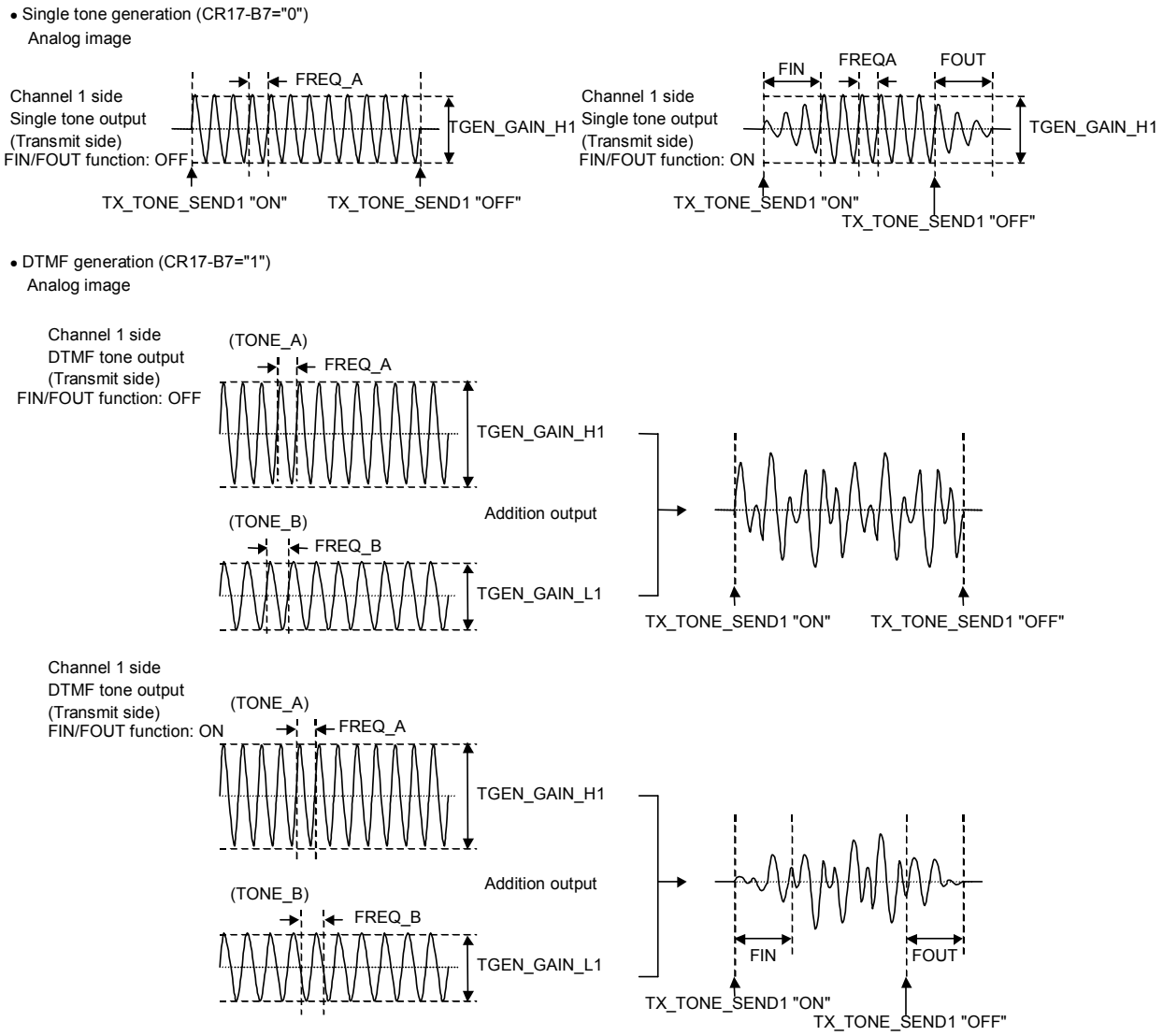


Figure 6 Tone Generator Block Diagram

In the explanation below, since the tone generation procedures of TONE_GEN1 and TONE_GEN2 are the same, TONE_GEN1has been taken as the example.



Notes:

- The initial setting of FIN (Fade In)/FOUT (Fade Out) function is OFF.
- When the output frequency setting is altered using the control register (CR17), sound stoppage or noises may occur at the change of the frequency.
- When the FIN (Fade In)/FOUT (Fade Out) function is enabled, tone output does not stop immediately even if tone output stop is set by rewriting the contents of CR17-B6 and CR17-B5 to “0” and the tome output becomes silent for only after expiration of the Fade Out time that is set here. Therefore, for B7 (tone type setting) and B4 to B0 (frequency setting), it is recommended to rewrite rewrite B6 and B5 to “0” while overwriting the same contents as those that are being output when tone ouptut is intended to be stopped.

Figure 7 Tone Generator Function (TONE_GEN1)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	—	–0.3 to +4.6	V
Digital input voltage	V_{DIN}	—	—0.3 to VDD+0.3	V
Storage temperature	T_{STG}	—	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{DD} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	—	3.0	3.3	3.6	V
Operating temperature range	Ta	—	–40	—	+85	°C
High level input voltage	V_{IH}	All the digital input pins	0.75 × V_{DD}	—	V_{DD} + 0.3	V
Low level input voltage	V_{IL}	All the digital input pins	–0.3	—	0.22 × V_{DD}	V
Digital input rise time	t_{ir}	All the digital input pins	—	2	20	ns
Digital input fall time	t_{if}		—	2	20	ns
Digital output load capacitance	C_{DL}	Digital output pins	—	—	50	pF
Digital output load resistance (pull-up resistor)	R_{DL}	Digital output pins (Open Drain pins(*1))	500	—	—	Ω
SG bypass capacitor	C_{SG}	Between SG and AGND	10 + 0.1	—	—	μF
VBG bypass capacitor	C_{VOUT}	Between and VBG and DGND	150	—	—	pF
VOUT bypass capacitor	C_{VBG}	Between VOUT1 and DGND1 and beween VOUT2 and DGND2	10 + 0.1	—	—	μF
Master clock frequency	f_{MCK}	—	–100 ppm	19.2	+100 ppm	MHz
Master clock duty ratio	D_{MCK}	MCK	40	50	60	%
Bit clock frequency	f_{BCK}	BCLKL, BCLKA	64	—	2048	kHz
Synchronous signal frequency (*2)	f_{SYNC}	SYNCL, SYNCA	–1000 ppm	8	+1000 ppm	kHz
Clock duty cycle(*3)	D_{CK}	BCLKL, BCLKA	40	50	60	%
Transmit/receive synchronous timing	t_{BS}	BCLKL to SYNCL, BCKLA to SYNCA	100	—	—	ns
	t_{SB}	SYNCL to BCLKL, SYNCA to BCLKA	100	—	—	ns
Synchronous signal width	t_{WS}	SYNCL, SYNCA	1 BCLK	—	100	μs
PCM and ADPCM setup time	t_{DS}	—	100	—	—	ns
PCM and ADPCM hold time	t_{DH}	—	100	—	—	ns

*1: Open drain pins: PCMLNO1, PCMLNO2, PCMADO1, PCMADO2, PCMACO1, PCMACO2, IS1, and IS2

*2: If generating SYNCL and SYNCA with different clocks, do not corrupt the sequence of the rising edges of SYNCL and SYNCA (which rises first) after a reset is released.

*3: It is not necessary to satisfy this specification as long as the digital interface specifications are satisfied.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current 1	I_{DD1}	At operation, no signal (V_{DD} = 3.3 V)	—	35	40	mA
Power supply current 2	I_{DD2}	At power-down (V_{DD} = 3.3 V, MCK input)	—	0.1	1.0	mA
Digital input pin Input leakage current	I_{IH}	V_{IN} = DVDD	—	0.01	50	μA
	I_{IL}	V_{IN} = 0.0 V	–50	–0.01	—	μA
Digital I/O pin Input leakage current	I_{OZH}	V_{IN} = DVDD	—	0.01	50	μA
	I_{OZL}	V_{IN} = 0.0 V	–50	–0.01	—	μA
High level output voltage	V_{OH}	Digital output pins and digital I/O pis I_{OH} = 4.0 mA	2.35	—	—	V
Low level output voltage	V_{OL}	Digital output pins and digital I/O pins I_{OL} = –4.0 mA	—	—	0.45	V
Input capacitance	C_{IN1}	Input pins	—	6	12	pF
	C_{IN2}	I/O pins	—	10	20	pF

Analog Interface Characteristics

(V_{DD} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SG output voltage	V_{SG}	SG	1.30	1.4	1.50	V

Reset Timing Characteristics

(V_{DD} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset signal time at Power ON	t_{FRST}	90% or more of a nominal power supply voltage	250	—	—	μs
Reset signal width	t_{RSTW}	—	1	—	—	μs
Reset start time	t_{RSTS}	—	0	—	1	μs
Reset end time	t_{RSTE}	—	—	—	200	ms

Digital Interface Characteristics

(V_{DD} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital output delay time PCM, ADPCM interface	t_{SDX}	R_{DL} = 500Ω, C_{DL} = 50 pF	0	—	100	ns
	t_{XD1}		0	—	100	ns
	t_{XD2}		0	—	100	ns
	t_{XD3}		0	—	100	ns

Microcontroller Interface Characteristics ($\overline{WR}$ and $\overline{RD}$ Pin Independent Control)

(V_{DD} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Address & chip select setup time (with respect to $\overline{WR}$ ↓)	t_{CWS}	MTYPE = 0 C_{DL} = 50 pF	10	—	—	ns
Address & chip select setup time (with respect to $\overline{WR}$ ↑)	t_{CWH}		3	—	—	ns
$\overline{WR}$ pulse width	t_{WW}		20	—	—	ns
Data input setup time	t_{DWS}		15	—	—	ns
Data input hold time	t_{DWH}		5	—	—	ns
Address & chip select setup time (with respect to $\overline{RD}$ ↓)	t_{CRS}		10	—	—	ns
Address & chip select setup time (with respect to $\overline{RD}$ ↑)	t_{CRH}		3	—	—	ns
$\overline{RD}$ pulse width	t_{RW}		20	—	—	ns
Data output delay time	t_{DOD}		—	—	15	ns
Data output hold time	t_{DOH}		0	—	—	ns
$\overline{CS}$ Disable time	t_{CD}		10	—	—	ns

Microcontroller Interface Characteristics ($\overline{WR}$ and $\overline{RD}$ Pin Shared Control)

(V_{DD} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Address setup time (with respect to $\overline{WR}$ ↓)	t_{WRWS}	MTYPE = 1 C_{DL} = 50 pF	10	—	—	ns
Address setup time (with respect to $\overline{WR}$ ↑)	t_{WRWH}		3	—	—	ns
$\overline{WR}$ pulse width	t_{WRW}		20	—	—	ns
Address setup time（with respect to $\overline{CS}$ ↓）	t_{CSWS}		10	—	—	ns
Address setup time (with respect to $\overline{CS}$ ↑)	t_{CSWH}		3	—	—	ns
$\overline{CS}$ pulse width	t_{CSW}		20	—	—	ns
Data input setup time	t_{DWS}		15	—	—	ns
Data input hold time	t_{DWH}		5	—	—	ns
Address setup time (with respect to $\overline{CS}$ ↓)	t_{CSRS}		10	—	—	ns
Address setup time (with respect to $\overline{CS}$ ↑)	t_{CSRH}		3	—	—	ns
Data output delay time	t_{DOD}		—	—	15	ns
Data output hold time	t_{DOH}		0	—	—	ns
$\overline{CS}$ Disable time	t_{CD}		10	—	—	ns

AC Characteristics (DTMF and Single Tone)

(V_{DD} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Frequency deviation	Df_{T1}	DTMF tone		–1.5	—	+1.5	%
	Df_{T2}	Single tone		–1.5	—	+1.5	%
Tone reference output level	V_{TL}	Transmit side tone (gain setting: –6dB)	DTMF (low tone group)	–10	–8	–6	dBm0
	V_{TH}		DTMF (high tone group), single tone	–8	–6	–4	dBm0
	V_{RL}	Receive side tone (gain setting: –6dB)	DTMF (low tone group)	–10	–8	–6	dBm0
	V_{RH}		DTMF (high tone group), single tone	–8	–6	–4	dBm0
DTMF tone level relative value	R_{DTMF}	V_{TH}/V_{TL}, V_{RH}/V_{RL}		1	2	3	dB

AC Characteristics (Gain Setting)

(V_{DD} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit/receive gain setting accuracy	D_G	For all the gain setting values	–1	0	+1	dB

AC characteristics (VOX Function)

(V_{DD} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Transmit VOX detection time (voice/silence detection time)	t_{VXON}	Silence → Voice	VOXO1 and VOXO2 pins See Figure 4. Difference beween voice/silence: 10 dB	—	5	—	ms
	t_{VXOFF}	Voice → Silence		140/300	160/320	180/340	ms
Transmit VOX detection threshold precision (voice detection threshold)	D_{VX}	For the detection threshold setting value by CR21-B6, B5 (VOX1 side) and CR22-B6, B5 (VOX2 side)		–2.5	0	+2.5	dB

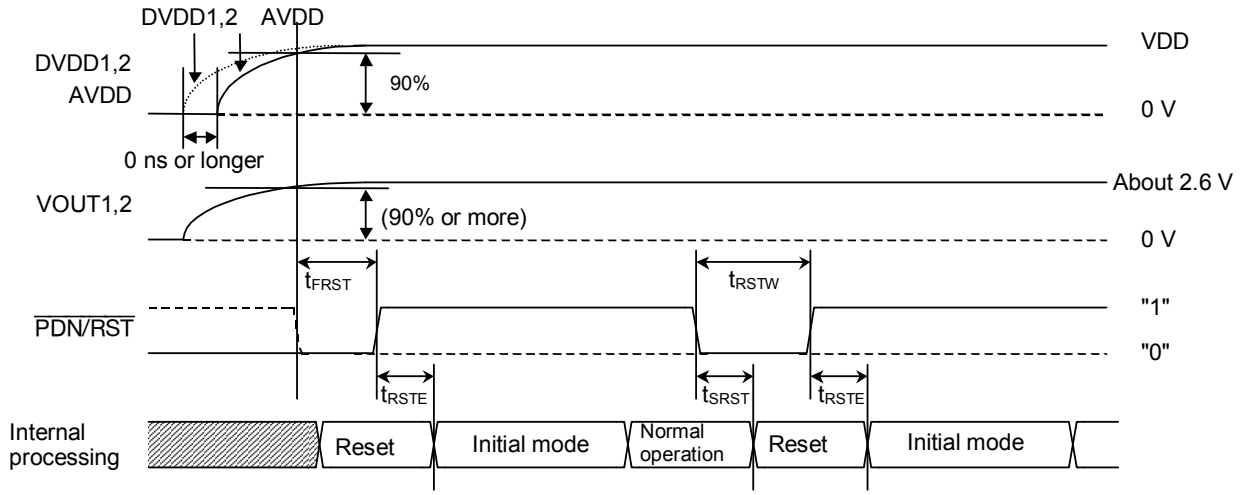
AC characteristics (tone detector function)

(V_{DD} = 3.0 to 3.6 V, Ta = –40 to +85°C)

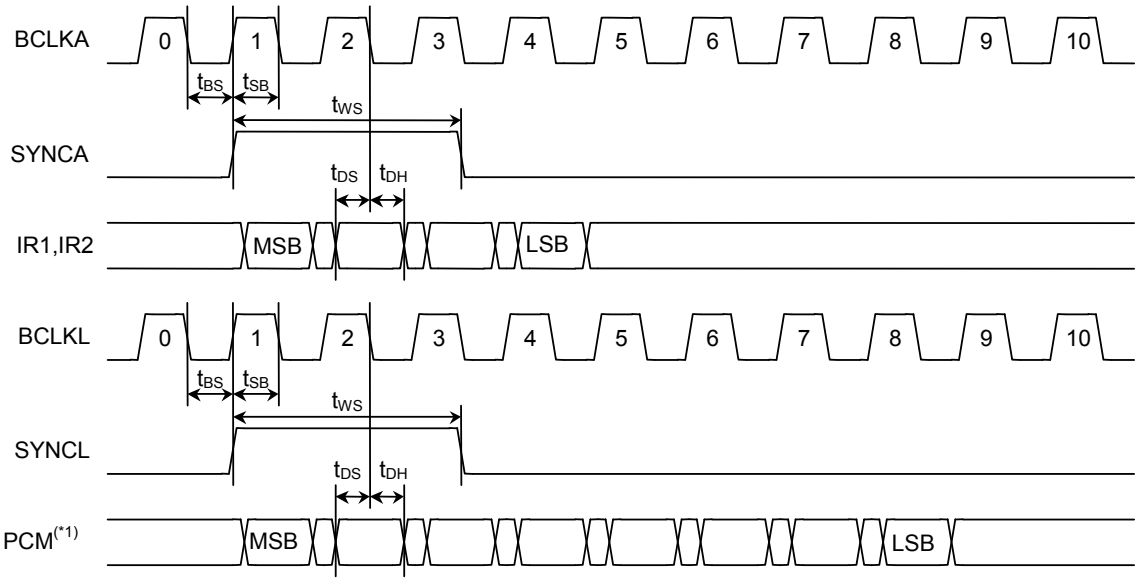
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection threshold precision	D_{LAC}	For set detection threshold	–2.5	0	+2.5	dB
Detection frequency range	D_{FR}	Detection threshold: –5.3dBm0 Detection frequency setting: 2100Hz	–10	0	+10	Hz
Non-detection frequency range	D_{NFRL}	Non-detect threshold setting: –5.3dBm0 Detection frequency setting: 2100Hz	—	—	–80	Hz
	D_{NFRH}		+80	—	—	Hz

TIMING DIAGRAMS

Reset Function

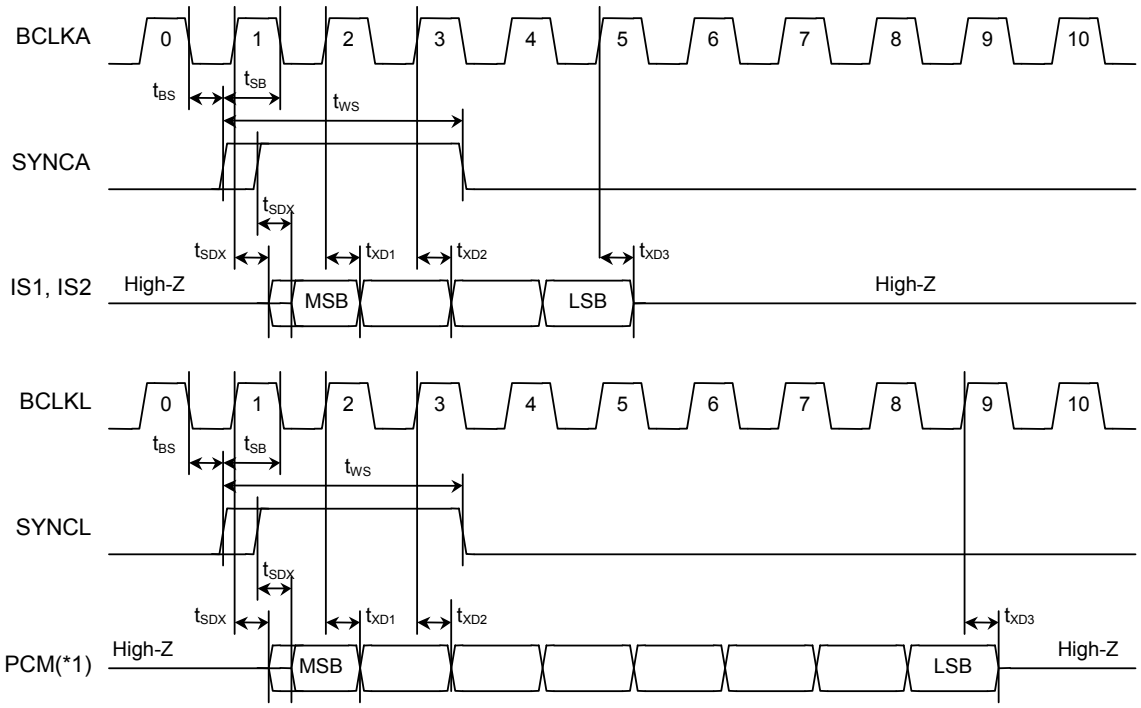


Input Timing of PCM and ADPCM



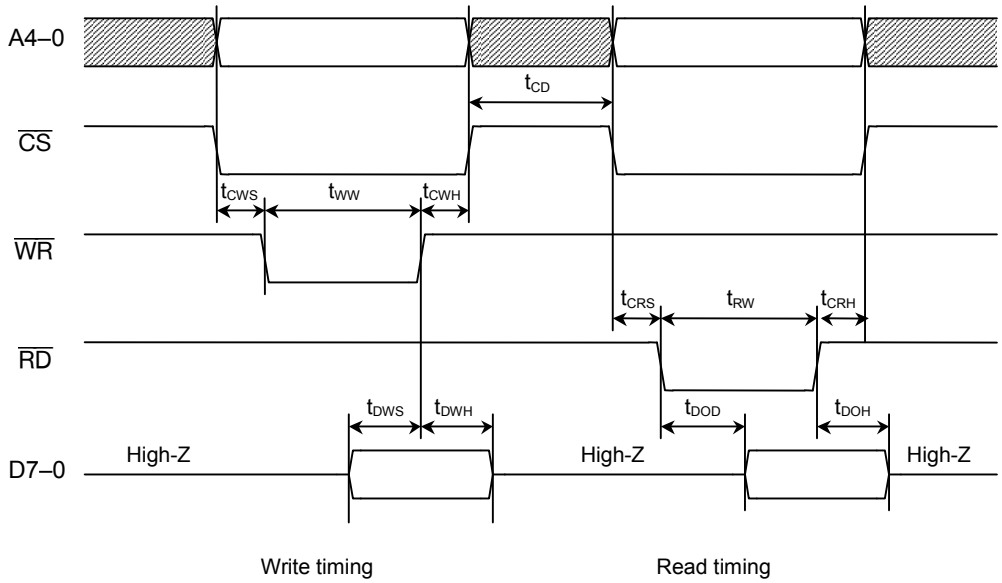
*1: PCMLNI1, PCMLNI2, PCMADI1, PCMADI2, PCMACI1, PCMACI2

Output Timing of PCM and ADPCM

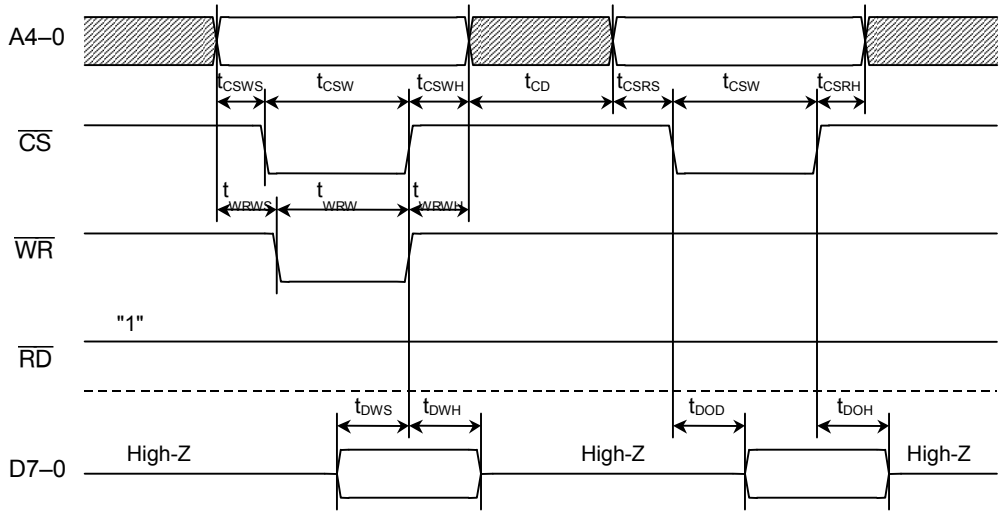


*1: PCMLNO1, PCMLNO2, PCMADO1, PCMADO2, PCMACO1, PCMACO2

Microcontroller Interface Write/Read Timing (WR/RD Independent Control)



Microcontroller interface Write/Read Timing (WR/RD Shared Control)



Write timing Read timing

FUNCTIONAL DESCRIPTION

Control registers
Table 1 shows a map of control registers.

Table 1-1 Control Register Map

Register name	Address					Data contents								R/W
	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	
CR0	0	0	0	0	0	SPDN	—	—	#PCMSEL	#IOSEL	—	—	#OPE_STAT	R/W
CR1	0	0	0	0	1	DMWR	—	—	—	—	—	—	—	R/W
CR2	0	0	0	1	0	CONTA1	ADPCM_RST1	DTHR1	TX_MUTE1	RX_MUTE1	RX_MLV21	RX_MLV11	RX_MLV01	R/W
CR3	0	0	0	1	1	CONTA2	ADPCM_RST2	DTHR2	TX_MUTE2	RX_MUTE2	RX_MLV22	RX_MLV12	RX_MLV02	R/W
CR4	0	0	1	0	0	INT	READY	—	—	TTDET2	RTDET2	TTDET1	RTDET1	R
CR5	0	0	1	0	1	TGEN_EXE_FLAG2	VOX_OUT2	VOX_MONI12	VOX_MONI02	TGEN_EXE_FLAG1	VOX_OUT1	VOX_MONI11	VOX_MONI01	R
CR6	0	0	1	1	0	A15	A14	A13	A12	A11	A10	A9	A8	R/W
CR7	0	0	1	1	1	A7	A6	A5	A4	A3	A2	A1	A0	R/W
CR8	0	1	0	0	0	D15	D14	D13	D12	D11	D10	D9	D8	R/W
CR9	0	1	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0	R/W
CR10	0	1	0	1	0	—	—	—	—	—	—	—	—	—
CR11	0	1	0	1	1	—	—	—	#PCM_SEL41	#PCM_SEL31	#PCM_SEL21	#PCM_SEL11	#PCM_SEL01	R/W
CR12	0	1	1	0	0	—	—	—	#PCM_SEL42	#PCM_SEL32	#PCM_SEL22	#PCM_SEL12	#PCM_SEL02	R/W
CR13	0	1	1	0	1	—	—	—	#ADPCM_SEL41	#ADPCM_SEL31	#ADPCM_SEL21	#ADPCM_SEL11	#ADPCM_SEL01	R/W
CR14	0	1	1	1	0	—	—	—	#ADPCM_SEL42	#ADPCM_SEL32	#ADPCM_SEL22	#ADPCM_SEL12	#ADPCM_SEL02	R/W
CR15	0	1	1	1	1	—	—	—	—	—	—	—	—	—

Note: In the R/W column,
R/W: Read/Write enable, R: Read only, —: Read/Write inhibit
Note: In the Data contents column,
—: Reserved bit. Do not change the initial value.
#: Control bit that can be changed only in initial mode

Table 1-2 Control Register Map

Register name	Address					Data contents								R/W
	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	
CR16	1	0	0	0	0	TX_TONE_GAIN31	TX_TONE_GAIN21	TX_TONE_GAIN11	TX_TONE_GAIN01	RX_TONE_GAIN31	RX_TONE_GAIN21	RX_TONE_GAIN11	RX_TONE_GAIN01	R/W
CR17	1	0	0	0	1	DTMF_SEL1	TX_TONE_SEND1	RX_TONE_SEND1	TONE41	TONE31	TONE21	TONE11	TONE01	R/W
CR18	1	0	0	1	0	TX_TONE_GAIN32	TX_TONE_GAIN22	TX_TONE_GAIN12	TX_TONE_GAIN02	RX_TONE_GAIN32	RX_TONE_GAIN22	RX_TONE_GAIN12	RX_TONE_GAIN02	R/W
CR19	1	0	0	1	1	DTMF_SEL2	TX_TONE_SEND2	RX_TONE_SEND2	TONE42	TONE32	TONE22	TONE12	TONE02	R/W
CR20	1	0	1	0	0	—	—	—	—	—	—	TDET_EN2	TDET_EN1	R/W
CR21	1	0	1	0	1	VOX_ON1	VOX_ON_LVL11	VOX_ON_LVL01	VOX_OFF_TIME1	—	VOX_IN1	RX_NOISE_LVL11	RX_NOISE_LVL01	R/W
CR22	1	0	1	1	0	VOX_ON2	VOX_ON_LVL12	VOX_ON_LVL02	VOX_OFF_TIME2	—	VOX_IN2	RX_NOISE_LVL12	RX_NOISE_LVL02	R/W
CR23	1	0	1	1	1	—	—	—	—	—	—	—	—	—
CR24	1	1	0	0	0	—	—	—	—	—	—	—	—	—
CR25	1	1	0	0	1	—	—	—	—	LPADL11	LPADL01	GPADL11	GPADL01	R/W
CR26	1	1	0	1	0	—	—	—	—	LPADL12	LPADL02	GPADL12	GPADL02	R/W
CR27	1	1	0	1	1	LTHR1	LAFF_RST1	LHLD1	LHD1	LCLP1	—	LATT1	LGC1	R/W
CR28	1	1	1	0	0	LTHR2	LAFF_RST2	LHLD2	LHD2	LCLP2	—	LATT2	LGC2	R/W
CR29	1	1	1	0	1	—	—	—	—	—	—	—	—	—
CR30	1	1	1	1	0	—	—	—	—	—	—	—	—	—
CR31	1	1	1	1	1	—	—	—	—	—	—	—	—	—

Note: In the R/W column,
R/W: Read/Write enable, R: Read only, —: Read/Write inhibit
Note: In the Data contents column,
—: Reserved bit. Do not change the initial value.
#: Control bit that can be changed only in initial mode

(1) CR0 (Basic operation mode setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR0	SPDN	—	—	PCMSEL	IOSEL	—	—	OPE_STAT
Initial value(*1)	0	0	0	0	0	0	0	0

*1: The initial value refers to the value that is set when this LSI is reset by the $\overline{PDN/RST}$ pin. (Also when reset by SPDN of B7, the bits other than CR0-B7 are set to their initial value.)

B7: Software power-down control
0: Normal operation 1: Power-down/reset
At power-down/reset, this LSI enters a power-down state. In this case, each bit of the control register, internal variables including internal data memories, and the echo canceler coefficients are reset.
This LSI enters the initial mode about 200 ms after the release of power-down/reset.
This bit is OR'ed with the inverted $\overline{PDN/RST}$ signal internally.

B6–B5: Resrved bits

B4: PCM coding format selection
0: μ-law 1: A-law
PCM coding format selection bit for digital speech signals. Set this bit to "0" to select the μ-law PCM coding format; set this bit to "1" to select A-law PCM coding format. The setting of this bit can be changed in initial mode only.

B3: PCM signal I/O control
PCM signal I/O control setting bit. (See Figure 1 and Figure 2)

B2–B1: Reserved bits

B0: Operation start control
0: Initial mode 1: Operation start

Initial mode:
This LSI enters the initial mode about 200 ms after release of reset/power-down. Start modification of the control registers and internal data memories after reading READY(CR4-B6) consecutively and detecting "1".
This LSI has several control registers and internal data memories which could be tuned only in this initial mode. For more details, please refer to Table 1-1, Table 1-2, Figure 9, Table 26, Table 27 and Table 28.
In this mode, the PCM output pin is in a high impedance state. The PCM input pin is processed internally as idle pattern input and the line echo canceler, ADPCM transcoder, tone generator, tone detector, and the MUTE and VOX functions are disabled.

Operation start:
By setting this bit to "1", READY (CR4-B6) is set to "0" and the LSI enters a normal operation mode. The line echo canceler, ADPCM transcoder, tone generator, tone detector, and MUTE and VOX functions are enabled dependent upon the control register setting.

(2) CR1 (internal data memory write control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR1	DMWR	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

B7: Internal data memory write control

0: Write inhibit 1: Write enable

This is a write command bit for internal data memory.

By writing "1" into this bit, data specified in CR8 (D15–D8) and CR9 (D7–D0) is written into the internal data memory whose address is specified by CR6 (A15–A8) and CR7 (A7–A0). For more details, please refer to descriptions under INTERNAL DATA MEMORY ACCESS METHOD.

B6–B0: Reserved bits

(3) CR2 (Channel 1 ADPCM section operation mode and I/O signal setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR2	CONTA1	ADPCM_ RST1	DTHR1	TX_ MUTE1	RX_ MUTE1	RX_ MLV21	RX_ MLV11	RX_ MLV01
Initial value	0	0	0	0	0	0	0	0

B7: Channel 1 ADPCM transcoder enable/through control
0: ADPCM transcoder enabled mode
1: ADPCM transcoder-through end-to-end 8-bit PCM mode
When this bit is set to "1", the ADPCM transcoder enters a through mode and the IS1 pin is configured to be an 8-bit serial input and the IR1 pin an 8-bit serial output.

B6: ADPCM reset on the channel 1 transmit/receive side (according to the G.726 specifications)
0: Normal operation 1: Reset
When this bit is set to "1", the ADPCM transcoder is reset. While the transcoder is reset, inputs from IR1 pin and PCMADI1 pin become invalid and IS1 pin and PCMADO1 pin output idle patterns.

B5: Channel 1 end-to-end 4-bit ADPCM transparent control
0: Normal mode 1: end-to-end 4-bit ADPCM transparent mode
In through mode, end-to-end 4-bit ADPCM transparent mode is applied and the PCM I/O pin is configured to be a 4-bit serial input/output. The line echo canceler, ADPCM transcoder, tone generator, tone detector, and MUTE and VOX functions are all disabled.

B4: Channel 1 transmit side ADPCM data mute control
0: Normal operation 1: Mute
When this bit is set to "1", IS1 pin outputs idle patterns.

B3: Channel 1 receive side ADPCM data mute enable control
0: Normal operation 1: Mute enabled
The mute level set in B2, B1 and B0 is enabled.

B2–B0: Channel 1 receive side speech data mute level setting
The voice bus mute level on the receive side can be set by controlling this bit.

Table 2 Channel 1 Receive Voice Bus Mute Level Setting

RX_MLV21	RX_MLV11	RX_MLV01	Level
0	0	0	Through
0	0	1	–6dB
0	1	0	–12dB
0	1	1	–18dB
1	0	0	–24dB
1	0	1	–30dB
1	1	0	–36dB
1	1	1	MUTE

(4) CR3 (Channel 2 ADPCM section operation mode and I/O signal setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR3	CONTA2	ADPCM_ RST2	DTHR2	TX_MUT E2	RX_MUT E2	RX_MLV 22	RX_MLV 12	RX_MLV 02
Initial value	0	0	0	0	0	0	0	0

B7: Channel 2 ADPCM transcoder enable/through control
0: ADPCM transcoder enabled mode
1: ADPCM transcoder-through end-to-end 8-bit PCM mode
When this bit is set to "1", the ADPCM transcoder enters a through mode and the IS2 pin is configured to be an 8-bit serial input and the IR2 pin an 8-bit serial output.

B6: ADPCM reset on the Channel 2 transmit/receive side (according to the G.726 specifications)
0: Normal operation 1: Reset
When this bit is set to "1", the ADPCM transcoder is reset. While the transcoder is reset, inputs from IR1 pin and PCMADI2 pin become invalid and IS2 pin and PCMADO2 pin output idle patterns.

B5: Channel 2 end-to-end 4-bit ADPCM transparent control
0: Normal mode 1: end-to-end 4-bit ADPCM transparent mode
In through mode, end-to-end 4-bit ADPCM transparent mode is applied and the PCM I/O pin is configured to be a 4-bit serial input/output. The line echo canceler, ADPCM transcoder, tone generator, tone detector, and MUTE and VOX functions are all disabled.

B4: Channel 2 transmit side ADPCM data mute control
0: Normal operation 1: Mute
When this bit is set to "1", IS2 pin outputs idle patterns.

B3: Channel 2 receive side ADPCM data mute enable control
0: Normal operation 1: Mute enabled
The mute level set in B2, B1 and B0 is enabled.

B2–B0: Channel 2 receive side speech data mute level setting
The voice bus mute level on the receive side can be set by controlling this bit.

Table 3 Channel 2 Receive Voice Bus Mute Level Setting

RX_MLV22	RX_MLV12	RX_MLV02	Level
0	0	0	Through
0	0	1	–6dB
0	1	0	–12dB
0	1	1	–18dB
1	0	0	–24dB
1	0	1	–30dB
1	1	0	–36dB
1	1	1	MUTE

(5) CR4 (READY and detection register, Read Only)

	B7	B6	B5	B4	B3	B2	B1	B0
CR4	INT	READY	—	—	TTDET2	RTDET2	TTDET1	RTDET1
Initial value	0	1	0	0	0	0	0	0

B7: Interrupt status register
0: When the $\overline{INT}$ pin is "1" 1: When the $\overline{INT}$ pin is "0"
Register where the logic of the $\overline{INT}$ pin is inverted. This register reflects a status of the $\overline{INT}$ pin. When the $\overline{INT}$ pin is "0", "1" is read. In other cases, "0" is read.

B6: Initial mode status register
0: In normal operation mode (not in the initial mode) 1: In initial mode
This LSI goes into the initial mode about 200 ms after release of power-down/reset. In initial mode, this bit becomes "1", which shows that the internal data access is possible. By setting OPE_STAT (CR0-B0)="1", this LSI gets out of the initial mode and goes into normal operation mode as well as this bit is automatically set to "0". It could be known by checking this bit if the LSI is currently in the initial mode.

B5–B4: Reserved bits

B3: Channel 2 transmit side tone detection status register
0: Not detected 1: Detected
Detected/Not detected status register bit of the tone detector on the channel 2 transmit side. For more details, please refer to Figure 5.

B2: Channel 2 receive side tone detection status register
0: Not detected 1: Detected
Detected/Not detected status register bit of the tone detector on the channel 2 receive side. For more details, please refer to Figure 5.

B1: Channel 1 transmit side tone detection status register
0: Not detected 1: Detected
Detected/Not detected status register bit of the tone detector on the channel 1 transmit side. For more details, please refer to Figure 5.

B0: Channel 1 receive side tone detection status register
0: Not detected 1: Detected
Detected/Not detected status register bit of the tone detector on the channel 1 receive side. For more details, please refer to Figure 5.

(6) CR5 (VOX function status register, Read Only)

	B7	B6	B5	B4	B3	B2	B1	B0
CR5	TGEN_EXE _FLAG2	VOX_ OUT2	VOX_ MONI12	VOX_ MONI02	TGEN_EXE _FLAG1	VOX_ OUT1	VOX_ MONI11	VOX_ MONI01
Initial value	0	0	0	0	0	0	0	0

B7: Channel 2 tone generator execution status register
0: Inactive 1: Operating
Channel 2 tone generator execution status register bit. At the start of tone generation, this bit is set to "1" and when tone is not generated, the bit is set to "0". When the Fade In/Fade Out function is enabled, this bit does not go back to "0" at the change of TX_TONE_SEND2 (CR19-B6) or RX_TONE_SEND2 (CR19-B5) from "1" to "0", and retains "1" till the completion of Fade Out, and after the completion of Fade Out, the bit is set to "0". Even after this bit has changed to "0", generation of tone signals may be continued for several SYNC cycles due to the LSI-internal processing delay.

B6: Channel 2 transmit side voice/silence detection
0: Silence 1: Voice

B5–B4: Channel 2 transmit side detected power indicator
Indicator bits for Channel 2 transmit side power. By reading these bits, power of signals on Channel 2 transmit side relative to voice/silence threshold set by CR22-B6, B5 can be known. This function is enabled when CR22-B7 is set to "1", that is, VOX function is ON. When CR22-B7 is set to "0", that is, VOX function is OFF, these bits stay "0" independently upon Channel 2 transmit side power.

Table 4 Channel 2 Transmit Side Relative Power

VOX_MONI12	VOX_MONI02	Relative power against the transmit side voice/silence threshold set by CR22-B6 and –B5
0	0	–10 dB or lower, or VOX disabled
0	1	–5 to –10 dB
1	0	0 to –5 dB
1	1	0 dB or higher

B3: Channel 1 tone generator execution status register
0: Inactive 1: Operating
Channel 1 tone generator execution status register bit. At the start of tone gernation, this bit is set to "1" and when tone is not generated, the bit is set to "0". When the Fade In/Fade Out function is enabled, this bit does not go back to "0" at the change of TX_TONE_SEND1 (CR17-B6) or RX_TONE_SEND1 (CR17-B5) from "1" to "0", and retains "1" till the completion of Fade Out, and after the completion of Fade Out, the bit is set to "0". Even after this bit has changed to "0", generation of tone signals may be continued for several SYNC cycles due to the LSI-internal processing delay.

B2: Channel 1 transmit side voice/silence detection
0: Silence 1: Voice

B1–B0: Channel 1 transmit side detected power indicator
Indicator bits for Channel 1 transmit side power. By reading these bits, power of signals on Channel 1 transmit side relative to voice/silence threshold set by CR21-B6, B5 can be known. This function is enabled when CR21-B7 is set to “1”, that is, VOX function is ON. When CR21-B7 is set to “0”, that is, VOX function is OFF, these bits stay “0” independently upon Channel 1 transmit side power.

Table 5 Channel 1 Transmit Side Relative Power

VOX_MONI11	VOX_MONI01	Relative power against the transmit side voice/silence threshold set by CR21-B6 and –B5
0	0	–10 dB or lower, or VOX disabled
0	1	–5 to –10 dB
1	0	0 to –5 dB
1	1	0 dB or higher

(7) CR6 (Internal data memory write register)

	B7	B6	B5	B4	B3	B2	B1	B0
CR6	A15	A14	A13	A12	A11	A10	A9	A8
Initial value	0	1	1	1	0	0	1	0

B7–0: Upper address control for internal data memory
Upper address setting register for internal data memory.
See the INTERNAL DATA MEMORY ACCESS for how to write into internal data memory.
The initial value of CR6 indicates the upper two digits of ”ML7202”.

(8) CR7 (Internal data memory write register)

	B7	B6	B5	B4	B3	B2	B1	B0
CR7	A7	A6	A5	A4	A3	A2	A1	A0
Initial value	0	0	0	0	0	0	1	0

B7–0: Lower address control for internal data memory
Lower address setting register for internal data memory.
See the INTERNAL DATA MEMORY ACCESS METHOD for how to write into internal data memory.
The initial value of CR7 indicates the lower two digits of “ML7202”.

(9) CR8 (Internal data memory write register)

	B7	B6	B5	B4	B3	B2	B1	B0
CR8	D15	D14	D13	D12	D11	D10	D9	D8
Initial value	0	0	0	0	0	0	0	1

B7–0: Upper data control for internal data memory
Upper data setting register for internal data memory.
See the INTERNAL DATA MEMORY ACCESS METHOD for how to write into internal data memory.
The initial value of CR8 indicates “-001” of “ML7202-001”.

(10) CR9 (Internal data memory write register)

	B7	B6	B5	B4	B3	B2	B1	B0
CR9	D7	D6	D5	D4	D3	D2	D1	D0
Initial value	0	0	0	0	0	0	0	1

B7–0: Lower data control for internal data memory
Lower data setting register for internal data memory.
See the INTERNAL DATA MEMORY ACCESS METHOD for how to write into internal data memory.

(11) CR10 (reserved register)

	B7	B6	B5	B4	B3	B2	B1	B0
CR10	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

B7–B0: Reserved bits

(12) CR11 (Channel 1 PCM I/O time slot assignment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR11	—	—	—	PCM_ SEL41	PCM_ SEL31	PCM_ SEL21	PCM_ SEL11	PCM_ SEL01
Initial value	0	0	0	0	0	0	0	0

B7–B5: Reserved bits

B4–B0: PCM CODEC time slot assignment control
Registers to control time PCM data slot assignment for channel 1. The setting of thse bits can be changed only in initial mode.The PCM data can be assigned to an arbitrary time slot as per Table 6 herebelow. The PCM I/O pins subject to this time slot assignment are as follows: PCMLNI1, PCMLNO1, PCMACI1, PCMACO1, PCMADI1, and PCMADO1.

Table 6 PCM CODEC Time Slot Assignment

B4	B3	B2	B1	B0	Assigned Time Slot	B4	B3	B2	B1	B0	Assigned Time Slot
0	0	0	0	0	Time Slot 1	1	0	0	0	0	Time Slot 17
0	0	0	0	1	Time Slot 2	1	0	0	0	1	Time Slot 18
0	0	0	1	0	Time Slot 3	1	0	0	1	0	Time Slot 19
0	0	0	1	1	Time Slot 4	1	0	0	1	1	Time Slot 20
0	0	1	0	0	Time Slot 5	1	0	1	0	0	Time Slot 21
0	0	1	0	1	Time Slot 6	1	0	1	0	1	Time Slot 22
0	0	1	1	0	Time Slot 7	1	0	1	1	0	Time Slot 23
0	0	1	1	1	Time Slot 8	1	0	1	1	1	Time Slot 24
0	1	0	0	0	Time Slot 9	1	1	0	0	0	Time Slot 25
0	1	0	0	1	Time Slot 10	1	1	0	0	1	Time Slot 26
0	1	0	1	0	Time Slot 11	1	1	0	1	0	Time Slot 27
0	1	0	1	1	Time Slot 12	1	1	0	1	1	Time Slot 28
0	1	1	0	0	Time Slot 13	1	1	1	0	0	Time Slot 29
0	1	1	0	1	Time Slot 14	1	1	1	0	1	Time Slot 30
0	1	1	1	0	Time Slot 15	1	1	1	1	0	Time Slot 31
0	1	1	1	1	Time Slot 16	1	1	1	1	1	Time Slot 32

(13) CR12 (Channel 2 PCM I/O time slot assignment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR12	—	—	—	PCM_ SEL42	PCM_ SEL32	PCM_ SEL22	PCM_ SEL12	PCM_ SEL02
Initial value	0	0	0	0	0	0	0	0

B7–B5: Reserved bits

B4–B0: PCM CODEC time slot assignment control
Registers to control PCM data time slot assignment for channel 2. The setting of these bits can be changed only in initial mode. The PCM data can be assigned to an arbitrary time slot as per Table 7 herebelow. The PCM I/O pins subject to this time slot assignment are as follows: PCMLNI2, PCMLNO2, PCMACI2, PCMACO2, PCMADI2, and PCMADO2.

Table 7 PCM CODEC Time Slot Assignment

B4	B3	B2	B1	B0	Assigned Time Slot	B4	B3	B2	B1	B0	Assigned Time Slot
0	0	0	0	0	Time Slot 1	1	0	0	0	0	Time Slot 17
0	0	0	0	1	Time Slot 2	1	0	0	0	1	Time Slot 18
0	0	0	1	0	Time Slot 3	1	0	0	1	0	Time Slot 19
0	0	0	1	1	Time Slot 4	1	0	0	1	1	Time Slot 20
0	0	1	0	0	Time Slot 5	1	0	1	0	0	Time Slot 21
0	0	1	0	1	Time Slot 6	1	0	1	0	1	Time Slot 22
0	0	1	1	0	Time Slot 7	1	0	1	1	0	Time Slot 23
0	0	1	1	1	Time Slot 8	1	0	1	1	1	Time Slot 24
0	1	0	0	0	Time Slot 9	1	1	0	0	0	Time Slot 25
0	1	0	0	1	Time Slot 10	1	1	0	0	1	Time Slot 26
0	1	0	1	0	Time Slot 11	1	1	0	1	0	Time Slot 27
0	1	0	1	1	Time Slot 12	1	1	0	1	1	Time Slot 28
0	1	1	0	0	Time Slot 13	1	1	1	0	0	Time Slot 29
0	1	1	0	1	Time Slot 14	1	1	1	0	1	Time Slot 30
0	1	1	1	0	Time Slot 15	1	1	1	1	0	Time Slot 31
0	1	1	1	1	Time Slot 16	1	1	1	1	1	Time Slot 32

(14) CR13 (Channel 1 ADPCM I/O time slot assignment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR13	—	—	—	ADPCM_ SEL41	ADPCM_ SEL31	ADPCM_ SEL21	ADPCM_ SEL11	ADPCM_ SEL01
Initial value	0	0	0	0	0	0	0	0

B7–B5: Reserved bits

B4–B0: ADPCM CODEC time slot assignment control
Registers to control ADPCM data time assignment for channel 1. The setting of these bits can be changed only in initial mode. The ADPCM data can be assigned to an arbitrary time slot as per Table 8. The ADPCM I/O pins subject to this time slot assignment are the IS1and IR1 pins.

Table 8 ADPCM CODEC Time Slot Assignment

B4	B3	B2	B1	B0	Assigned Time Slot	B4	B3	B2	B1	B0	Assigned Time Slot
0	0	0	0	0	Time Slot 1	1	0	0	0	0	Time Slot 17
0	0	0	0	1	Time Slot 2	1	0	0	0	1	Time Slot 18
0	0	0	1	0	Time Slot 3	1	0	0	1	0	Time Slot 19
0	0	0	1	1	Time Slot 4	1	0	0	1	1	Time Slot 20
0	0	1	0	0	Time Slot 5	1	0	1	0	0	Time Slot 21
0	0	1	0	1	Time Slot 6	1	0	1	0	1	Time Slot 22
0	0	1	1	0	Time Slot 7	1	0	1	1	0	Time Slot 23
0	0	1	1	1	Time Slot 8	1	0	1	1	1	Time Slot 24
0	1	0	0	0	Time Slot 9	1	1	0	0	0	Time Slot 25
0	1	0	0	1	Time Slot 10	1	1	0	0	1	Time Slot 26
0	1	0	1	0	Time Slot 11	1	1	0	1	0	Time Slot 27
0	1	0	1	1	Time Slot 12	1	1	0	1	1	Time Slot 28
0	1	1	0	0	Time Slot 13	1	1	1	0	0	Time Slot 29
0	1	1	0	1	Time Slot 14	1	1	1	0	1	Time Slot 30
0	1	1	1	0	Time Slot 15	1	1	1	1	0	Time Slot 31
0	1	1	1	1	Time Slot 16	1	1	1	1	1	Time Slot 32

(15) CR14 (Channel 2 ADPCM I/O time slot assignment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR14	—	—	—	ADPCM_ SEL42	ADPCM_ SEL32	ADPCM_ SEL22	ADPCM_ SEL12	ADPCM_ SEL02
Initial value	0	0	0	0	0	0	0	0

B7–B5: Reserved bits

B4–B0: ADPCM CODEC time slot assignment control
Registers to control ADPCM data time slot assignment for channel 2. The setting of these bits can be changed only in initial mode. The ADPCM data can be assigned to an arbitrary time slot as per Table 9 herebelow. The ADPCM I/O subject to this time slot assignment are the IS2 and IR2 pins.

Table 9 ADPCM CODEC Time Slot Assignment

B4	B3	B2	B1	B0	Assigned Time Slot	B4	B3	B2	B1	B0	Assigned Time Slot
0	0	0	0	0	Time Slot 1	1	0	0	0	0	Time Slot 17
0	0	0	0	1	Time Slot 2	1	0	0	0	1	Time Slot 18
0	0	0	1	0	Time Slot 3	1	0	0	1	0	Time Slot 19
0	0	0	1	1	Time Slot 4	1	0	0	1	1	Time Slot 20
0	0	1	0	0	Time Slot 5	1	0	1	0	0	Time Slot 21
0	0	1	0	1	Time Slot 6	1	0	1	0	1	Time Slot 22
0	0	1	1	0	Time Slot 7	1	0	1	1	0	Time Slot 23
0	0	1	1	1	Time Slot 8	1	0	1	1	1	Time Slot 24
0	1	0	0	0	Time Slot 9	1	1	0	0	0	Time Slot 25
0	1	0	0	1	Time Slot 10	1	1	0	0	1	Time Slot 26
0	1	0	1	0	Time Slot 11	1	1	0	1	0	Time Slot 27
0	1	0	1	1	Time Slot 12	1	1	0	1	1	Time Slot 28
0	1	1	0	0	Time Slot 13	1	1	1	0	0	Time Slot 29
0	1	1	0	1	Time Slot 14	1	1	1	0	1	Time Slot 30
0	1	1	1	0	Time Slot 15	1	1	1	1	0	Time Slot 31
0	1	1	1	1	Time Slot 16	1	1	1	1	1	Time Slot 32

(16) CR15 (reserved register)

	B7	B6	B5	B4	B3	B2	B1	B0
CR15	—	—	—	—	—	—	—	—
Initial value	1	0	1	0	0	0	0	0

B7–B0: Reserved bits

(17) CR16 (Channel 1 tone generator gain adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR16	TX_TONE _GAIN31	TX_TONE _GAIN21	TX_TONE _GAIN11	TX_TONE _GAIN01	RX_TONE _GAIN31	RX_TONE _GAIN21	RX_TONE _GAIN11	RX_TONE _GAIN01
Initial value	0	0	0	0	0	0	0	0

B7–B4: Tone generator transmit side gain adjustment
Bits for adjusting the transmit side attenuator (ATTtgtx1) gain on the channel 1 tone generator. Transmit side gain can be changed by controlling these bits.

Table 10 Transmit Side Tone Generator Gain Setting

B7	B6	B5	B4	Tone generator gain	B7	B6	B5	B4	Tone generator gain
0	0	0	0	–36 dB	1	0	0	0	–20 dB
0	0	0	1	–34 dB	1	0	0	1	–18 dB
0	0	1	0	–32 dB	1	0	1	0	–16 dB
0	0	1	1	–30 dB	1	0	1	1	–14 dB
0	1	0	0	–28 dB	1	1	0	0	–12 dB
0	1	0	1	–26 dB	1	1	0	1	–10 dB
0	1	1	0	–24 dB	1	1	1	0	–8 dB
0	1	1	1	–22 dB	1	1	1	1	–6 dB

B3–B0: Tone generator receive side gain adjustment
Bits for adjusting the receive side attenuator (ATTtgtx1) gain on the channel 1 tone generator. Receive side gain can be changed by controlling these bits.

Table 11 Receive Side Tone Generator Gain Setting

B3	B2	B1	B0	Tone generator gain	B3	B2	B1	B0	Tone generator gain
0	0	0	0	–36 dB	1	0	0	0	–20 dB
0	0	0	1	–34 dB	1	0	0	1	–18 dB
0	0	1	0	–32 dB	1	0	1	0	–16 dB
0	0	1	1	–30 dB	1	0	1	1	–14 dB
0	1	0	0	–28 dB	1	1	0	0	–12 dB
0	1	0	1	–26 dB	1	1	0	1	–10 dB
0	1	1	0	–24 dB	1	1	1	0	–8 dB
0	1	1	1	–22 dB	1	1	1	1	–6 dB

The original level of output tone from TONE_A (high-tone group) generator and TONE_B (low-tone group) generator are fixed as follows (see Figure 6):
DTMF tone (low-tone group) : –2 dBm0
DTMF tone (high-tone group) and single tone : 0 dBm0

Hence, for instance, assuming TGEN_GAIN_H1 and TGEN_GAIN_L1 are set to 0 dB (default), if you set the CR16-B3, B2, B1, B0 to [1, 1, 1, 1] (= -6dB), then, the output level from the PCMLNO1 pin will be as follows;
DTMF tone (low-tone group) : –8 dBm0
DTMF tone (high-tone group) and single tone : –6 dBm0

Note:
As shown in Figure 6, the ATTtgtx1 and the ATTtgrx1 are attenuators to tune a level of tones after addition of output of TONE_A generator and that of TONE_B generator. On the other hand, levels of tones before addition of output of TONE_A generator and that of TONE_B generator can be tuned by the TGEN_GAIN_H1 and the TGEN_GAIN_L1.
Each gain of the TGEN_GAIN_H1 and the TGEN_GAIN_L1 can be changed through internal data memory access. See the write method of the INTERNAL DATA MEMORY ACCESS METHOD and Table 26 Internal data memory related control registers for the way to change the internal data memory setting.

(18) CR17 (Channel 1 tone generator operation mode and frequency setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR17	DTMF_ SEL1	TX_TONE _SEND1	RX_TONE _SEND1	TONE41	TONE31	TONE21	TONE11	TONE01
Initial value	0	0	0	0	0	0	0	0

B7: Selection between DTMF tone and single tone
0: Single tone 1: DTMF tone
A register bit to select between single tone and DTMF tone for Channel 1 tone generator. When this bit is set to "1", DTMF tone is selected and when this bit is set to "0", single tone is selected. The frequency of tone can be changed by CR17-B4, B3, B2, B1, B0 and internal data memory access.

B6: Execution of tone generation toward the transmit side
0: Does not execute tone generation 1: Executes tone generation
Selection bit for execution of tone generation toward the transmit side on the channel 1.
This LSI does not have tone generators respectively toward transmit side and toward receive side but shares the common tone generators toward both directions. Hence, if the execution of tone generation toward the transmit side gets enabled while tone generation on the receive side is being enabled, the transmit side would start receiving tone signals at an arbitrary and perhaps odd timing in terms of a phase of the waveform of the tone so that slight noises may take place dependent upon the timing. When using the tone generator in such a manner, it is recommended to utilize the tone fade function to minimize the noises.

B5: Execution of tone generation toward the receive side
0: Does not execute tone generation 1: Executes tone generation
Selection bit for execution of tone generation toward the receive side on the channel 1.
This LSI does not have tone generators respectively toward transmit side and toward receive side but shares the common tone generators toward both directions. Hence, if the execution of tone generation toward the receive side gets enabled while tone generation on the transmit side is being enabled, the receive side would start receiving tone signals at an arbitrary and perhaps odd timing in terms of a phase of the waveform of the tone so that slight noises may take place dependent upon the timing. When using the tone generator in such a manner, it is recommended to utilize the tone fade function to minimize the noises.

B4–B0: Tone frequency setting
Output frequency setting bit of channel 1 tone generator

Table 12 Tone Generator Output Frequency Setting (when CR17-B7="1")

B4	B3	B2	B1	B0	Frequency
*	0	0	0	0	697 Hz + 1209 Hz (1)
*	0	0	0	1	697 Hz + 1336 Hz (2)
*	0	0	1	0	697 Hz + 1477 Hz (3)
*	0	0	1	1	697 Hz + 1633 Hz (A)
*	0	1	0	0	770 Hz + 1209 Hz (4)
*	0	1	0	1	770 Hz + 1336 Hz (5)
*	0	1	1	0	770 Hz + 1477 Hz (6)
*	0	1	1	1	770 Hz + 1633 Hz (B)
*	1	0	0	0	852 Hz + 1209 Hz (7)
*	1	0	0	1	852 Hz + 1336 Hz (8)
*	1	0	1	0	852 Hz + 1477 Hz (9)
*	1	0	1	1	852 Hz + 1633 Hz (C)
*	1	1	0	0	941 Hz + 1209 Hz (*)
*	1	1	0	1	941 Hz + 1336 Hz (0)
*	1	1	1	0	941 Hz + 1477 Hz (#)
*	1	1	1	1	941 Hz + 1633 Hz (D)

Table 13 Tone Generator Output Frequency Setting (when CR17-B7="0")

The following table shows default single tone frequencies.

B4	B3	B2	B1	B0	Frequency	B4	B3	B2	B1	B0	Frequency
0	0	0	0	0	440 Hz	1	0	0	0	0	1109 Hz
0	0	0	0	1	466 Hz	1	0	0	0	1	1175 Hz
0	0	0	1	0	494 Hz	1	0	0	1	0	1245 Hz
0	0	0	1	1	523 Hz	1	0	0	1	1	1319 Hz
0	0	1	0	0	554 Hz	1	0	1	0	0	1397 Hz
0	0	1	0	1	587 Hz	1	0	1	0	1	1480 Hz
0	0	1	1	0	622 Hz	1	0	1	1	0	1568 Hz
0	0	1	1	1	659 Hz	1	0	1	1	1	1661 Hz
0	1	0	0	0	698 Hz	1	1	0	0	0	1760 Hz
0	1	0	0	1	740 Hz	1	1	0	0	1	400 Hz
0	1	0	1	0	784 Hz	1	1	0	1	0	1000 Hz
0	1	0	1	1	831 Hz	1	1	0	1	1	2000 Hz
0	1	1	0	0	880 Hz	1	1	1	0	0	2667 Hz
0	1	1	0	1	932 Hz	1	1	1	0	1	1300 Hz
0	1	1	1	0	988 Hz	1	1	1	1	0	2080 Hz
0	1	1	1	1	1047 Hz	1	1	1	1	1	3000 Hz

The frequency for a single tone can be tuned in initial mode through internal data memory access. See the write method of the INTERNAL DATA MEMORY ACCESS METHOD and Table 26 Internal data memory related control registers for the way to change the internal data memory setting.

(19) CR18 (Channel 2 tone generator gain adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR18	TX_TONE _GAIN32	TX_TONE _GAIN22	TX_TONE _GAIN12	TX_TONE _GAIN02	RX_TONE _GAIN32	RX_TONE _GAIN22	RX_TONE _GAIN12	RX_TONE _GAIN02
Initial value	0	0	0	0	0	0	0	0

B7–B4: Tone generator transmit side gain adjustment
Bits for adjusting the transmit side attenuator (ATTtgtx2) gain on the channel 2 tone generator. Transmit side gain can be changed by controlling these bits.

Table 14 Transmit Side Tone Generator Gain Setting

B7	B6	B5	B4	Tone generator gain	B7	B6	B5	B4	Tone generator gain
0	0	0	0	–36 dB	1	0	0	0	–20 dB
0	0	0	1	–34 dB	1	0	0	1	–18 dB
0	0	1	0	–32 dB	1	0	1	0	–16 dB
0	0	1	1	–30 dB	1	0	1	1	–14 dB
0	1	0	0	–28 dB	1	1	0	0	–12 dB
0	1	0	1	–26 dB	1	1	0	1	–10 dB
0	1	1	0	–24 dB	1	1	1	0	–8 dB
0	1	1	1	–22 dB	1	1	1	1	–6 dB

B3–B0: Tone generator receive side gain adjustment
Bits for adjusting the receive side attenuator (ATTtgtx2) gain on the channel 2 tone generator. Receive side gain can be changed by controlling these bits.

Table 15 Transmit Side Tone Generator Gain Setting

B3	B2	B1	B0	Tone generator gain	B3	B2	B1	B0	Tone generator gain
0	0	0	0	–36 dB	1	0	0	0	–20 dB
0	0	0	1	–34 dB	1	0	0	1	–18 dB
0	0	1	0	–32 dB	1	0	1	0	–16 dB
0	0	1	1	–30 dB	1	0	1	1	–14 dB
0	1	0	0	–28 dB	1	1	0	0	–12 dB
0	1	0	1	–26 dB	1	1	0	1	–10 dB
0	1	1	0	–24 dB	1	1	1	0	–8 dB
0	1	1	1	–22 dB	1	1	1	1	–6 dB

The original level of output tone from TONE_C (high-tone group) generator and TONE_D (low-tone group) generator are as follows (see Figure 6):

DTMF tone (low-tone group)	: –2 dBm0
DTMF tone (high-tone group) and single tone	: 0 dBm0

Hence, for instance, assuming TGEN_GAIN_H2 and TGEN_GAIN_L2 are set to 0 dB (default), if you set the CR18-B3, B2, B1, B0 to [1, 1, 1, 1] (= -6dB), then, the output level from the PCMLNO2 pin will be as follows;

DTMF tone (low-tone group)	: –8 dBm0
DTMF tone (high-tone group) and single tone	: –6 dBm0

Note:
As shown in Figure 6, the ATTtgtx2 and the ATTtgrx2 are attenuators to tune a level of tones after addition of output of TONE_C generator and that of TONE_D generator. On the other hand, levels of tones before addition of output of TONE_C generator and that of TONE_D generator can be tuned by the TGEN_GAIN_H2 and the TGEN_GAIN_L2.
Each gain of the TGEN_GAIN_H2 and the TGEN_GAIN_L2 can be changed through internal data memory access. See the write method of the INTERNAL DATA MEMORY ACCESS METHOD and Table 26 Internal data memory related control registers for the way to change the internal data memory setting.

(20) CR19 (Channel 2 tone generator operation mode and frequency setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR19	DTMF_ SEL2	TX_TONE _SEND2	RX_TONE _SEND2	TONE42	TONE32	TONE22	TONE12	TONE02
Initial value	0	0	0	0	0	0	0	0

B7: Selection between DTMF tone and single tone
0: Single tone 1: DTMF tone
A register bit to select between single tone and DTMF tone for Channel 2 tone generator. When this bit is set to "1", DTMF tone is selected and when this bit is set to "0", single tone is selected. The frequency of tone can be changed by CR19-B4, B3, B2, B1, B0 and internal data memory access.

B6: Execution of tone generation toward the transmit side
0: Does not execute tone generation 1: Executes tone generation
Selection bit for execution of tone generation toward the transmit side on the channel 2.
This LSI does not have tone generators respectively toward transmit side and toward receive side but shares the common tone generators toward both directions. Hence, if the execution of tone generation toward the transmit side gets enabled while tone generation on the receive side is being enabled, the transmit side would start receiving tone signals at an arbitrary and perhaps odd timing in terms of a phase of the waveform of the tone so that slight noises may take place dependent upon the timing. When using the tone generator in such a manner, it is recommended to utilize the tone fade function to minimize the noises.

B5: Execution of tone generation toward the receive side
0: Does not execute tone generation 1: Execute tone generation
Selection bit for execution of tone generation toward the receive side on the channel 2.
This LSI does not have tone generators respectively toward transmit side and toward receive side but shares the common tone generators toward both directions. Hence, if the execution of tone generation toward the receive side gets enabled while tone generation on the transmit side is being enabled, the receive side would start receiving tone signals at an arbitrary and perhaps odd timing in terms of a phase of the waveform of the tone so that slight noises may take place dependent upon the timing. When using the tone generator in such a manner, it is recommended to utilize the tone fade function to minimize the noises.

B4–B0: Tone frequency setting
Output frequency setting bit of channel 2 tone generator

Table 16 Tone Generator Output Frequency Setting (when CR19-B7="1")

B4	B3	B2	B1	B0	Frequency
*	0	0	0	0	697 Hz + 1209 Hz (1)
*	0	0	0	1	697 Hz + 1336 Hz (2)
*	0	0	1	0	697 Hz + 1477 Hz (3)
*	0	0	1	1	697 Hz + 1633 Hz (A)
*	0	1	0	0	770 Hz + 1209 Hz (4)
*	0	1	0	1	770 Hz + 1336 Hz (5)
*	0	1	1	0	770 Hz + 1477 Hz (6)
*	0	1	1	1	770 Hz + 1633 Hz (B)
*	1	0	0	0	852 Hz + 1209 Hz (7)
*	1	0	0	1	852 Hz + 1336 Hz (8)
*	1	0	1	0	852 Hz + 1477 Hz (9)
*	1	0	1	1	852 Hz + 1633 Hz (C)
*	1	1	0	0	941 Hz + 1209 Hz (*)
*	1	1	0	1	941 Hz + 1336 Hz (0)
*	1	1	1	0	941 Hz + 1477 Hz (#)
*	1	1	1	1	941 Hz + 1633 Hz (D)

Table 17 Tone Generator Output Frequency Setting (when CR19-B7="0")

The following table shows default single tone frequencies.

B4	B3	B2	B1	B0	Frequency	B4	B3	B2	B1	B0	Frequency
0	0	0	0	0	440 Hz	1	0	0	0	0	1109 Hz
0	0	0	0	1	466 Hz	1	0	0	0	1	1175 Hz
0	0	0	1	0	494 Hz	1	0	0	1	0	1245 Hz
0	0	0	1	1	523 Hz	1	0	0	1	1	1319 Hz
0	0	1	0	0	554 Hz	1	0	1	0	0	1397 Hz
0	0	1	0	1	587 Hz	1	0	1	0	1	1480 Hz
0	0	1	1	0	622 Hz	1	0	1	1	0	1568 Hz
0	0	1	1	1	659 Hz	1	0	1	1	1	1661 Hz
0	1	0	0	0	698 Hz	1	1	0	0	0	1760 Hz
0	1	0	0	1	740 Hz	1	1	0	0	1	400 Hz
0	1	0	1	0	784 Hz	1	1	0	1	0	1000 Hz
0	1	0	1	1	831 Hz	1	1	0	1	1	2000 Hz
0	1	1	0	0	880 Hz	1	1	1	0	0	2667 Hz
0	1	1	0	1	932 Hz	1	1	1	0	1	1300 Hz
0	1	1	1	0	988 Hz	1	1	1	1	0	2080 Hz
0	1	1	1	1	1047 Hz	1	1	1	1	1	3000 Hz

The frequency for a single tone can be tuned in initial mode through internal data memory access. See the write method of the INTERNAL DATA MEMORY ACCESS METHOD and Table 26 Internal data memory related control registers for the way to change the internal data memory setting.

(21) CR20 (Tone detector operation setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR20	—	—	—	—	—	—	TDET_EN2	TDET_EN1
Initial value	0	0	0	0	0	0	0	0

B7–B2: Reserved bits

B1: Channel 2 tone detector ON/OFF control
0: OFF 1: ON
Channel 2 tone detector ON/OFF selection bit. When this bit is set to "1", the detector is set to ON and CR4-B3 and B2 (TTDET2 and RTDET2) is enabled to shows the tone detection results.
The tone detector consists of a detection section, an ON guard timer, and an OFF guard timer. The default of the detection frequency is 2100 Hz, the default of the detection threshold is –5.3 dBm0, the default of the ON guard timer is 5 ms, and that of the OFF guard timer is 5 ms. The detection frequency, detection threshold, and ON guard and OFF guard times can be changed through internal data memory access.

B0: Channel 1 tone detector ON/OFF control
0: OFF 1: ON
Channel 1 tone detector ON/OFF selection bit. When this bit is set to "1", the detector is set to ON and CR4-B1 and B0 (TTDET1 and RTDET1) is enabled to shows the tone detection results.
The tone detector consists of a detection section, an ON guard timer, and an OFF guard timer. The default of the detection frequency is 2100 Hz, the default of the detection threshold is –5.3 dBm0, the default of the ON guard timer is 5 ms, and that of the OFF guard timer is 5 ms. The detection frequency, detection threshold, and ON guard and OFF guard times can be changed through internal data memory access.

(22) CR21 (Channel 1 VOX function control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR21	VOX_ON 1	VOX_ON _LVL11	VOX_ON _LVL01	VOX_OFF _TIME1	—	VOX_IN1	RX_NOISE _LVL11	RX_NOISE _LVL01
Initial value	0	0	0	0	0	0	0	0

B7: Channel 1 VOX function ON/OFF control
0: OFF 1: ON
Channel 1 VOX function ON/OFF selection bit. By setting this bit to "1", on the transmit side, the voice/silence detection is enabled; on the receive side, background noise generation as per an input into the VOXI1 pin is enabled. When this bit is set to "0", the settings of the CR21-B6 to B4, B2 to B0 become invalid and the CR5-B1 to B0 stays "0".

B6–B5: Voice/silence detection threshold setting on the Channel 1 transmit side
Bits for setting the voice/silence detection threshold on the channel 1 transmit side

Table 18 Channel 1 Transmit Side Voice/Silence Detection Threshold Setting

VOX_ON_LVL11	VOX_ON_LVL01	Threshold
0	0	–20 dBm0
0	1	–25 dBm0
1	0	–30 dBm0
1	1	–35 dBm0

Note: For the detection threshold, a pad from –1 dB to –5 dB can be inserted for the values indicated above.
The value of the adjusting pad can be changed in initial mode only. See the INTERNAL DATA MEMORY ACCESS METHOD and Table 26 Internal data memory related control registers for the way to change the internal data memory setting.

B4: Channel 1 hang-over time (see Figure 4) setting
0: 160 ms 1: 320 ms
Channel 1 hang-over time selection bit. By controlling this bit, a silence detection guard time from voice to silence can be set.

B3: Reserved bit

B2: VOX input signal setting on the Channel 1 receive side
0: Internal background noise transmit 1: Voice receive signal transmit
VOX input signal setting bit on the Channel 1 transmit side. When this bit is set to "1", receive side speech signals are fed to the RinL1. When this bit is set to "0", the background noise generator's output is fed to the RinL1 instead of the receive side speech signals. When using this bit, set the VOXI1 pin to "0".
When the application has a means to detect silence with the receive side speech signals, this function could be made use of as comfort noise generator.

B1–B0: Channel 1 external setting background noise level

Table 19 Channel 1 Receive Side Background Noise Level Setting

RX_NOISE_LVL11	RX_NOISE_LVL01	Level
0	0	No noise
0	1	–55 dBm0
1	0	–45 dBm0
1	1	–35 dBm0

(23) CR22 (Channel 2 VOX function control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR22	VOX_ON 2	VOX_ON _LVL12	VOX_ON _LVL02	VOX_OFF _TIME2	—	VOX_IN2	RX_NOISE _LVL12	RX_NOISE _LVL02
Initial value	0	0	0	0	0	0	0	0

B7: Channel 2 VOX function ON/OFF control
0: OFF 1: ON
Channel 2 VOX function ON/OFF selection bit. By setting this bit to "1", on the transmit side, the voice/silence detection is enabled; on the receive side, background noise generation as per an input into the VOXI2 pin is enabled. When this bit is set to "0", the settings of the CR22-B6 to B4, B2 to B0 become invalid and the CR5-B5 to B4 stays "0".

B6–B5: Voice/silence detection threshold setting on the Channel 2 transmit side
Bits for setting the voice/silence detection threshold on the channel 2 transmit side

Table 20 Channel 2 Transmit Side Voice/Silence Detection Threshold Setting

VOX_ON_LVL12	VOX_ON_LVL02	Threshold
0	0	–20 dBm0
0	1	–25 dBm0
1	0	–30 dBm0
1	1	–35 dBm0

Note: For the detection threshold, a pad from –1 dB to –5 dB can be inserted for the value indicated above.
The value of the adjusting pad can be changed in initial mode only. See the INTERNAL DATA MEMORY ACCESS METHOD and Table 26 Internal data memory related control registers for the way to change the internal data memory setting.

B4: Channel 2 hang-over time (see Figure 4) setting
0: 160 ms 1: 320 ms
Channel 2 hang-over time selection bit. By controlling this bit, a silence detection guard time from voice to silence can be set.

B3: Reserved bit

B2: VOX input signal setting on the Channel 2 receive side
0: Internal background noise transmit 1: Voice receive signal transmit
VOX input signal setting bit on the Channel 2 transmit side. When this bit is set to "1", receive side speech signals are fed to the RinL2. When this bit is set to "0", the background noise generator's output is fed to the RinL2 instead of the receive side speech signals. When using this bit, set the VOXI2 pin to "0".
When the application has a means to detect silence with the receive side speech signals, this function could be made use of as comfort noise generator.

B1–B0: Channel 2 external setting background noise level

Table 21 Channel 2 Receive Side Background Noise Level Setting

RX_NOISE_LVL12	RX_NOISE_LVL02	Level
0	0	No noise
0	1	–55 dBm0
1	0	–45 dBm0
1	1	–35 dBm0

(24) CR23 (reserved register)

	B7	B6	B5	B4	B3	B2	B1	B0
CR23	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

B7–B0: Reserved bits

(25) CR24 (reserved register)

	B7	B6	B5	B4	B3	B2	B1	B0
CR24	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

B7–B0: Reserved bits

(26) CR25 (Channel 1 line echo canceler I/O level control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR25	—	—	—	—	LPADL11	LPADL01	GPADL11	GPADL01
Initial value	0	0	0	0	0	0	0	0

B7–B4: Reserved bits

B3–B2: Line side input level control
Bits for setting the level of PAD (LPADL1) for line echo canceler input SinL1 loss

Table 22 Channel 1 Loss PAD Level Setting

LPADL11	LPADL01	Level
0	0	0 dB
0	1	–6 dB
1	0	–12 dB
1	1	–18 dB

B1–B0: Line side output level control
Bits for setting the level of PAD (GPADL1) for line echo canceler output SoutL1 gain

Table 23 Channel 1 Gain PAD Level Setting

GPADL11	GPADL01	Level
0	0	0 dB
0	1	+6 dB
1	0	+12 dB
1	1	+18 dB

(27) CR26 (Channel 2 line echo canceler I/O level control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR26	—	—	—	—	LPADL12	LPADL02	GPADL12	GPADL02
Initial value	0	0	0	0	0	0	0	0

B7–B4: Reserved bit

B3–B2: Line side input level control
Bits for setting the level of PAD (LPADL2) for line echo canceler input SinL2 loss

Table 24 Channel 2 Loss PAD Level Setting

LPADL12	LPADL02	Level
0	0	0 dB
0	1	–6 dB
1	0	–12 dB
1	1	–18 dB

B1–B0: Line side output level control
Bits for setting the level of PAD (GPADL2) for line echo canceler output SoutL2 gain

Table 25 Channel 2 Gain PAD Level Setting

GPADL12	GPADL02	Level
0	0	0 dB
0	1	+6 dB
1	0	+12 dB
1	1	+18 dB

(28) CR27 (Channel 1 line echo canceler operation mode)

	B7	B6	B5	B4	B3	B2	B1	B0
CR27	LTHR1	LAFF_RST1	LHLD1	LHD1	LCLP1	—	LATT1	LGC1
Initial value	0	0	0	0	0	0	0	0

B7: Through mode control
0: Normal mode (echo cancellation operation) 1: Through mode
When this bit is set to "0", an echo canceler works. When this bit is set to "1", data of RinL1 and SinL1 are output to RouteL1 and SoutL1 respectively as they are without echo cancellation. The echo canceler coefficients are kept frozen during through mode and not reset.

B6: FIR filter (LAFF) coefficients reset control
0: Normal operation 1: Rest of coefficients
A bit to reset the adaptive FIR filter (LAFF) coefficients of the line echo canceler.

B5: Coefficients updating control
0: Normal mode (updates coefficients) 1: Freezes coefficients
When this bit is set to "0", the adaptive FIR filter (LAFF) keeps updating its own coefficients adaptively as per a state of the echo path between echo-originating signals at the RoutL1 and returning echo signals at the SinL1, which is normal operation with an echo canceler. When this bit is set to "1", the adaptive FIR filter (LAFF) freezes its own coefficients and keeps echo cancellation operation with the frozen coefficients. Hence, note that echo cancellation is not done if this bit is set to "1" from the beginning since the initial values of coefficients are all zero. This function is enabled when LTHR1 is in normal mode.

B4: Howling director control
0: OFF 1: ON
This function detects and tries to suppress howling. This function is enabled when LTHR1 is in normal mode.

B3: Center clip control
0: OFF 1: ON
When the ATTsL1 output of the line echo canceler is –57 dBm0 or less, the center clip function forcibly makes it mute by transforming the PCM codes to the minimum positive value (FFh in μ-law; B5h in A-law). This function is enabled when LTHR1 is in normal mode.

B2: Reserved bit

B1: Attenuator control
0: ON 1: OFF
This bit is used to select ON/OFF of the ATT function that complements echo attenuation which is by the adaptive FIR filter and prevents howling with the attenuators (ATTsL1 and ATTrL1) that are provided for RinL1 input and SoutL1 output of the line echo canceler. When signals are input to RinL1 only, an ATTofSoutL1 (ATTsL1) is inserted. When signals are input to SinL1 only or both SinL1 and RinL1, an ATT of RinL1 input (ATTrL1) is inserted. Each ATT value is about 6 dB. This function is enabled when LTHR1 is in normal mode.

B0: Gain controller control
0: OFF 1: ON
This bit is used to select ON/OFF of the gain control function that controls the RinL1 input level and prevents howling and an excessive input to RinL1 which may bring decrease in echo attenuation through the gain controller that is provided for RinL1 input of the line echo canceler. This function becomes effective from about –24 dBm0 as the RinL1 level and the RinL1 level is controlled within the range of 0 to –8.5 dB. This function is enabled when LTHR1 is in normal mode.

(29) CR28 (Channel 2 line echo canceler operation mode)

	B7	B6	B5	B4	B3	B2	B1	B0
CR28	LTHR2	LAFF_RST2	LHLD2	LHD2	LCLP2	—	LATT2	LGC2
Initial value	0	0	0	0	0	0	0	0

B7: Through mode control
0: Normal mode (echo cancellation operation) 1: Through mode
When this bit is set to "0", an echo canceler works. When this bit is set to "1", data of RinL2 and SinL2 are output to RouteL2 and SoutL2 respectively as they are without echo cancellation. The echo canceler coefficients are kept frozen during through mode and not reset.

B6: FIR filter (LAFF) coefficients reset control
0: Normal operation 1: Rest of coefficients
A bit to reset the adaptive FIR filter (LAFF) coefficients of the line echo canceler.

B5: Coefficients updating control
0: Normal mode (coefficients updating) 1: Fixed coefficients
When this bit is set to "0", the adaptive FIR filter (LAFF) keeps updating its own coefficients adaptively as per a state of the echo path between echo-originating signals at the RoutL2 and returning echo signals at the SinL2, which is normal operation with an echo canceler. When this bit is set to "1", the adaptive FIR filter (LAFF) freezes its own coefficients and keeps echo cancellation operation with the frozen coefficients. Hence, note that echo cancellation is not done if this bit is set to "1" from the beginning since the initial values of coefficients are all zero This function is enabled when LTHR2 is in normal mode.

B4: Howling director control
0: OFF 1: ON
This function detects and tries to suppress howling. This function is enabled when LTHR2 is in normal mode.

B3: Center clip control
0: OFF 1: ON
When the ATTsL2 output of the line echo canceler is –57 dBm0 or less, the center clip function forcibly makes it mute by transforming the PCM codes to the minimum positive value (FFh in μ-law; B5h in A-law). This function is enabled when LTHR2 is in normal mode.

B2: Reserved bit

B1: Attenuator control
0: ON 1: OFF
This bit is used to select ON/OFF of the ATT function that complements echo attenuation which is by the adaptive FIR filter and prevents howling with the attenuators (ATTsL2 and ATTrL2) that are provided for RinL2 input and SoutL2 output of the line echo canceler. When signals are input to RinL2 only, an ATT of SoutL2 (ATTsL2) is inserted. When signals are input to SinL2 only or both SinL2 and RinL2, an ATT of RinL2 input (ATTrL2) is inserted. Each ATT value is about 6 dB. This function is enabled when LTHR2 is in normal mode.

B0: Gain controller control
0: OFF 1: ON
This bit is used to select ON/OFF of the gain control function that controls the RinL2 input level and prevents howling through the gain controller that is provided for RinL2 input of the line echo canceler. This function becomes effective from about –24 dBm0 as the RinL2 level and the RinL2 level is controlled within the range of 0 to –8.5 dB. This function is enabled when LTHR2 is in normal mode.

(30) CR29 (reserved register)

	B7	B6	B5	B4	B3	B2	B1	B0
CR29	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

B7–B0: Reserved bit

(31) CR30 (reserved register)

	B7	B6	B5	B4	B3	B2	B1	B0
CR30	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

B7–B0: Reserved bit

(32) CR31 (reserved register)

	B7	B6	B5	B4	B3	B2	B1	B0
CR31	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

B7–B0: Reserved bit

MICROCONTROLLER CONTROL METHOD

The following flowchart shows the microcontroller control method by the parallel microcontroller interface.

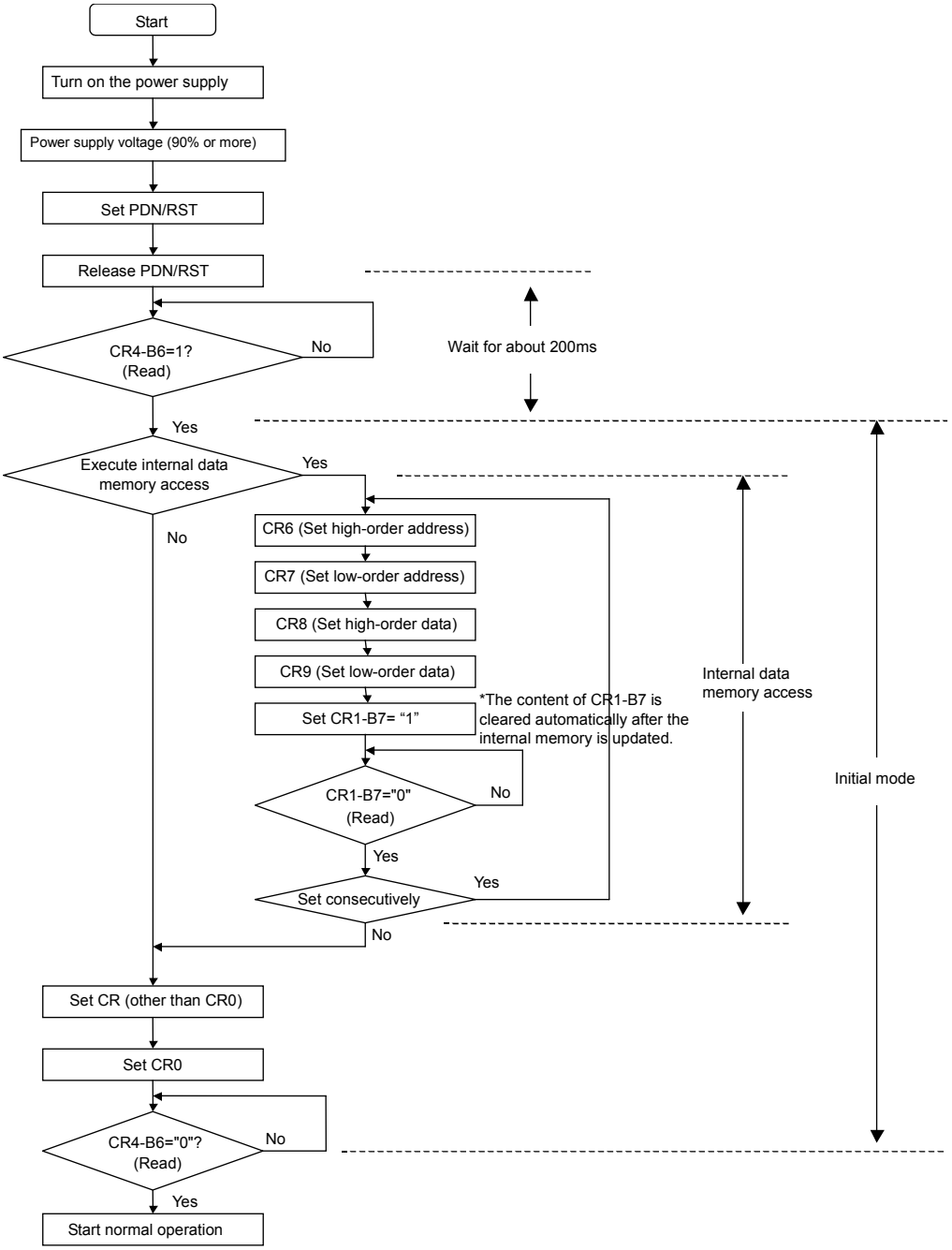


Figure 8 Flowchart of microcontroller control

INTERNAL DATA MEMORY ACCESS METHOD

Write method

The 8-bit registers (CR6–CR9) that were mapped in the control registers are assigned as follows.

16-bit address of the internal data memory (A15–A0)

16-bit write data (D15–D0)

The initial mode is entered about 200 ms after release of power-down reset by the $\overline{PDN}/\overline{RST}$ pin or the SPDN bit (CR0-B7) and the READY bit (CR4-B6) is set to "1". In this write enabled state and after the internal memory address and write data are set in CR6 to CR9, the internal data memory write operation for one word is completed by setting DMWR (CR1-B7) to "1". After completion of write operation, DMWR (CR1-B7) is cleared to "0" automatically. Figure 9 shows the internal data memory setting method.

When rewriting multiple memories, repeat the write operation indicated above. Operation starts when OPE_STAT (CR0-B0) is set to "1" after termination of all the write operations.

Internal data memory can be rewritten in a mode other than the initial mode. In that case, use the same method as above for changing the contents of the internal data memory. Tables 26 to 28 list internal data memory related registers.

Note: When data is set in the internal data memory during operation, data is read in the LSI internal section synchronized with the SYNC signal (8k Hz). Therefore, retain the state for 250□s or more.

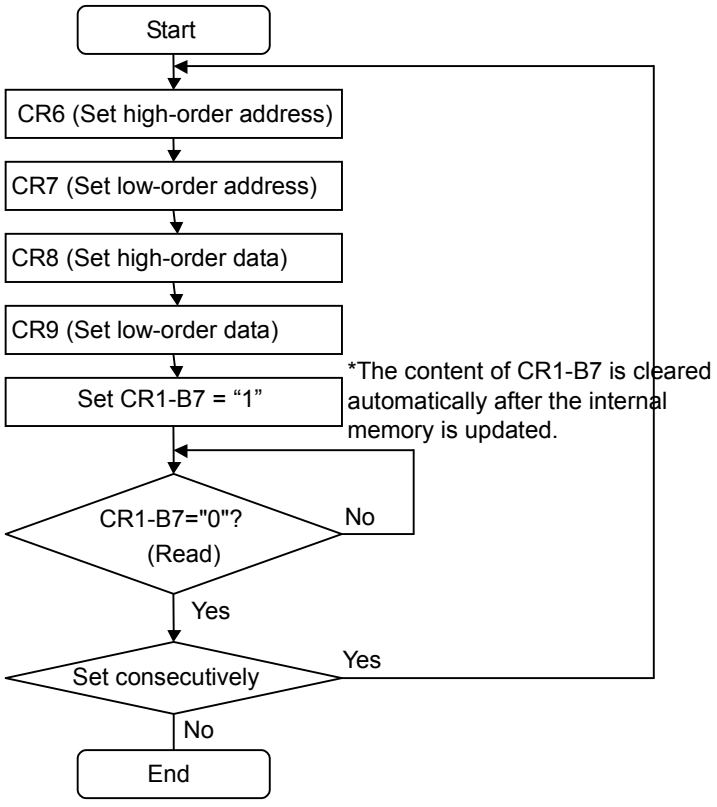


Figure 9 Internal data memory access flowchart (write)

Internal data memory related registers

Table 26 Internal data memory related control registers (page 1 of 3)

Function	Internal data memory name	Address	Initial value		Change enable mode		
			Data	Data value	In initial mode	When stopped	In operation
TONE_GEN1	Single tone frequency (TGEN_FREQ_T0_1 / CR17:B4-B0=00000)	0000h	0E14h	440 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T1_1 / CR17:B4-B0=00001)	0001h	0EE9h	466 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T2_1 / CR17:B4-B0=00010)	0002h	0FCFh	494 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T3_1 / CR17:B4-B0=00011)	0003h	10BCh	523 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T4_1 / CR17:B4-B0=00100)	0004h	11BAh	554 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T5_1 / CR17:B4-B0=00101)	0005h	12C9h	587 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T6_1 / CR17:B4-B0=00110)	0006h	13E7h	622 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T7_1 / CR17:B4-B0=00111)	0007h	1517h	659 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T8_1 / CR17:B4-B0=01000)	0008h	1656h	698 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T9_1 / CR17:B4-B0=01001)	0009h	17AEh	740 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T10_1 / CR17:B4-B0=01010)	000Ah	1917h	784 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T11_1 / CR17:B4-B0=01011)	000Bh	1A98h	831 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T12_1 / CR17:B4-B0=01100)	000Ch	1C29h	880 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T13_1 / CR17:B4-B0=01101)	000Dh	1DD3h	932 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T14_1 / CR17:B4-B0=01110)	000Eh	1F9Eh	988 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T15_1 / CR17:B4-B0=01111)	000Fh	2181h	1047 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T16_1 / CR17:B4-B0=10000)	0010h	237Dh	1109 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T17_1 / CR17:B4-B0=10001)	0011h	259Ah	1175 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T18_1 / CR17:B4-B0=10010)	0012h	27D7h	1245 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T19_1 / CR17:B4-B0=10011)	0013h	2A35h	1319 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T20_1 / CR17:B4-B0=10100)	0014h	2CB4h	1397 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T21_1 / CR17:B4-B0=10101)	0015h	2F5Ch	1480 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T22_1 / CR17:B4-B0=10110)	0016h	322Dh	1568 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T23_1 / CR17:B4-B0=10111)	0017h	3527h	1661 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T24_1 / CR17:B4-B0=11000)	0018h	3852h	1760 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T25_1 / CR17:B4-B0=11001)	0019h	0CCDh	400 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T26_1 / CR17:B4-B0=11010)	001Ah	2000h	1000 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T27_1 / CR17:B4-B0=11011)	001Bh	4000h	2000 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T28_1 / CR17:B4-B0=11100)	001Ch	5558h	2667 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T29_1 / CR17:B4-B0=11101)	001Dh	299Ah	1300 Hz	yes	no	no

Table 27 Internal data memory related control registers (page 2 of 3)

Function	Internal data memory name	Address	Initial value		Change enable mode		
			Data	Data value	In initial mode	When stopped	In operation
TONE_GEN1	Single tone frequency (TGEN_FREQ_T30_1 / CR17:B4-B0=11110)	001Eh	428Fh	2080 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T31_1 / CR17:B4-B0=11111)	001Fh	6000h	3000 Hz	yes	no	no
	Tone output gain (TGEN_GAIN_H1)	0020h	0100h	0 dB	yes	yes	no
	Tone output gain (TGEN_GAIN_L1)	0021h	0100h	0 dB	yes	yes	no
	Fade control (TGEN_FADE_CONT1)	0022h	0000h	Stop	yes	yes	no
	Fade In step (TGEN_FADE_IN_ST1)	0023h	4C10h	+1.5 dB	yes	yes	no
	Fade Out step (TGEN_FADE_OUT_ST1)	0024h	35D9h	–1.5 dB	yes	yes	no
	Tone Fade Out time (TGEN_FADE_OUT_TIM1)	0025h	0021h	33Sync	yes	yes	no
TONE_GEN2	Single tone frequency (TGEN_FREQ_T0_2 / CR19:B4-B0=00000)	0030h	0E14h	440 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T1_2 / CR19:B4-B0=00001)	0031h	0EE9h	466 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T2_2 / CR19:B4-B0=00010)	0032h	0FCFh	494 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T3_2 / CR19:B4-B0=00011)	0033h	10BCh	523 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T4_2 / CR19:B4-B0=00100)	0034h	11BAh	554 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T5_2 / CR19:B4-B0=00101)	0035h	12C9h	587 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T6_2 / CR19:B4-B0=00110)	0036h	13E7h	622 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T7_2 / CR19:B4-B0=00111)	0037h	1517h	659 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T8_2 / CR19:B4-B0=01000)	0038h	1656h	698 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T9_2 / CR19:B4-B0=01001)	0039h	17AEh	740 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T10_2 / CR19:B4-B0=01010)	003Ah	1917h	784 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T11_2 / CR19:B4-B0=01011)	003Bh	1A98h	831 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T12_2 / CR19:B4-B0=01100)	003Ch	1C29h	880 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T13_2 / CR19:B4-B0=01101)	003Dh	1DD3h	932 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T14_2 / CR19:B4-B0=01110)	003Eh	1F9Eh	988 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T15_2 / CR19:B4-B0=01111)	003Fh	2181h	1047 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T16_2 / CR19:B4-B0=10000)	0040h	237Dh	1109 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T17_2 / CR19:B4-B0=10001)	0041h	259Ah	1175 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T18_2 / CR19:B4-B0=10010)	0042h	27D7h	1245 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T19_2 / CR19:B4-B0=10011)	0043h	2A35h	1319 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T20_2 / CR19:B4-B0=10100)	0044h	2CB4h	1397 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T21_2 / CR19:B4-B0=10101)	0045h	2F5Ch	1480 Hz	yes	no	no

Table 28 Internal data memory related control registers (page 3 of 3)

Function	Internal data memory name	Address	Initial value		Change enable mode		
			Data	Data value	In initial mode	When stopped	In operation
TONE_GEN2	Single tone frequency (TGEN_FREQ_T22_2 / CR19:B4-B0=10110)	0046h	322Dh	1568 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T23_2 / CR19:B4-B0=10111)	0047h	3527h	1661 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T24_2 / CR19:B4-B0=11000)	0048h	3852h	1760 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T25_2 / CR19:B4-B0=11001)	0049h	0CCDh	400 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T26_2 / CR19:B4-B0=11010)	004Ah	2000h	1000 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T27_2 / CR19:B4-B0=11011)	004Bh	4000h	2000 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T28_2 / CR19:B4-B0=11100)	004Ch	5558h	2667 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T29_2 / CR19:B4-B0=11101)	004Dh	299Ah	1300 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T30_2 / CR19:B4-B0=11110)	004Eh	428Fh	2080 Hz	yes	no	no
	Single tone frequency (TGEN_FREQ_T31_2 / CR19:B4-B0=11111)	004Fh	6000h	3000 Hz	yes	no	no
	Tone output gain (TGEN_GAIN_H2)	0050h	0100h	0 dB	yes	yes	no
	Tone output gain (TGEN_GAIN_L2)	0051h	0100h	0 dB	yes	yes	no
	Fade control (TGEN_FADE_CONT2)	0052h	0000h	Stop	yes	yes	no
	Fade In step (TGEN_FADE_IN_ST2)	0053h	4C10h	+1.5 dB	yes	yes	no
	Fade Out step (TGEN_FADE_OUT_ST2)	0054h	35D9h	–1.5 dB	yes	yes	no
	Tone Fade Out time (TGEN_FADE_OUT_TIM2)	0055h	0021h	33Sync	yes	yes	no
TDET1	Tone detection threshold (main signal) (TDET_S_TH1)	0084h	1EBBh	–5.3 dBm0	yes	yes	no
	Tone detection threshold (noise) (TDET_N_TH1)	0099h	1EBBh	–5.3 dBm0	yes	yes	no
	ON guard timer (TDET_ON_TIM1)	009Ah	0028h	5 ms	yes	yes	no
	OFF guard timer (TDET_OFF_TIM1)	009Bh	0028h	5 ms	yes	yes	no
	Detection frequency (TDET_FREQ1)	----h	—	2100 Hz	yes	×	no
TDET2	Tone detection threshold (main signal) (TDET_S_TH2)	00B4h	1EBBh	–5.3 dBm0	yes	yes	no
	Tone detection threshold (noise) (TDET_N_TH2)	00C9h	1EBBh	–5.3 dBm0	yes	yes	no
	ON guard timer (TDET_ON_TIM2)	00CAh	0028h	5 ms	yes	yes	no
	OFF guard timer (TDET_OFF_TIM2)	00CBh	0028h	5 ms	yes	yes	no
	Detection frequency (TDET_FREQ2)	----h	—	2100 Hz	yes	no	no
VOX1	Voice/silence detection threshold adjusting pad (VOX_LPAD1)	0061h	4000h	0 dB	yes	no	no
VOX2	Voice/silence detection threshold adjusting pad (VOX_LPAD2)	0069h	4000h	0 dB	yes	no	no

Tone generator function

A. Single tone frequency internal data memory
<TGEN_FREQ_T0_1 to TGEN_FREQ_T31_1> Address: 0000h to 001Fh
<TGEN_FREQ_T0_2to TGEN_FREQ_T31_2> Address: 0030h to 004Fh
Use the following expression when changing the tone frequency.
Calculation expression: A × 8.192 (where A is the desired frequency after change)
<Example> When the desired frequency is 2100 Hz:
2100 × 8.192 = 17203.2 = 17203d = 4333h (Round off to the nearest whole number)
Upper limit value: 3000 Hz (Data: 6000h)
Lower limit value: 300 Hz (Data: 099Ah)

B. Internal data memory for tone output gain control
<TGEN_GAIN_H1> Address: 0020h, Initial value: 0100h (0 dB)
<TGEN_GAIN_L1> Address: 0021h, Initial value: 0100h (0 dB)
<TGEN_GAIN_H2> Address: 0050h, Initial value: 0100h (0 dB)
<TGEN_GAIN_L2> Address: 0051h, Initial value: 0100h (0 dB)
The default of the output gain is 0 dB. Use the following expression to change the output gain (X).
Calculation expression: 10^(X/20) × 256
<Example> Setting the gain to –6 dB
10^(–6/20) × 256 = 128.3d = 128d = 0080h (Round off to the nearest whole number)
Upper limit value: +12 dB (Data: 03FBh)
Lower limit value: –12 dB (Data: 0040h)
Note: If the setting has been so made that TGEN_GAIN_H1, TGEN_GAIN_L1, TGEN_GAIN_H2, or TGEN_GAIN_L2 individually or the result of adding them exceeds +3 dBm0, the tone will be saturated regardless of the setting of ATTtgtxt1, ATTtgrx1, ATTtgtx2, and ATTgrx2 of the succeeding stage, and as a result, the related AC characteristics specified in this specification are not satisified.

C. Internal data memory for tone fade control
<TGEN_FADE_CONT1> Address: 0022h, Initial value: 0000h (Stop)
<TGEN_FADE_CONT2> Address: 0052h, Initial value: 0000h (Stop)
Setting “0001h” in this data memory enables the Fade In/Fade Out function of tone fade control.
0000h: Disable Fade In/Fade Out
0001h: Enable Fade In/Fade Out
Note: When using this control, set a correct Fade Out time.

D. Fade In step
<TGEN_FADE_IN_ST1> Address: 0023h, Initial value: 4C10h (+1.5 dB)
<TGEN_FADE_IN_ST2> Address: 0053h, Initial value: 4C10h (+1.5 dB)
Use the following expressing to change step amount X.
Calculation expression: 10^(X/20) × 16384
<Example> Setting the step value to +1.5 dB
10^(1.5/20) × 16384=19472.42=19472d=4C10h (Round off to the nearest whole number)
Maximum step value: Approx. +6.0 dB (Data: 7FFFh)
Minimum step value: Approx. +0.1 dB (Data: 40BEh)

E. Fade Out step
<TGEN_FADE_OUT_ST1> Address: 0024h, Initial value: 35D9h (–1.5 dB)
<TGEN_FADE_OUT_ST2> Address: 0054h, Initial value: 35D9h (–1.5 dB)
Use the following expression to change step amount X.
Calculation expression: 10^(X/20) × 16384
<Example> Setting the step value to –1.5 dB
10^(–1.5/20) × 16384 = 13785.41 = 13785d = 35D9h (Round off to the nearest whole number)
Maximum step value: Approx. –6.0 dB (Data: 2000h)
Minimum step value: Approx. –0.1 dB (Data: 3F44h)

F. Internal data memory for tone Fade Out time control
<TGEN_FADE_OUT_TIM1> Address: 0025h, Initial value: 002Bh (33Sync)
<TGEN_FADE_OUT_TIM2> Address: 0055h, Initial value: 002Bh (33Sync)
Use the following expression to change the fade out time.
Calculation expression: 48.2 dB/ "Fade Out step value" dB
<Example> When the step value is 1.5 dB:
48.2/1.5 = 32.13 = 33d = 0021h (Round up to the nearest whole number)
Upper limit value: 482 Sync (Data: 01E2h)
Lower limit: 9 Sync (Data: 0009h)

Tone detection function

A. Internal data memory for detection threshold (main signal) control
<TDET_S_TH1> Address: 0084h, Initial value: 1EBBh (–5.3 dBm0)
<TDET_S_TH2> Address: 00B4h, Initial value: 1EBBh (–5.3 dBm0)
Use the following expression to change the value when using X as the main signal detection threshold.
Calculation expression: 10^((X – 3.17)/20) × 2/PI × 32768
<Example> When detection threshold = –5.3 dBm0
10^((–5.3 – 3.17)/20) × 2/PI × 32768 = 7867.37d = 1EBBh (Round off to the nearest whole number)
Upper limit value: –5.3 dBm0 (Data: 1EBBh)
Lower limit value: –30 dBm0 (Data: 01CAh)

B. Internal data memory for detection threshold (noise) control
<TDET_N_TH1> Address: 0099h, Initial value: 1EBBh (–5.3 dBm0)
<TDET_N_TH2> Address: 00C9h, Initial value: 1EBBh (–5.3 dBm0)
Use the following expression to change the value when using X as the main signal detection threshold.
Calculation expression: 10^((X–3.17)/20) × 2/PI × 32768
<Example> When detection threshold = –5.3 dBm0
10^((–5.3 – 3.17)/20) × 2/PI × 32768 = 7867.37d = 1EBBh (Round off to the nearest whole number)
Upper limit value: –5.3 dBm0 (Data: 1EBBh)
Lower limit value: –30 dBm0 (Data: 01CAh)
To stop the noise detection function, write 7FFFh in the internal data memory (TDET_N_TH1/TDET_N_TH2) that is indicated above.

C. Internal data memory for ON guard timer
<TDET_ON_TIM1> Address: 009Ah, Initial value: 0028h (5 ms)
<TDET_ON_TIM2> Address: 00CAh, Initial value: 0028h (5 ms)
Use the following expression to change the timer value.
Calculation expression: Guard timer value (ms)/0.125(ms)
<Example> ON guard timer = 5 ms
5/0.125 = 40d = 0028h
Upper limit value: 4095.875 ms (Data: 7FFFh)
Lower limit value: 0.125 ms (Data: 0001h)

D. Internal data memory for OFF guard timer
<TDET_OFF_TIM1> Address: 009Bh, Initial value: 0028h (5 ms)
<TDET_OFF_TIM2> Address: 00CBh, Initial value: 0028h (5 ms)
Use the following expression to change the timer value.
Calculation expression: Guard timer value (ms)/0.125(ms)
<Example> ON guard timer = 5 ms
5/0.125 = 40d = 0028h
Upper limit value: 4095.875 ms (Data: 7FFFh)
Lower limit value: 0.125 ms (Data: 0001h)

E. Internal data memory for detection frequency control
<TDET_FREQ1> Address:----h, Initial value:—
<TDET_FREQ2> Address:----h, Initial value:—
This function is used for changing a detection frequency. Contact ROHM's responsible sales person when changing the detection frequency.

VOX function

A. Voice/silence detection threshold adjusting pad (for loss)
<VOX_LPAD1> Address: 0061h, Initial value: 4000h (0 dB)
<VOX_LPAD2> Address: 0069h, Initial value: 4000h (0 dB)
Use the following expression to change the voice/silence detection threshold adjusting value
Calculation expression: 10^(–X/20) × 16384
<Example> Setting the voice/silence detection threshold adjusting value to –1 dB
10^(–(–1.0)/20) × 16384 = 18383.15 = 18383d = 47CFh (Round off to the nearest whole number)
Upper limit value: –1.0 dB (Data: 47CFh)
Lower limit value: –5.0 dB (Data: 71CFh)

DATA COMMUNICATION

Set the following parameters for data communication.

1.
4-bit (32 kbps) data communication
DTHR1 (CR2-B5) = "1" :Channel 1
DTHR2 (CR3-B5) = "1" :Channel 2

2.
8-bit (64 kbps) data communication
CONTA1 (CR2-B7) = "1", LTHR1 (CR27-B7) = "1" :Channel 1
CONTA2 (CR3-B7) = "1", LTHR2 (CR28-B7) = "1" :Channel 2

Notes:
1. At the start and switching of data/voice communication, a data loss/data errors of several SYNC cycles occur.
2. In data through of LTHR1/2 only, PCM data "–0" is changed to "+0" when it is output.
3. DTHR1 = "1", DTHR2 = "1", CONTA1 = "1"+LTHR1 = "1", and CONTA2 = "1"+LTHR2 = "1" are set, the line echo canceler, tone generator, tone detection, VOX function, and MUTE function are disabled.

Table 29 Full scale table (μ-law, A-law)

Input level	μ̃-law								A-law							
	MSB								MSB							
+ Full scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
+0	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
–0	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
– Full scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

NOTES ON USE

1. To prevent operation errors and deterioration of the characteristics of the LSI, use a stable power supply of low noise (in particular high-frequency spark noise or pulse noise).

2. To guarantee the electrical characteristics, use a power supply byass capacitor with better high frequency characteristics and install it in the proximity of the LSI pins.

3. To guarantee the electrical characteristics, use an analog signal ground (SG pin) bypass capacitor with better high frequency characteristics and install it in the proximity of the LSI pins.

4. To guarantee the electrical characteristics, use a bypass capacitor with a better high frequency characteristics for regulator reference voltage output (VBG pin) and regulator output (VOUT1 and VOUT2 pins), and install it in the proximity of the LSI pins.

5. Connect the AGND, DGND1, and DGND2 pins with the system ground as close as possible under low impedance.

6. Turn on the analog power supply and digital power supply simulatneously or digital power supply prior to analog power supply.

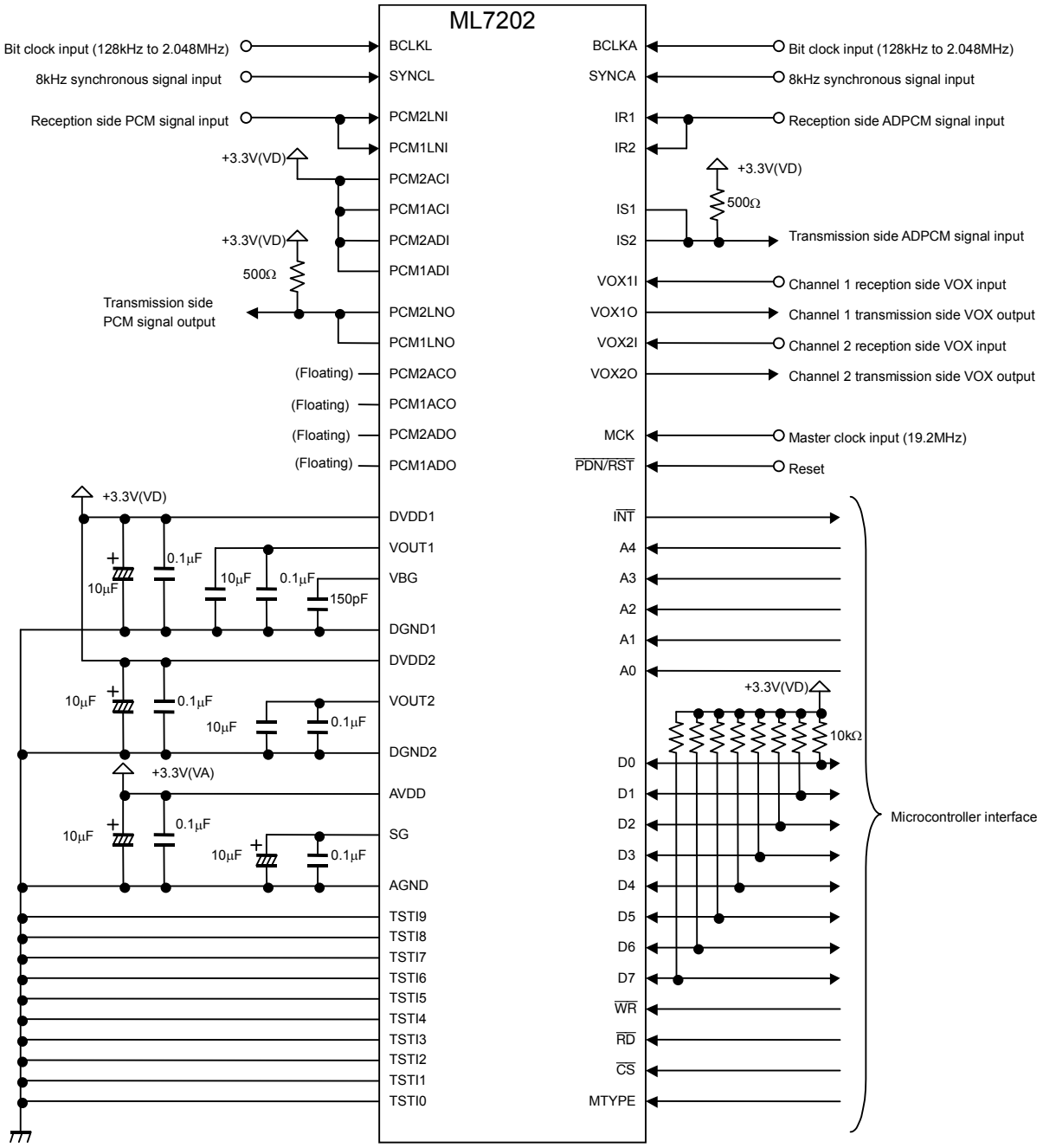
7. After turning on the power supply, execute Reset using the $\overline{\text{PDN/RST}}$ pin immediately, with the master clock being input without fail. (For instance, when this LSI is maintained in a power-down state while the device waits for originating call or terminating call, first execute the Reset described above and then wait for the originating call or terminating call.)

8. PCM output pins and ADPCM output pins require an external pull-up resistor since they are open drain pins.

9. Make the setting of the E.R.L (Echo Return Loss) so that it will be attenuated. If the E.R.L is to be amplified, it is recommended to use the function of the loss PAD and gain PAD that are provided in the I/O section of the line echo canceler.
   E.R.L refers to attenuation of echo amount from an echo canceler output (RoutL1/RoutL2) to an echo canceler input (SinL1/SinL2).

10. The recommended input level to the line echo canceler is –10 to –20 dBm0.

APPLICATION CIRCUIT



Setting conditions

- IOSEL setting: CR0-B3 = "0"
- When PCM time slot is assigned (setup control registers: CR11 and CR12)
- When ADPCM time slot is assigned (setup control registers: CR13 and CR14)

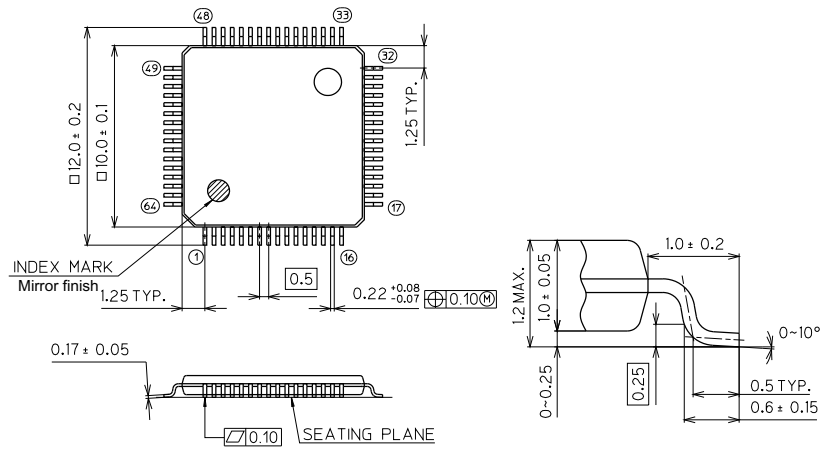
Note

- The bit clock frequency varies according to the PCM-ADPCM time slot assignment conditions.

PACKAGE DIMENSIONS

(Unit: mm)

TQFP64-P-1010-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.26 TYP.
Rev. No./Last Revised	4/Oct. 28, 1996

LAPIS Semiconductor Co.,Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7202-001-01	Sep. 08 2004	–	65	Final edition 1

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