#### **Product specification**

# FDN8601





## 100 V, 2.7 A, 109 m $\Omega$

### Features

- Max r<sub>DS(on)</sub> = 109 mΩ at V<sub>GS</sub> = 10 V, I<sub>D</sub> = 1.5 A
- Max  $r_{DS(on)}$  = 175 m $\Omega$  at V<sub>GS</sub> = 6 V, I<sub>D</sub> = 1.2 A
- High performance trench technology for extremely low r<sub>DS(on)</sub>
- High power and current handling capability in a widely used surface mount package
- Fast switching speed
- 100% UIL tested
- RoHS Compliant

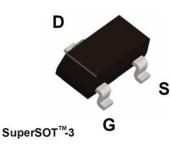


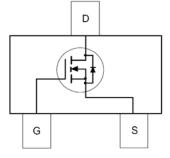
## **General Description**

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench<sup>®</sup> process that has been optimized for  $r_{DS(on)}$ , switching performance and ruggedness.

## Applications

- Primary DC-DC Switch
- Load Switch





#### MOSFET Maximum Ratings TA = 25 °C unless otherwise noted

Symbol	Parameter		Ratings	Units	
V <sub>DS</sub>	Drain to Source Voltage		100	V	
V <sub>GS</sub>	Gate to Source Voltage		±20	V	
1	-Continuous	(Note 1a)	2.7	•	
D	-Pulsed		12	— A	
E <sub>AS</sub>	Single Pulse Avalanche Energy	(Note 3)	13	mJ	
D	Power Dissipation	(Note 1a)	1.5	W	
P <sub>D</sub>	Power Dissipation	(Note 1b)	0.6	vv	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range		-55 to +150	°C	

#### **Thermal Characteristics**

$R_{ ext{ heta}JC}$	Thermal Resistance, Junction to Case	(Note 1)	75	°C/M	
$R_{ heta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	80	°C/W	

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
8601	FDN8601	SSOT-3	7 "	8 mm	3000 units





### **Product specification**

# **FDN8601**

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	octeristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		68		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V			1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±100	nA
On Chara	cteristics (Note 2)					
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	2.0	3.0	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \ \mu$ A, referenced to 25 °C		-8		mV/°C
	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.5 A		85.4	109	mΩ
r <sub>DS(on)</sub>		V <sub>GS</sub> = 6 V, I <sub>D</sub> = 1.2 A		117	175	
		$V_{GS}$ = 10 V, I <sub>D</sub> = 1.5 A, T <sub>J</sub> = 125 °C		143	183	
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1.5 A		8		S
Dynamic	Characteristics					
C <sub>iss</sub>	Input Capacitance			156	210	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 50 \text{ V}, \text{ V}_{GS} = 0 \text{ V},$		47	65	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f = 1 MHz		2.7	5	pF
R <sub>g</sub>	Gate Resistance			1.0		Ω
	Characteristics					
t <sub>d(on)</sub>	Turn-On Delay Time			4.3	10	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 1.5 A,		1.3	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, \text{ R}_{GEN} = 6 \Omega$		7.8	16	ns
t <sub>f</sub>	Fall Time			3.4	10	ns

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1 MHz	156	210	pF
C <sub>oss</sub>	Output Capacitance		47	65	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		2.7	5	pF
R <sub>g</sub>	Gate Resistance		1.0		Ω

t <sub>d(on)</sub>	Turn-On Delay Time		4.3	10	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 1.5 A,	1.3	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS}$ = 10 V, $R_{GEN}$ = 6 $\Omega$	7.8	16	ns
t <sub>f</sub>	Fall Time		3.4	10	ns
Qg	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V	3	5	nC
Qg	Total Gate Charge	$V_{GS} = 0 V \text{ to } 5 V V_{DD} = 50 V,$	1.8	3	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	I <sub>D</sub> = 1.5 A	0.9		nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		0.8		nC

#### **Drain-Source Diode Characteristics**

V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.5 A (Note 2	)	0.81	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 1.5 A, di/dt = 100 A/μs		29	46	ns
Q <sub>rr</sub>	Reverse Recovery Charge	$T_{\rm F} = 1.5$ Å, u/ut = 100 Å/µs		15	27	nC

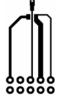
Notes:

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 80 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper





b) 180 °C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300  $\mu s,$  Duty cycle < 2.0%.

3. Starting T\_J = 25 °C; N-ch: L = 3 mH, I\_{AS} = 3 A, V\_DD = 100 V, V\_GS = 10 V.